VIC VECTOR

GROUP 3

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OVERVIEW

- Re-create Atari's© *Tempest* using an FGPA as the basis of the emulator
  - Implement many original features from the original arcade game
- Model original hardware in Verilog
- User input via spinner-wheel and push-button
  - Constructed in similar fashion to the original user controller
- Output graphics using concert-style laser

GOALS AND OBJECTIVES

- Re-create and preserve the popular Atari© *Tempest* game on modern technology
- Use original ROMs
- Same performance as original game (including bugs)
- Output vector-style graphics using concert-style laser
- Re-create a similar game controller to the original
- Implement original hardware

REQUIREMENTS AND SPECIFICATIONS

Software:

- Runs on original game timings at approximately 1.5 MHz clock speed
- Less than 250kb ROM and RAM

Hardware:

- PCB Board will be no larger than 5” x 5”
- 38 FPGA I/O Ports

User Interface and Gameplay:

- The game will save top 8 high scores
- Contains 16 different level shapes
- One player

Power Supply:

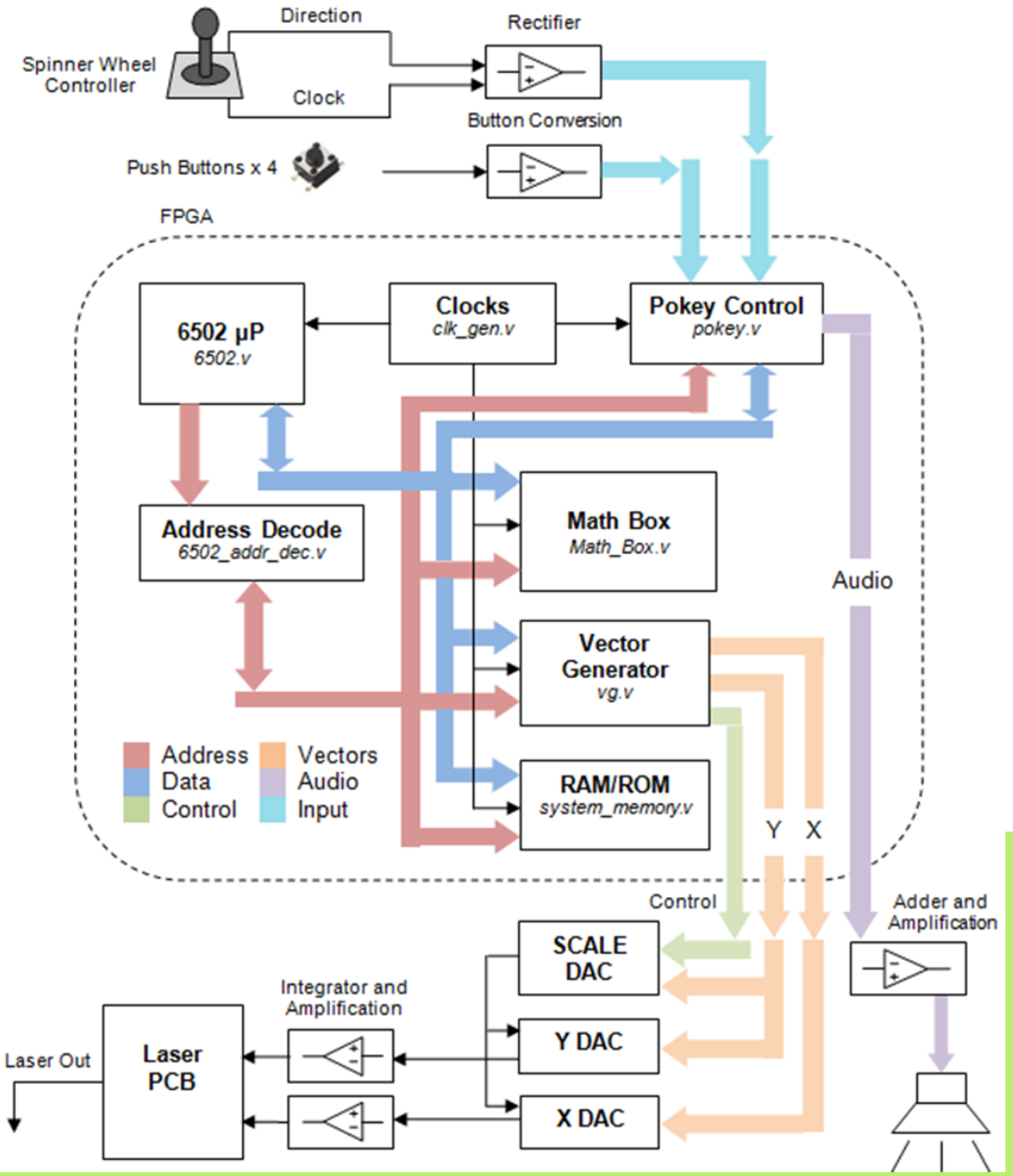
- Powered by 120 V power outlet

I/O:

- Controlled by a dial capable of 360° of motion
- 4-button controller
- Controller deck 7” x 5”
- Output by laser galvanometer under $300.00
- Output refresh rates above 30 frames per second (fps)

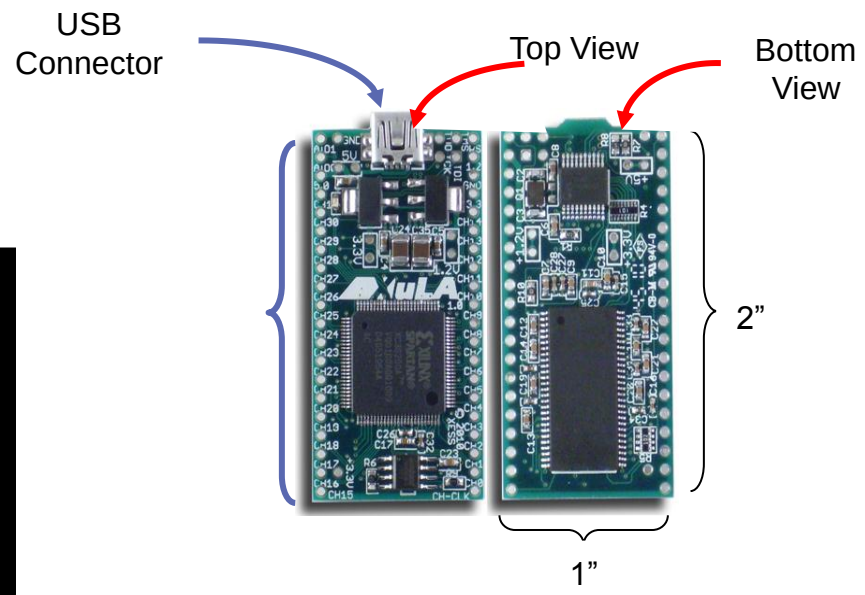
OVERALL SYSTEM DESIGN

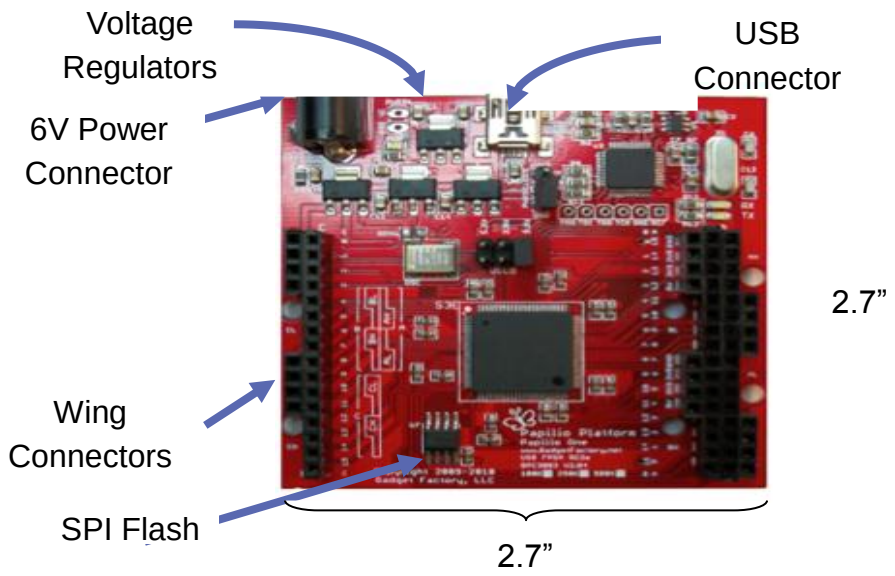
- PCB Connections
  - Input and Output Analog Circuits on one PCB board
  - Place holder pins to hold FPGA
- Overall Structure Flow
  - Input received from user controller as analog signal and converted to digital signal
  - Digital signal is passed to FPGA for appropriate computations
  - FPGA passes result to be converted back to analog and then forwarded to the laser output



FPGA CHOICES

XuLA Board	Parameter	Papilio One
$70	Price	$50 - 75
Spartan 3A 200 K	Chipsets	Spartan 3E 100K, 250K, 500K
32	I/O Pins	48
12 MHz	Clock	32 MHz
5, 3.3, 1.2 V	Voltage Pins	5, 3.3, 2.5, 1.2 V





MEMORY CONSIDERATIONS

Memory needed to be instantiated by FPGA Block RAM

Component	# ROM/RAM	Address Bytes	Data Bits	Bits
6502	2 RAM 10 ROM	1024 2048	8 8	16k 160k
Math Box	6 ROM	256	4	6k
Vector Generator	4 RAM 2 ROM	1024 2048	8 8	32k 32k
TOTAL				**246 kbits**

1kbits = 1024 bits

Spartan 3E 500K Chip is capable of addressing up to 360 kbits

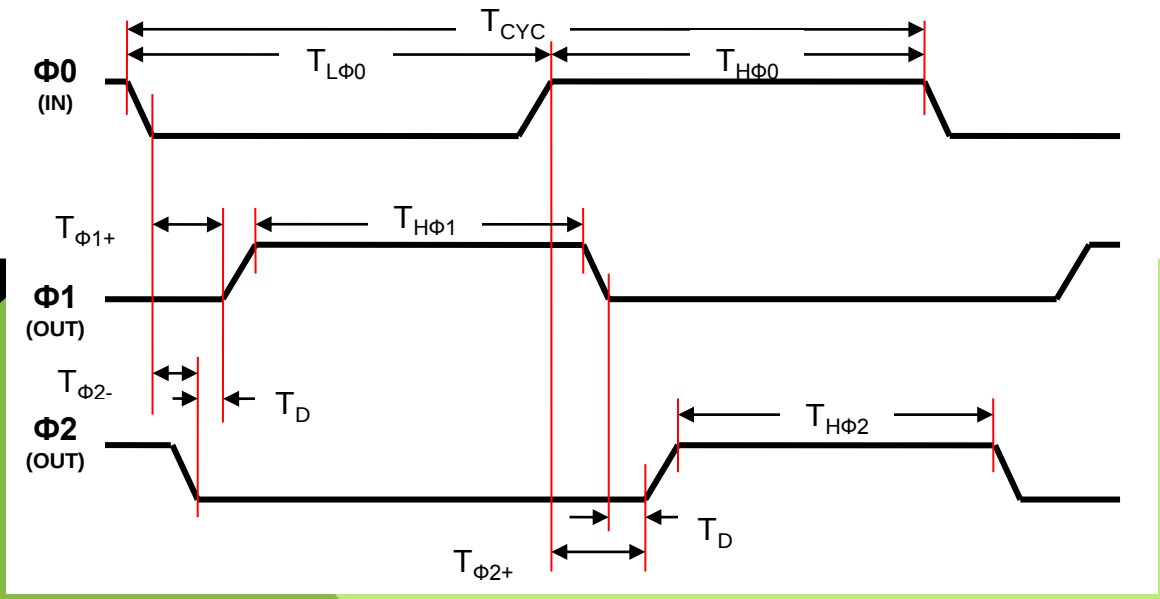
CLOCK GENERATION

- Clocks needed: 12 MHz, 6 MHz, 3 MHz, 1.5 MHz, Φ1, Φ2
- Input clock: 32 MHz
  - 3 Digital Clock Management modules:

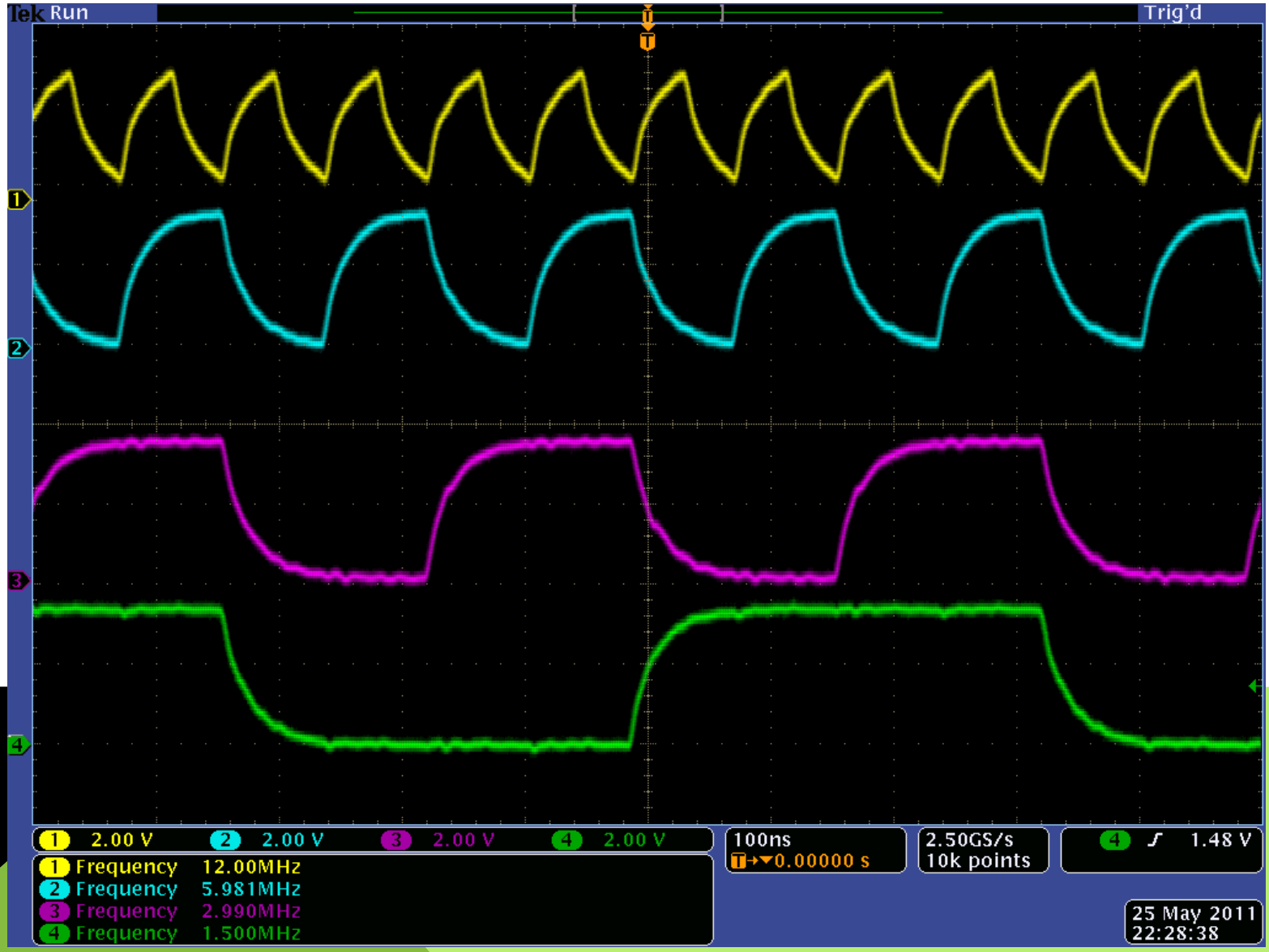
    32*3 = 96 MHz

    96 / 8 = 12 MHz
- Positive Edge Counters generate the remaining signals
- 96 MHz is used to manage Φ1 and Φ2 based on the diagram below

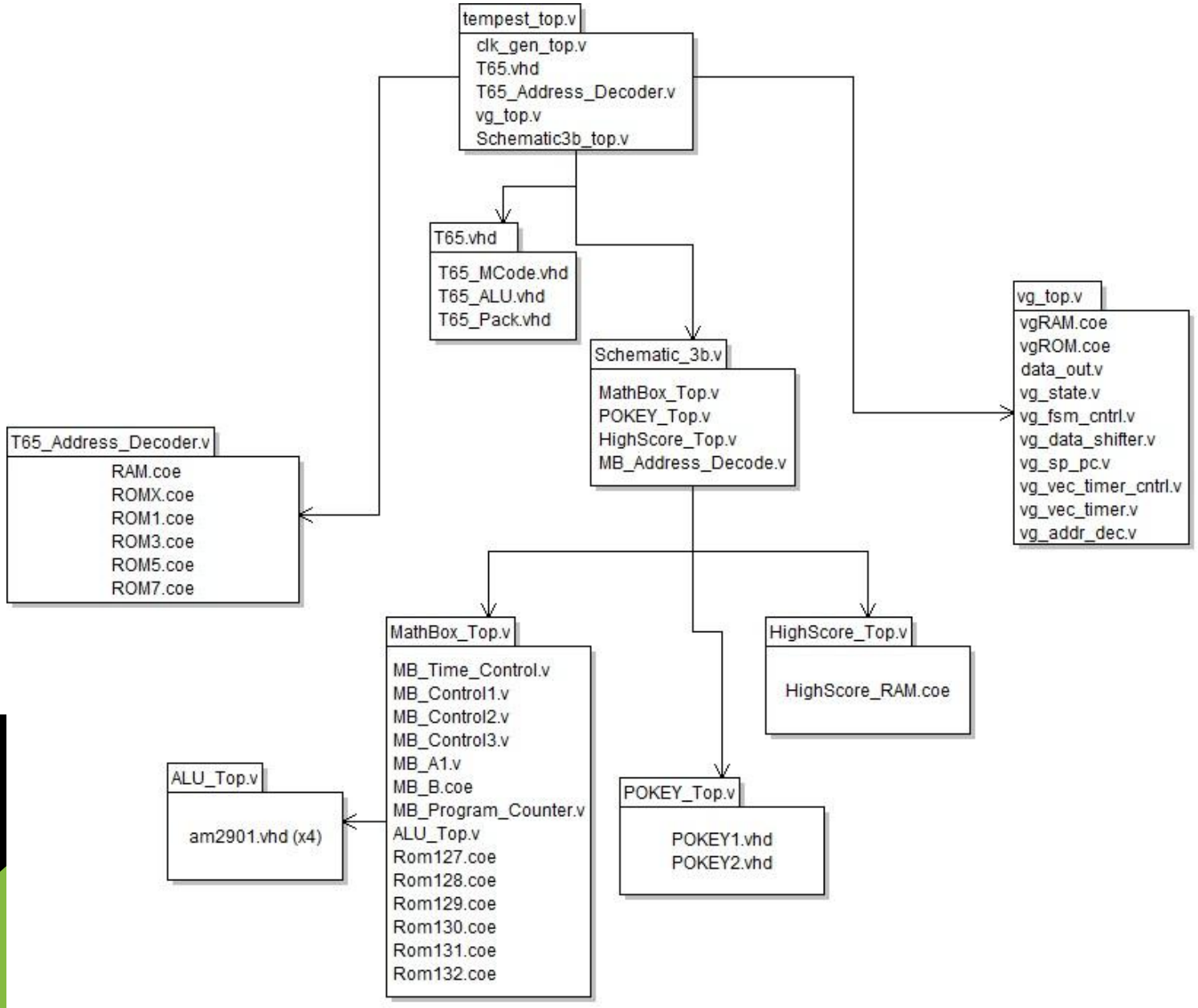
Timing Waveforms for the 6502 Phase Clocks



CLOCK GENERATION



SOFTWARE LAYOUT



6502 MICROPROCESSOR AND 6502 ADDRESS DECODER

ROBERT HIGGINBOTHAM

6502 MICROPROCESSOR INSTRUCTION SET

- 56 total instructions
  - Expanded to include more Op-Codes for various addressing modes
  - Contains R-type, J-Type, and I-type instructions
  - Supports BCD Operations

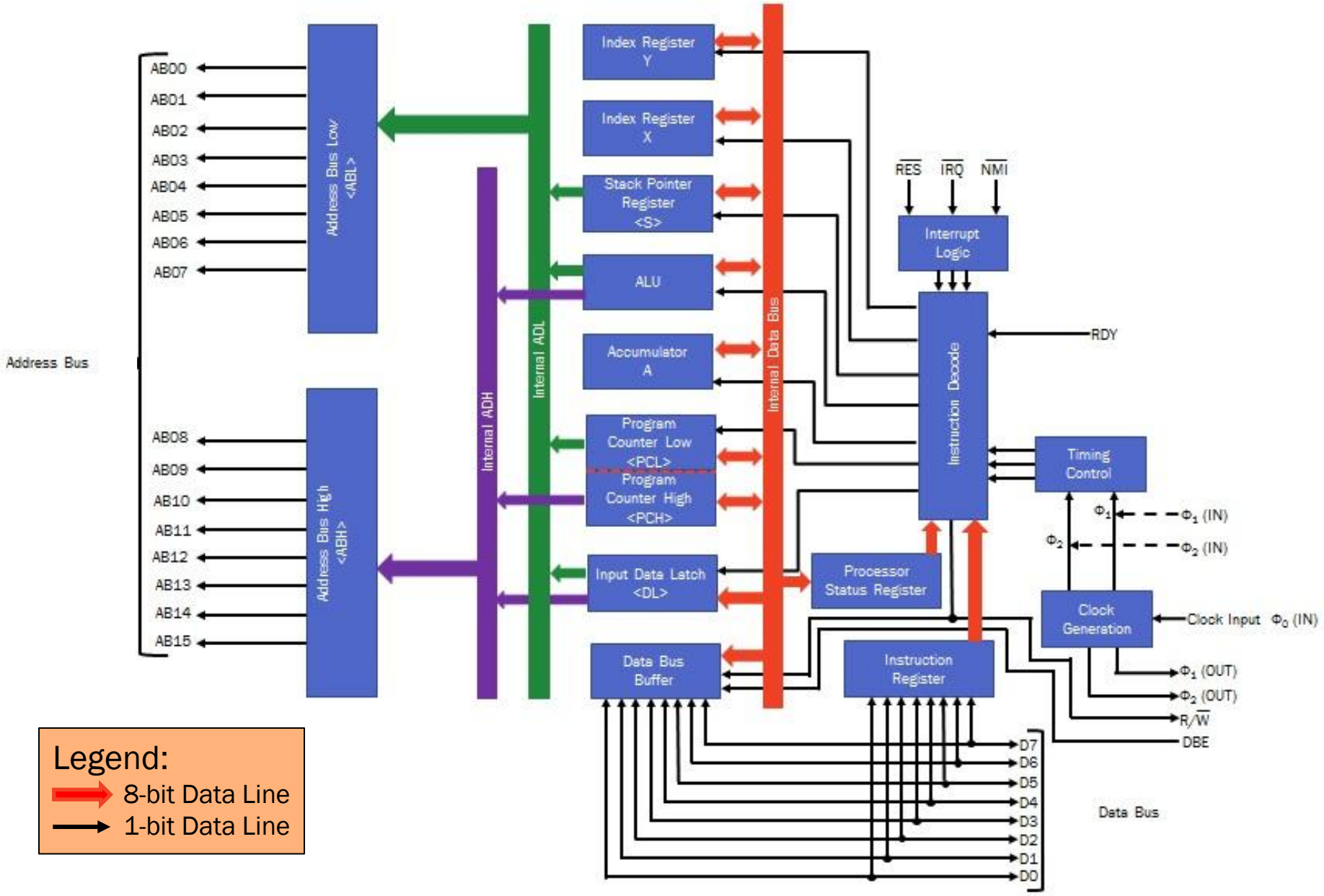
Addressing Mode	Op-Code
Immediate	69h
Zero Page	65h
Zero Page, X	75h
Absolute	6Dh
Absolute, X	7Dh
Absolute, Y	79h
(Indirect, X)	61h
(Indirect, Y)	71h

ADC - Add Memory to Accumulator with Carry Instruction

6502 MICROPROCESSOR BUSSES AND TIMING

- 3 Main Bus lines (data, address-high, address-low)
  - Each bus is 8-bit wide – allows for 8-bit data words and 16-bit address words
  - In general, each bus is isolated, but sometimes may be latched into each other
- Utilizes a 2-phase clocking system – allows for more efficient use of clock signals
  - Φ_1 phase clock
  - Φ_2 phase clock
- Outside the 6502, buses are connected to properly interface the Vector Generator, Math Box, RAM,ROM, and other hardware components
  - All external components are asynchronous
    - Data is accessed during a high Φ_2 phase clock signal
    - Data is latched during high Φ_1 phase clock signal

6502 MICROPROCESSOR INTERNAL ARCHITECTURE



Legend:
- 8-bit Data Line
- 1-bit Data Line

6502 VHDL CODE

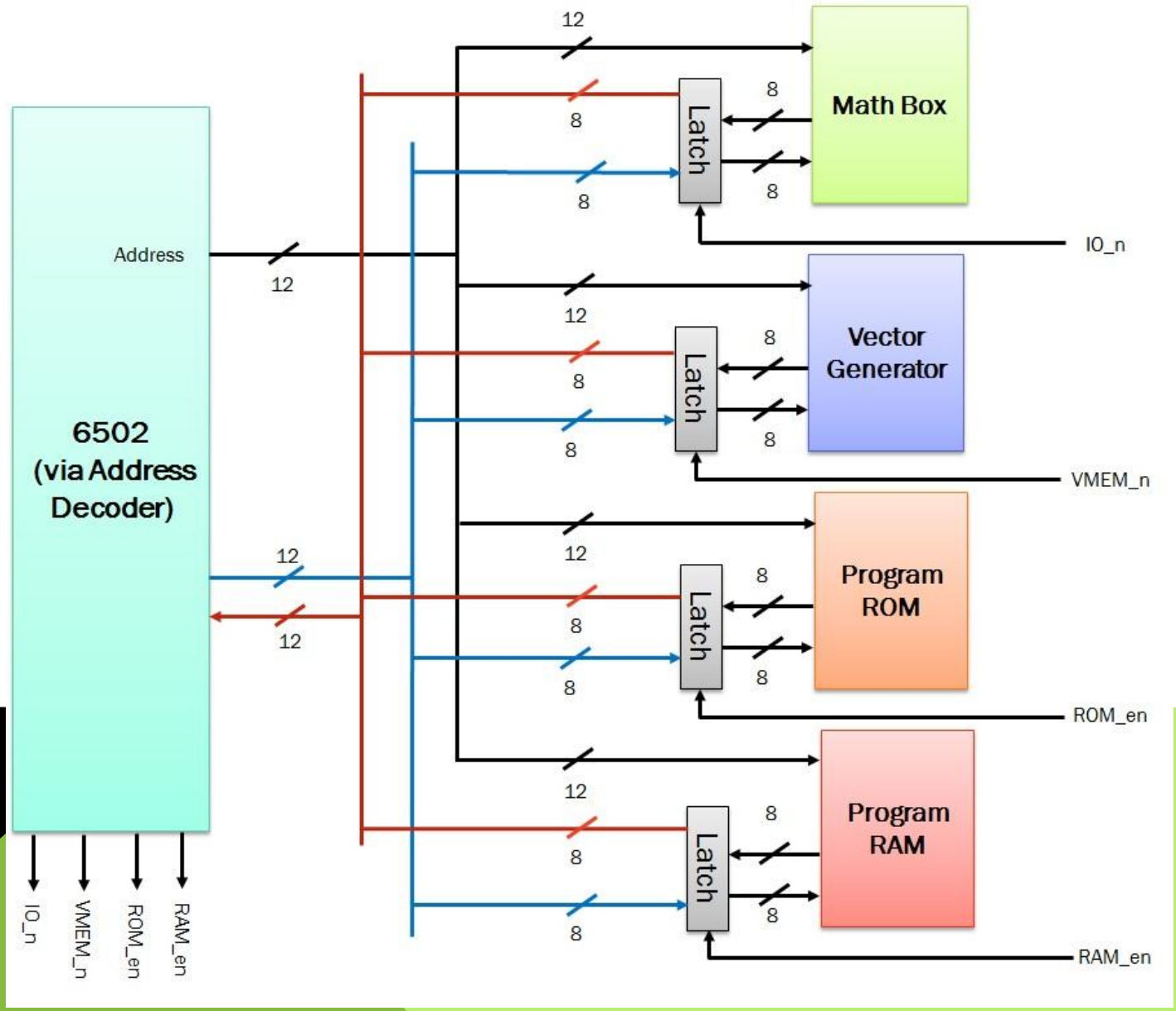
- Available as open-source code
- Originally used in an FPGA Emulator project for Atari© *Asteroids*
- Has the capability of supporting the following microprocessors
  - 6502
  - 65C02 (work in progress)
  - 65816 (work in progress)
- Consists of 4 modules
  - T65_Pack.vhd
  - T65.vhd
  - T65_ALU.vhd
  - T65_MCode.vhd

6502 TOP MODULE (T65.VHD)

- Functionality:
  - Passes data to T65_ALU and T65_MCode modules through Bus A and Bus B
  - Sets Program Status Register based on Op-Code
  - Controls Stack and PC Registers
  - Handles execution of Interrupt Subroutines

- Testing:
  - Simulation of individual test scripts checking Interrupt functionality
  - Simulation of Atari© Tempest Program ROM's

6502 ADDRESS DECODER



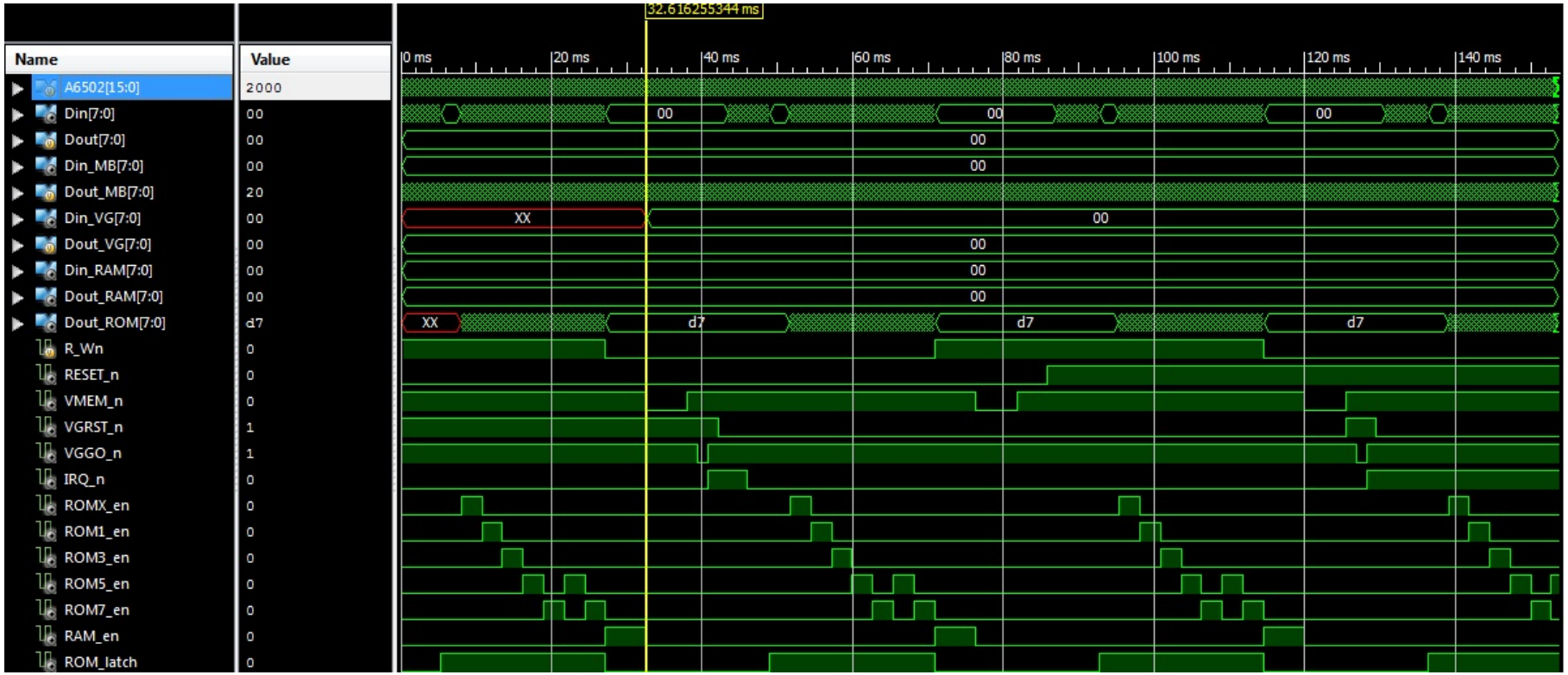
6502 TESTING (WITH ADDRESS DECODER)

Stand-Alone:

- Simulation of individual test scripts

With Vector Generator:

- Simulation of individual test scripts
- Simulation of Atari© *Tempest* Program ROMs



ATARI© MEMORY MAP

Atari© Memory Map										
Hexadecimal Address	**R/W**	**Data**								**Function**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
0000-7FFF	R/W	D	D	D	D	D	D	D	D	Program RAM (2K)
0800-080F	W					D	D	D	D	Color RAM
0C00	R								D	Right Coin Switch
0C00	R							D		Center Coin Switch
0C00	R						D			Left Coin Switch
0C00	R					D				Slam Switch
0C00	R				D					Self-Test Switch
0C00	R			D						Diag. Step Switch
0C00	R		D							HALT
0C00	R	D								3KHz
0D00	R	D	D	D	D	D	D	D	D	Option Switch Inputs
0E00	R	D	D	D	D	D	D	D	D	Option Switch Inputs
2000-2FFF	R/W	D	D	D	D	D	D	D	D	Vector RAM (4K)
3000-3FFF	R	D	D	D	D	D	D	D	D	Vector ROM (4K)
4000	W								D	Right Coin Counter
4000	W							D		Center Coin Counter
4000	W					D				Video Invert X
4000	W				D					Video Invert Y
4000	W									VG GO

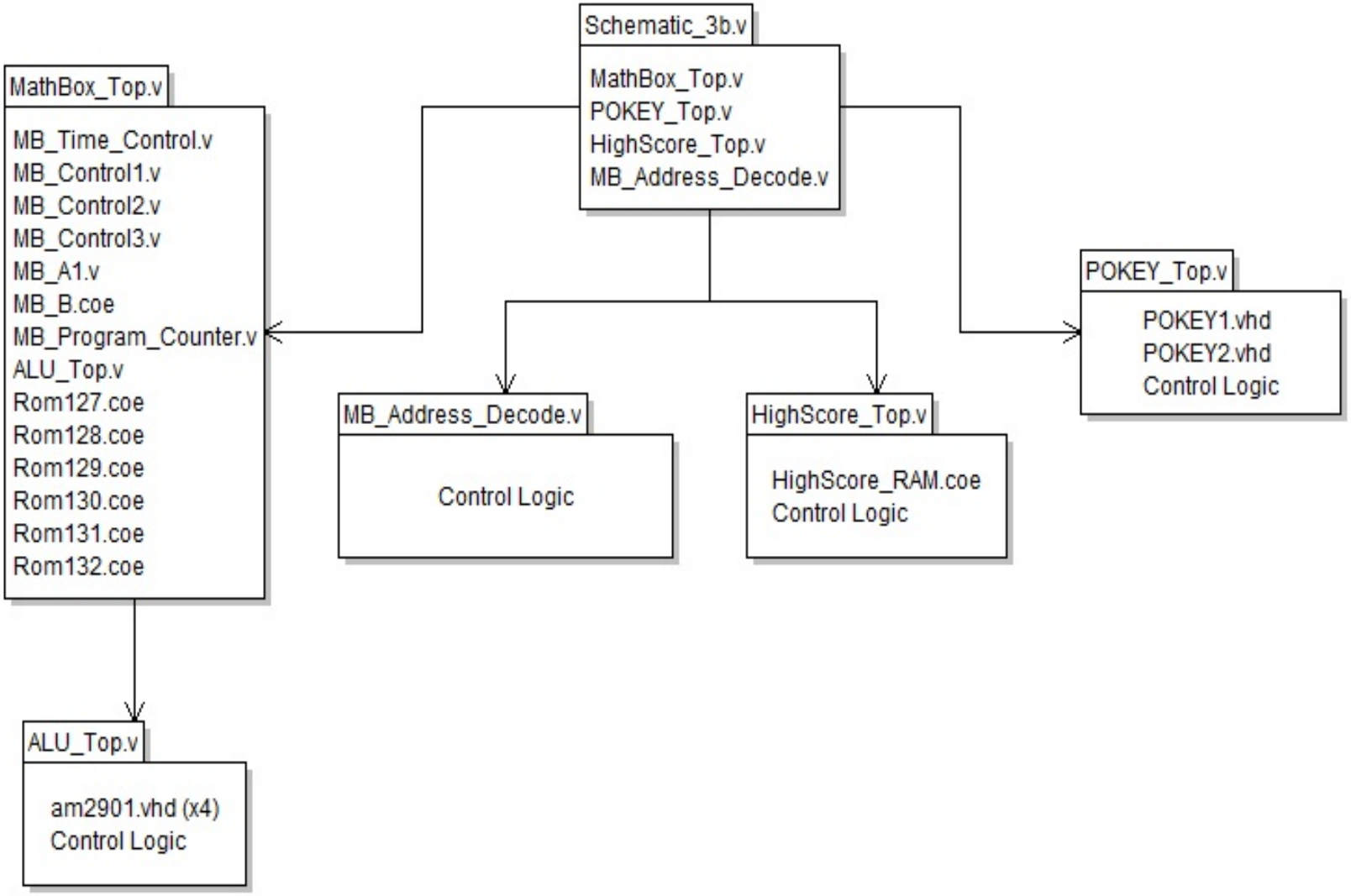
ATARI© MEMORY MAP

Atari© Memory Map										
Hexadecimal Address	**R/W**	**Data**								**Function**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
5000	W									WD CLEAR
5800	W									VG Reset
6000-603F	W	D	D	D	D	D	D	D	D	EAROM Write
6040	W	D	D	D	D	D	D	D	D	EAROM Control
6040	R	D								Math Box Status
6050	R	D	D	D	D	D	D	D	D	EAROM Read
6060	R	D	D	D	D	D	D	D	D	Math Box Read
6070	R	D	D	D	D	D	D	D	D	Math Box Read
6080-609F	W	D	D	D	D	D	D	D	D	Math Box Start
60C0-60CF	R/W	D	D	D	D	D	D	D	D	Custom Audio Chip 1
60D0-60DF	R/W	D	D	D	D	D	D	D	D	Custom Audio Chip 2
60E0	R								D	One Player Start
60E0	R							D		Two Player Start
60E0	R						D			FLIP
9000-DFFF	R	D	D	D	D	D	D	D	D	Program ROM (20K)
E000-FFFF	**R**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**Reset/Interrupt Vectors**

MATH BOX, ADDRESS DECODER AND POKEY

DREW HANSON

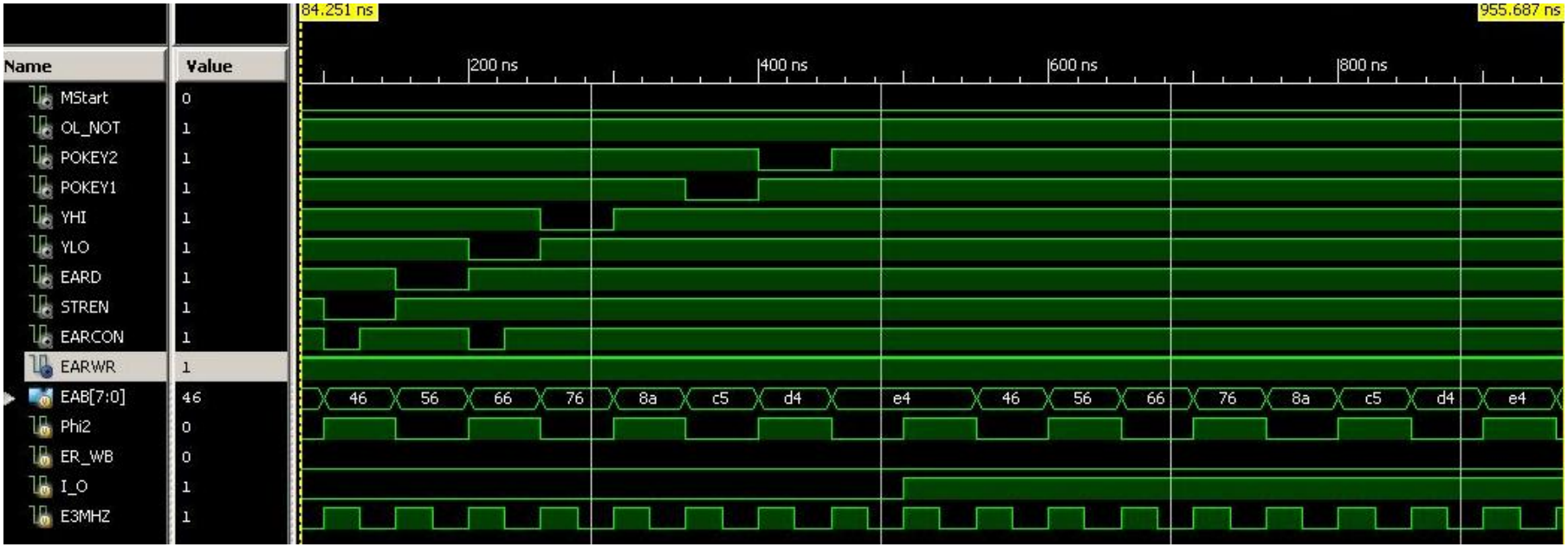
VERILOG MODULE LAYOUT



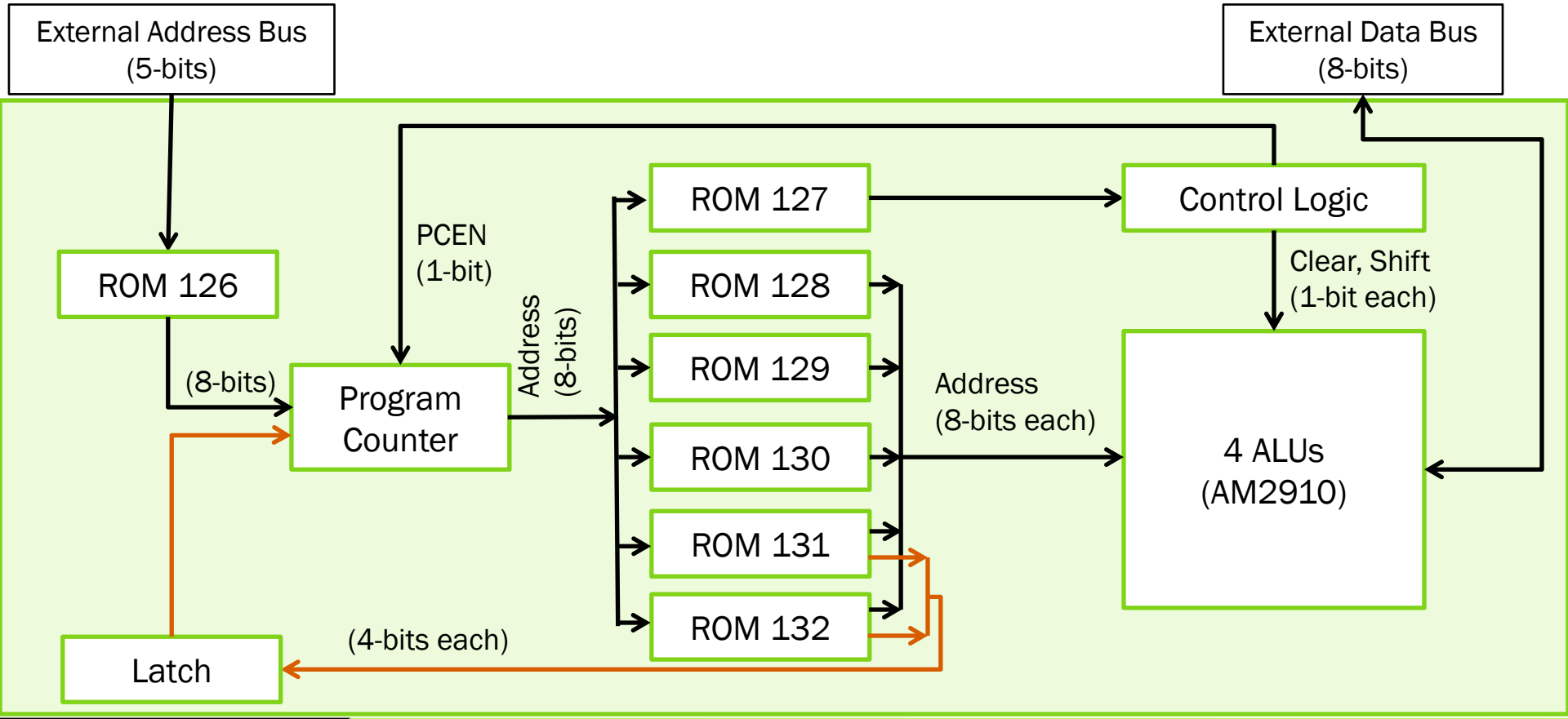
AUXILIARY ADDRESS DECODER

- Reads in bits 4-7 from External Address Bus (EAB)
- Address is decoded using basic logic and decoders
- Based on memory map, either Math Box, High Score or ‘POKEY’ is activated
- Upon activation, the Math Box, High Score or ‘POKEY’ will be enabled to read to or write from External Data Bus (EDB)

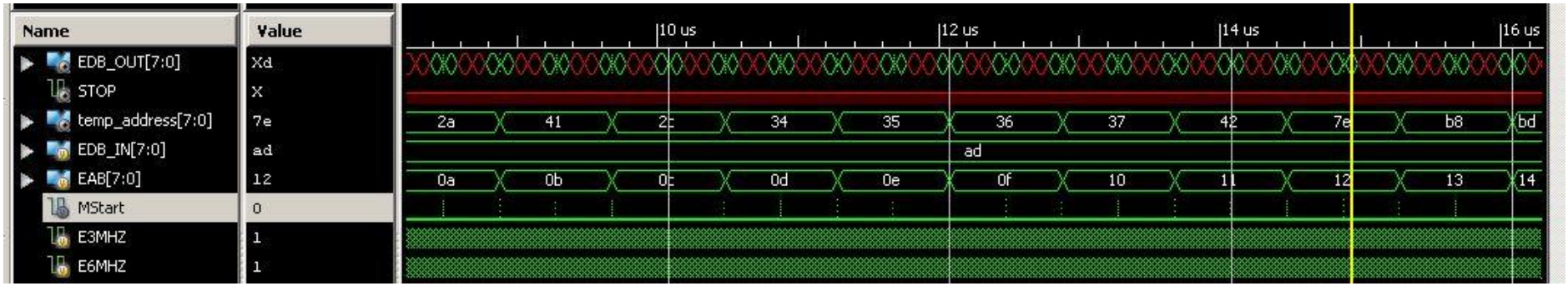
EAB SIMULATION



MATH BOX


External Address Bus
(5-bits)
External Data Bus
(8-bits)
ROM 126
(8-bits)
Program
Counter
PCEN
(1-bit)
Address
(8-bits)
ROM 127
ROM 128
ROM 129
ROM 130
ROM 131
ROM 132
Control Logic
Clear, Shift
(1-bit each)
Address
(8-bits each)
4 ALUs
(AM2910)
Latch
(4-bits each)

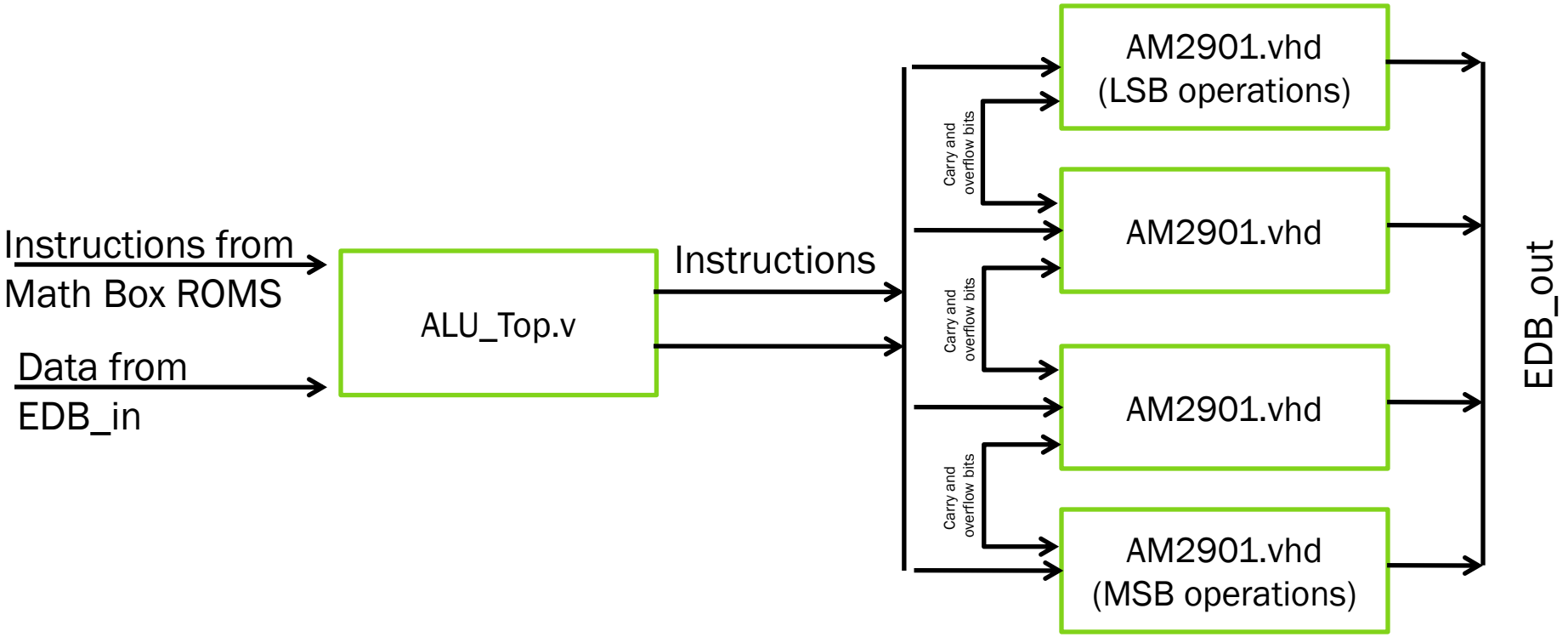
MATH BOX MICROCODE EXECUTION



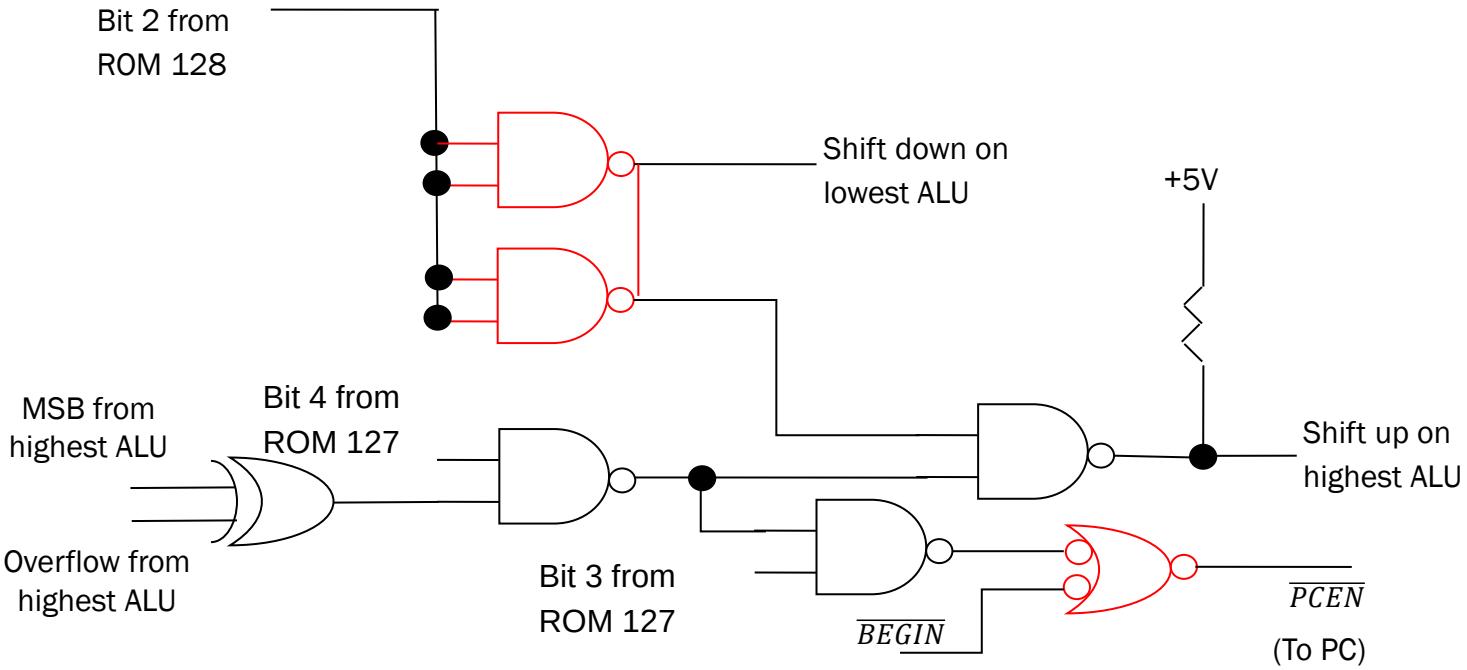
MATH BOX - ALUs

- AM2901 Microprocessor bit-slice
- 8 bits input/output
  - 2 4-bit inputs
  - From/to EDB
- 8 functions plus shifts
  - From ROMs 127-132
- Can be connected together for operations on 32 bit values
  - 2 16-bit inputs
- Coding: Used VHDL code with permission.
  - Adjustments were made for better compatibility in Verilog simulation

ALU DATA FLOW

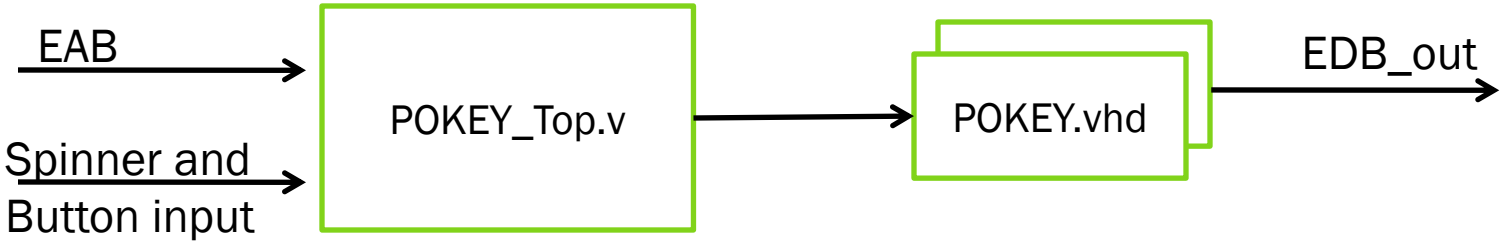


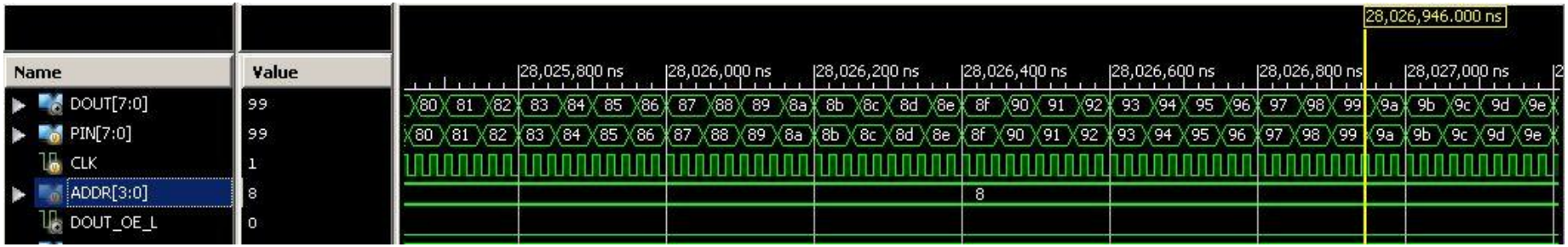
MATH BOX – CONTROL LOGIC



POKEYS

- Reads data from spinner wheel and buttons
- Reads data from coin in, and difficulty switch
- Output audio data
- Used open source code





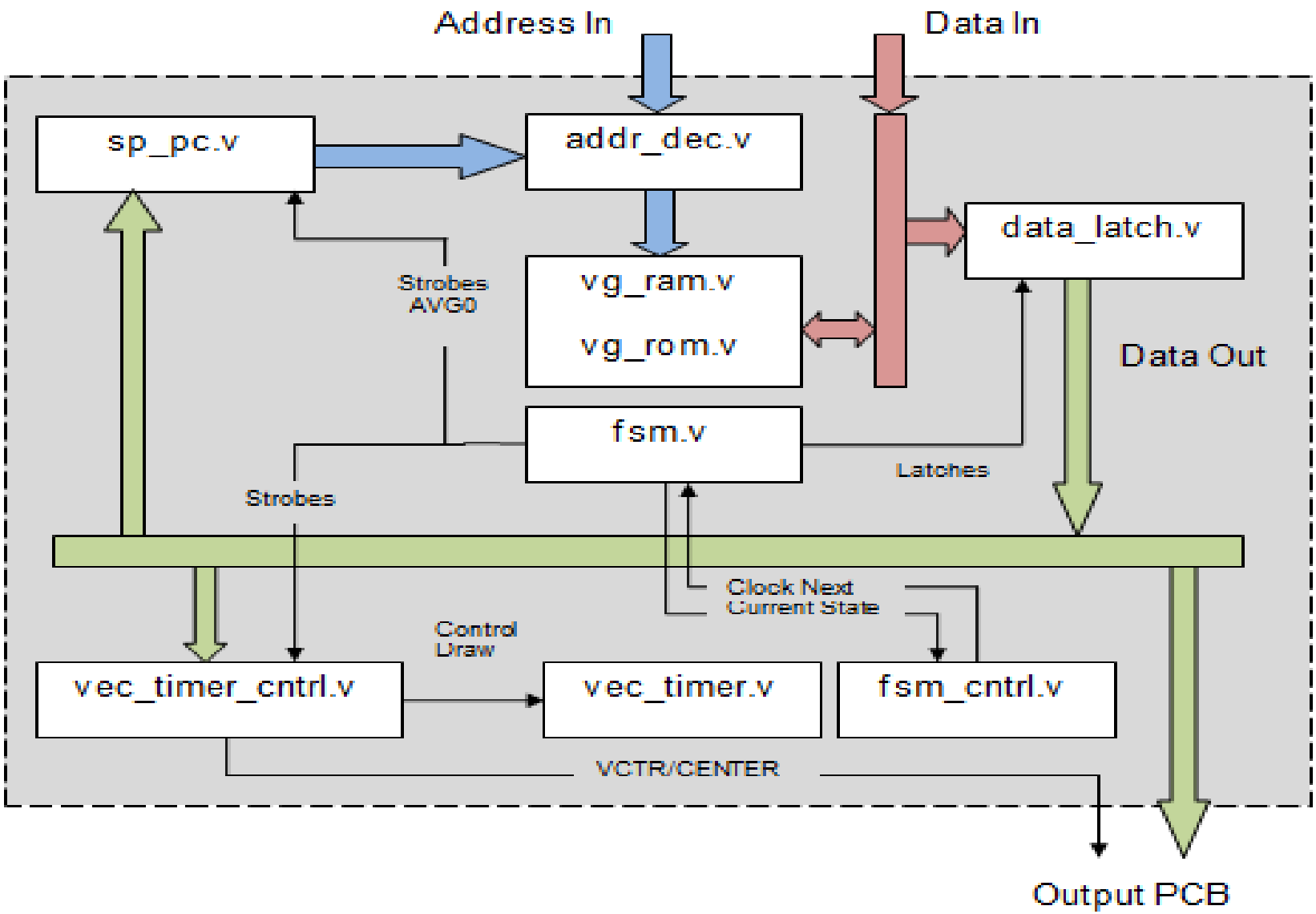
HIGH SCORE MEMORY

- Activated by Auxiliary Board Address Decoder
- Main Component (Rewritable ROM)– ER 2055
- Address is read from EAB
- Data is written to High Score ROM via EDB
- Data can be written to EDB when high scores need to be displayed

VECTOR GENERATOR

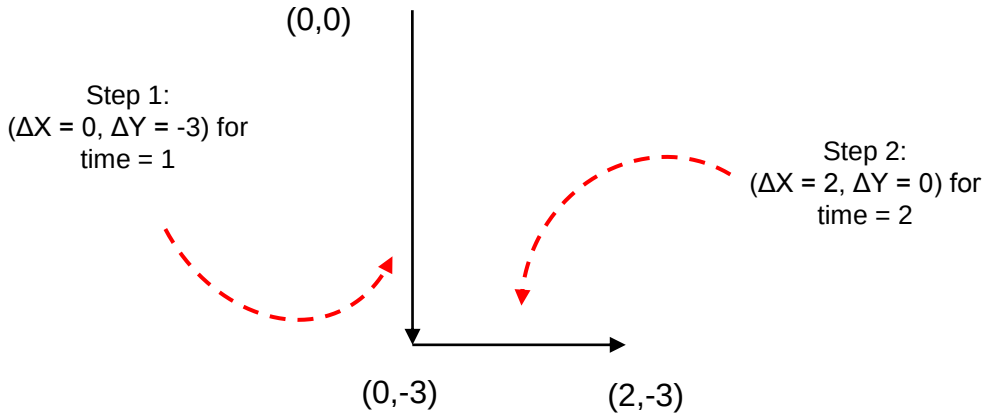
TONY CAMARANO

VECTOR GENERATOR VERILOG DESIGN



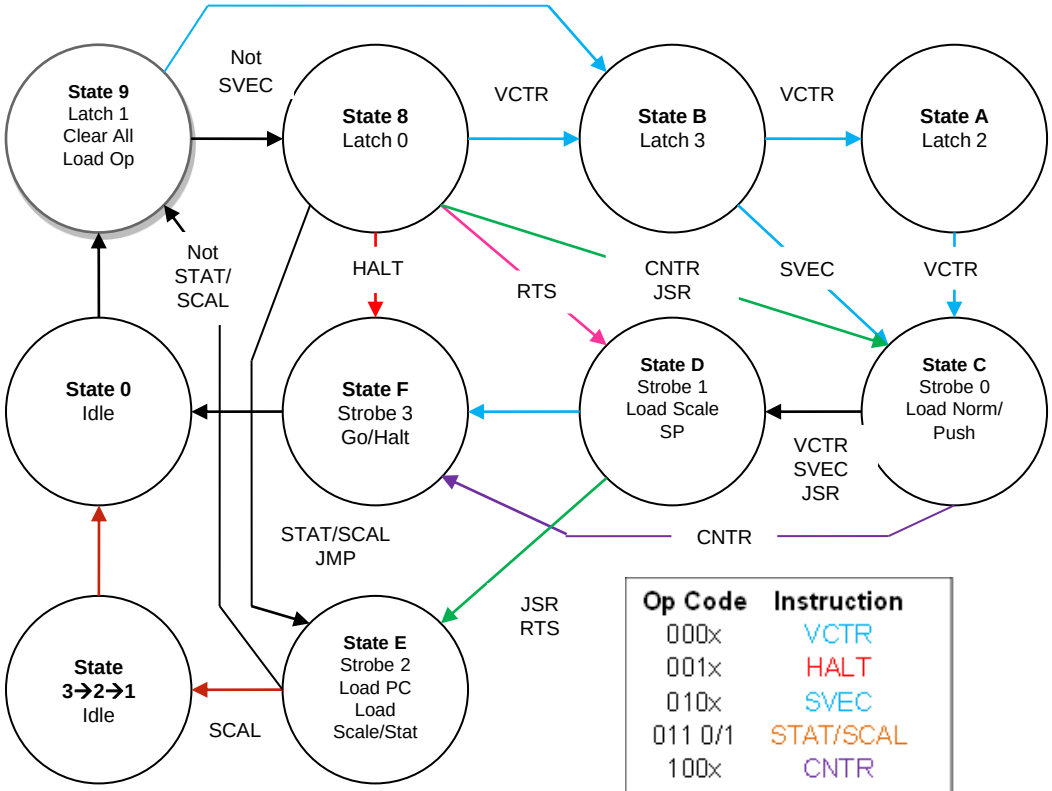
SPECIFICATIONS AND REQUIREMENTS OF THE ATARI VECTOR GENERATOR

- Outputs changes in X-Y vector coordinates, 10-bit 2's complement numbers
- 13-bit Address Bus
- 8-bit Data Bus
- 1024x1024 resolution
- Little Endian PC and 4-word Stack
- State machine with 8 micro-instructions
- 16 levels of brightness intensity
- 8 binary scaling settings

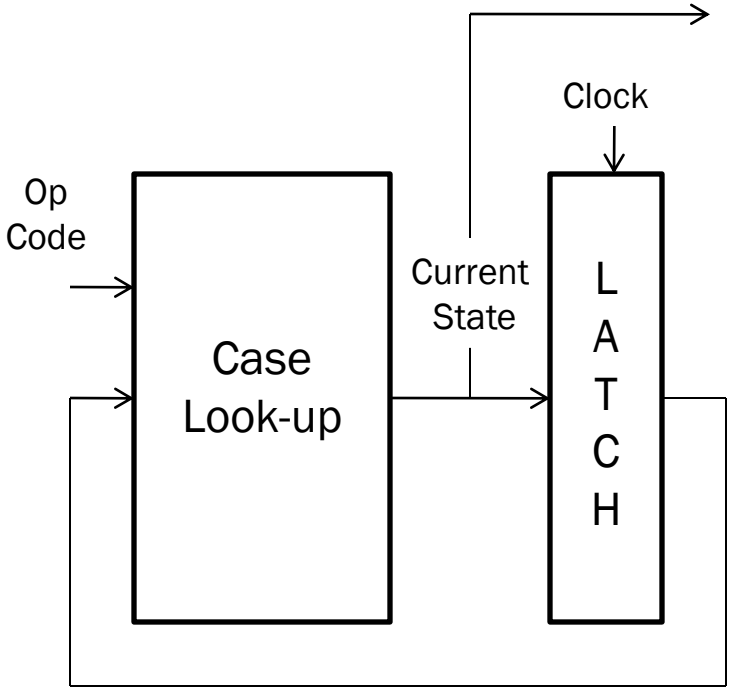


VG FSM AND INSTRUCTIONS

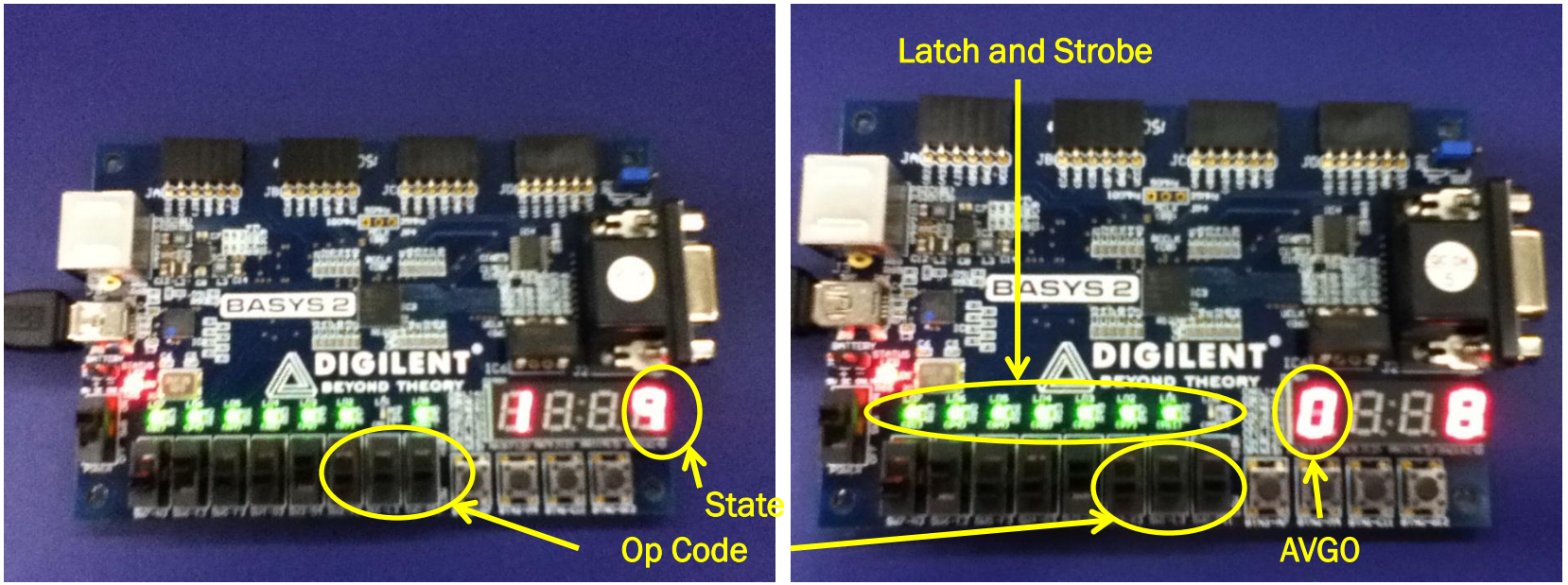
- 8 micro-instructions: draw, scale, address manipulation
- ATARI PROM → Verilog Case Statement



Op Code	Instruction
000x	VCTR
001x	HALT
010x	SVEC
011 0/1	STAT/SCAL
100x	CNTR
101x	JSR
110x	RTS
111x	JMP



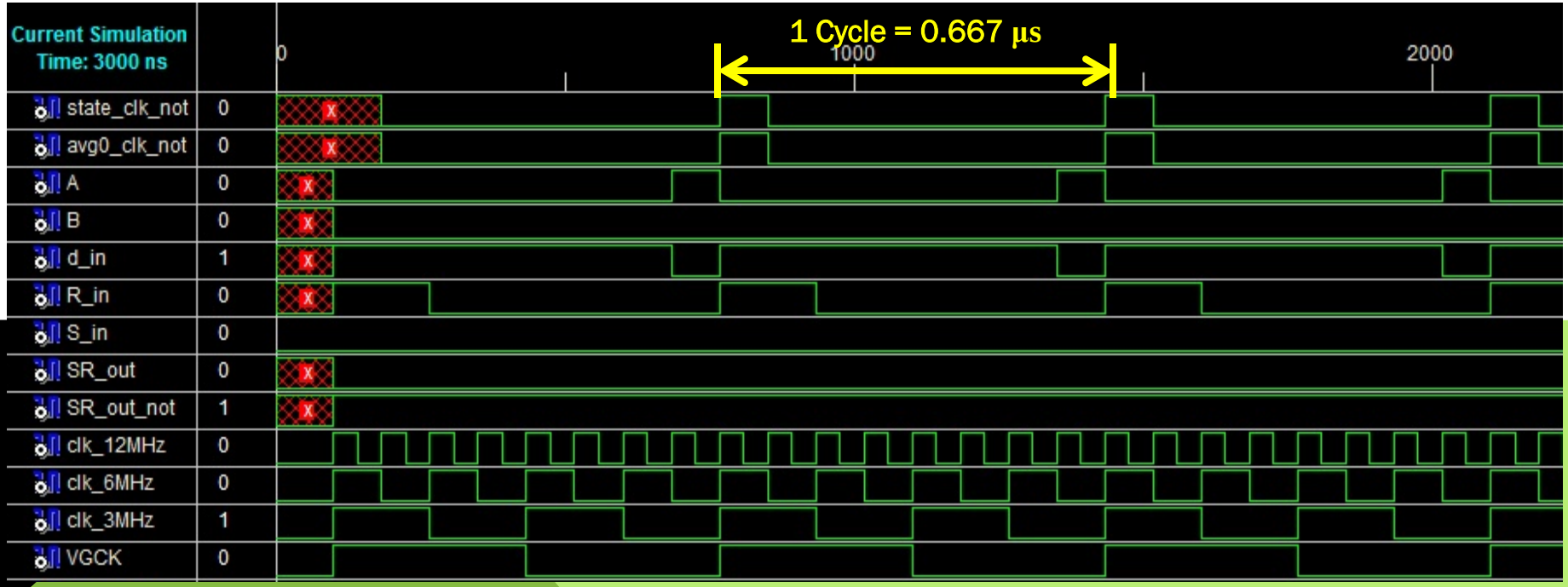
VG FSM AND INSTRUCTIONS



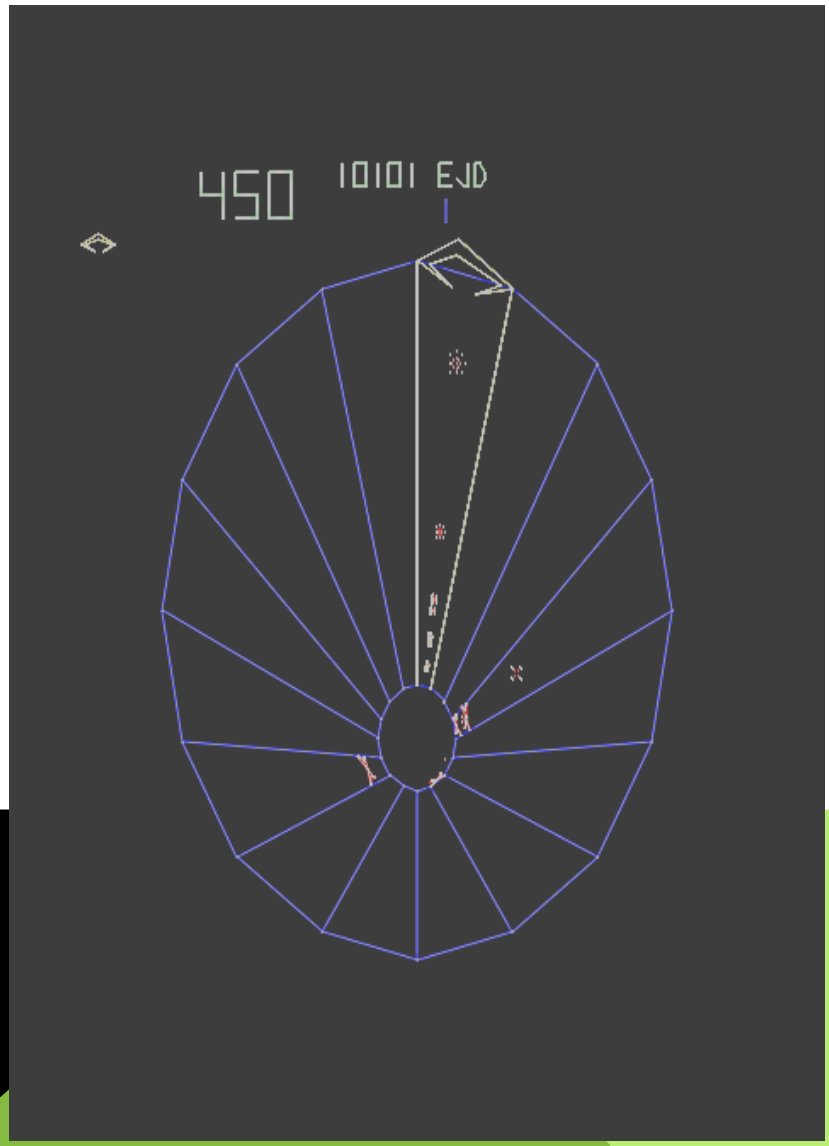
VG FSM TIMING CONTROL

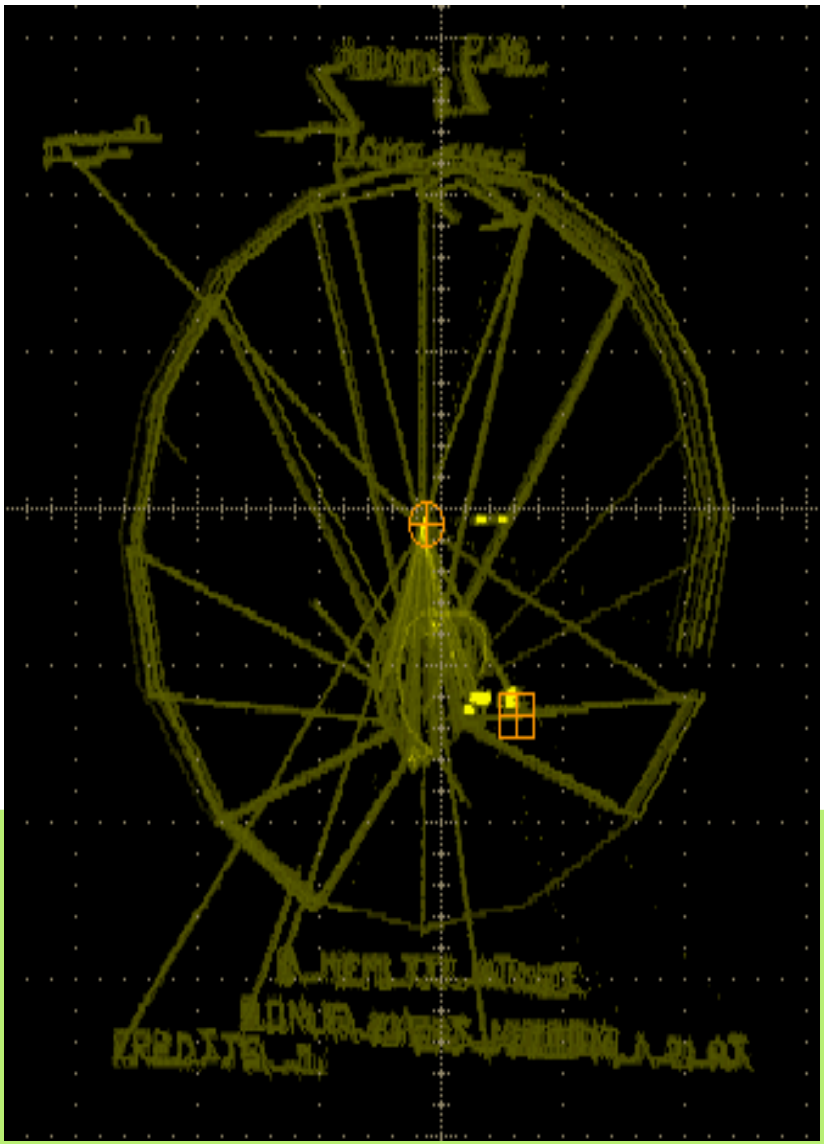
- Simulation of the clock signals used in the FSM
  - state_clk_not controls the latch to the FSM
  - avg0_clk_not clears decoder and varies AVG0 (LSB of VG address bus)
- Original Atari specs:
  - VCTR: 8 states/8 cycles → Total Time = 5.3 μs

8*0.667 μs = 5.333 μs

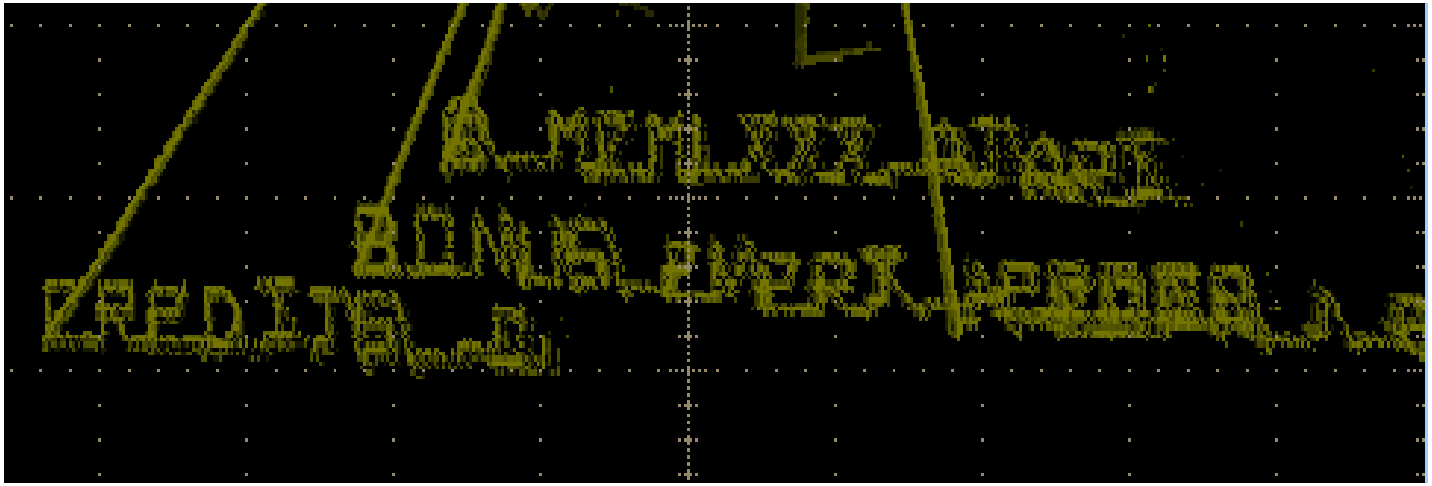


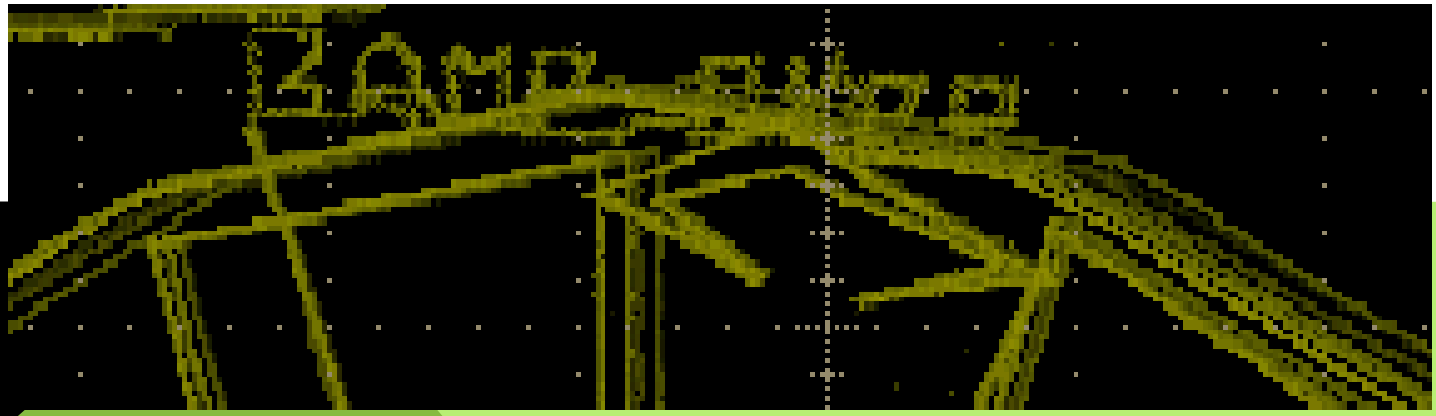
STATIC GAME IMAGE (1)





STATIC GAME IMAGE (2)



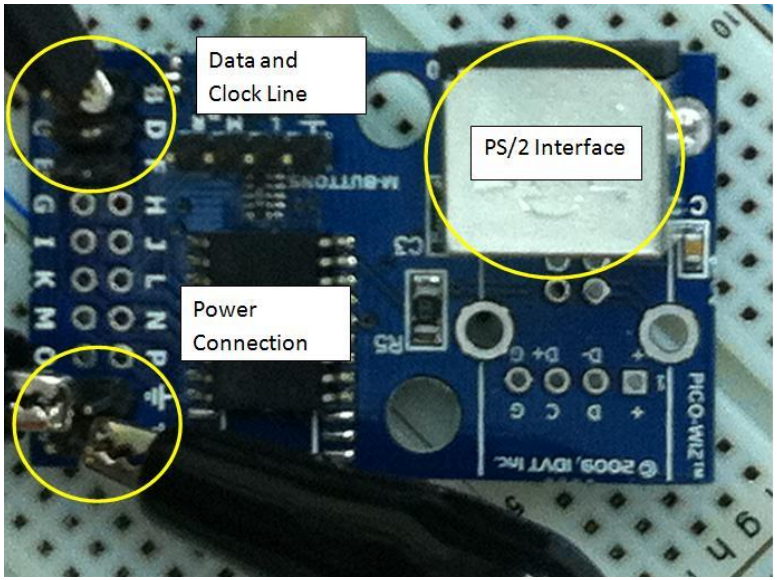


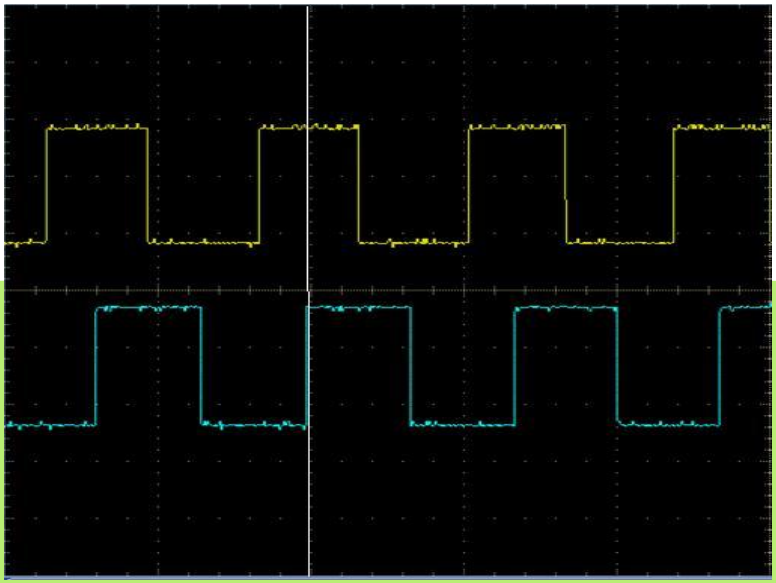
I/O PCB DESIGN

ROBERT BAKER

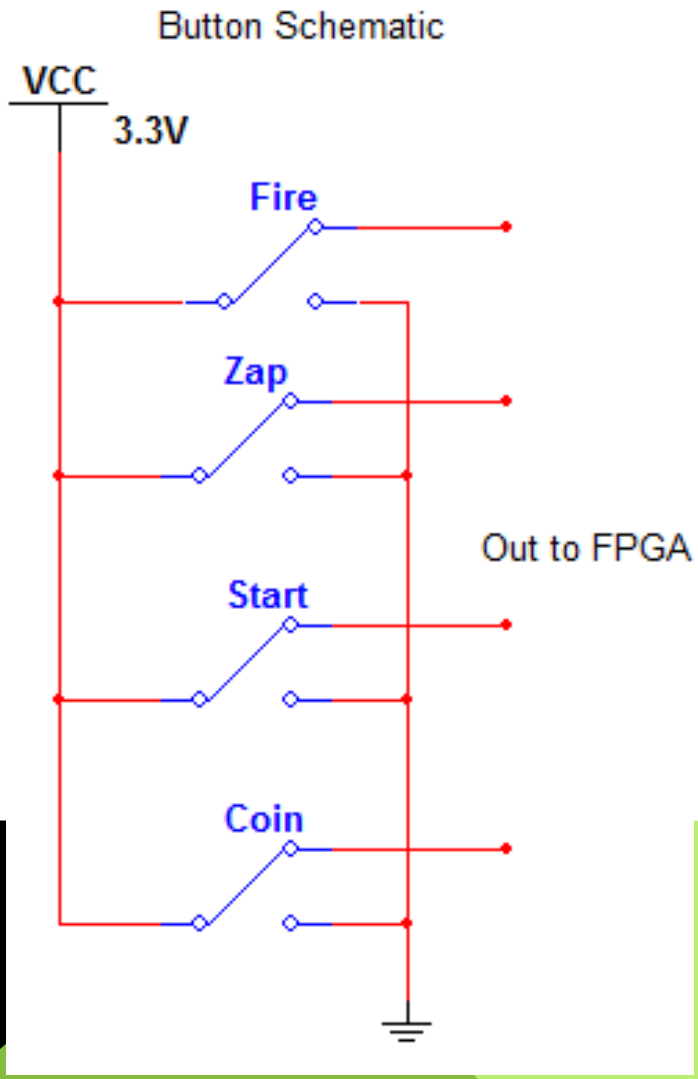
SPINNER WHEEL INPUT

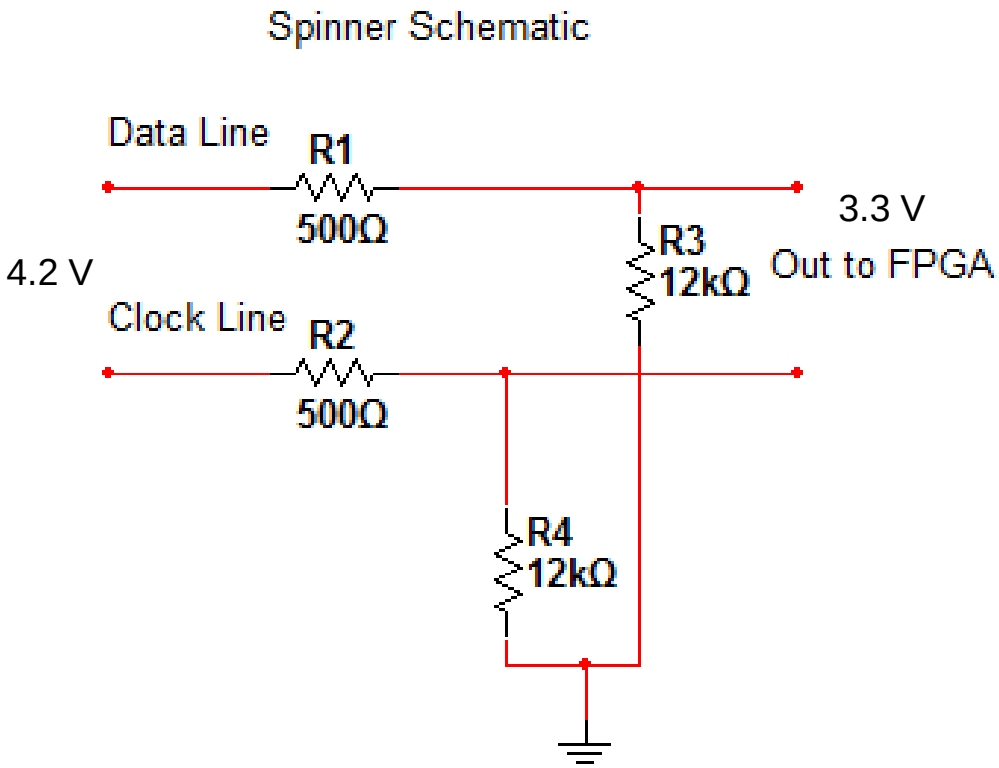
- Power – 5 VDC
- Output:
  - V High = 4 volts
  - V Low = 0 Volts
- Uses Optical Encoder
  - Clock line
  - Data line
- High Frequency
- Implemented digital delay counter





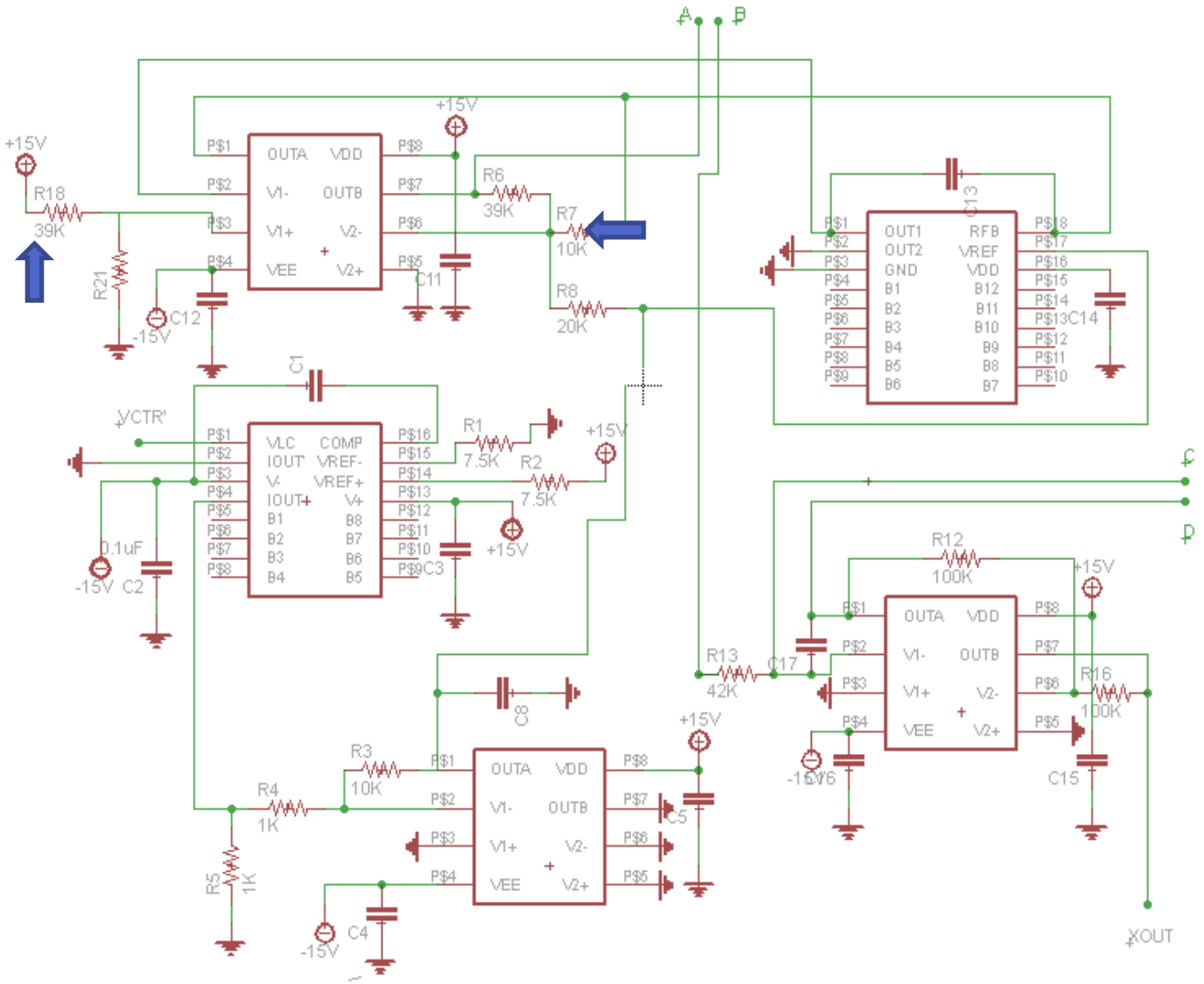
INPUT SCHEMATIC





X/Y OUTPUT SCHEMATIC

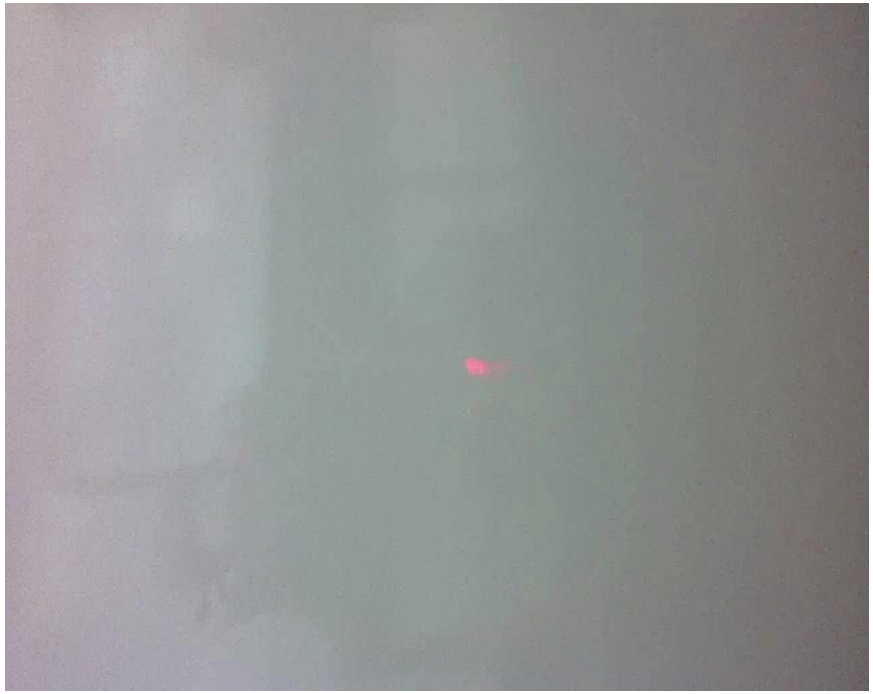
- Components powered by +/- 15V from regulator – IA0515D
- 26mA current draw from circuit
- ~35mV Input offset
- Accuracy of 10k resistors
- Analog switch at AB, CD

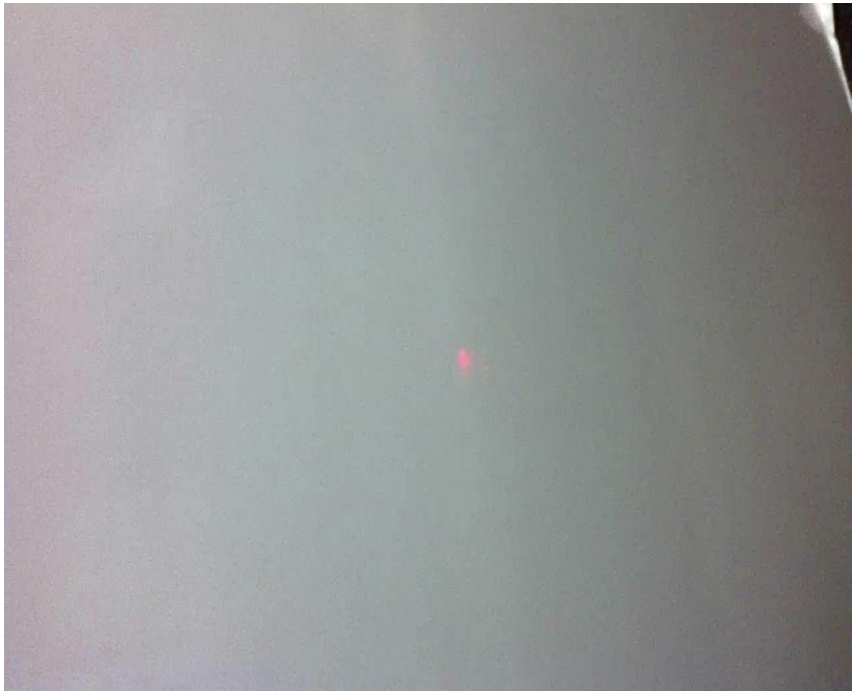


OUTPUT TIMING CONSIDERATIONS (1)

- Longest drawing time: $t \approx 2.73$ ms $\rightarrow RC \approx 2.73$
- Maximum voltage (± 5 VDC) charged for this amount of time
- Some tuning was necessary:
  - R = 25 kΩ
  - C = 0.1 μF
  - Output gain = 10 chosen based on real game image
- Timing specific to original game hardware
  - Only 2 FPS
  - Increase of clock speed improves image stability but reduces image size, due to the RC values used.

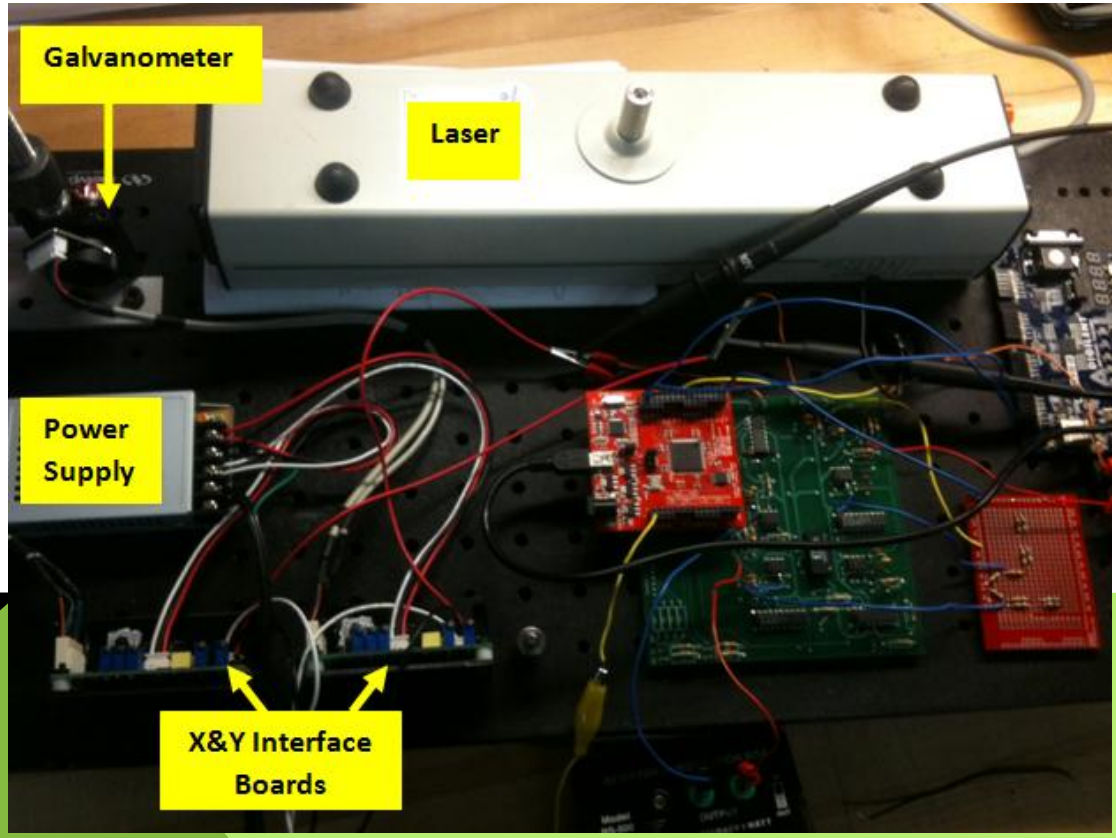
OUTPUT TIMING CONSIDERATIONS (2)



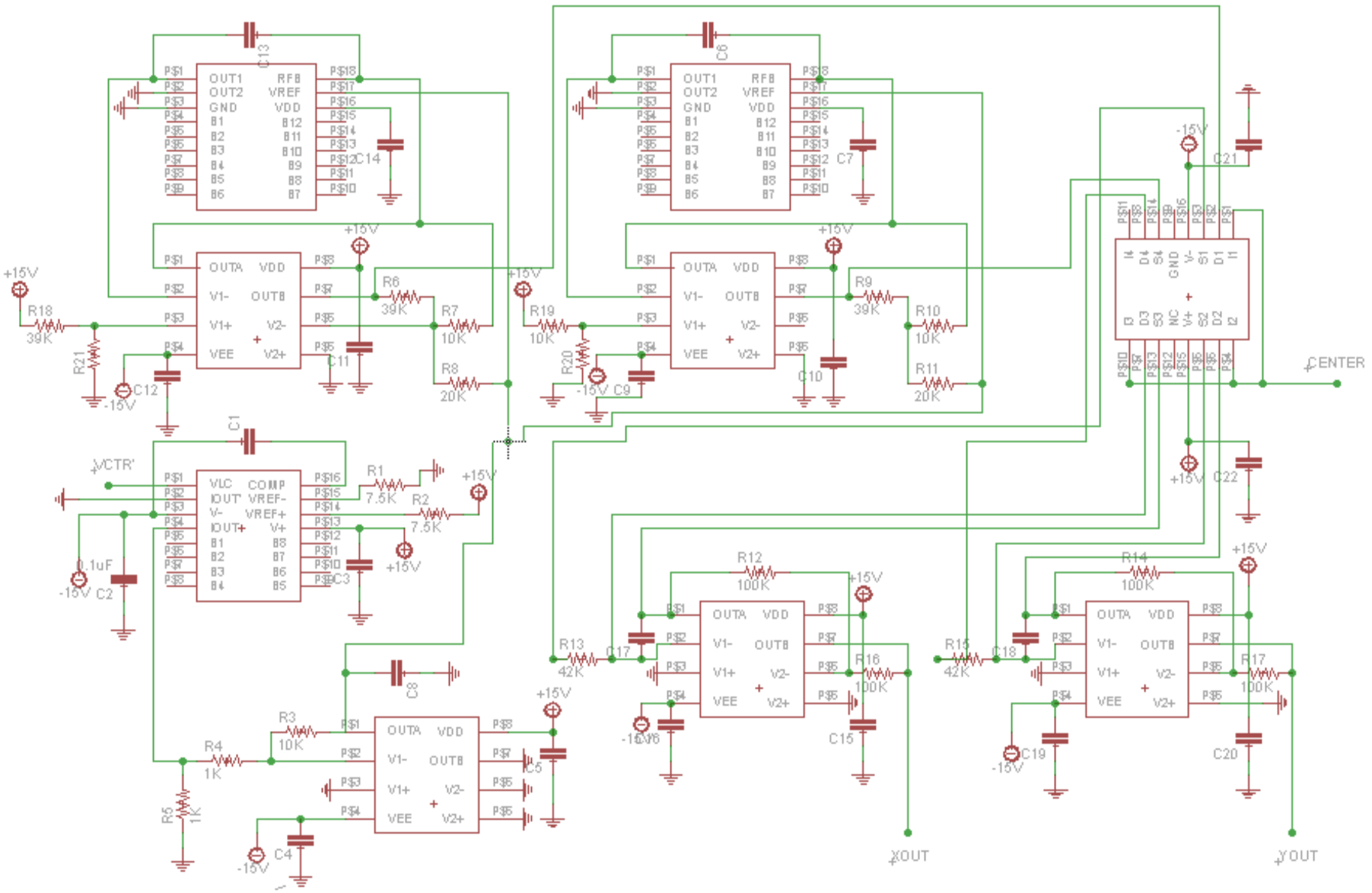


LASER

- Galvanometer Scanner
- Draws vectors on a surface via +/- 5Volt signals received from the output of PCB
- Monochromatic – Red laser

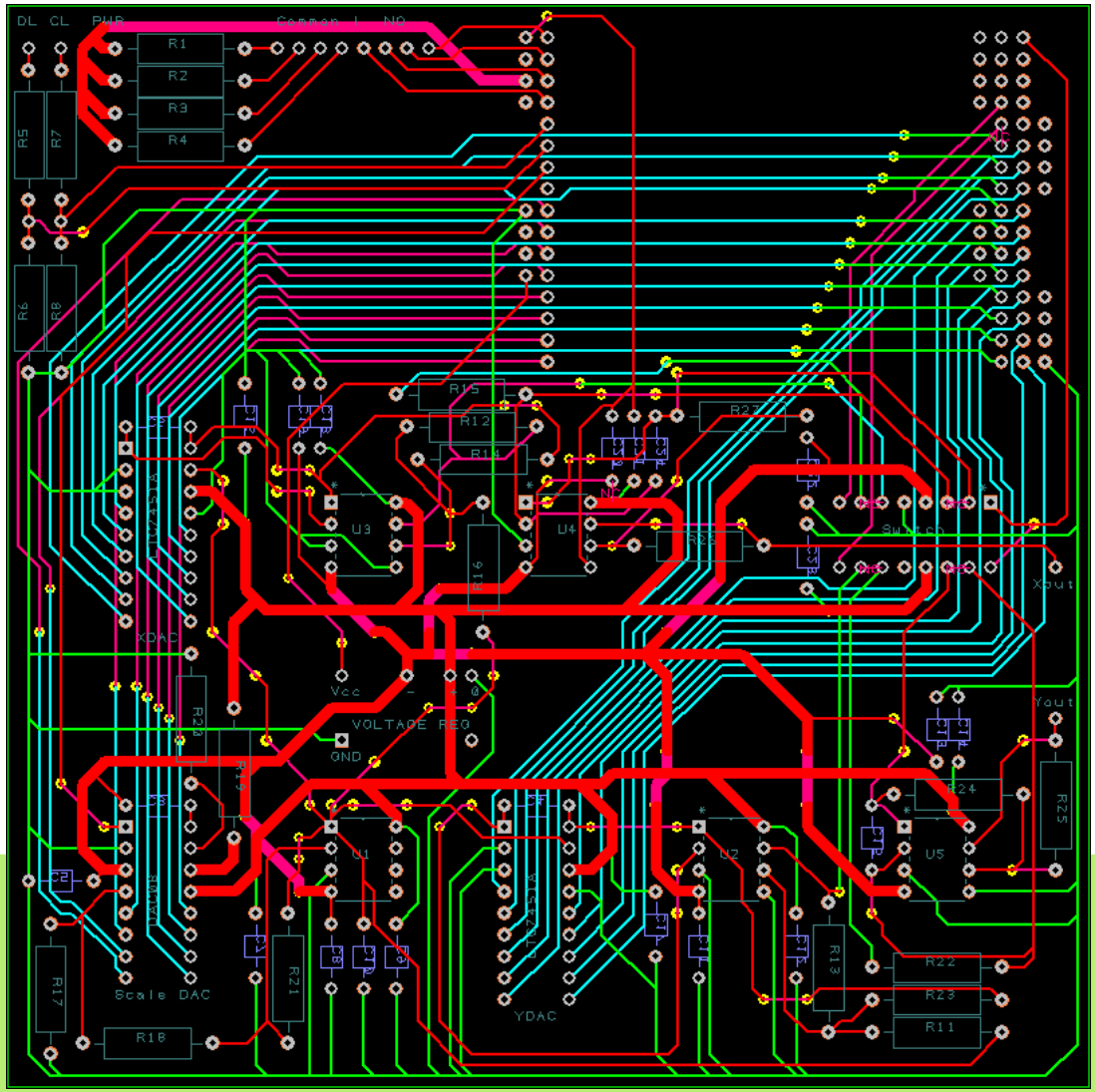


FINAL SCHEMATIC



FINAL PCB DESIGN

- 5” x 5”
- Designed with all through-hole components for simplicity
- 4 layers required



BUDGET

Component	Quantity	Cost Per Unit	Estimated Total Cost	Actual Total Cost
PCM1741E – IC DAC	3	$4.19	$12.57	$28.36
LM324AM/NOPB – IC Op Amp	4	$1.22	$4.88	$10.52
Concave Button	4	$1.95	$7.80	$16.96
NPN-BJT Transistor	2	$0.419	$0.838	$0
CMOS Inverter	2	$0.279	$0.558	$0
Resistors, Capacitors, etc.	NA	NA	≈$5.00	$10.00
Arcade Spinner Wheel	1	$69.95	$69.95	$79.60
Papilio One 500K FPGA Board	1	$74.99	$74.99	$81.41
Galvo-Scanner & Laser	1	$106	$106	$0
PCB Milling Costs	NA	NA	≈$75.00	$39.31
Unforeseen Costs	NA	NA	≈$50.00	$84.08
Total			**$413.59**	**$350.24**