Printer Dover

Spruce version 11.2 -- spooler version 11.2

File: MemC-Rev-Be.sil etc.

Creation date: 23-Sep-79 16:12:37

For: Spruce

26 total sheets = 25 pages, 1 copy.

Problems encountered:
Font HELVETICA24B substituted for font HELVE24.

DORADO SCHEMATICS

Memory Control

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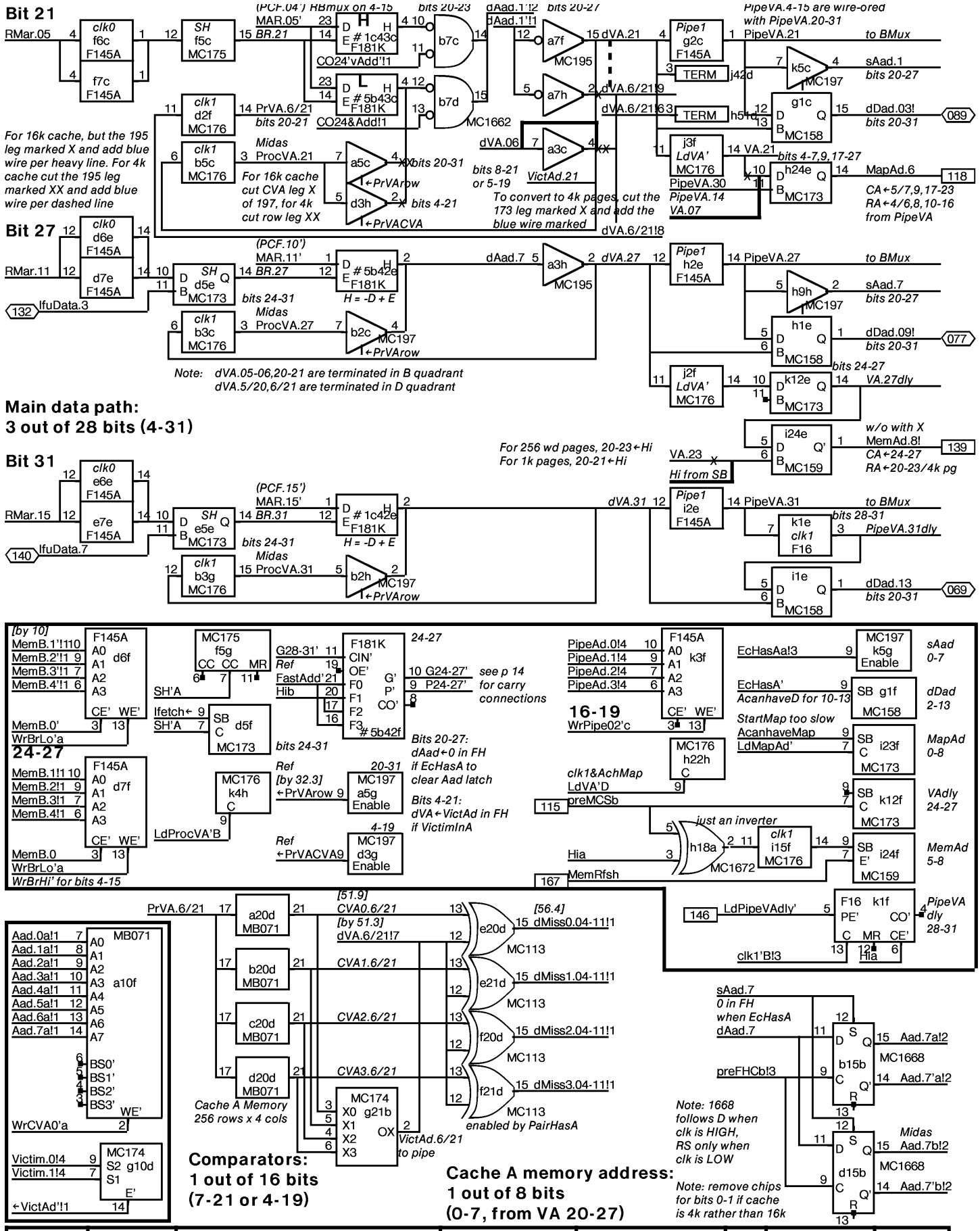
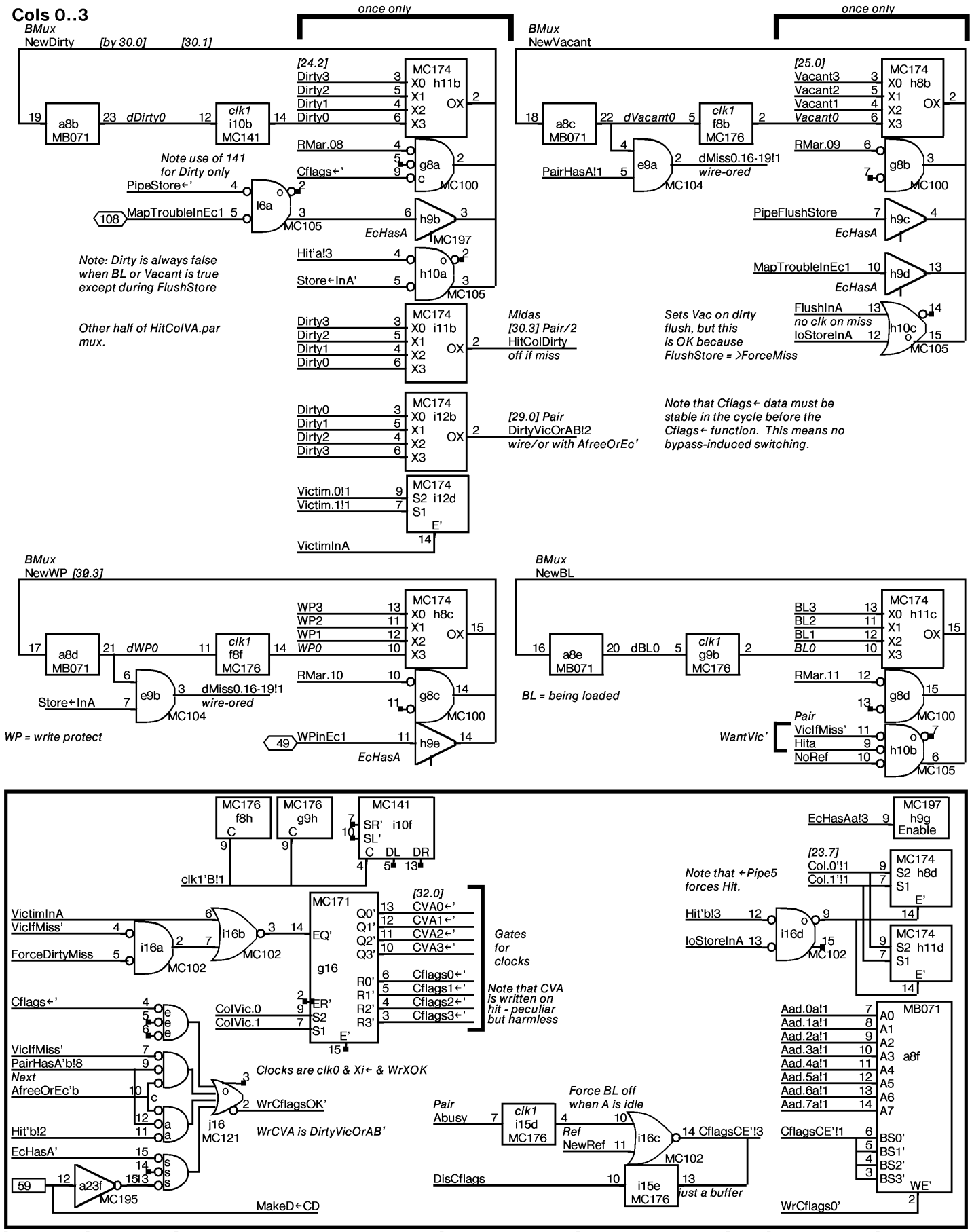
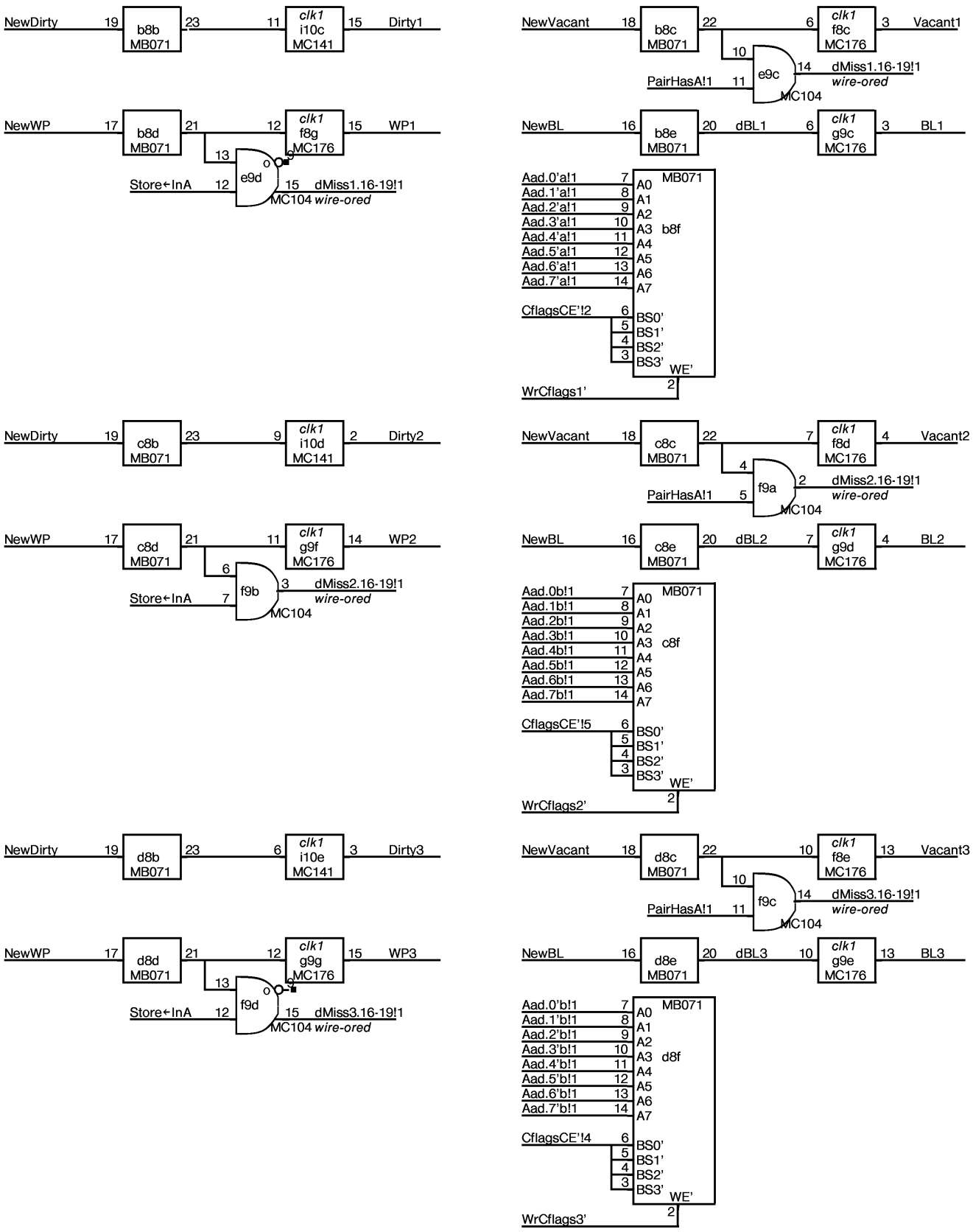
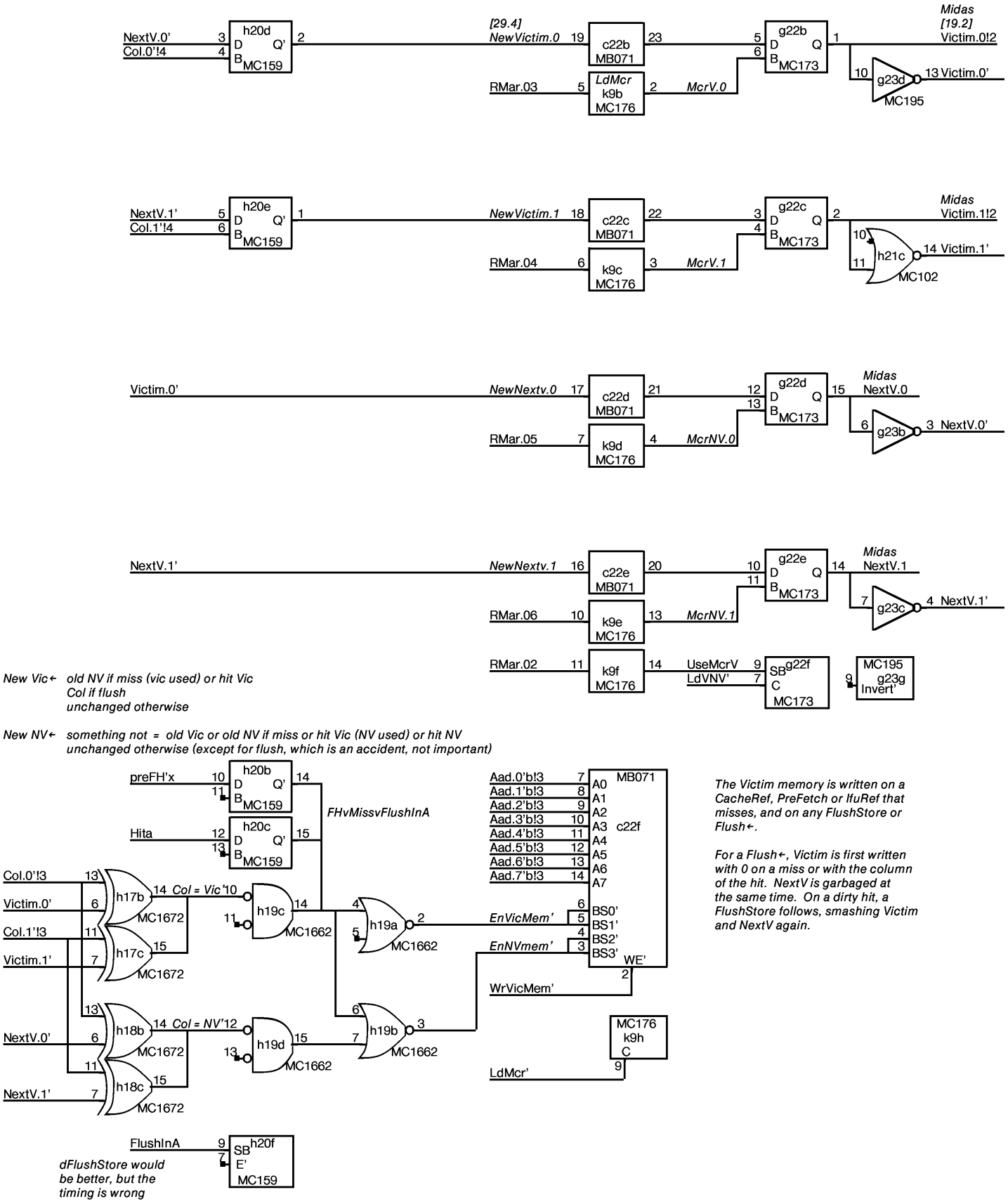

Bit 21
Bit 27
Bit 31
Main data path:
3 out of 28 bits (4-31)
16-19
24-27
Comparators:
1 out of 16 bits
(7-21 or 4-19)
Cache A memory address:
1 out of 8 bits
(0-7, from VA 20-27)
Note: dVA.05-06,20-21 are terminated in B quadrant
dVA.5/20,6/21 are terminated in D quadrant
For 16k cache, but the 195 leg marked X and add blue wire per heavy line. For 4k cache cut the 195 leg marked XX and add blue wire per dashed line
For 16k cache cut CVA leg X of 197, for 4k cut row leg XX
To convert to 4k pages, cut the 173 leg marked X and add the blue wire marked
For 256 wd pages, 20-23←Hi
For 1k pages, 20-21←Hi
Cache A Memory
256 rows x 4 cols
enabled by PairHasA
Note: 1668 follows D when clk is HIGH, RS only when clk is LOW
Note: remove chips for bits 0-1 if cache is 4k rather than 16k
XEROX PARC
Project Dorado
Drawing Main data paths
File MemC01.sil
Designer Lampson
Rev Be
Date 7/01/79
Page 01



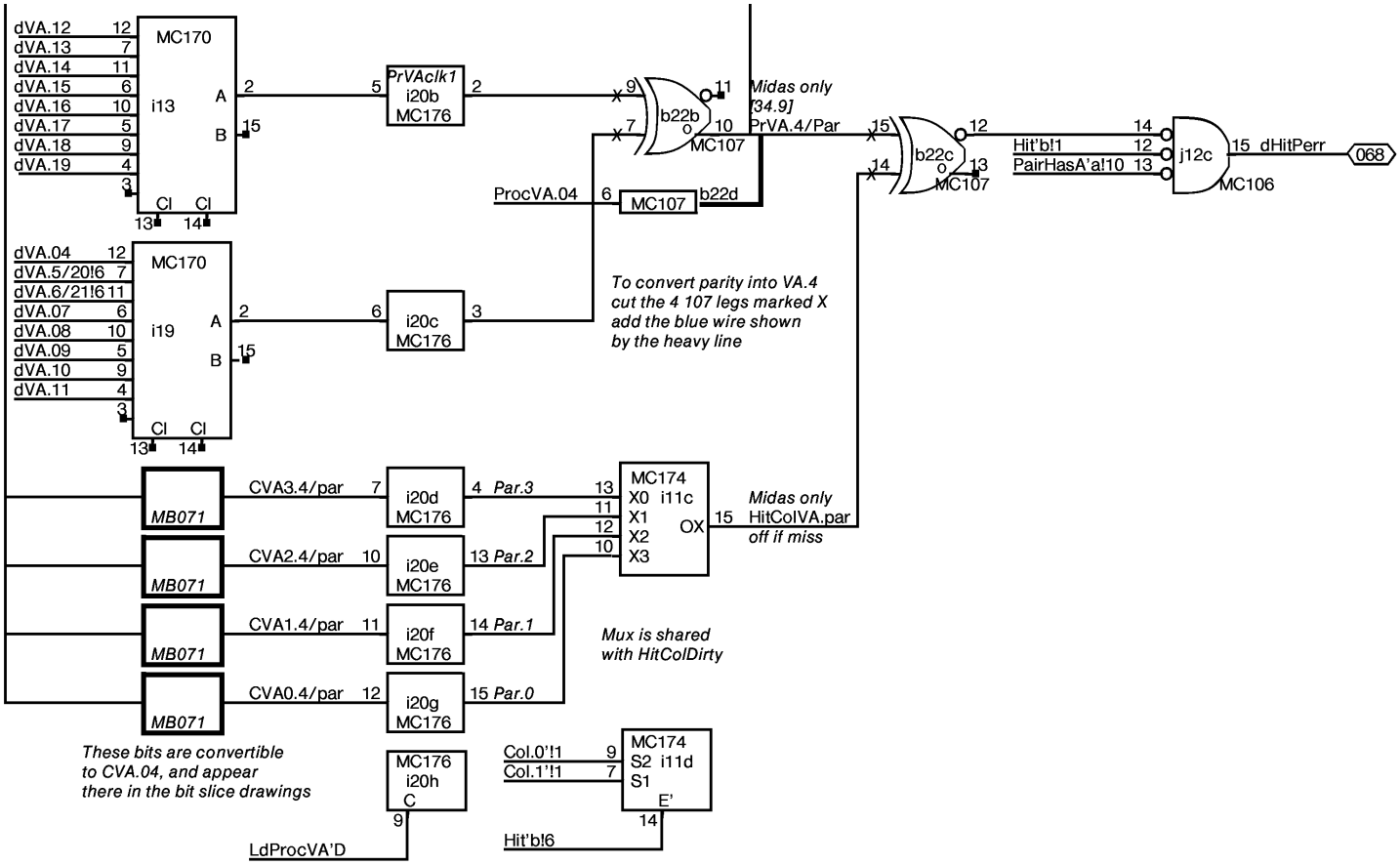
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Cache flags	MemC02.sil	Lampson	Be	7/01/79	02

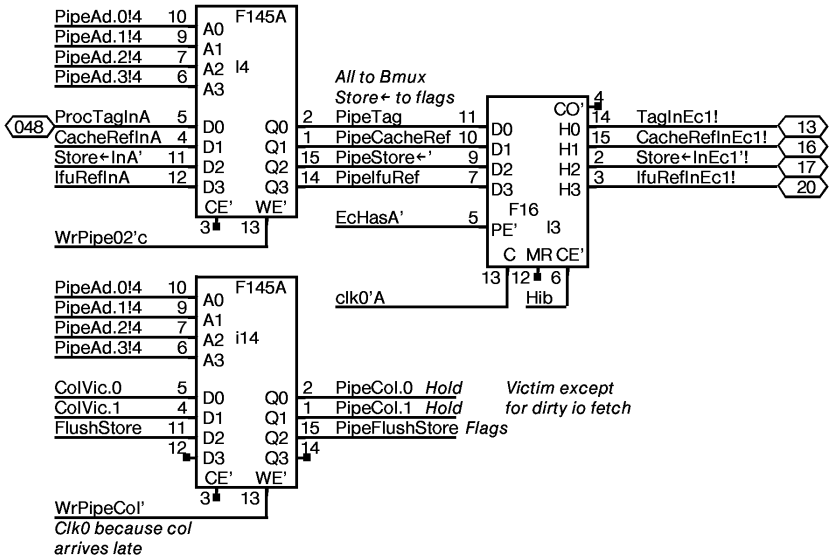


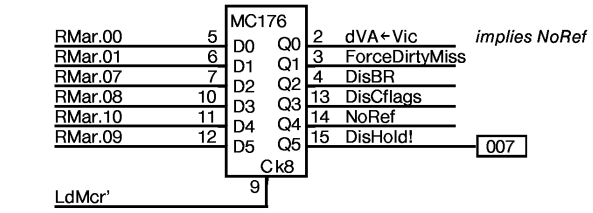
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Cache flags, cols1-3	MemC03.sil	Lampson	Be	7/01/79	03



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Victim + NextVictim	MemC04.sil	Lampson	Be	7/01/79	04

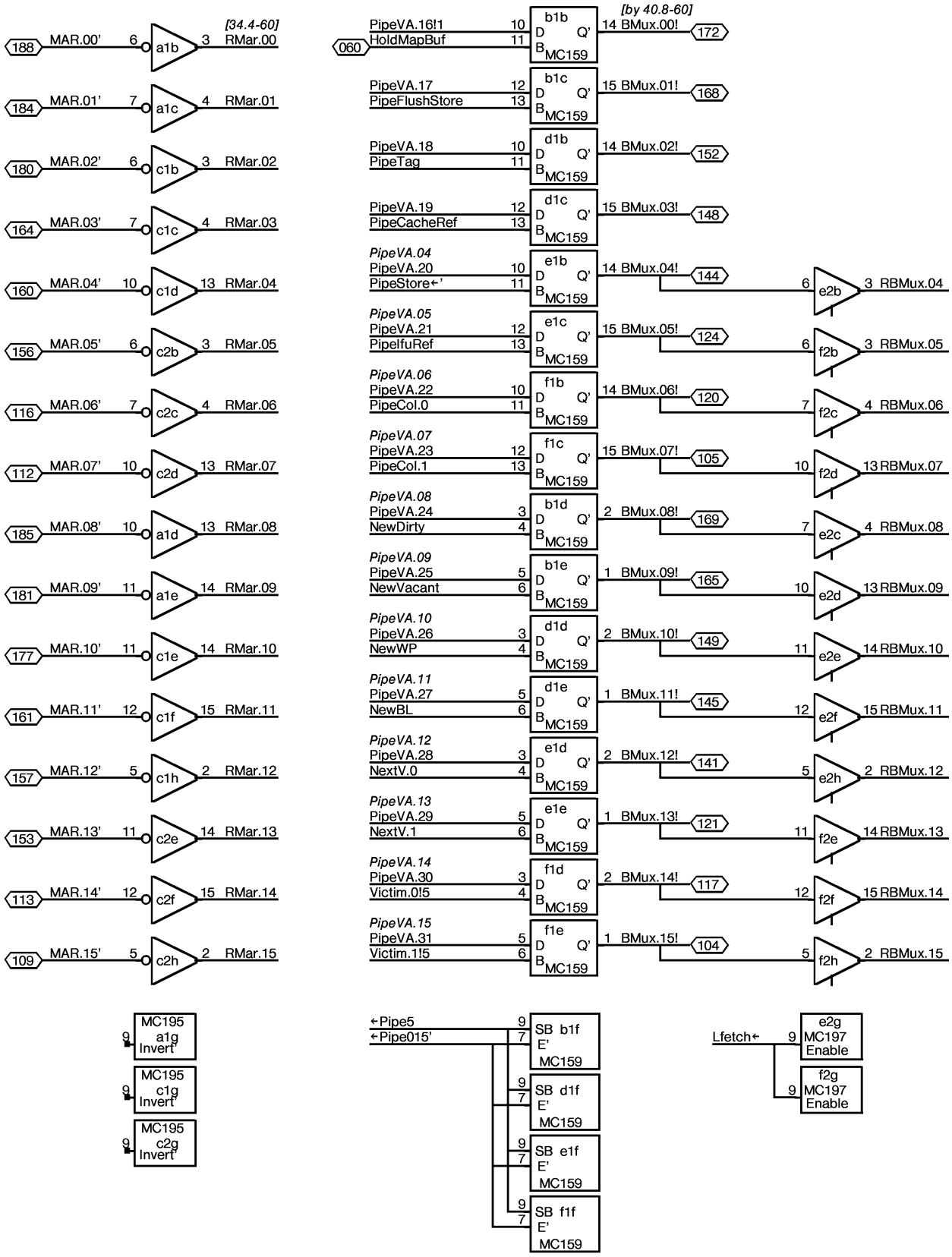




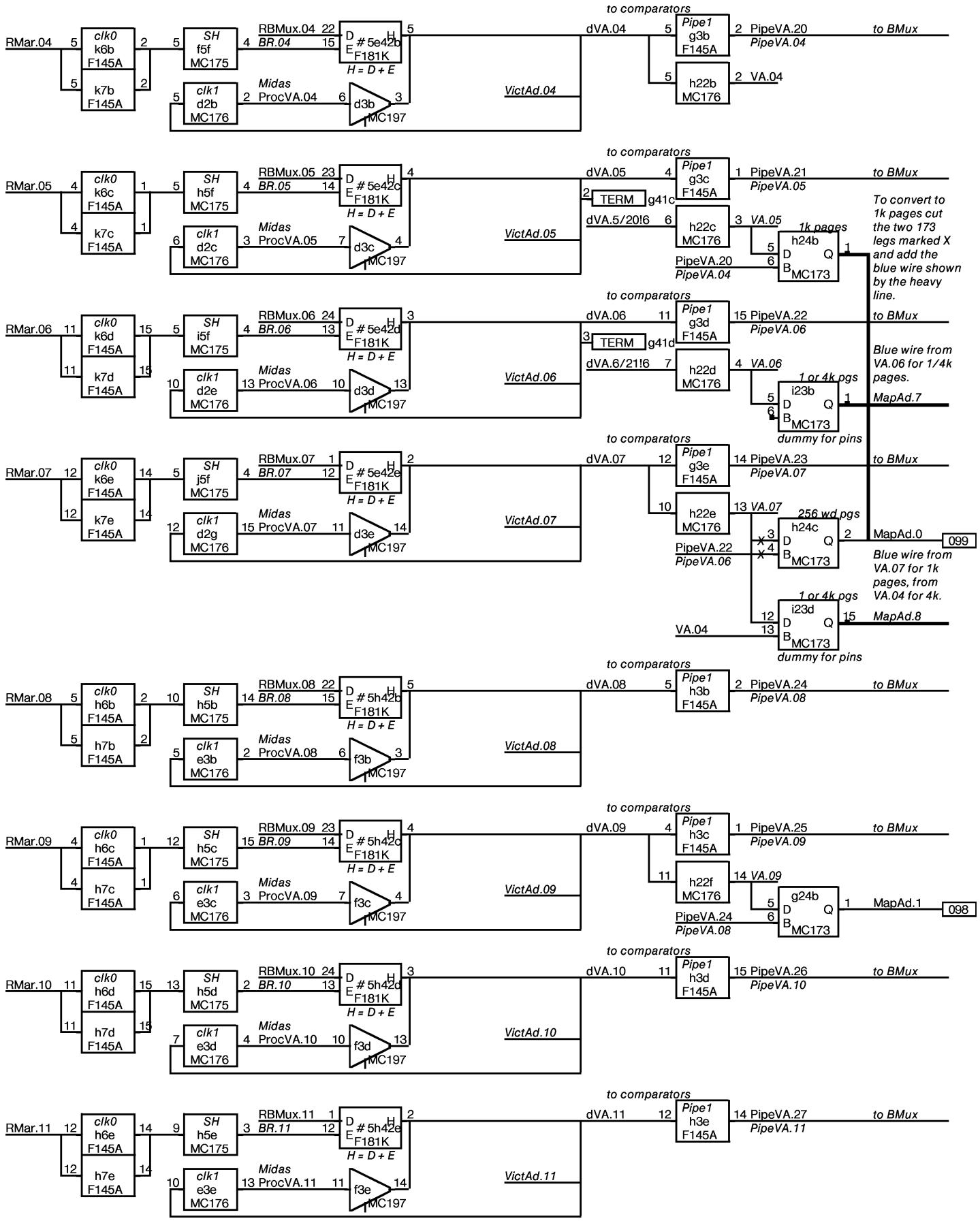


Mcr also includes 5 bits on Vic page

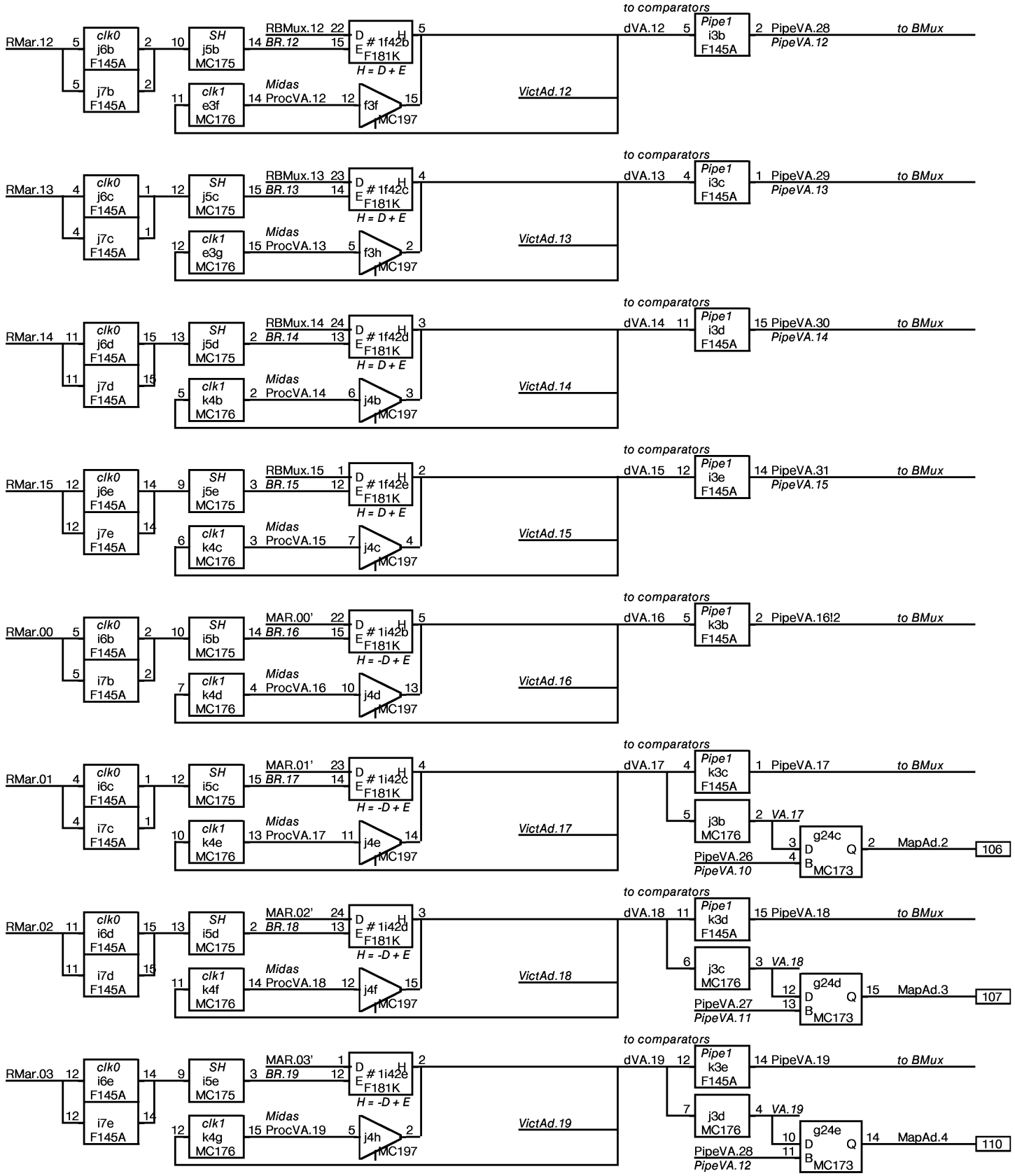
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Parity, pipe, Mcr	MemC05.sil	Lampson	Be	7/01/79	05



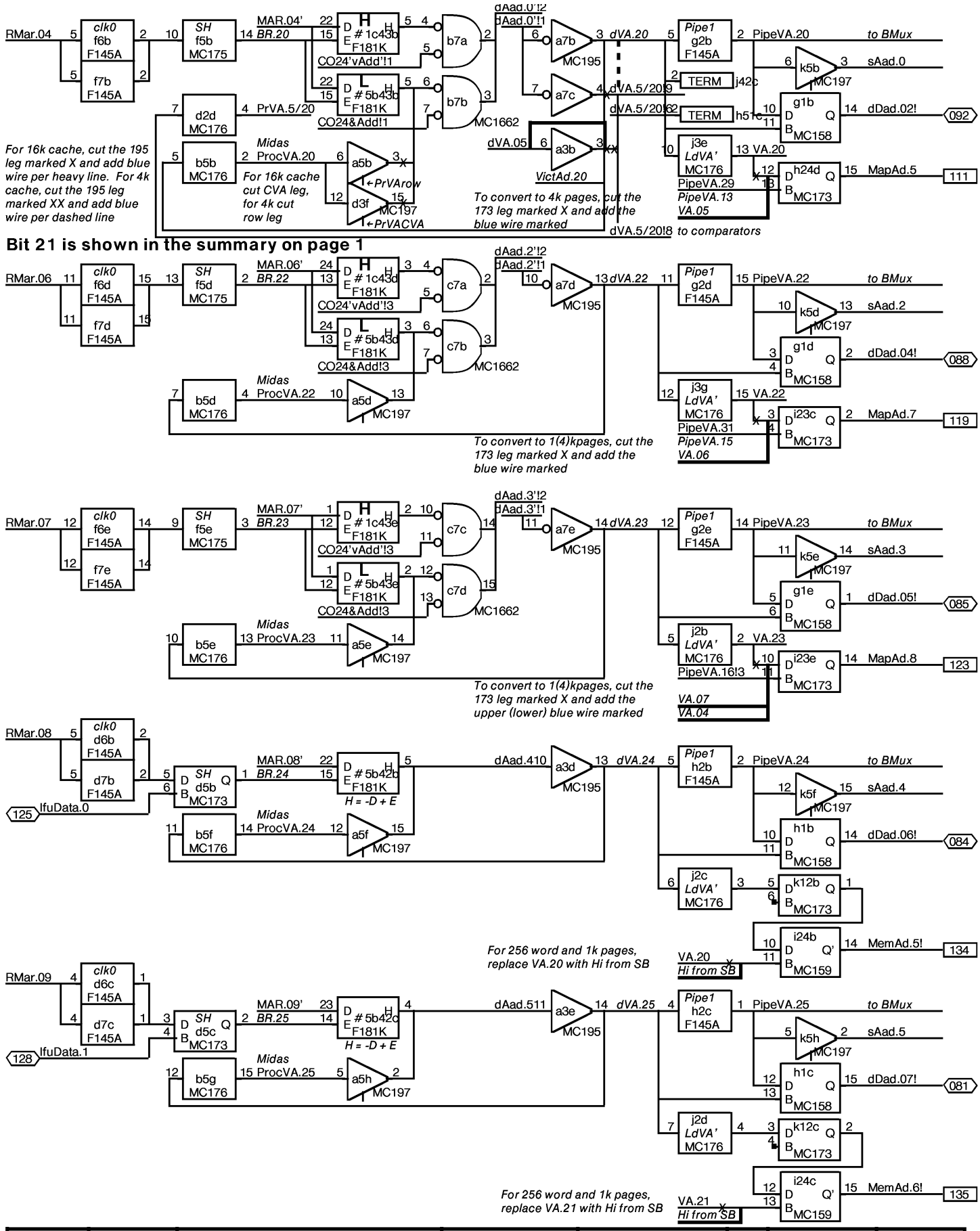
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Mar and BMux interface	MemC06.sil	Lampson	Be	7/01/79	06



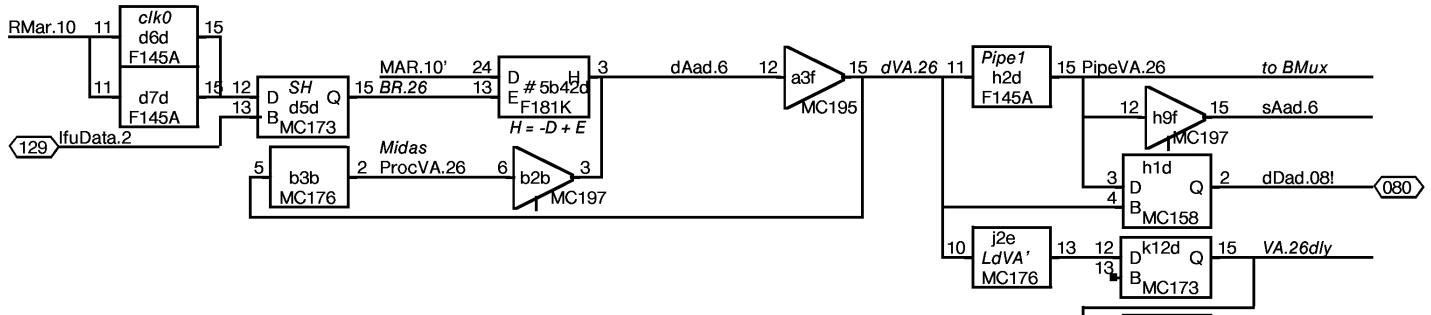
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 4-11	MemC07.sil	Lampson	Be	7/01/79	07



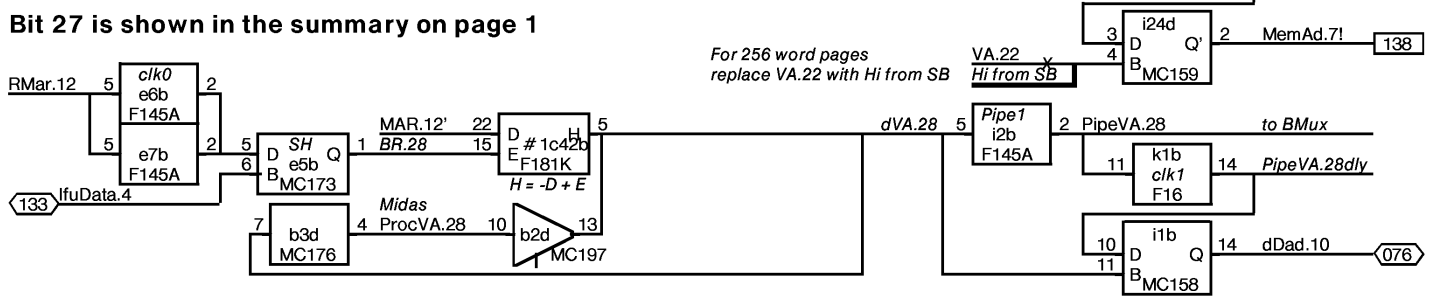
XEROX PARCb	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 12-19	MemC08.sil	Lampson	Be	7/01/79	08

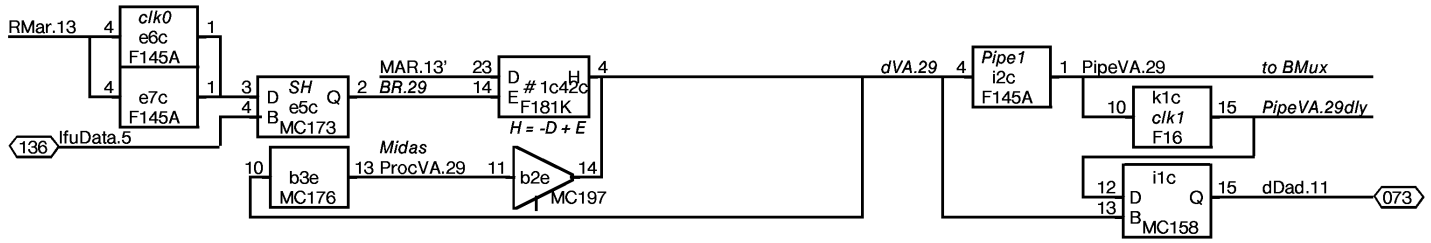


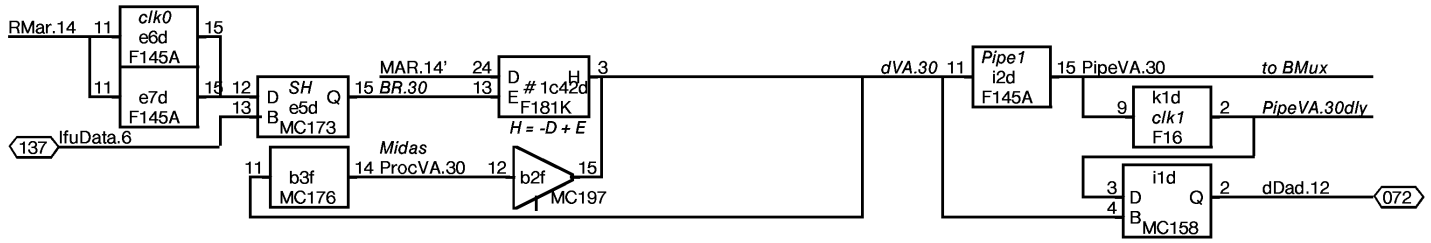
XEROX PARC	Project	Drawing	File	Desiogner	Rev	Date	Page
	Dorado	Main data paths: 20-26	MemC09.sil	Lampson	Be	7/01/79	09



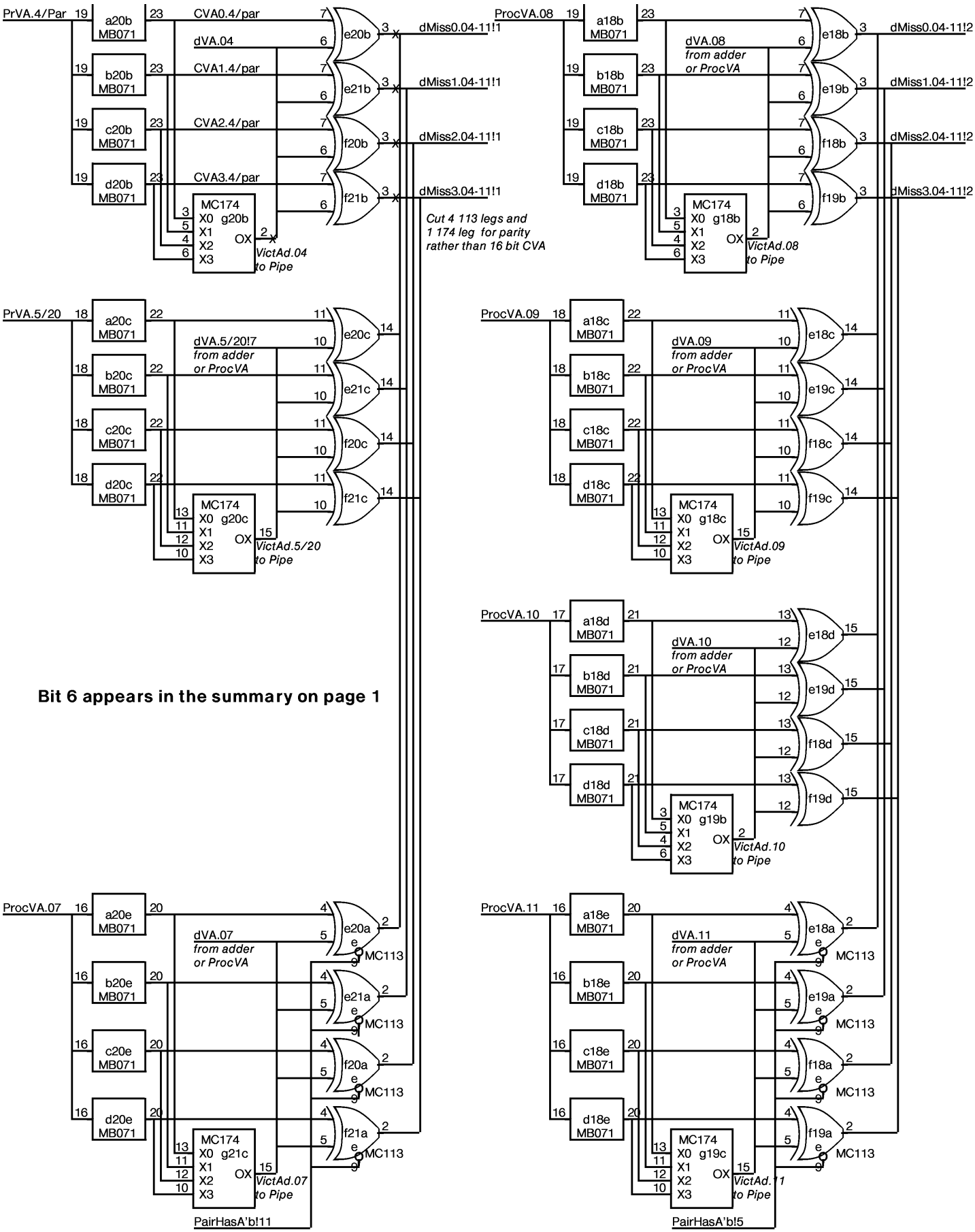
Bit 27 is shown in the summary on page 1



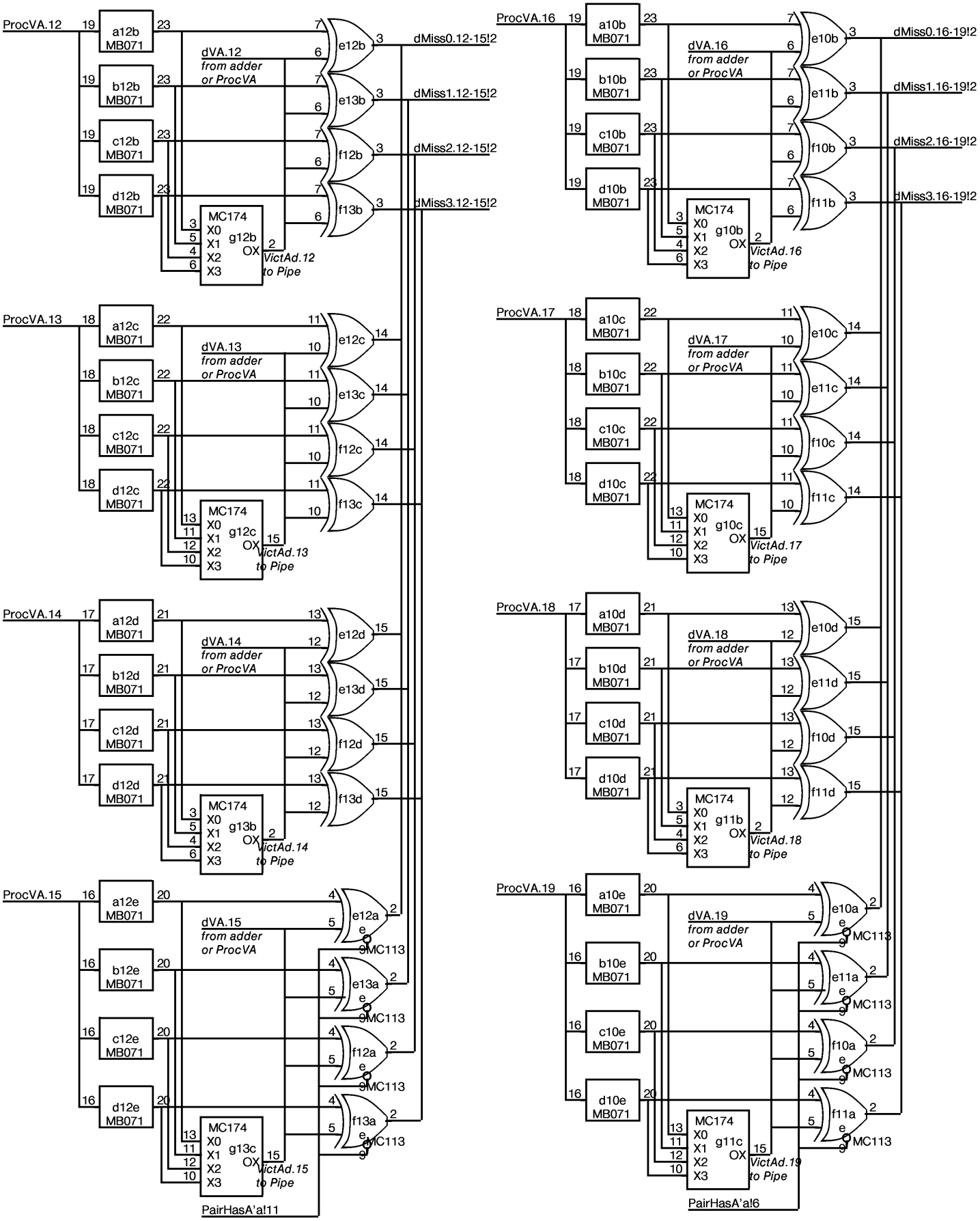




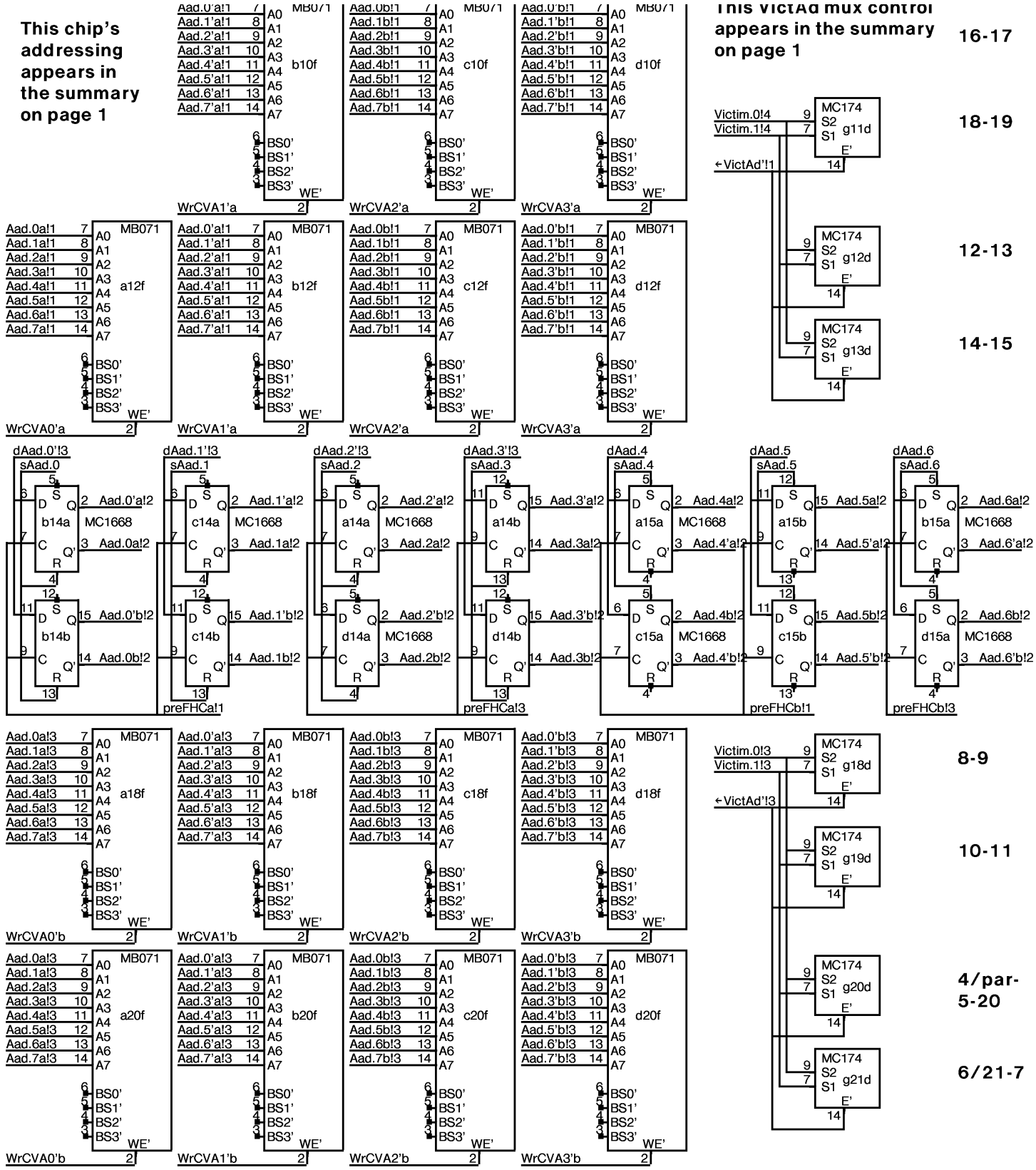
Bit 31 is shown in the summary on page 1



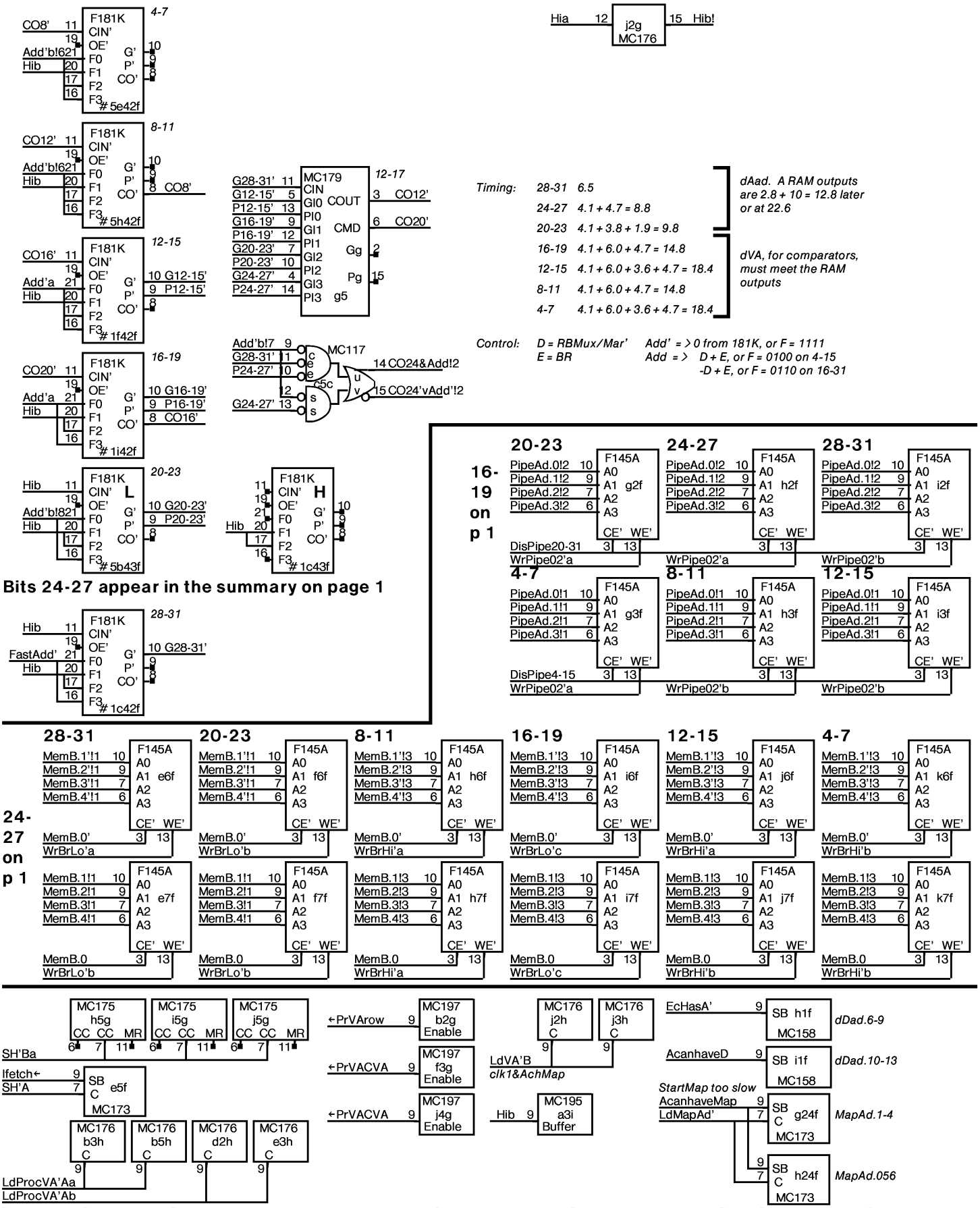
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CVA and comparators: 4-11	MemC11.sil	Lampson	Be	7/01/79	11



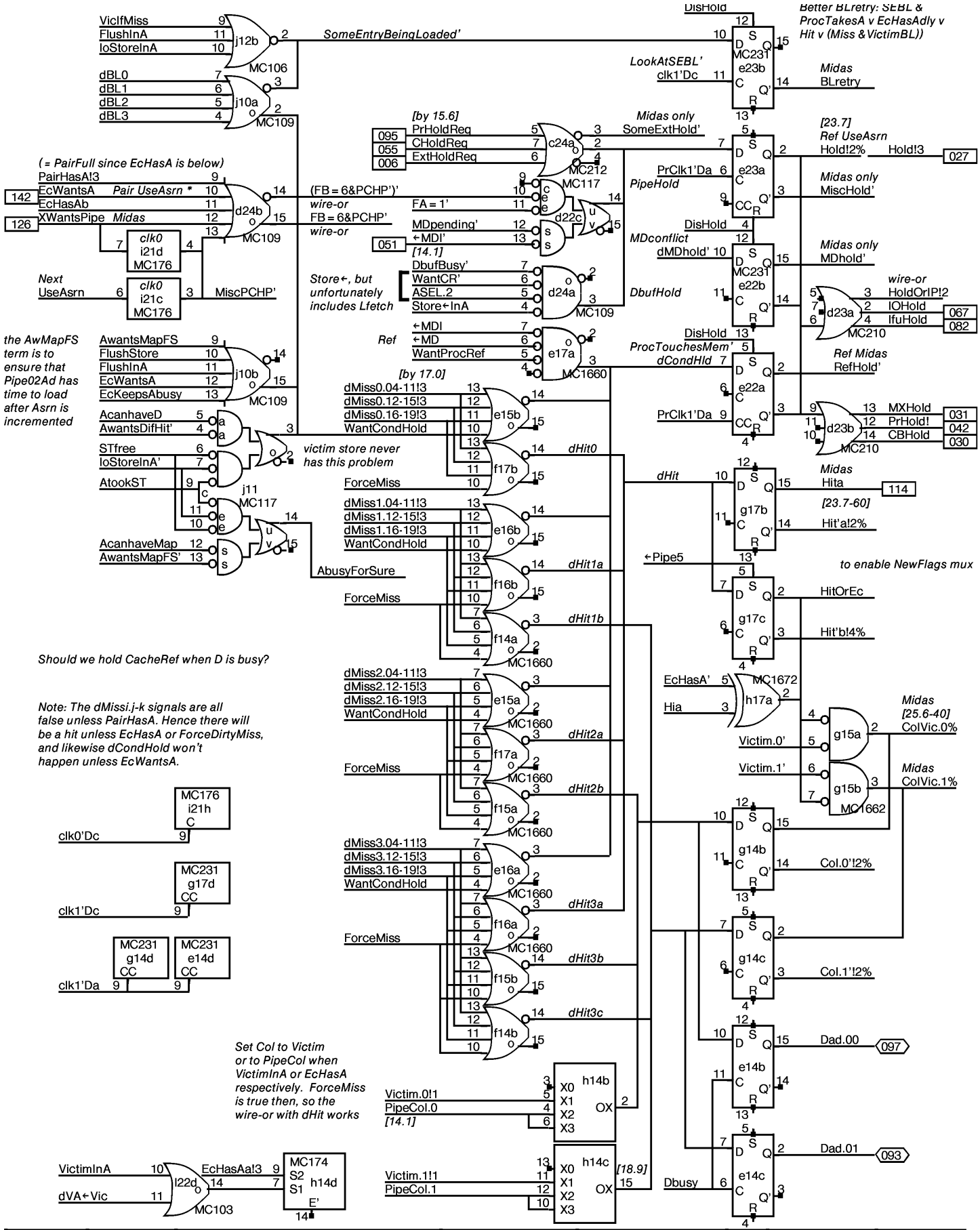
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CVA and comparators: 12-19	MemC12.sil	Lampson	Be	7/01/79	12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	A memory addressing	MemC13.sil	Lampson	Be	7/01/79	13



XEROX PARC	Project: Dorado	Drawing: Carry logic and misc control Pipe and BR addressing	File: MemC14.sil	Designer: Lampson	Rev: Be	Date: 7/01/79	Page: 14



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Miss, Hold	MemC15.sil	Lampson	Be	7/01/79	15

FIRST HALF

015 ASEL.0 13 b24c 9 Hold WantProcRef
IgnoreProc12 15 MC103 UseAsrn Pair WantProcRef'!2
WantProcRef'!1

023 ASEL.1'! 6 a23b 3 Hold ASEL.1

[10.3] 011 FF.0mem'

MC117 d22b 3 [14.1] Pair WantCR
Hold WantCR'

CacheRefInA' 5 Dbusy 4 b24a 2 MC103

34 ProcTag 5 35 MDMtag' 4 b22a 3 MC107 [18.1] MDMdataGood [18.9] dMDhold'

044 DdataGood' 4 e e e DdataGood

38 At=Curt' 9 DcomingIfHit' Hold
19 ←MDI [by 15.1] 10 c
39 DcomingForCt' 12 a 11 a b23 MC121 3 o 2 ←MDI' and DmaybeComing and CondHold will hold the instruction if there is a miss
←MDI' and Dcoming from Ec

15 s 14 s 13 s DontWantResp

[by 12.3] Hold 18 ←MD 7 D S Q 2 MC231 C j15a Q' 3 CC R 4 5
IgnoreProc 6
clk1'Db 9

←MDdly' 62
13 k23d 9 12 clk0 i21g MC176 15 Hold MDpending'
HoldOrIP 15 MC101

11 b24d 14 WantAltRef' MC103
WantProcRef'!3 10

Pair 014 EmuOrFT' 9 k16b 7 Pair WantPrivRef' UseAsrn WantPrivRef
11 6 MC105
Wprefetch← 10

026 ASEL.2'! 7 a23c 4 Pair ASEL.2 7 b24b 3 Pair Store←IfCR'
6

MC162 a24 Q0 6 Q1 5 Q2 4 Q3 3 Q4 13 Q5 12 Q6 11 Q7 10 E' E' 15 2
14 S4 9 S2 7 S1
5 clk1 i15b 2 Main Lfetch←
Main Ifetch←

[10.3] Pair 022 FF.1mem

MC176 i15h C 9 clk1'Db

9 MC195 a23g Invert'

Note: Ref signals not gated with Hold have Want in their names.

SECOND HALF

sloppy, but OK because VictimInA is true for many cycles

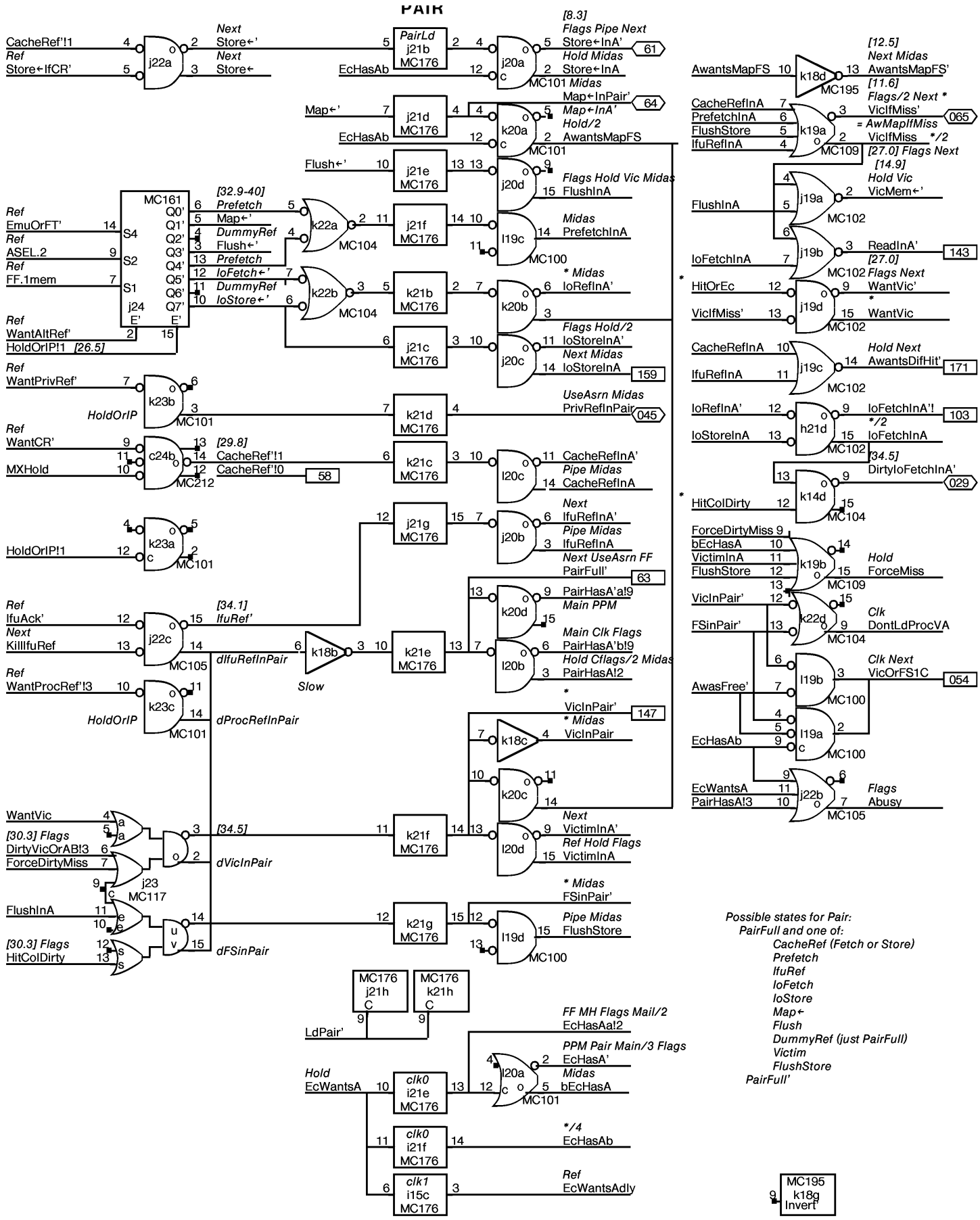
VicInPair 4 dVA←Vic 5 k17a 2 MC103 ←VictAd 5 k18h 2 MC195 ←VictAd'!2

WantProcRef'!0 7 D S Q 2 c17a C MC231 Q' 3 CC R 4 5
clk1'Da 6
[23.7] Hold!1 10 11 g15c 14 MC1662 [27.0] Flags NewRef 5 h15a 2 MC102 [30.8-60] ←PrVACVA
12 13 g15d 15 MC1662 Pair EcWantsAdly 6 7 h15b 3 MC102 Midas ←PrVArow
Main
Hit'a!3 12 13 h15d 9 MC1662 Pair IfuAck' 7 5 6 h16a 3 4 2 MC211 [29.8] Add'a Add'b!9% FastAdd'%
UseAsrn IfuAckIfHit' 15 MC102 IfuAck! 183

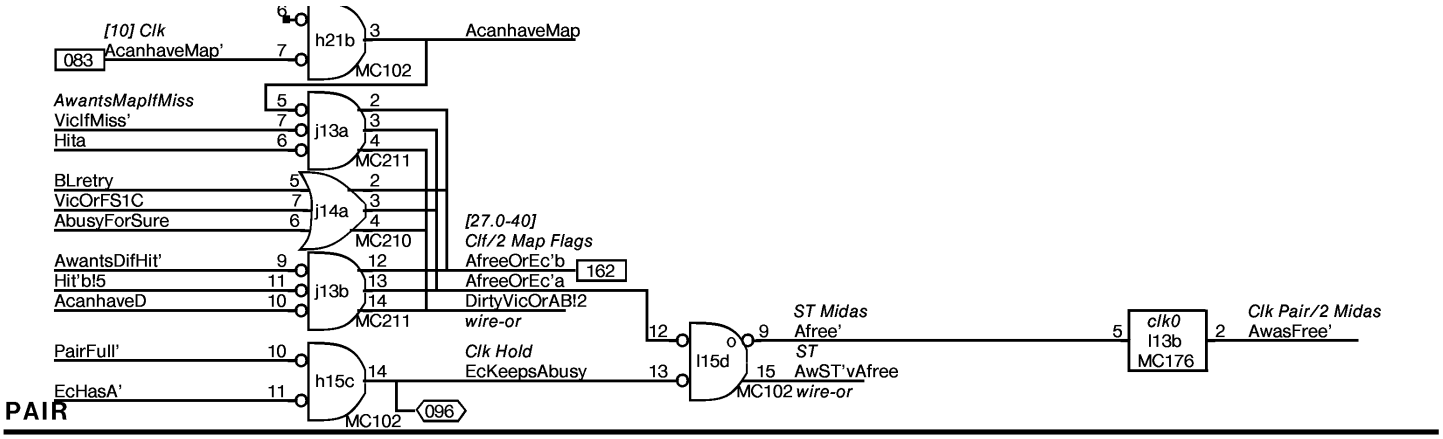
131 WantIfuRef' 10 D S Q 15 clk1 d17b C Q' 14 R 13 12
Hold WantCondHold 7 D S Q 2 clk1 d17c C Q' 3 R 4 5 6
Midas only WantCHdly'

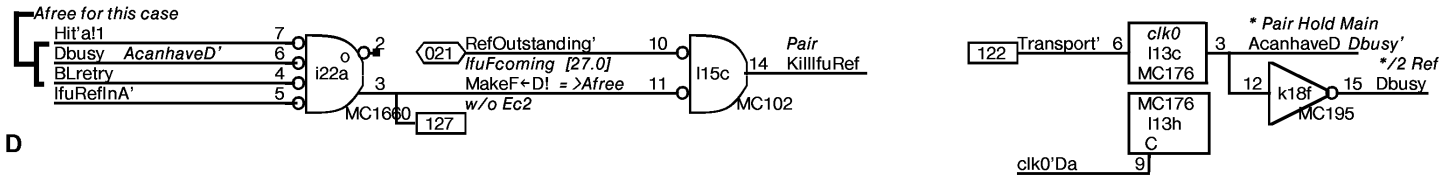
MC231 d17d CC 9 clk1'Da

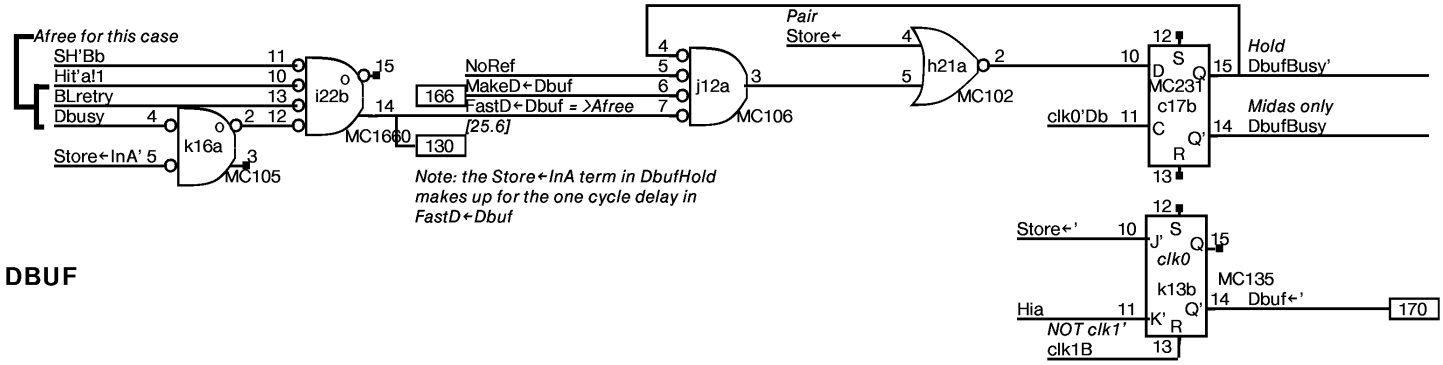
XEROX PARC	Project Dorado	Drawing Ref decoding	File MemC16.sil	Designer Lampson	Rev Be	Date 7/02/79	Page 16

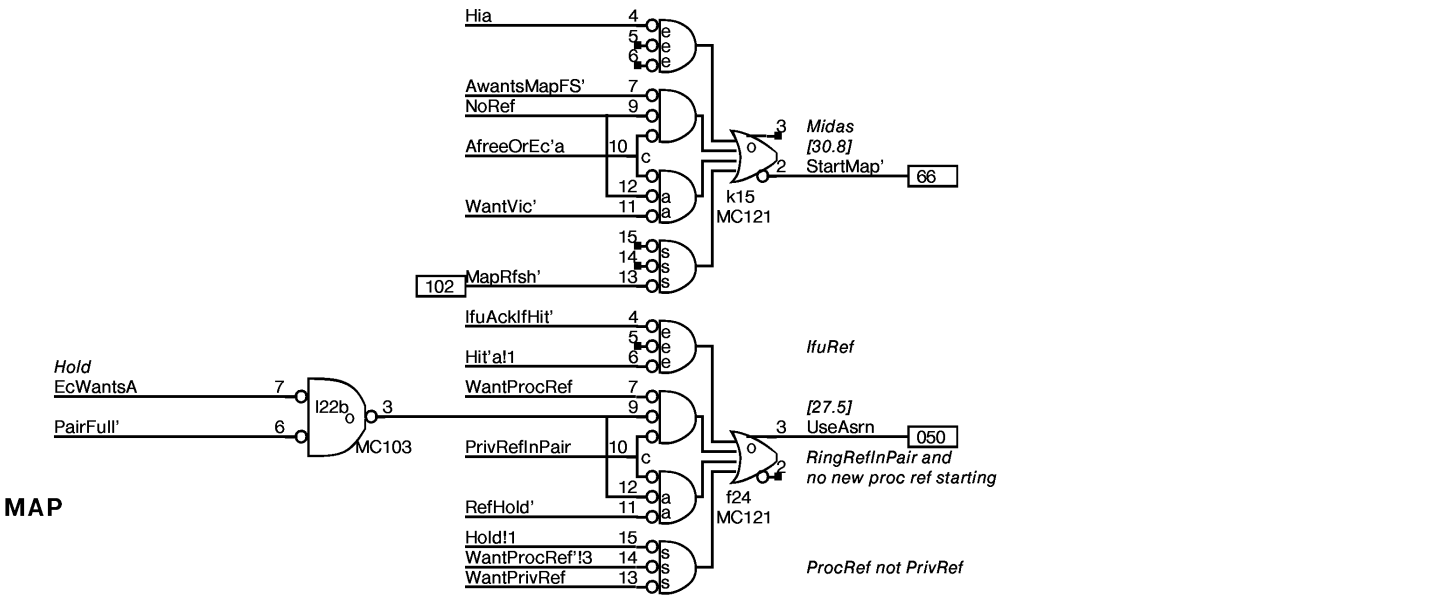


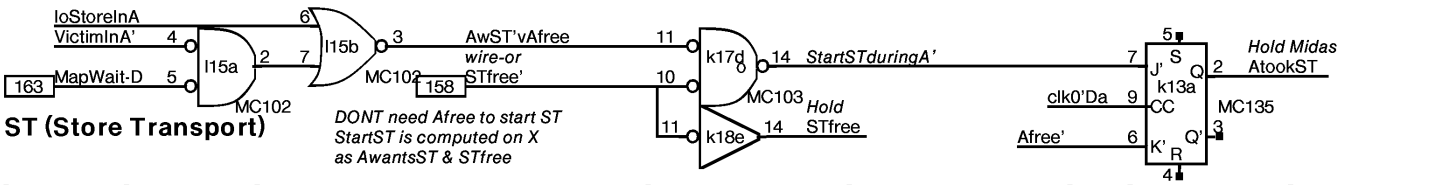
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Pair	MemC17.sil	Lampson	Be	7/02/79	17



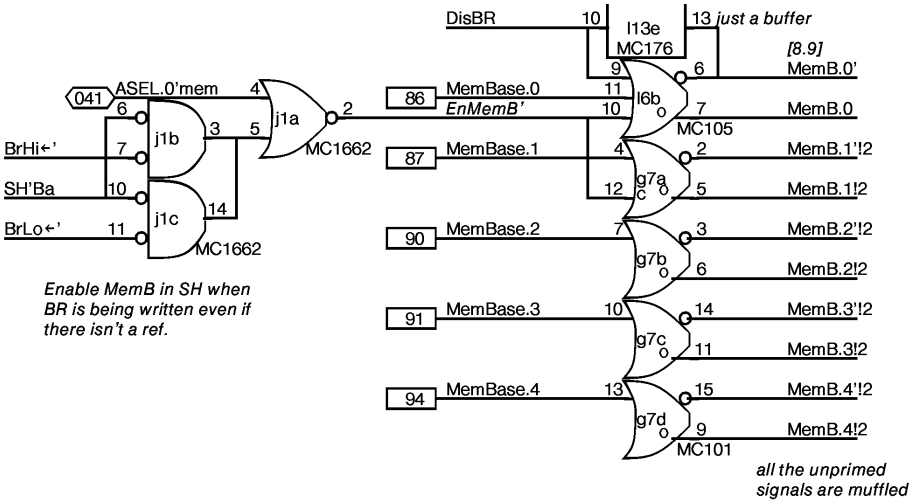


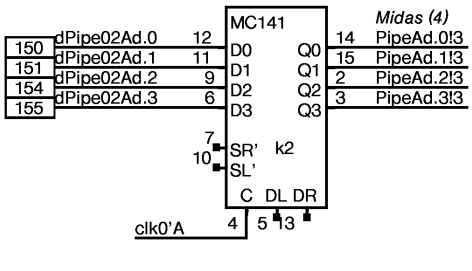


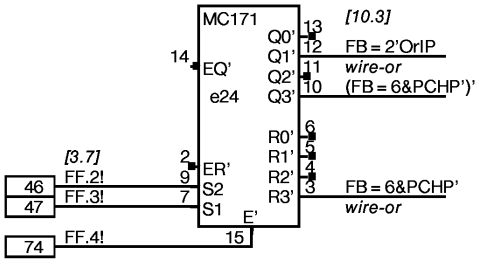


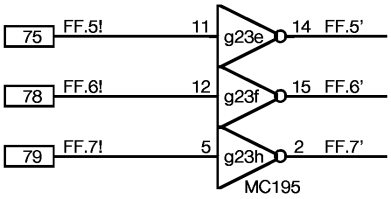


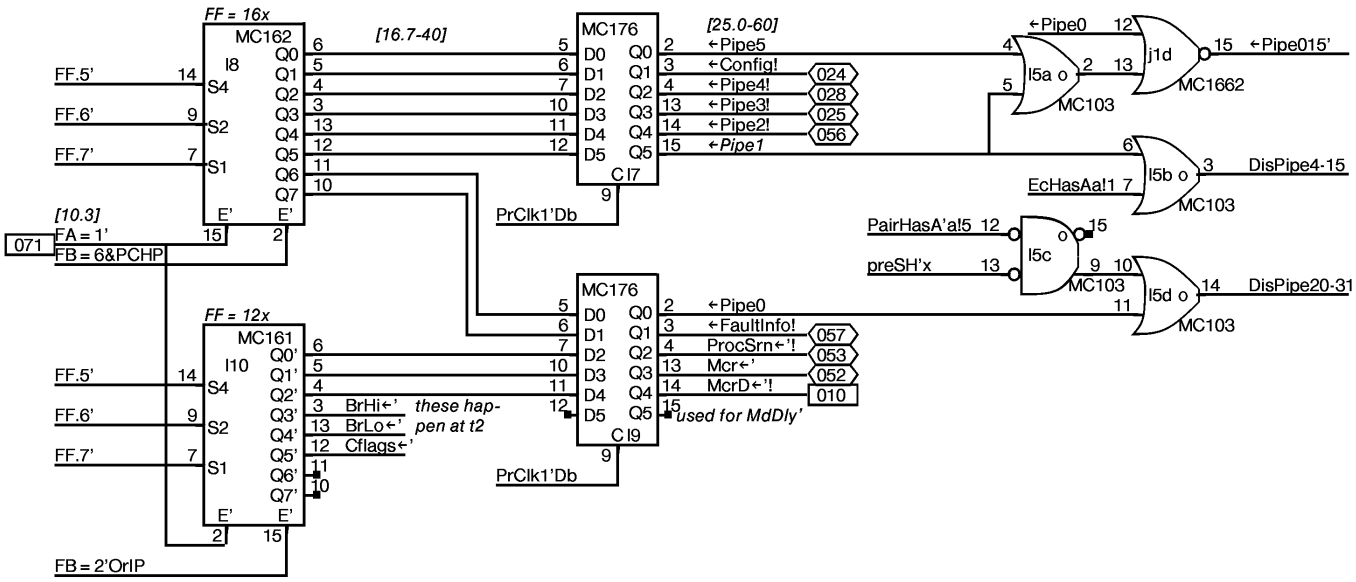
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Next	MemC18.sil	Lampson	Be	7/02/79	18



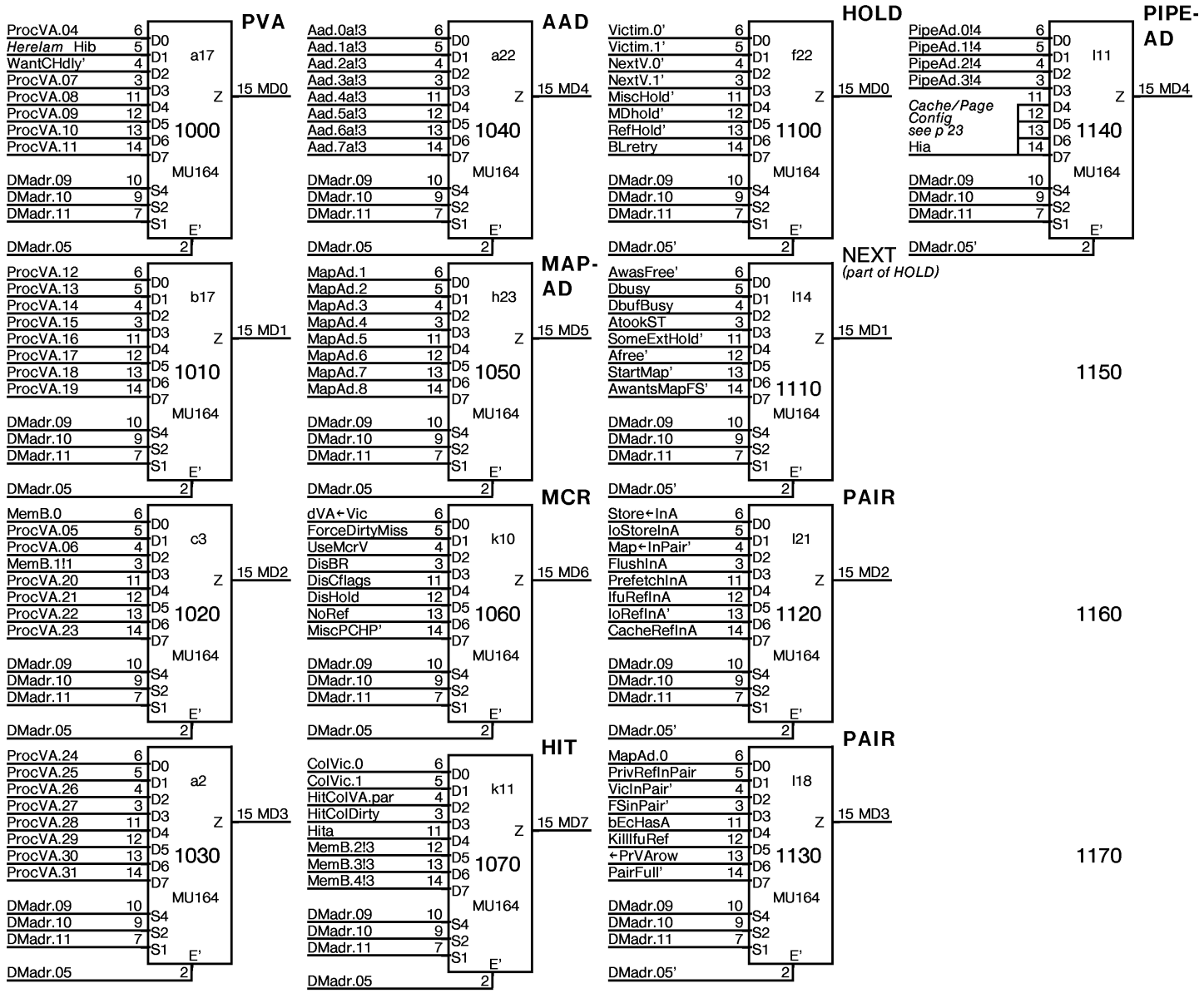




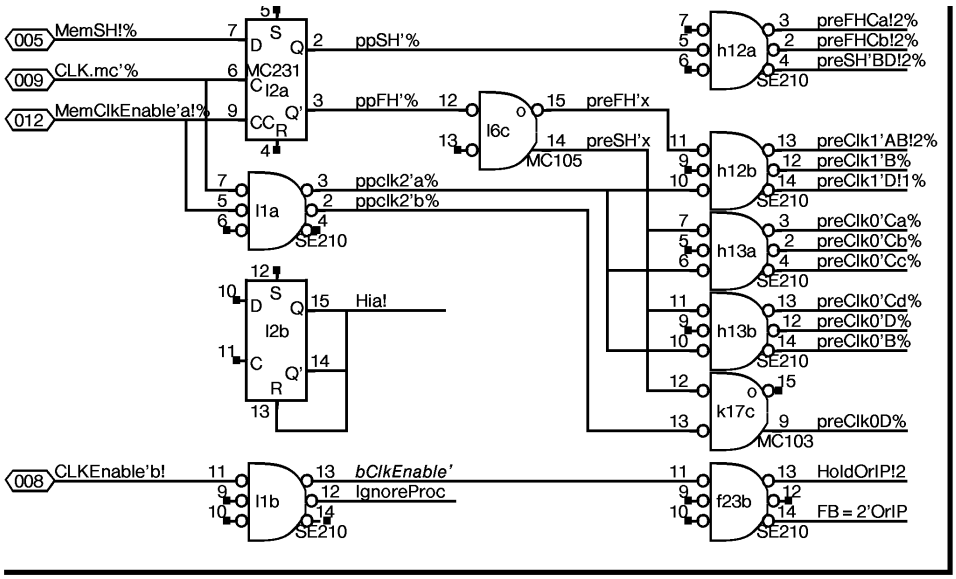


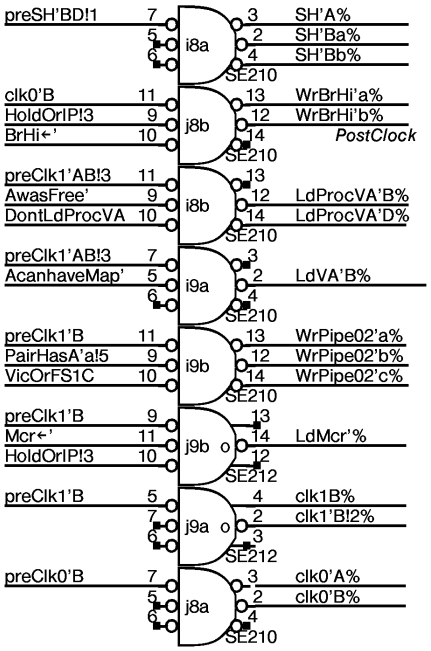


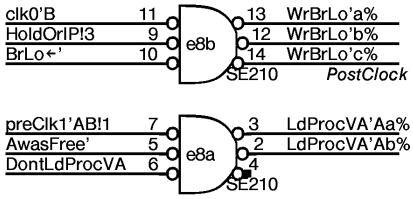
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	FF decoding, PipeAd, MemB	MemC19.sil	Lampson	Be	7/01/79	19



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Midas control and mufflers	MemC20.sil	Lampson	Be	7/01/79	20





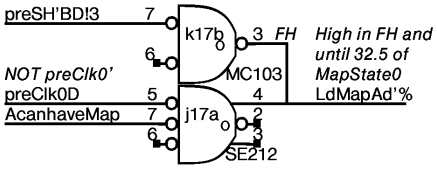


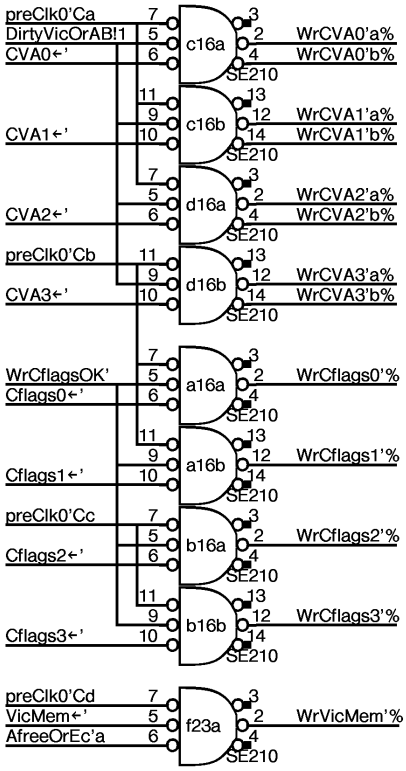
MapAd must be

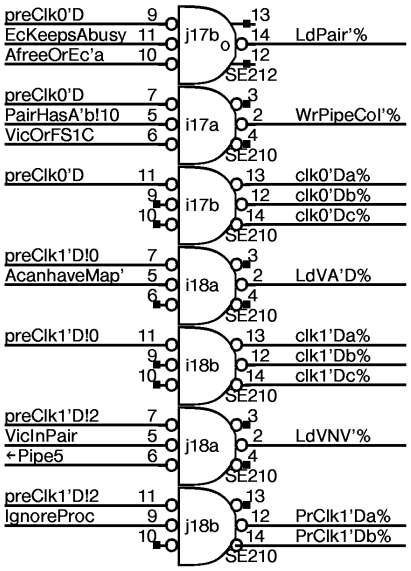
low by 12.8 before clk0 of StartMap
to: let row MapAd through by 6 before clk0

high from clk0 or StartMap to 27.5 after
to: hold row MapAd

low by 2.8 before clk0 after StartMap
to: let col MapAd through by 4 after clk0







XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clock distribution	MemC21.sil	Lampson	Be	7/01/79	21

	a	b	c	d	e	f	g	h	i	j	k	l
1	RMar 0189 DMadr.2,5 195i	BD 0189	RMar 2-4,10-12 195i	BMux driver 231011	451213	671415	2-5 158	6-9 dDad 2-13	10-13 158	MemB←37 ←Pipe015' 1662	PipeVAdly 28-31 F16	Clock 210
2	MU ProcVA 24-31	Proc 197	5-7,13-15 195i	176	RBMux 4, 8-12 197	5-7,13-15 197	Pipe 20-31 PipeAd!2		VA Hib	PipeAd!3 141	ovh Hia 231
3	dVA buf 22-27 195	VA/dr 26-31 176	MU PrVA56,20-23 MemB.0-1	ProcVA & dr 197	& 5/20,6/21	4-13 197	Pipe 4-15 PipeAd!1		17-27 176	Pipe 16-19 PipeAd!4	PipeTag F16
4	24-27 181k	Adder	28-31 181k	4-7 181k	Adder	12-15 181k	8-11 181k	Adder	16-19 181k	ProcVA & dr 197 14-19 176	145
5	ProcVA & dr 197 20-25 176		Cout.24' 117	IfuD/BR 24-31 173	173	BR latch 4,20-23 175	Cout12,20' 179	5,8-11 175	BR latch 6,16-19	7,12-15 175	sAad.0-5 197	disPipe/3 ←Pipe15' 103
6	20-23 181k L	Adder	H 20-23 181k	Base register RAMs			+	Base register RAMs				MemB.0! D←ec,pSHx 105
7	dVAbuf.20-23 dVA.56/2021 195i	dAad.0-3 mux 1662	1662	24-27 145	28-31	20-23 145	MemB.1-4 101	8-11 145	16-19	12-15	4-7 145	FF PRclk1 176
8	Aada	Aad'a Cache flags	Aadb	Aad'b	LdProcVA' WrBrHi' 210	Cflags reg 176	Cf←RMar 100	New 174	Clocks		Mcr 176	decod- 162
9					Miss←Cflags 104	104	Cflags reg BL + 176	sAad 6-7 197			176	ing PRclk1 176
10		A bits 16-19			Comparators		Victad	Cflags 105	Dirty 141	SEBL WantCH 109	MU Mcr	161
11					16-19		16-19	174	HitColDirty Parity 174	AbusyFS WantCH 117	MU MemB.2-4 +5	MU PipeAd +4
12		A bits 12-15			Comparators		Victad	Pre 210	DirtyVicOrAB 174	dDbufBusy! dHitPerr SEBL 106	VAdly 173	+
13					12-15		12-15	clocks 210	dVA.12-19 parity 170	Afree 211	Dbuf←' AtookST 135	Next/2 MB.0 176.0
14	2/3	0 1 Aad latches		2/3	Dad.0-1 231	Col	Col.0-1 231	PipeCol 174	145	210	DirtyIoF! 104	MU
15	4/5 1668	6/7	4/5	6/7 1668	Hold	1660	ColVic.0-1 NewR,HorEc 1662	IfuAck'! ←PrVA/2 EcKeepsAB 102	Lfetch EcwAdly ABdly MCS 176.1	←MdDly' 231 1	StartMap 121	Afree! AwST/2 KillIfuRef 102
16	CVA/Cflags clocks 210			210	1660	Hit	Clk En 171	Add' 211	Cflags misc 102	WrCflagsOK 121	WantPrivRf! FastD←Dbuf 105	+
17	MU PrVA 4,7-19 +2		WantPRdly DbufBusy 231	IfuAckIfHit 231	ProcTchMem 1660	1660	Hit 231	HitOrEc' Col = Vic' 1672	Clocks		←preClk0 MapAdLd StST,←VicA 103	+
18		A bits 8-11			Comparators		Victad	Col = NV' preMCS' New 1672			Pair/3 Next/2 ←VictAd 195i	MU Pair
19					8-11		8-11	VNV EnVNV 1662	dVA.4-11 parity 170	WantVic! VicM←,RdInA AwDifHit 102	ForceMiss VicIfMiss 109	VicOrFS1C (EcHasA) 100
20		A bits 7, 20-21, parity or bits 4-7			Comparators		Victad	stuff 159	Parity PrVAclk1 176	101	PairInA (EcHasA)	101
21					4,7,20-21 or 4-		4,7,20-1 or 4-7	Vic.1',IoFiA AchMap dDbufBusy 102	dPCHP,Pr/2 UsaAsrndly MdPend 176.0	Pair 176	176	MU Pair
22	MU Aad	dMdH,dPerr dVA.4/par 107	VNV	WantCR,CR' dMDc,PipH 117	RefH, MdH 231	MU xHold/3 BLretry VNV	VNV 173	VA 4-7,9 176	FastD←Dbuf MakeF←D! 1660	St←,IfuRef Abusy 105	Pref,IoRef DntLdPrVA! 104	Midas/2! D←Dbuf Pcol←Vic 103
23	ASEL12 mkD←CD 195i	dMDhold 121	RAM	xxHold dMiscH 210	MiscH, BLrty 231	WrVicMem IP buf 210	NextV' Vic.0' FF-5-7' 195i	MU	78 173	dVic/FS 117	Pair/3,MDd (HoldOrIP) 101	Midas 164
24	WantRef decodes 162	WantPR! DcomingIH St←icr,wAR 103	xxHold CacheRef' 212	dDbufHold PCHP 109	FB decode 171	UseAsrn 121	1-4 MapAd 173	056 173	MemAd 159	Ref decodes 161	overhead 176	176

Exxx ←MDI ←MD Asel FF.0-3 PRhold FF.4-7 MemBase MemAd 5-8

XEROX PARC	Project Dorado	Reference Layout	File MemC22.sil	Designer Lampson	Rev Be	Date 7/01/79	Page 22

CACHE CONFIGURATIONS

4k CacheConfig = 3			16k CacheConfig = 2			16k without parity CacheConfig = 1		
Position	*Chip*	*Cut (X) or wire (pin-pin)*	*Position*	*Chip*	*Cut (X) or wire (pin-pin)*	*Position*	*Chip*	*Cut (X) or wire (pin-pin)*
a03	195	3x 4x cut 5-6 from 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21
a07	195	2-15 3-4 connect 20-21 to 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21
a05	197	3x 4x read ProcVA.20-21 for CVA	d03	197	2x 15x read ProcVA.20-21 for row	d03	197	2x 15x read ProcVA.20-21 for row
b14	1668	remove disconnect Aad.0						
c14	1668	remove disconnect Aad.1						
e20	113	3x	e20	113	3x	b22	107	7x 9x 14x 15x 6-10 connect 4 to 4/par disconnect Perr reporting
e21	113	3x	e21	113	3x			
f20	113	3x	f20	113	3x			
f21	113	3x keep parity from comparators	f21	113	3x			
g20	174	2x keep parity from CVA	g20	174	2x			
			l11	164	12x make CacheConfig = 2	l11	164	11x make CacheConfig = 1

PAGE SIZE CONFIGURATIONS

256 words PageConfig = 3			1k words PageConfig = 2			4k words PageConfig = 1		
Position	*Chip*	*Cut (X) or wire (pin-pin)*	*Position*	*Chip*	*Cut (X) or wire (pin-pin)*	*Position*	*Chip*	*Cut (X) or wire (pin-pin)*
i24	159	4x 6x 11x 13x 4-6-11-13-9 MemRA←0 0 0 0	i24	159	11x 13x 11-13-9 MemRA←0 0 22 23			MemRA←20 21 22 23
			h24	173	3x 4x 1-2 MapAd.0←4-5 for 6-7	h24	173	10x 12x 10-3 12-5 MapAd.5,6←5,7 for 20,21
			i23	173	3x 10x 3-5 10-12 MapAd.7,8←6,7 for 22,23	i23	173	3x 10x 3-5 10-13 MapAd.7,8←6,4 for 22,23
			l11	164	14x make PageConfig = 2	l11	164	13x make PageConfig = 1

Note: Muffler signals 1144-1147 specify the configuration as follows:
1144-1145 are CacheConfig
1146-1147 are PageConfig
and the meaning of their values is as listed in the tables above

Need information here about the two missing holes

CURRENTLY NONE