

INTERNATIONAL STANDARD ISO 11898-1:2003 TECHNICAL CORRIGENDUM 1

Published 2006-05-15

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION • МЕЖДУНАРОДНАЯ ОРГАНИЗАЦИЯ ПО СТАНДАРТИЗАЦИИ • ORGANISATION INTERNATIONALE DE NORMALISATION

Road vehicles — Controller area network (CAN) — Part 1:

Data link layer and physical signalling

TECHNICAL CORRIGENDUM 1

Véhicules routiers — Gestionnaire de réseau de communication (CAN) —

Partie 1: Couche liaison de données et signalisation physique

RECTIFICATIF TECHNIQUE 1

Technical Corrigendum 1 to ISO 11898-1:2003 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 3, *Electrical and electronic equipment*.

Page 2, 4.2:

Replace definition for "bit stuffing" with:

"frame coding method providing bus state changes required for periodic resynchronization when using an NRZ bit representation"

Page 2, 4.8:

Replace definition for "contention-based arbitration" with:

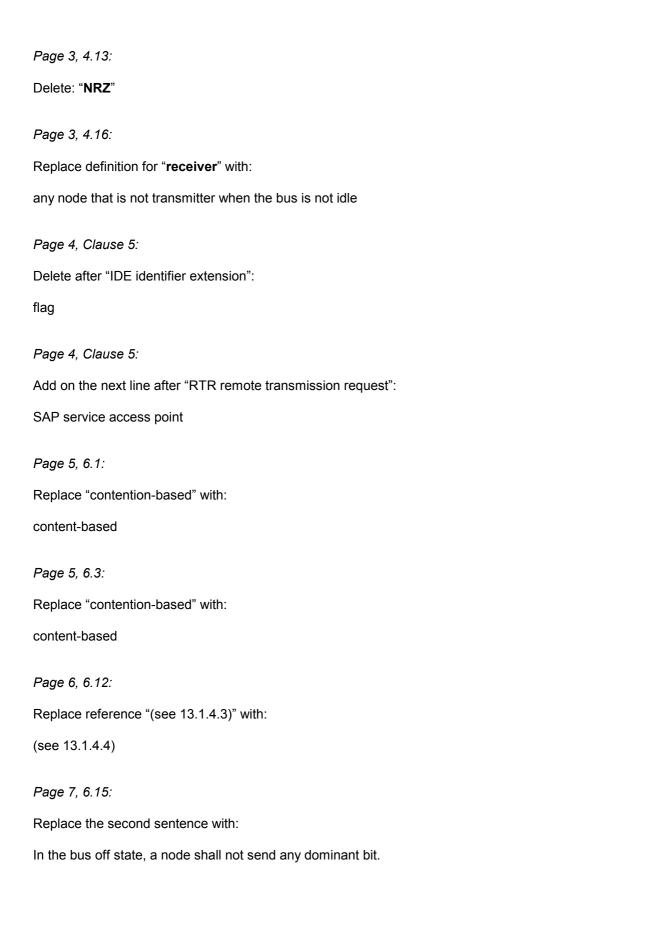
content-based arbitration

CSMA arbitration procedure resolving bus-contention when multiple nodes simultaneously access the bus

ICS 43.040.15

Ref. No. ISO 11898-1:2003/Cor.1:2006(E)

ISO 11898-1:2003/Cor.1:2006(E)



Page 8, Figure 2:
Replace "M-PC" with:
M-PCI
Page 15, Table 4:
Move Table 4 to 8.4.2.3
Page 15, Figure 4:
Replace figure title with:
Figure 4 — LLC remote frame
Page 24, 10.4.2.2:
Replace third paragraph with:
If a node with a pending transmission samples a dominant bit at the third bit of intermission and is error active or has been the receiver of the previous frame, with the next bit it shall start transmitting its message with the first bit of its identifier without first transmitting a SOF bit and without becoming receiver.
Page 25, 10.4.2.4:
Replace the second sentence of the second paragraph with:
Receivers shall accept recessive and dominant bits as reserved bit r0.
Page 27, 10.4.4.2:
Replace the first sentence with:
Two forms of error flag may be used, the active error flag and the passive error flag, where
— the active error flag shall consist of six consecutive dominant bits, and
 the passive error flag shall consist of six consecutive recessive bits unless it is overwritten by dominant bits from other nodes.
and add the following two sentences:
An error passive node transmitting a passive error flag waits for six consecutive bits of equal polarity, beginning at the start of the passive error flag. The passive error flag is complete when these six equal bits have been detected.
Page 28, 10.4.5.1:
Replace "overall flag" with:
overload flag

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Page 29, 10.5:

Replace the first sentence with:

The frame segments SOF, arbitration field, control field, data field, and CRC sequence shall be coded by the method of bit stuffing.

Page 30, Figure 10:

Replace figure with:

		Arb	itratior	Control field							Dat	ta field			CRC field								
	(base) ID								DLC									Sequence					
SOF	Bit 28	Bit 27	É	Bit 19	Bit 18	RTR	E	LO	Bit 3	Bit 2	Bit 1	Bit 0	Byte 0	Byte 1	É	Byte 6	Byte 7	Bit 14	Bit 13	É	Bit 1	Bit 0	Delimite

MSB (first bit transmitted)

LSB

Page 30, Figure 11:

Replace figure with:

	Arbitration field													Control field							ata fie	ld		CRC field					
1.	(base) ID						(extended) ID						DLC								Sequence				$\overline{}$				
SOF	Bit 28 Bit 27	É	Bit 19	Bit 18	SRR	301		Bit 16	É	Bit 1	Bit 0	RTR	Ξ	5	Bit 3	Bit 2	Bit 1	Bit 0	Byte 0	Byte 1	É	Byte 6	Byte 7	Bit 14	Bit 13	É	Bit 1	Bit 0	Delimiter

MSB (first bit transmitted)

LSB

Page 30, 10.7:

Replace the reference "8.3.3" with:

8.3.4

Page 31, 10.8.4, 10.8.6, and 10.8.8:

Replace "contention-based" with:

content-based

Page 31, 10.8.5:

Replace second sentence with:

A MAC error frame shall be transmitted as specified in 10.10.

Page 31, 10.8.8:

Replace second sentence with:

Within one system, each information shall be assigned by a unique identifier.

Page 33, 10.11:

Replace "The start of reactive overload frames due to condition a) above" with:

The start of LLC-requested overload frames due to condition a) above

Page 38, 12.4.2.5:

Replace "take into consideration" in the second sentence with:

meet

Page 38, 12.4.2.5:

Delete:

(both shall be met)

Page 38, 12.4.2.5:

Replace the formulas 1) and 2) with:

1)
$$df \le \frac{t(Phase_Seg1,Phase_Seg2)\min}{2 \times (13 \times t_{bit} - t_{Phase_Seg2})}$$

$$2) df \le \frac{t_{SJW}}{20 \times t_{bit}}$$

Page 43, 13.1.4.4:

Replace the second and third paragraphs with:

A node which is in the bus off state shall have no influence on the bus. It shall not send any frames nor send acknowledgement, error frames, overload frames. Whether such a node accepts frames from the bus depends on the implementation.

A node which is in the bus off state may become error-active (no longer bus off) with its error counters both set to zero (0) after having monitored one hundred and twenty-eight (128) occurrences of eleven (11) consecutive recessive bits on the bus (see Figure 16). The start of the recovery sequence may be initiated by software or hardware depending on the implementation.

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Page 43, 13.1.4.4:

Replace reference "6.14" in the NOTE with:

6.15

Page 44, Figure 16:

Replace "User_Request" with:

Recovery sequence