Question **1**

Not yet answered

Marked out of 1.00

Consider a personal computer that has two memories to store data and instructions separately. How many data buses do you think will be available for fetching instructions and data to the processor?

- a. 2
- b. 1
- c. 0
- d. 1 or 2

Clear my choice

Question **2**

Not yet answered

Marked out of 1.00

Consider a memory of capacity 4MB. How many address lines do you think are needed to address all the locations of the given memory?

- a. 4,194,604
- b. 4,194,504
- c. 4,193,304
- d. 4,194,304

Clear my choice

Question **3**

Not yet answered

Marked out of 1.00

Identify the correct statement related to Control Unit of Vonn Neumann computer

- a. Control Unit contains both Program Counter and Instruction Register.
- b. Control unit is not responsible for decoding of instructions.
- c. Control unit has general purpose registers that can be used in arithmetic and logical operations.
- d. Control Unit is used to store data and instructions.

Clear my choice

Question **4**

Not yet answered

Marked out of 1.00

Calculate the second biggest even number in 4-digit Octal number system.

- a. 7772
- b. 6664
- c. 7774
- d. 8886

Clear my choice

Question **5**

Not yet answered

Marked out of 1.00

The standard form of the given Boolean expression is :F=a'+b'

- a. ab'+ab+b'a+a'b'
- b. ab+b+b'a+ba'
- c. a'b'+a'b+b'a
- d. ab'+ab+a'+b'

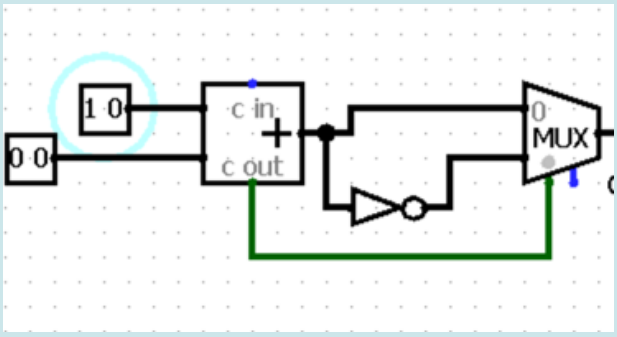
Clear my choice

Question **6**

Not yet answered

Marked out of 1.00

Compute the output of the following combinational circuit:



- a. 00
- b. 10
- c. 01
- d. 11

Clear my choice

Question **7**

Not yet answered

Marked out of 1.00

1. Compute the Borrow output ($\mathbf{B_o}$)for the following combination of bits:

A	**B**	**D=A-B**	**B_o**
1	1	0	a
0	1	1	b

- a. a=0 and b=1
- b. a=1 and b=0
- c. a=1 and b=1
- d. a=0 and b=0

Clear my choice

Question **8**

Not yet answered

Marked out of 1.00

1. Identify the content of register AX after the execution of 4th instruction:

Given: Memory location 10A0H has content 22H

1. MOV CL, [10A0H]
2. ADD CL,20H
3. MOV AH,CL
4. MOV AL,AH

- a. 40H
- b. 2020H
- c. 4242H
- d. 20H

Clear my choice

Question **9**

Not yet answered

Marked out of 1.00

Identify the properties of processors that are based on RISC architecture

- a. The length of all instructions in RISC are not fixed and the design is simple.
- b. The length of all instructions in RISC are not fixed and the architecture is highly pipelined.
- c. RISC instructions are complex and use large register sets with simple Register-Register architecture.
- d. Control unit of RISC is hardwired and the memory references are less.

Clear my choice

Question **10**

Not yet answered

Marked out of 1.00

Identify the instruction format organization used in the following instruction: R1 ← R2

- a. Data register organization.
- b. Stack Organization.
- c. General register organization.
- d. Accumulator organization.

Clear my choice

Question **11**

Not yet answered

Marked out of 10.00

Answer all the following questions:

Instructions: Take the picture of your answers, copy all the pictures to word file and upload here.

1. Simplify the following Boolean expression using K-map and draw the circuit for simplified expression using basic gates.

$F(A,B,C)=\sum m(1,2,3)+ \sum d(5,7)$

2. Implement a 32:1 multiplexer using following instructions:

a. Use a combination of 16:1, 8:1 and 4:1 multiplexer.

b. You are allowed to use only one 16:1 and one 8:1 multiplexer.

c. Identify the correct number of select bits in each multiplexer used.

Maximum size for new files: 5GB

Files

You can drag and drop files here to add them.

◄ Links to Essential software

Jump to...