# Scripts for Easier Use of Spice (SEUS): A Perl script package for simulating and creating batches of circuit netlists for Monte Carlo simulations when using *Ngspice* or *Ngspice*-based simulators

Michael A. Turi[1]

1 Computer Engineering Program, California State University, Fullerton

Summary

Spice, or Spice-based, circuit simulators are typically used for the simulation of electronic circuits at the transistor level. Many simulators are derived from Spice to support alternative simulation settings or support simulating alternative devices. *Ngspice* is an open-source Spice circuit simulator ("Ngspice, the open source Spice circuit simulator," n.d.). This Perl script package, *Scripts for Easier Use of Spice* or SEUS, assists users to more easily run *Ngspice* to simulate circuit netlists and create batches of circuit netlists for Monte Carlo simulations ("SEUS," n.d.). Monte Carlo simulations are used in many fields, but for circuit design, these are often used to simulate the effect of parameter, voltage, and/or temperature (PVT) variations on circuits. Parameter variations may change the physical dimensions of transistors or other devices and affect the intended operation and/or performance of a circuit. Likewise, variations in operational voltages and temperatures may affect the intended operation and/or performance of a circuit. *Ngspice* and many other Spice simulators support Monte Carlo simulations, however, older Spice simulators do not provide this support. SEUS was originally created to generate varied circuit netlists for Monte Carlo simulation when using *University of Florida's Spice3-UFDG (Linux version 3.71)*; this simulator is derived from an older version of *Ngspice* without Monte Carlo simulation support, but has a built-in model for n- and p-type silicon-on-insulator FinFET, or tri-gate, transistors (Fossum et al., 2004; Fossum, Trivedi, Chowdhury, Kim, & Zhang, 2006). Without SEUS, a user cannot generate circuits with PVT variations for Monte Carlo simulations when using the UFDG (University of Florida Double-Gate) MOSFET transistor model. Since its creation, SEUS has been revised to work with current versions of *Ngspice*.

SEUS is a Perl script package to simulate electronic circuit netlists and create batches of circuit netlists for Monte Carlo simulations when using *Ngspice* or *Ngspice*-based simulators. SEUS should be run in a Linux environment and has been primarily developed and tested using CentOS 7 and Ubuntu 18.04.3 LTS. It is recommended to use at least Perl version 5.10; SEUS has been primarily developed and tested using Perl versions since 5.10 and current development and testing uses Perl versions 5.16.3 and 5.26.1. No additional Perl packages or modules are required to run SEUS. A user wishing to run a Monte Carlo simulation would use the following SEUS scripts:

1. *init_batch_spice.pl*: The Perl script to create the varied circuit netlists for a Monte Carlo simulation should be run first
2. *batchexec_spice.pl* and *run_spice.pl*: The *batchexec_spice.pl* Perl script should be used to run the *run_spice.pl* Perl script to simulate a batch of Monte Carlo circuit netlists

3. *MeasSpice.pm* and *meas_template.pl*: A Perl measurement script, modeled after *meas_template.pl*, should use functions from the *MeasSpice.pm* Perl module to make measurements from *Ngspice* simulation output; this is the preferred method. If desired, the *ezwave_measurement_scripts/meas_ezwave.pl* Perl script can instead be used to run a TCL measurement script, modeled after *ezwave_measurement_scripts/meas_template.tcl*, to make measurements using Mentor Graphics EZWave.

Other files present in the SEUS package are:

- *paper.md* and *paper.bib*: The source files for this paper
- *README.md*: A Markdown README containing more information about SEUS as well as a thorough walkthrough of how to perform Monte Carlo simulations with SEUS
- *LICENSE.txt*: The full SEUS license text using AGPL-3.0-or-later
- *SeusDefs.pm*: A Perl module with definitions for SEUS
- *netgen_spice.pl*: A Perl script to clean-up and organize a circuit netlist. This is called by *run_spice.pl* and *init_batch_spice.pl*.
- *mkout_spice.pl*: A Perl script to convert *Ngspice* ".o" output to other output formats for waveform viewers, Microsoft Excel, etc. This is called by *run_spice.pl*.

SEUS is designed for use by anyone using *Ngspice* or *Ngspice*-based simulators; especially individuals using older simulators without Monte Carlo simulation support. The Monte Carlo initialization algorithm used by *init_batch_spice.pl* has already been published (Turi & Delgado-Frias, 2017a), and the SEUS package has enabled the use of Monte Carlo simulations for a few engineering publications (Turi & Delgado-Frias, 2017b, n.d.). SEUS can enable additional research or learning to take place when analyzing the affects of PVT variations on circuit design.

Acknowledgements

References

Fossum, J. G., Ge, L., Chiang, M.-H., Trivedi, V. P., Chowdhury, M. M., Mathew, L., Workman, G. O., et al. (2004). A process/physics-based compact model for nonclassical CMOS device and circuit design. *Solid-State Electronics*, *48*(6), 919–926. doi:10.1016/j.sse.2003.12.030

Fossum, J. G., Trivedi, V. P., Chowdhury, M. M., Kim, S.-H., & Zhang, W. (2006). *Recent upgrades and applications of UFDG* (Vol. 3, pp. 674–679). Technical Proceedings of the 2006 NSTI Nanotechnology Conference and Trade Show (Workshop on Compact Modeling). Retrieved from https://briefs.techconnect.org/papers/recent-upgrades-and-applications-of-ufdg/

Ngspice, the open source Spice circuit simulator. (n.d.). http://ngspice.sourceforge.net/.

SEUS: Scripts for easier use of Spice. (n.d.). https://bitbucket.org/miketuri/perl-spice-sim-seus/.

Turi, M. A., & Delgado-Frias, J. G. (2017a). *An implemented, initialization algorithm for many-dimension, Monte Carlo circuit simulations using Spice.* IEEE 7th Annual Computing and Communication Workshop and Conference (CCWC). doi:10.1109/CCWC.2017.7868469

Turi, M. A., & Delgado-Frias, J. G. (2017b). Full-VDD and near-threshold performance of 8T FinFET SRAM cells. *Integration, the VLSI Journal*, *57*(2), 169–183. doi:10.1016/j.vlsi.2016.12.003

Turi, M. A., & Delgado-Frias, J. G. (n.d.). Effective low leakage 6T and 8T FinFET SRAMs: Using cells with reverse-biased FinFETs, near-threshold operation, and power gating. *IEEE Transactions on Circuits and Systems II: Express Briefs, to appear.* doi:10.1109/TCSII.2019.2922921