Abraham Gonzalez

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Education

***Ph.D.* — Electrical Engineering and Computer Science** Aug. 2018 - Now
University of California, Berkeley

***Bachelors of Science* — Electrical Engineering** Aug. 2014 - May 2018
The University of Texas at Austin
GPA - Overall 3.98/4.00 Major 3.98/4.00

Experience

ADEPT Lab Ph.D. Student Aug. 2018 - Now
ADEPT Lab — Berkeley, CA

- Research focus: Microarchitecture, Warehouse-scale computing, Architecture tooling.
- Main developer of BOOM, a Linux booting open-source RISC-V out-of-order core.
- Main developer of the Chipyard SoC framework.

BEAGLE: Heterogeneous Multi-Core Multi-Accelerator Chip in Intel 22FFL May 2019 - Jan. 2020
ADEPT Lab — Berkeley, CA

- Led tapeout as well as integrated core, accelerator, and uncore IP into new Chipyard SoC framework.
- Coordinated interaction between Berkeley and Intel during physical design process.
- SoC Components: In-Order Rocket core with systolic array accelerator, Out-of-Order BOOM core with vector accelerator, shared L2, independent clock domains, multiple IOs (GPIO, SPI, I2C, UART, SerDes).

Scalable Performance CPU Development Group Intern May 2018 - Aug. 2018
Intel — Austin, TX

- Worked on debugging tools for microcontroller integration team.
- Helped setup infrastructure between firmware team and microcontroller integration team to speed up work.

Microsystems Technology Lab Intern Jun. 2017 - Aug. 2017
Massachusetts Institute of Technology — Cambridge, MA

- Researched variations in electroplating growth in redistribution layers under the supervision of Dr. Boning.
- Designed various neural networks and machine learning models for electroplating growth using Tensorflow.
- Presented final research poster summarizing work (2nd place at SHPE Conference 2017) and participated in multiple MITSRP workshops.

QCA Research Assistant May 2015 - Aug. 2016
The University of Texas at Austin — Austin, TX

- Researched and designed Quantum Cellular Automata (QCA) circuitry with Dr. Swartzlander.
- Optimized QCA implementations of the Carry-Lookahead and Conditional Sum adder through QCA Designer.
- Reported back to Dr. Swartzlander on results and improvements to QCA circuit designs and layouts.

Office Shared Graphics Explore Intern May 2016 - Aug. 2016
Microsoft — Redmond, WA

- Created and added new features within the Office Ink suite using C++.
- Created physical network of Arduino microcontrollers for OneWeek Hack-a-thon that once connected to each other sent a unique code to main server (HTTP requests).

UIM Driver Intern May 2015 - Aug. 2015
Qualcomm — San Diego, CA

- Designed software framework for smartcard interaction in C++/CLI and C++.
- Integrated framework into .NET application managing smartcards via CCID by utilizing APDU transmission and logging; file system viewing; file data parsing and manipulation; and smartcard reader management.

Skills

Hardware Experience: RISC-V, Chisel/Verilog/VHDL, ARM Assembly
Software Experience: C/C++/C#/CLI, Python/Bash, Make, Git, TensorFlow/PyTorch
Other Experience: AWS EC2, Cadence Physical Design tooling

Professional Leadership and Membership

Member of LAGSES (Fall 2018-Now)
Vice President (Spr. 2018), Corres. Secretary (Fall 2017), and member (Spr. 2016-Now) of HKN Honor Society
Academic Director (Fall 2016-Fall 2017), and member (Fall 2014-Now) of Society of Hispanic Professional Engineers

Accomplishments

UC Berkeley: Analog Devices Outstanding Designer (Spr. 2020), Berkeley Fellowship (Fall 2018), EECS Excellence Award (Fall 2018), GEM Fellowship (Spr. 2018)
UT Austin: Highest Honors (Spr. 2017), Distinguished College Scholar (Spr. 2017/2018), College Scholar (Spr. 2016), R. Rocca (Fall 2017), V. L. Hand Endowed (Fall 2016), and TI Diversity Scholarship (Fall 2015)