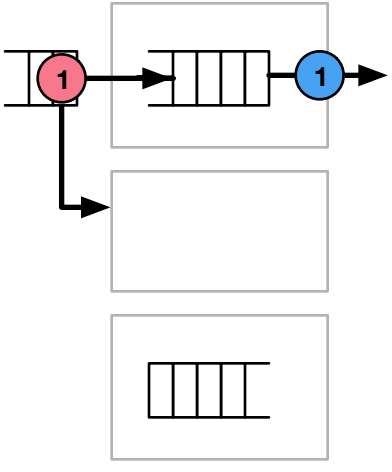
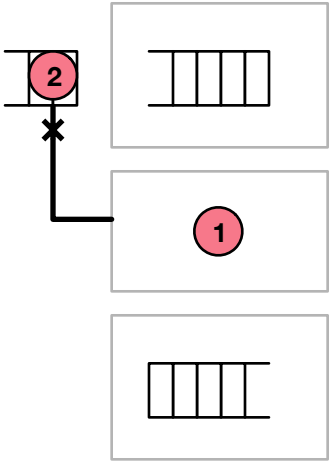


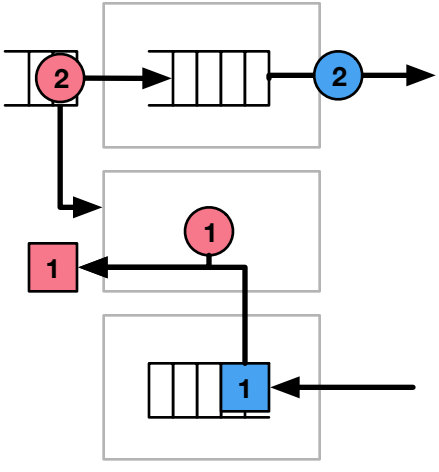
(a) Host Cycle k, Target Cycle n

A target read request enters the ingress unit and the timing model. The ingress unit translates it into a host read request and forwards it to the host memory system.



(b) Host Cycle k+1, Target Cycle n

On the next host cycle, the timing model determines that the target read request is ready to respond. The host memory system has yet to return the data, so the timing model stalls the target. Target time does not advance and a new target request is stalled outside the model.



(c) Host Cycle k+L, Target Cycle n+1

After L host cycles, the host memory system returns the read data. The timing model uses this data to issue a response to the target. Target time can now advance and the next target request enters the model.