Chiselizing SDR Blocks

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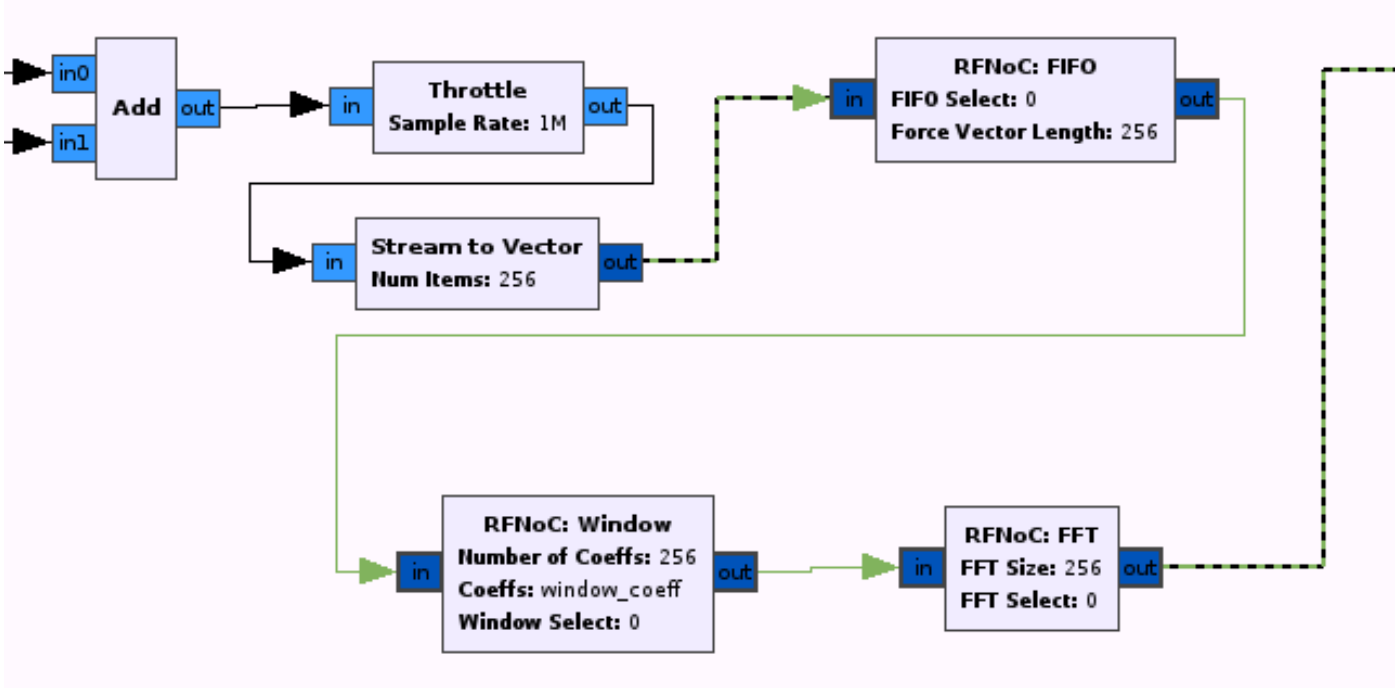
Overview

- Intro to RFNoC
- RFNoC Blocks
- Example: `addsub`
- Recurring patterns in Verilog and Chisel
- Goals

Intro to RFNoC



- FPGA toolkit for GNU radio
- Allows chaining of hardware and software blocks

Intro to RFNoC

- Accelerators implemented in Verilog
- NoC: packet headers on top of AXI4 Streaming crossbar
- Designers write parametrized blocks with ready/valid/last and settings registers

Intro to RFNoC

- Designers write parametrized blocks
- GNU Radio frontend elaborates instances
- RFNoC configurator assigns endpoint addresses and parametrizes RFNoC shim modules (`noc_shell`)
- Parametrizes and generates Verilog for NoC

RFNoC Blocks

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- Blocks have simple FIFO interfaces
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- *We want people to write these in Chisel*