Digital Circuits
Final Solutions

1. **Waveforms** *(30 points)*
Determine the waveform of the output. No need to justify the answer.

(a) Assume $Q = 0$ initially. *(10 points)*

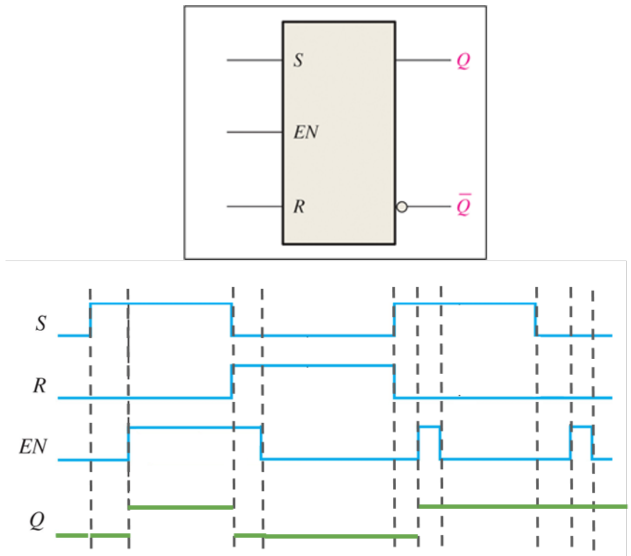


Figure 1: Problem 1(a) Solution.

(b) Assume initially $Q_0 = Q_1 = Q_2 = Q_3 = Q_4 = 0$. *(10 points)*

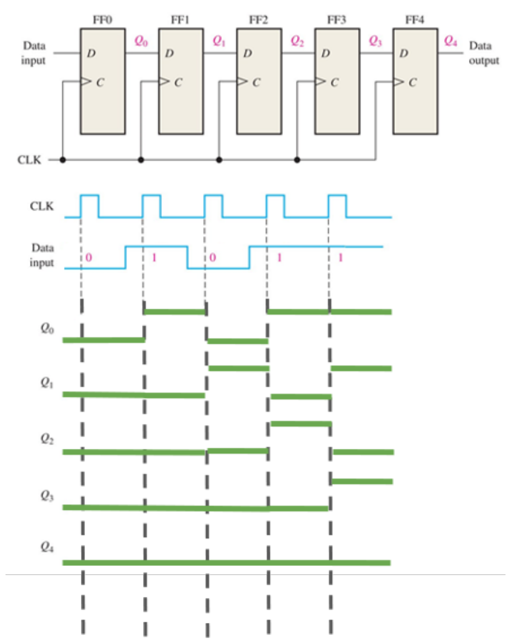


Figure 2: Problem 1(b) Solution.

(c) Assume $D_0 = D_1 = D_3 = 0$ and $D_2 = 1$. *(10 points)*

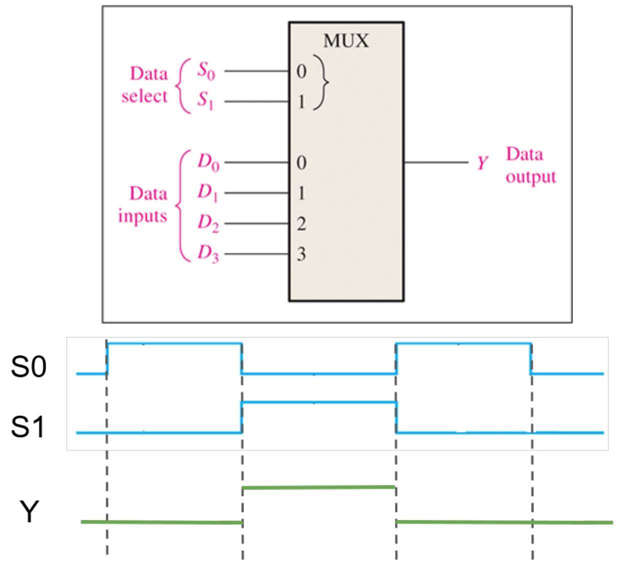


Figure 3: Problem 1(c) Solution.

2. Mix of Problems *(30 points)*

(a) Show that $AB + \bar{A}C + BC = AB + \bar{A}C$. *(10 points)*
(Hint: You are allowed to use Rule 1 - 12 from Chapter 4, but you have to specify the rule you are using.).

(b) Find a minimum SOP form of $A\bar{D} + AC + \bar{A}\bar{C}D + \bar{A}BD + BCD$. *(10 points)*

(c) Consider the BCD to 7-segment decoder. Find a minimum POS form of $\overline{RBO}$ using A_3, A_2, A_1, A_0 and $\overline{RBI}$. *(10 points)*

Solution:

(a) We have

$$
\begin{aligned}
AB + \bar{A}C + BC &= AB + \bar{A}C + ABC + \bar{A}BC \\
&= (AB + ABC) + \bar{A}C + \bar{A}CB \\
&= AB + \bar{A}C.
\end{aligned}
$$

(b) Consider the truth table

A	B	C	D	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Table 1: Problem 2(b) Solution-table.

Then,the Karnaugh map is given by

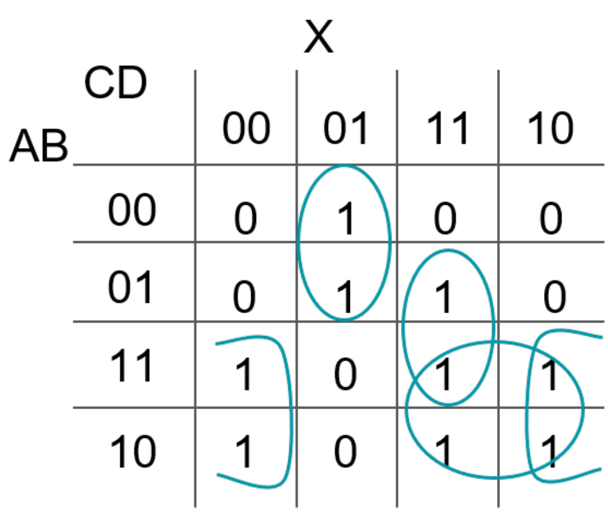


Figure 4: Problem 2(b) Solution.

Thus, $X = \bar{A}\bar{C}D + BCD + AC + A\bar{D}$, or equivalently $X = \bar{A}\bar{C}D + \bar{A}BD + AC + A\bar{D}$.

(c) $\overline{RBO} = \overline{RBI} + A_3 + A_2 + A_1 + A_0$.

3. Absolute Value *(20 points)*
Design a digital block which computes the absolute value of 4-bit binary number under two's complement system. In this design, assume that only AND, OR, NOT gates are

available. More precisely, the input signal A has four bits $A_3A_2A_1A_0$ and the output signal B has four bits $B_3B_2B_1B_0$. If A is smaller than or equal to 0 (under two's complement system), than $B = A$. On the other hand, if A is greater than 0, than $B = -A$ under two's complement system. I.e., $B = -|A|$. Note that A_3 is the MSB and A_0 is the LSB of A.

(a) Construct a truth table of B_0, B_1, B_2, B_3. *(10 points)*

(b) Use a Karnaugh map to reduce B_0, B_1, B_2, B_3 to minimum SOP forms. *(10 points)*

Solution:

(a) The truth table is given by

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Table 2: Problem 3(a) Solution.

(b) The Karnaugh map is given by

Figure 5: Problem 3(b) Solution.

B3

A3A2 \ A1A0	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

B1

A3A2 \ A1A0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	0	1	1
10	0	0	1	1

B2

A3A2 \ A1A0	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	1	1	1	1
10	0	0	0	0

B0

A3A2 \ A1A0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

Thus,

$$
\begin{aligned}
B_3 =& A_3 + A_2 + A_1 + A_0 \\
B_2 =& A_2A_3 + \bar{A}_2\bar{A}_3\bar{A}_0 + \bar{A}_2\bar{A}_3A_1 + A_2\bar{A}_1\bar{A}_0 \\
B_1 =& A_3A_1 + A_1\bar{A}_0 + \bar{A}_3\bar{A}_1A_0 \\
B_0 =& A_0.
\end{aligned}
$$

4. **Priority Encoder** *(40 points)*
Design a 2-bit priority encoder which takes A_0, A_1, A_2, A_3 as inputs, and outputs B_0, B_1, N. A priority encoder is exactly the same with basic encoder. However it produces a binary output corresponding to the highest number when there are more than two active inputs. The additional output will be activated $N = 1$ if and only if $A_0 = A_1 = A_2 = A_3 = 0$. For example, if $A_1 = A_2 = 1$ and $A_0 = A_3 = 0$, then $B_0 = 0, B_1 = 1$ and $N = 0$ which corresponds to the highest active input A_2. Note that we do not care B_0 and B_1 when $A_0 = A_1 = A_2 = A_3 = 0$. Further assume that only AND, OR, NOT gates are available.

   (a) Reduce N to a minimum SOP form. You do not need to justify your answer *(5 points)*

   (b) Construct a truth table of B_0 and B_1. *(5 points)*

   (c) Use a Karnaugh map to reduce B_0 to a minimum SOP form. *(10 points)*

   (d) Use the Quine-McClusckey method to reduce B_1 to a minimum POS form. Note that you have to merge maxterms (inputs result in 0 for the output). *(10 points)*

(e) Use two 2-bit priority encoders, construct a 3-bit priority encoder which takes $A_0, A_1, \ldots, A_7$ as inputs and outputs B_0, B_1, B_2 and N. You are allowed to use basic gates (AND, OR, NOT) as well, but the number of additional gates should be minimized. Fill the following diagram and justify your answer. *(10 points)*

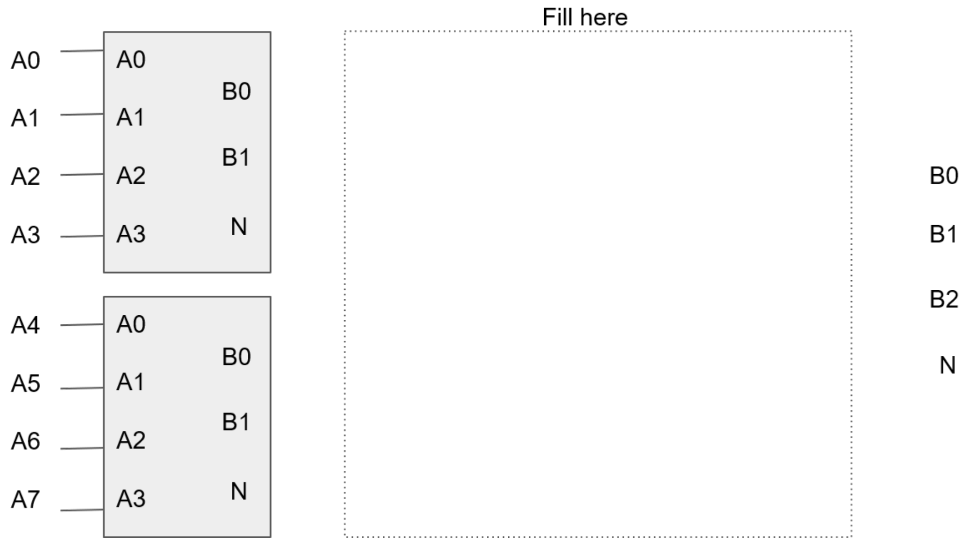


Figure 6: Problem 4(e)

Solution:

(a) $N = \bar{A}_0\bar{A}_1\bar{A}_2\bar{A}_3$.

(b) The truth table is given by

A_3	A_2	A_1	A_0	B_1	B_0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Table 3: Problem 4(b) Solution.

(c) The Karnaugh map is given by Thus, we have

$$B_0 = A_3 + \bar{A}_2 A_1$$

(d) Using the Quine-McClusckey method, we first have

Number of 1s	Maxterm	$A_3A_2A_1A_0$	First Level
0	m_0	0000 ✓	(m_0, m_1) 000x
			(m_0, m_2) 00x0
1	m_1	0001 ✓	(m_1, m_3) 00x1
1	m_2	0010 ✓	(m_2, m_3) 001x
2	m_3	0011 ✓	

Table 4: Problem 4(d)-1 Solution.

Then,

First Level	Number of 1s	Second Level
(m_0, m_1) 000x ✓	0	(m_0, m_1, m_2, m_3) 00xx
(m_0, m_2) 00x0 ✓	0	
(m_1, m_3) 00x1 ✓	1	
(m_2, m_3) 001x ✓	1	

Table 5: Problem 4(d)-2 Solution.

Thus, we have

$$B_1 = A_2 + A_3$$

(e) Clearly, $N = N_0N_1$. If $N_1 = 0$, then $B_2 = 1$, $B_1 = B_{11}$, and $B_0 = B_{10}$. If $N_1 = 1$ and $N_0 = 0$, then $B_2 = 0$, $B_1 = B_{01}$, and $B_0 = B_{00}$. Thus,

$$\begin{aligned} B_2 =& \bar{N}_1 \\ B_1 =& B_{11}\bar{N}_1 + B_{01}N_1 \\ B_0 =& B_{10}\bar{N}_1 + B_{00}N_1 \end{aligned}$$

5. **Moore Machine** *(30 points)*
Design a 3-bit counter using JK flip-flops where the current state $A = A_2A_1A_0$ and the next state $B = B_2B_1B_0$ have the following relation.

- If the current state is $A = 000$, then the next state is $B = 100$.
- If the current state is $A = 001$, then the next state is $B = 110$.
- If the current state is an odd number and $A \neq 001$, then the next state is $B = \frac{3A+1}{2}$ modulo 8.
- If the current state is an even number and $A \neq 000$, then the next state is $B = \frac{A}{2}$.

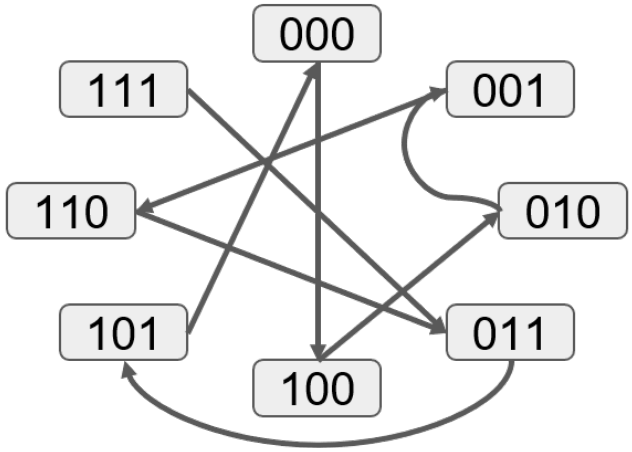
For example, if $A = 111$, then $B = 011$.

(a) Draw a state diagram. *(5 points)*
(b) Fill the next-state table. *(5 points)*
(c) Draw the JK flip-flop transition table. *(5 points)*
(d) Draw the Karnaugh maps. *(5 points)*
(e) Show the logic expressions. *(5 points)*
(f) Implement the counter. *(5 points)*
You are allowed to use AND, OR, NOT, XOR, XNOR gates.

Solution:

(a) The state diagram is given in Figure 7.

Figure 7: Problem 5(a) Solution.



(b) The next-state table is given in Table 6.

Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	0	0	0
1	1	0	0	1	1
1	1	1	0	1	1

Table 6: Problem 5(b) Solution

(c) The JK flip-flop transition table is given in Table 7.

$Q_N \to Q_{N+1}$	J	K
$0 \to 0$	0	x
$0 \to 1$	1	x
$1 \to 0$	x	1
$1 \to 1$	x	0

Table 7: Problem 5(c) Solution

(d) K-maps are given in Figure 8

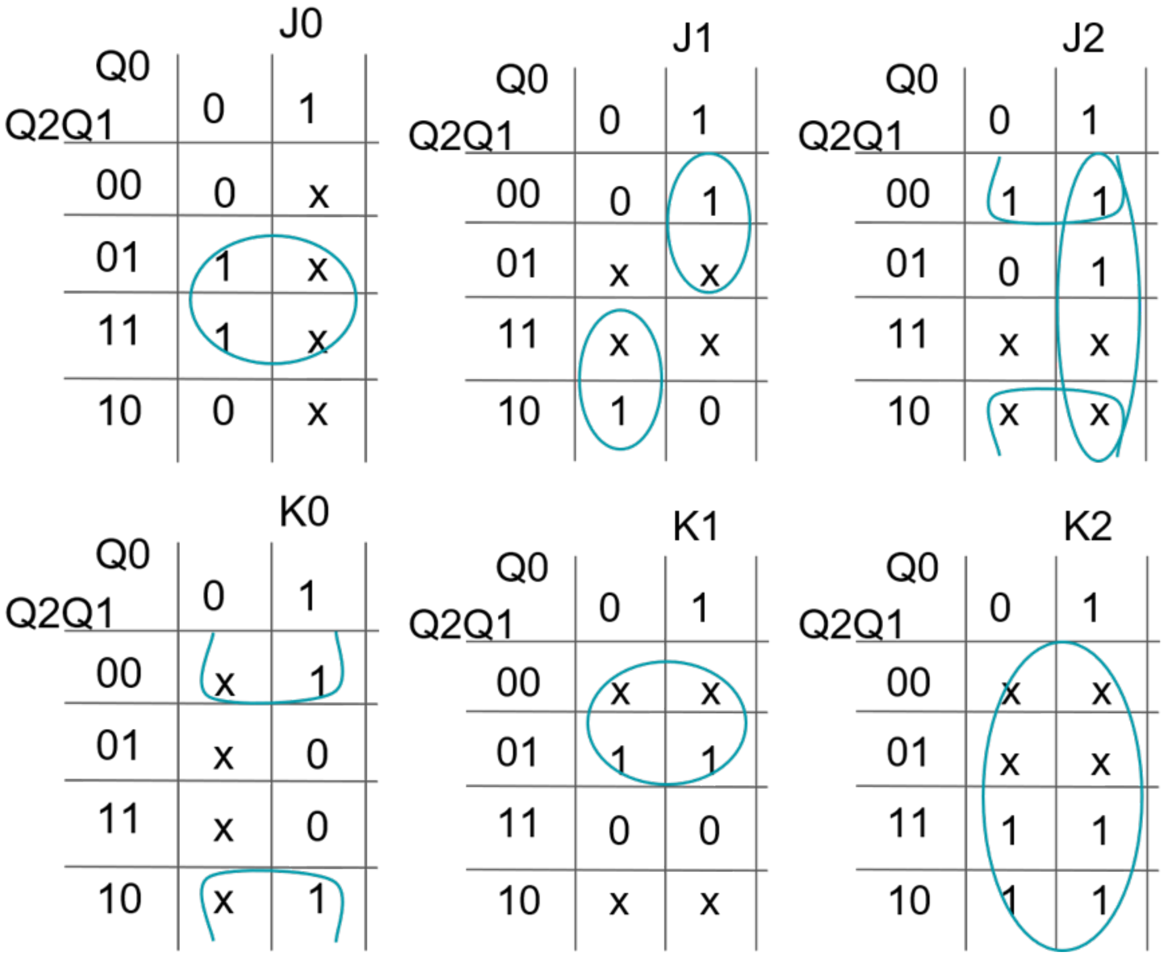


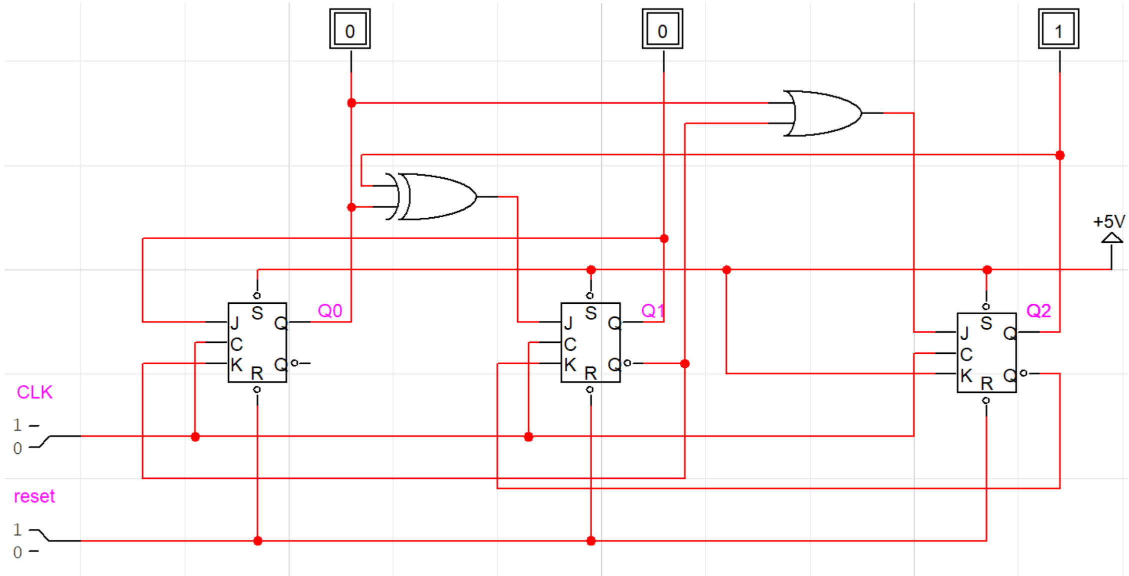
Figure 8: Solution 5(d)

(e) Then, the logic expressions are

$$\begin{aligned}
J_0 &= Q_1 \\
K_0 &= \bar{Q}_1 \\
J_1 &= Q_0\bar{Q}_2 + \bar{Q}_0 Q_2 = Q_0 \oplus Q_2 \\
K_1 &= \bar{Q}_2 \\
J_2 &= Q_0 + \bar{Q}_1 \\
K_2 &= 1
\end{aligned}$$

(f) Finally, the circuit is given in Figure 9.

Figure 9: Problem 5(f) Solution.



You do not need to specify RESET.

6. **Mealy Machine** *(30 points)*
Design a 3-bit counter using T flip-flops where the current state $A = A_2A_1A_0$ with input X and the next state $B = B_2B_1B_0$ have the following relation.

- If $X = 0$, it is an even counter $0, 2, 4, 6$.
- If $X = 1$, it is an odd counter $1, 3, 5, 7$.
- If A is an even number and $X = 1$, then $B = A + 1$.
- If A is an odd number and $X = 0$, then $B = A + 1$. If $A = 7$ and $X = 0$, then $B = 0$.

Note that T flip-flop toggles the output $Q = \bar{Q}_0$ if $T = 1$ and maintains the output $Q = Q_0$ if $T = 0$ where Q_0 is the previous output state.

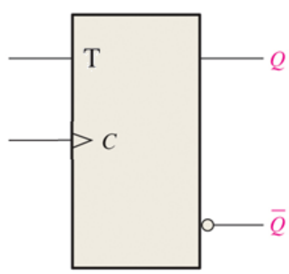


Figure 10: Problem 6 T flip-flop.

Note that you are not allowed to use other flip-flops (such as JK flip-flop).

(a) Draw a state diagram. *(5 points)*

(b) Fill the next-state table. *(5 points)*

(c) Draw the T flip-flop transition table. *(5 points)*

(d) Draw the Karnaugh maps of T_0, T_1 and T_2. *(5 points)*

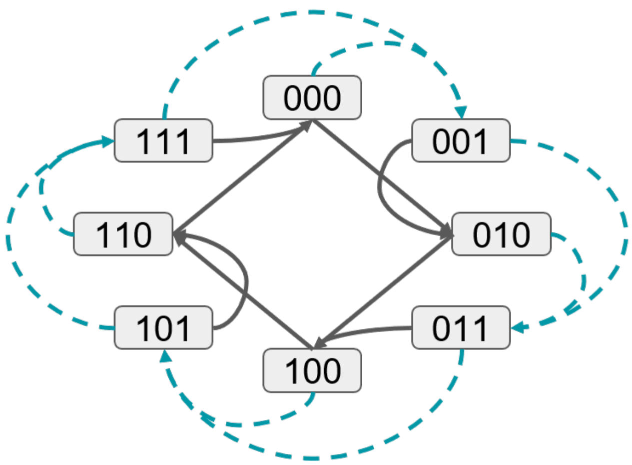
(e) Show the logic expressions for T_0, T_1 and T_2. *(5 points)*

(f) Implement the counter using three T flip-flops. *(5 points)*
You are allowed to use AND, OR, NOT, XOR, XNOR gates.

Solution:

(a) The state diagram is given in Figure 11.

Figure 11: Problem 6(a) Solution.



(b) The next-state table is given in Table 8.

Q_2	Q_1	Q_0	X	Q_2	Q_1	Q_0
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	0	1	1
0	1	1	0	1	0	0
0	1	1	1	1	0	1
1	0	0	0	1	1	0
1	0	0	1	1	0	1
1	0	1	0	1	1	0
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	1	1	1	1
1	1	1	0	0	0	0
1	1	1	1	0	0	1

Table 8: Problem 6(b) Solution

(c) The T flip-flop transition table is given in Table 9.

$Q_N \rightarrow Q_{N+1}$	T
$0 \rightarrow 0$	0
$0 \rightarrow 1$	1
$1 \rightarrow 0$	1
$1 \rightarrow 1$	0

Table 9: Problem 6(c) Solution

(d) K-maps are given in Figure 12

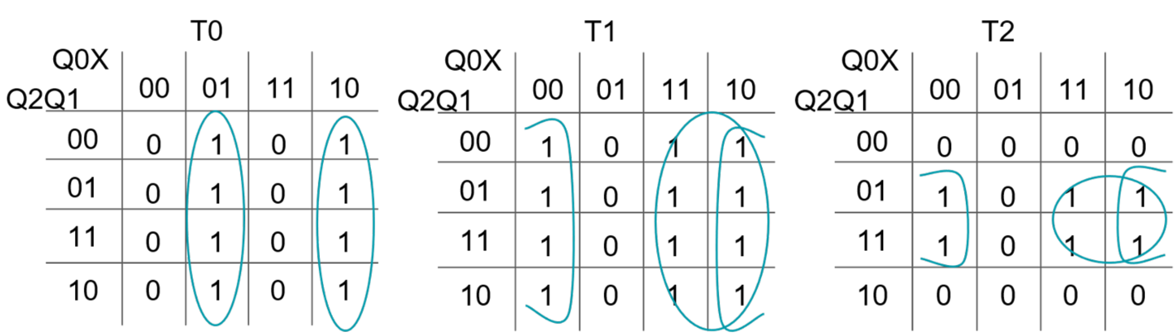


Figure 12: Solution 6(d)

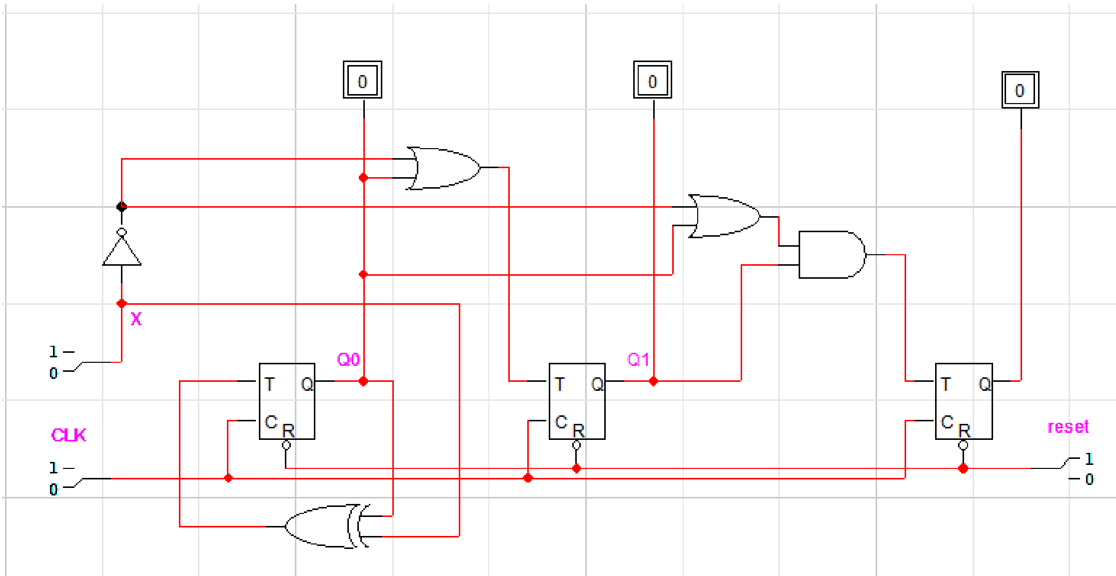
(e) Then, the logic expressions are

$$T_0 = \bar{Q}_0 X + Q_0 \bar{X} = Q_0 \oplus X$$

$$T_1 = Q_0 + \bar{X}$$
$$T_2 = Q_1\bar{X} + Q_1Q_0 = Q_1(\bar{X} + Q_0)$$

(f) Finally, the circuit is given in Figure 13.

Figure 13: Problem 6(f) Solution.



You do not need to specify RESET.