Digital Circuits
Midterm Solutions

1. **Mix of Questions** *(40 points)*
   Answer the following 8 questions. Simple reasoning will be enough. Each of them worth 5 points.

   (a) Covert the binary number $1011.01_{(2)}$ to decimal.

   (b) Add binary numbers $101.011_{(2)} + 11.101_{(2)}$ (Your answer should be a binary number as well).

   (c) Determine the 2's complement of 10011000.

   (d) Construct a truth table of $X = \bar{A}B + AB\bar{C} + \bar{A}\bar{C} + A\bar{B}C$.

   (e) Convert $X = \overline{AB(\overline{C}D + EF)}$ to sum-of-product (SOP) form.

   (f) Implement a logic circuit for $X = AD + B\bar{C}$.

   (g) For the full-adder with input $A = 0$, $B = 1$, $C_{in} = 1$, determine the outputs Σ and C_{out}.

   (h) Design a simple decoder that detects the presence of the binary code 0110.

Solution: Mix of Questions

(a) $2^3 + 2^1 + 2^0 + 2^{-2} = 11.25$.

(b) 1001.

(c) 1's complement of the given number is 01100111. We need to add 1 after that which gives us 01101000.

(d) $X = \bar{A}B + AB\bar{C} + \bar{A}\bar{C} + A\bar{B}C$.

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

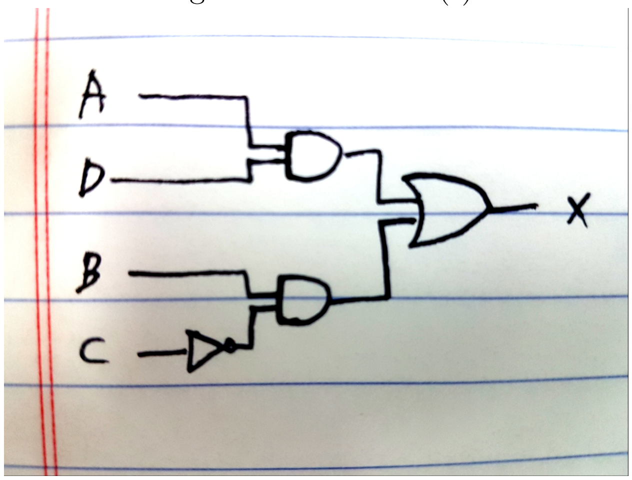
(e) We have

$$X = \overline{AB(\bar{C}D + EF)} \tag{1}$$
$$= \overline{AB} + \overline{\bar{C}D + EF} \tag{2}$$

$$= \bar{A} + \bar{B} + \overline{\bar{C}D} \cdot \overline{EF} \quad (3)$$
$$= \bar{A} + \bar{B} + (C + \bar{D})(\bar{E} + \bar{F}) \quad (4)$$
$$= \bar{A} + \bar{B} + C\bar{E} + \bar{D}\bar{E} + C\bar{F} + \bar{D}\bar{F}. \quad (5)$$

(f) Figure 1 shows the logic circuit.

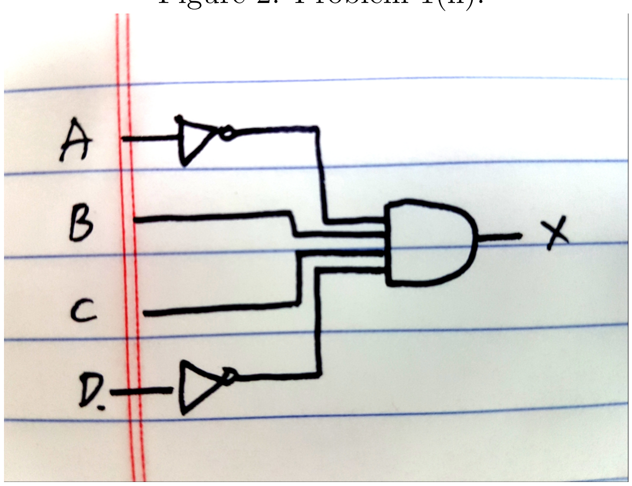
Figure 1: Problem 1(f).



(g) $\Sigma = 0$ and $C_{out} = 1$.

(h) Figure 2 shows the decoder.

Figure 2: Problem 1(h).



2. Karnaugh Map *(30 points)*
Let $X = \overline{(A + B\overline{C})(AC + \overline{D})} + \bar{A}B\bar{C}\bar{D}$.

(a) Develop a truth table of X. *(10 points)*
(Hint: You can simplify the formula first)

(b) Use a Karnaugh map to reduce X to a minimum SOP form. *(10 points)*

(c) Use a Karnaugh map to reduce X to a minimum POS form. *(10 points)*

Solution: Karnaugh Map.

(a) We can simplify X first.

$$X = \overline{(A + B\overline{C})(AC + \overline{D})} + \bar{A}B\bar{C}\bar{D} \tag{6}$$
$$= \overline{A + B\overline{C}} + \overline{AC + \overline{D}} + \bar{A}B\bar{C}\bar{D} \tag{7}$$
$$= \bar{A}(\bar{B} + C) + (\bar{A} + \bar{C})D + \bar{A}B\bar{C}\bar{D} \tag{8}$$
$$= \bar{A}\bar{B} + \bar{A}C + \bar{A}D + \bar{C}D + \bar{A}B\bar{C}\bar{D}. \tag{9}$$

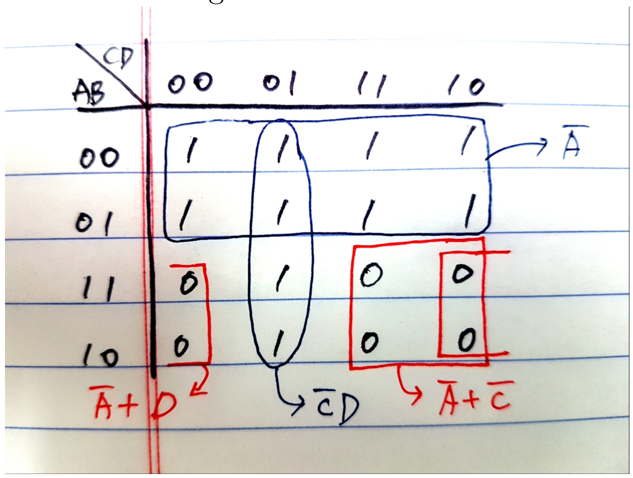
This provides

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

(b) It is not hard to show that $X = \bar{A} + \bar{C}D$.

(c) It is not hard to show that $X = (\bar{A} + D)(\bar{A} + \bar{C})$.

Figure 3: Problem 2.



3. Functions of Combinational Logic *(30 points)*

(a) For the multiplexer in Figure 4, input states are given by $D_0 = 1, D_1 = 1, D_2 = 0, D_3 = 0$. Then, determine the output waveform when the data-select inputs are sequenced as shown by the waveforms in Figure 5. *(15 points)*

Figure 4: Multiplexer.

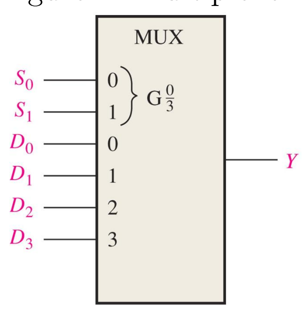
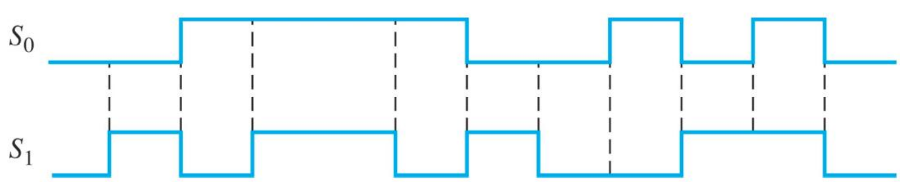
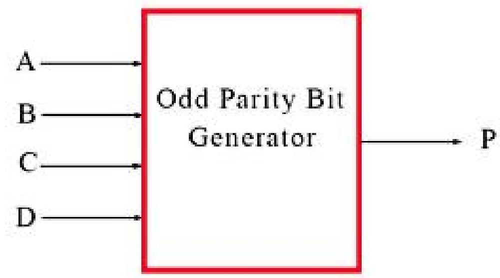


Figure 5: Data-Select Input Waveforms.



(b) Suppose you have two 4-bit odd parity generators as decribed in Figure 6. This 4-bit odd parity generators outputs 1 if even numbers of inputs are 1 and outputs 0 if odd numbers of inputs are 1. For example, the output is $P = 1$ if $A = 1, B = 0, C = 1, D = 0$, and the output is $P = 0$ if $A = 1, B = 0, C = 1, D = 1$. Construct 8-bit odd parity generator using two 4-bit odd parity generators with one additional logic gate. *(15 points)*
(Hint: Again, 8-bit odd parity generator outputs 1 if even number of inputs are 1 and outputs 0 if odd numbers of inputs are 1)

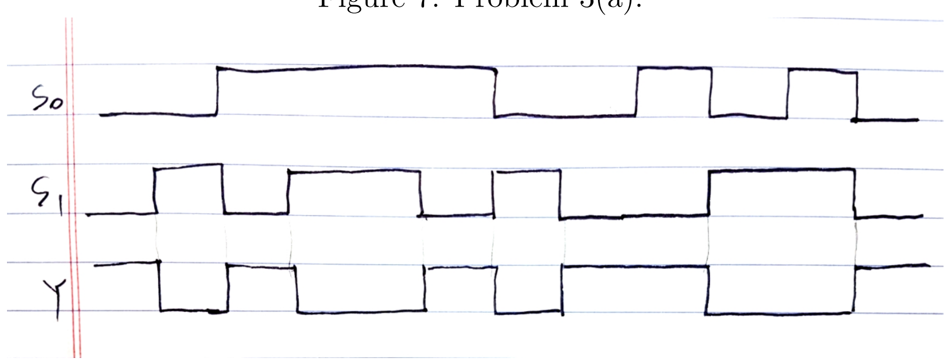
Figure 6: Data-Select Input Waveforms.



Solution: Functions of Combinational Logic

(a) Figure 7 shows the output waveform. $Y = 1$ if and only if $S_1 = 0, S_0 = 0$ or $S_1 = 0, S_0 = 1$. In other words, $Y = \bar{S}_1$.

Figure 7: Problem 3(a).



(b) Figure 8 shows the 8-bit odd parity generators using two 4-bit odd parity generator and one XNOR gate. This is because the output should be 1 if and only if two 4-bit odd parity generators have the same output.

Figure 8: Problem 3(b) 8-bit Odd Parity Generator.