Digital Circuits
Final, Friday June 9th

Instructions:

- You have **two hours**, 7PM - 9PM
- The exam has 3 questions, totaling 100 points.
- You are allowed to carry the textbook, your own notes and other course related material with you. Electronic reading devices [including cell phones, ipads, laptops, etc.] are not allowed.
- You are required to provide a detailed explanation of how you arrived at your answers.
- Good Luck!

1. Mix of Questions *(30 points)*

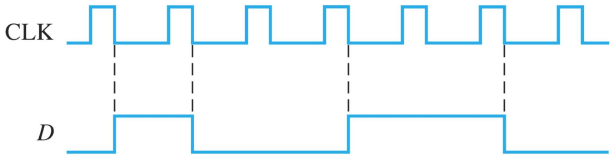
Answer the following 6 questions. Drawing waveform is enough for problem (a) to (e) (reasoning is not required). Each of them worth 5 points.

(a) Draw the output of a gated D latch for the inputs in Figure 1. Assume Q is initially HIGH

Figure 1: Problem 1(a).

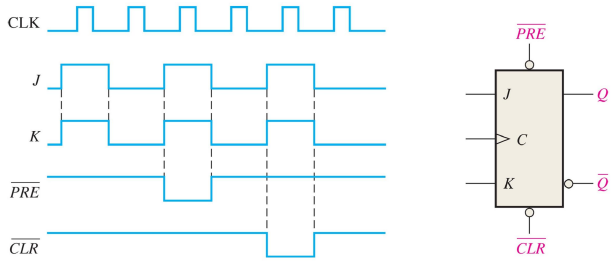
(b) Draw the Q output relative to the clock for a positive edge-triggering D flip-flop with the inputs in Figure 2. Assume Q is initially LOW.

Figure 2: Problem 1(b).



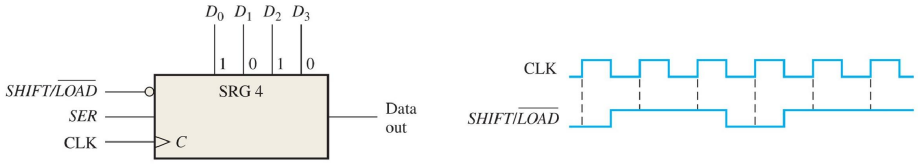
(c) Draw the Q output relative to the clock for a positive edge-triggering J-K flip-flop with the inputs in Figure 3. Assume Q is initially LOW.

Figure 3: Problem 1(c).



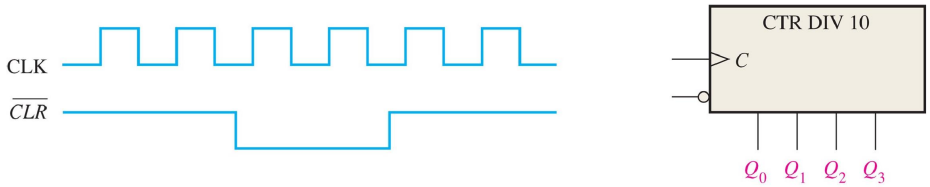
(d) The shift register in Figure 4 has $SHIFT/\overline{LOAD}$ and CLK inputs. The parallel data inputs are $D_0 = 1$, $D_1 = 0$, $D_2 = 1$, and $D_3 = 0$ as shown. Assume the register is cleared intially, and the serial data input (SER) is a 0. Draw the data-output waveform in relation to the inputs.

Figure 4: Problem 1(d).



(e) A BCD decade counter is shown in Figure 5. The waveforms are applied to the clock and clear inputs as indicated. Draw the counter output waveforms (Q_0, Q_1, Q_2, and Q_3) in proper relation to these inputs. The clear input is asynchronous and the counter is initially in the binary 0111 state ($Q_3 = 0$, $Q_2 = Q_1 = Q_0 = 1$).

Figure 5: Problem 1(e).



(f) For the cascaded counter in Figure 6, determine the frequency of the waveform at each point inticated by circled number.

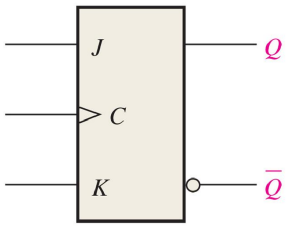
Figure 6: Problem 1(f).

2. Design Problems *(30 points)*

(a) Design an asynchronous counter using four D flip-flops that counts from 0000 to 1110 (that has 15 states). *(10 points)*

(b) Design 4-bit serial in/serial out shift register with four J-K flip-flops. Specify how your shift register takes data input and CLK. Also specify how your shift register outputs the data. You are NOT allowed to use D flip-flops. *(10 points)*

Figure 7: J-K flip-flop.



(c) Design 4-bit Johnson counter with four J-K flip-flops. You are NOT allowed to use D flip-flops. *(10 points)*

Extra Pages for Problem 2.

3. Design of Synchronous Counters. *(40 points)*
Design a counter to produce the following binary sequence using J-K flip-flops.

$$0, 2, 4, 6, 1, 3, 5, 0, 2, 4, 6, 1, 3, 5, \ldots.$$

Please follow 6 steps to design the counter.

(a) Draw a state diagram. *(5 points)*
(Hint: We have 7 states from 000 to 110)

(b) Fill the next-state table. *(10 points)*
(Hint: Use don't care when the present state is 111)

(c) Draw the flip-flop transition table. *(5 points)*

(d) Draw the Karnaugh maps. *(10 points)*

(e) Show the logic expressions. *(5 points)*

(f) Implement the counter (draw the circuit with flip-flops). *(5 points)*

Extra Pages for Problem 3.

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