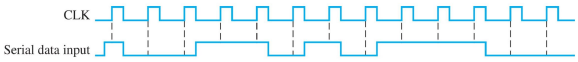
**Digital Circuits: Homeworks #5**

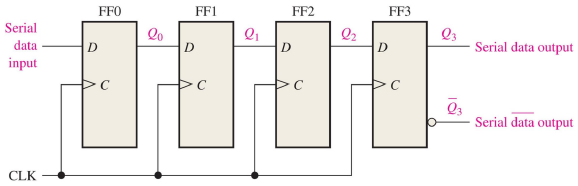
Due on Wednesday, June 7, 2017

Note: Late homework is not accepted. Good luck.

1. **Shift Register Data I/Os.**
   For the data input and clock in Figure 1a, determine the states of each flip-flop in the shift register of Figure 1b and show the $Q$ waveforms. Assume that the register contains all 1s initially.



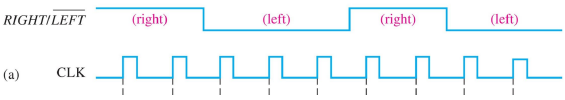

(a) Input Waveform.



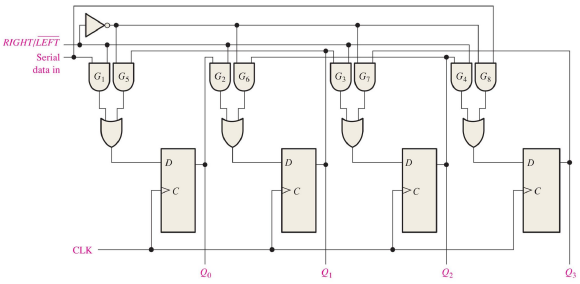

(b) Serial In/Serial Out Shift Register.

Figure 1: Input Waveform and Serial In/Serial Out Shift Register.

2. **Bidirectional Shift Registers.**
   Determine the state of the shift register of Figure 2b after each clock pulse for the given $RIGHT/\overline{LEFT}$ control input waveform in Figure 2a. Assume that $Q_0 = 0$, $Q_1 = 1$, $Q_2 = 1$, $Q_3 = 0$, and that the serial data-input line is HIGH.




(a) Input Waveform.




(b) 4-bit Bidirectional Shift Register.

Figure 2: 4-bit Bidirectional Shift Register and Input Waveform.

3. **Synchronous Counters.**
   Determine the sequence of the counter in Figure 3. Show the complete timing diagram of $Q_0$, $Q_1$, and $Q_2$ waveforms for 10 clock pulses. Begin with the counter cleared.

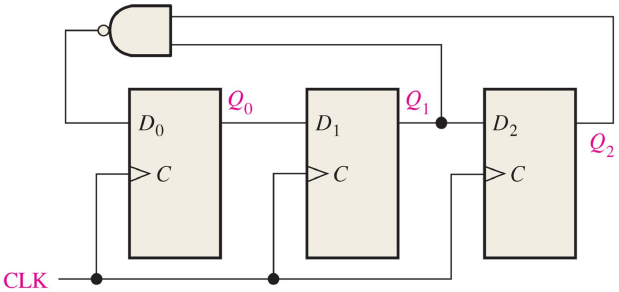



Figure 3: Synchronous Counter.

4. **Design of Synchronous Counters.**
   Design a counter to produce the following binary sequence using J-K flip-flops.

$$1, 4, 3, 5, 7, 6, 2, 1, 4, 3, 5, \ldots .$$

   Please follow 6 steps to design the counter.
   (Hint: We have 7 states from 001 to 111. You can start from drawing the state diagram.)
   (Hint2: Use don't care when the present state is 000.)