Digital Circuits
Final Solutions

1. Waveforms *(20 points)*
Determine the waveform of the output. No need to justify the answer.

(a) Consider the 2-bit decoder where all inputs and outputs are ACTIVE-HIGH. *(10 points)*

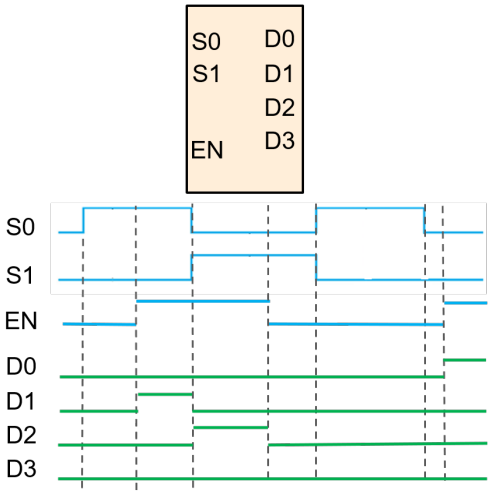


Figure 1: Problem 1(a) Solution.

(b) Assume initially $Q_0 = Q_1 = Q_2 = Q_3 = 0$ where all flip flops are positive edge triggered. *(10 points)*

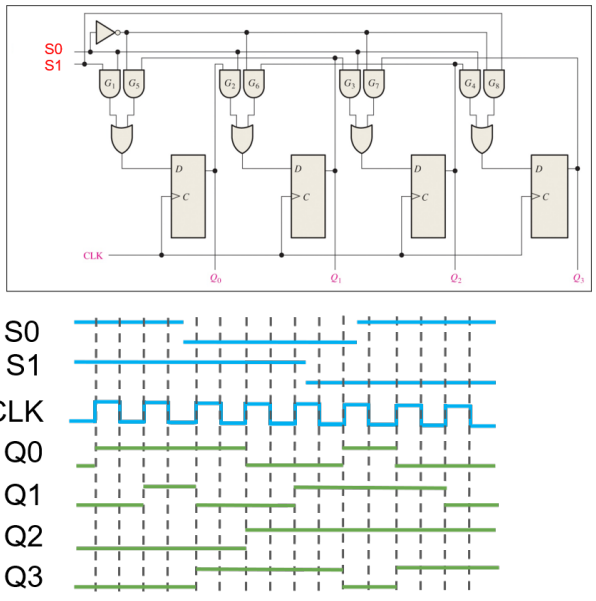


Figure 2: Problem 1(b) Solution.

2. Mix of Problems *(40 points)*
Answer the following questions. You have to justify your answer.

(a) Show that XOR operation is associative. *(10 points)*

(b) Show that NOR operation is not associative *(10 points)*
(Hint: It is enough to show that (A NOR B) NOR $C \neq A$ NOR (B NOR C) for some A, B, C)

(c) Construct $X = ABD + \bar{A}C$ with 5 NOR gates only. You are NOT allowed to use any other gates (Inverter is NOT allowed as well). *(10 points)*
(Note: your NOR gates can take as many input as you want)

(d) Consider a 4-bit comparator that compares $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ is given. It outputs G ($G = 1$ iff $A > B$), E ($E = 1$ iff $A = B$), and L ($L = 1$ iff $A < B$). Use this 4-bit comparator, design a digital block for X that checks whether $C \geq 2 \times D$ where $C = C_3C_2C_1C_0$ and $D_3D_2D_1D_0$. In other words, $X = 1$ if and only if $C \geq 2 \times D$. You are allowed to use additional input (VCC, GND) and gates, but your final design should be minimized.

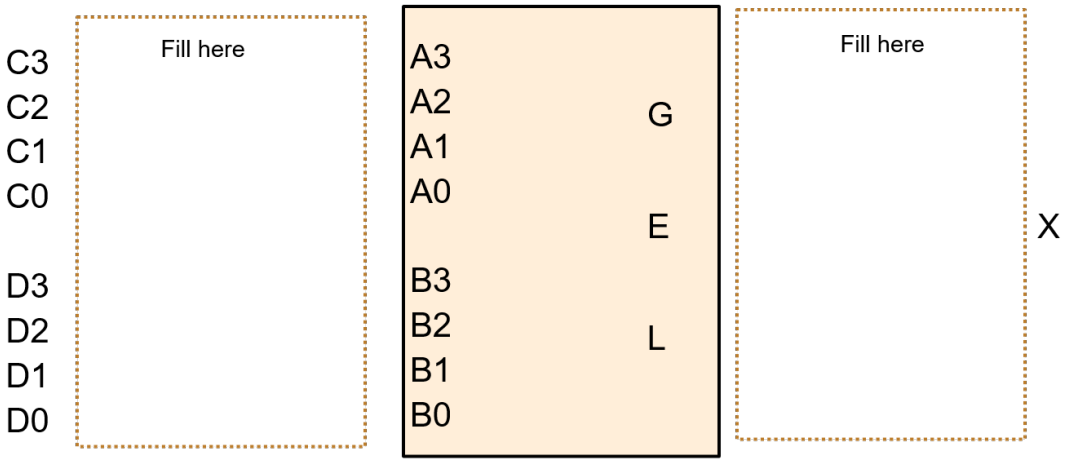


Figure 3: Problem 2(d).

Solution:

(a) We have

$$\begin{aligned}(A \oplus B) \oplus C =& \overline{A\bar{B} + \bar{A}B}C + (A\bar{B} + \bar{A}B)\bar{C} \\ =& (\bar{A} + B)(A + \bar{B})C + A\bar{B}\bar{C} + \bar{A}B\bar{C} \\ =& ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C}\end{aligned}$$

where you can also show that

$$A \oplus (B \oplus C) = ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C}.$$

You can prove the same result with truth table as well.

(b) Clearly,

$$(0 \text{ NOR } 1) \text{ NOR } 1 = 0$$
$$0 \text{ NOR } (1 \text{ NOR } 1) = 1.$$

(c) Using Karnaugh map (or Boolean algebra), we have

$$X = (A + C)(\bar{A} + D)(\bar{A} + B).$$

If $\bar{A}$ is available, we can construct the circuit with 3 OR gates, and single AND gates. All 4 gates can be replaced with NOR gates, and we can generate $\bar{A}$ with single NOR gate.

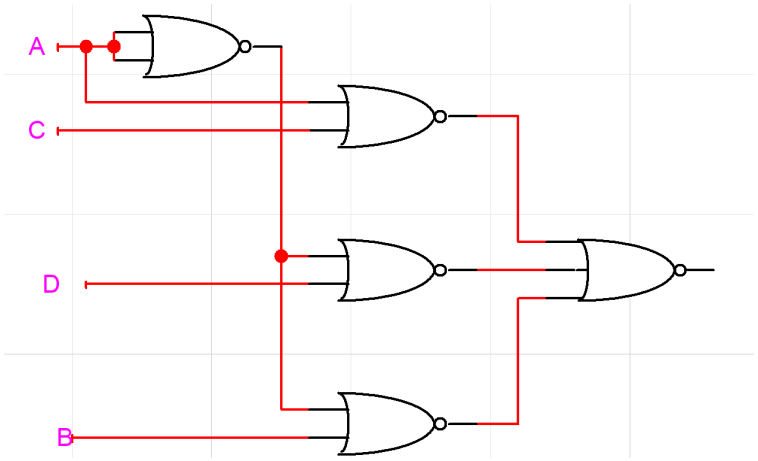


Figure 4: Problem 2(c) Solution.

(d) $C \geq 2 \times D$ is equivalent to $\lfloor C/2 \rfloor \geq D$. Thus, we can compare $0C_3C_2C_1$ and $D_3D_2D_1D_0$, then check G AND E (or $\bar{L}$).

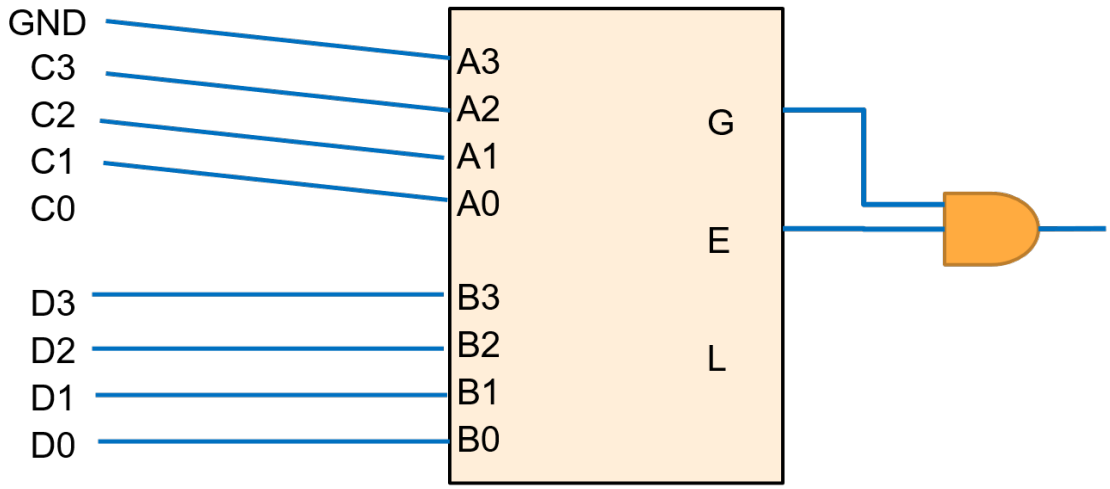


Figure 5: Problem 2(d) Solution.

3. Count the Number of Leading Zeros *(20 points)*

Design a digital block which counts the number of leading zeros of 4-bit binary number. In this design, assume that only AND, OR, NOT gates are available. More precisely, the input signal A has four bits $A_3A_2A_1A_0$ and the output signal B has five bits $B_4B_3B_2B_1B_0$. If the number of leading zero is k, then $B_k = 1$ and all other B's are zero. For example, if $A_3A_2A_1A_0 = 0110$, then $B_4B_3B_2B_1B_0 = 00010$, and if $A_3A_2A_1A_0 = 0001$, then $B_4B_3B_2B_1B_0 = 01000$. We call this block by "4-bit leading zero counter".

(a) Reduce B_0, B_1, B_2, B_3, B_4 to minimum SOP forms. *(10 points)*
(Hint: if you can get correct forms with reasonable explanation, you do not have to draw a Karnaugh map.)

(b) Using the above block, design another digital block which counts the number of leading zeros of 8-bit binary numbers, where the input signal has eight bits $A_7A_6 \cdots A_0$, and the output signal B has nine bits $B_8B_7 \cdots B_0$. You are allowed to use two "4-bit leading zero counter" blocks, and additional AND, OR, NOT gates. *(10 points)*

Solution:

(a) We have

$$\begin{aligned}
B_0 &= A_3 \\
B_1 &= \bar{A}_3 A_2 \\
B_2 &= \bar{A}_3 \bar{A}_2 A_1 \\
B_3 &= \bar{A}_3 \bar{A}_2 \bar{A}_1 A_0 \\
B_4 &= \bar{A}_3 \bar{A}_2 \bar{A}_1 \bar{A}_0.
\end{aligned}$$

(b) Let $B_{04}B_{03} \cdots B_{00}$ be the output of leading zero counter of $A_3A_2A_1A_0$, while $B_{14}B_{13} \cdots B_{10}$ be the output of leading zero counter of $A_7A_6A_5A_4$,

$$\begin{aligned}
B_0 &= B_{10} \\
B_1 &= B_{11} \\
B_2 &= B_{12} \\
B_3 &= B_{13} \\
B_4 &= B_{14}B_{00} \\
B_5 &= B_{14}B_{01} \\
B_6 &= B_{14}B_{02} \\
B_7 &= B_{14}B_{03} \\
B_8 &= B_{14}B_{04}.
\end{aligned}$$

4. Flip Sign *(30 points)*

Design a 4-bit sign converter which takes $A = A_3A_2A_1A_0$ as an input, and the output $B = B_3B_2B_1B_0$ is a two's complement of A. For example, if $A_3A_2A_1A_0 = 1010$, then $B_3B_2B_1B_0 = 0110$.

(a) Draw truth tables for each output B_3, B_2, B_1, B_0. *(10 points)*
(Hint: you can always apply "two's complement operation" even in the case where we cannot convert the sign in two's complement number system.)

(b) Reduce each output B_0, B_1, B_2, B_3 to minimum SOP form. You may want to use Karnaugh map. *(10 points)*

(c) In two's complement number system, there exists a number which we cannot convert the sign. Let E be the output to indicate whether we cannot convert the sign of input, i.e., $E = 1$ if we cannot convert the sign of $A = A_3A_2A_1A_0$. Describe the Boolean expression for E using input signal A_3, A_2, A_1, A_0. *(10 points)*

Solution:

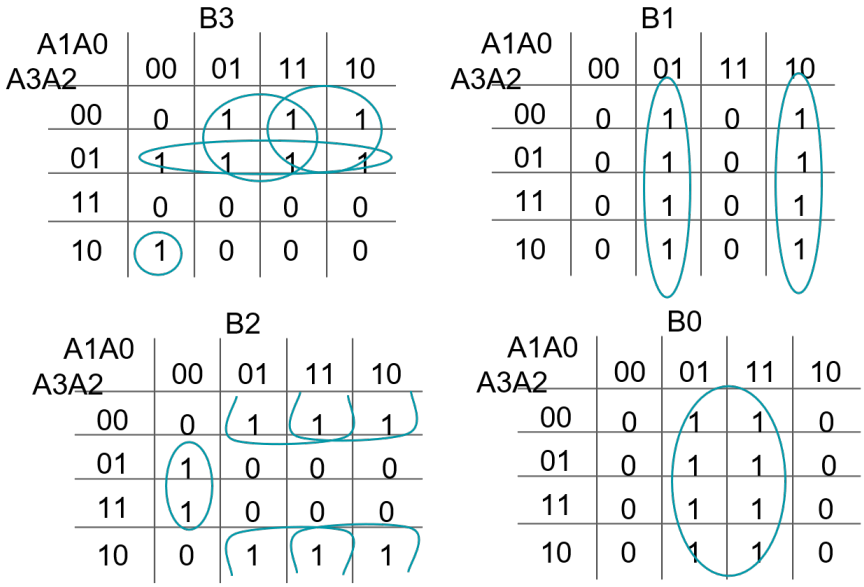
(a) The truth table is given by

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Table 1: Problem 4(a) Solution.

(b) The Karnaugh map is given by

Figure 6: Problem 4(b) Solution.



We have

$$
\begin{aligned}
B_3 &= A_3\bar{A}_2\bar{A}_1\bar{A}_0 + \bar{A}_3A_2 + \bar{A}_3A_0 + \bar{A}_3A_1 \\
B_2 &= A_2\bar{A}_1\bar{A}_0 + \bar{A}_2A_0 + \bar{A}_2A_1 \\
B_1 &= A_1\bar{A}_0 + \bar{A}_1A_0 = A_1 \oplus A_0 \\
B_0 &= A_0
\end{aligned}
$$

(c) We cannot convert the sign of $A_3A_2A_1A_0 = 1000$, thus $E = A_3\bar{A}_2\bar{A}_1\bar{A}_0$.

5. Mealy Machine *(30 points)*

Design a 3-bit up/down counter using JK flip-flops with input X where the state is under 2's complement system. If $X = 0$, it counts $-4, -3, -2, -1, 0, 1, 2, 3, -4, -3, \ldots$. If $X = 1$, it flips the sign $3 \leftrightarrow -3$, $2 \leftrightarrow -2$, and $1 \leftrightarrow -1$. If $X = 1$ and the current state is 0 or -4, the state remains the same, i.e., $0 \rightarrow 0$, and $-4 \rightarrow -4$. For example,

- If the current state is 001 and $X = 0$, then the next state is $B = 010$.
- If the current state is 101 and $X = 1$, then the next state is $B = 011$.
- If the current state is 000 and $X = 1$, then the next state is $B = 000$.

(a) Draw a state diagram. *(5 points)*

(b) Fill the next-state table. *(5 points)*

(c) Draw the JK flip-flop transition table. *(5 points)*

(d) Draw the Karnaugh maps. *(5 points)*

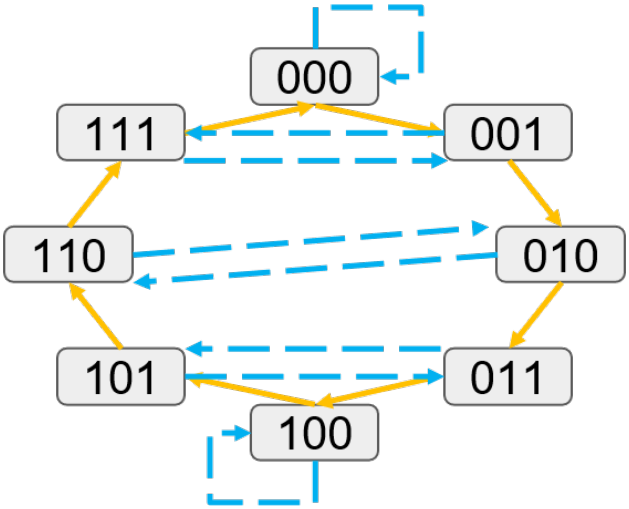
(e) Show the logic expressions in minimum SOP forms. *(5 points)*

(f) Implement the counter. *(5 points)*
You are allowed to use JK flip flops, AND, OR, NOT, XOR, XNOR gates. You do not need to specify PRE or CLR of flip flops.

Solution:

(a) The state diagram is given in Figure 7.

Figure 7: Problem 5(a) Solution.



(b) The next-state table is given in Table 2.

Q_2	Q_1	Q_0	X	Q_2	Q_1	Q_0
0	0	0	0	0	0	1
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	1	1	1
0	1	0	0	0	1	1
0	1	0	1	1	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	1
1	0	0	0	1	0	1
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	0	1	1
1	1	0	0	1	1	1
1	1	0	1	0	1	0
1	1	1	0	0	0	0
1	1	1	1	0	0	1

Table 2: Problem 5(b) Solution

(c) The JK flip-flop transition table is given in Table 3.

$Q_N \rightarrow Q_{N+1}$	J	K
$0 \rightarrow 0$	0	x
$0 \rightarrow 1$	1	x
$1 \rightarrow 0$	x	1
$1 \rightarrow 1$	x	0

Table 3: Problem 5(c) Solution

(d) K-maps are given in Figure 8

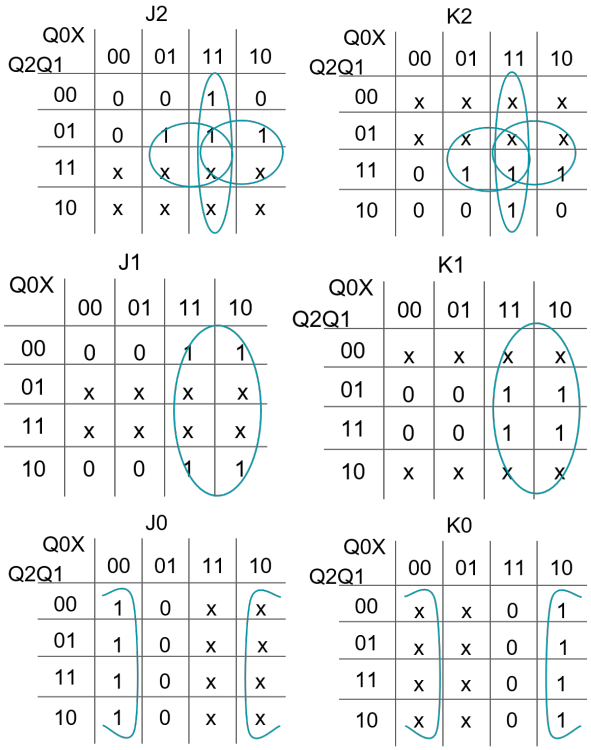


Figure 8: Solution 5(d)

(e) Then, the logic expressions are

$$
\begin{aligned}
J_0 &= \bar{X} \\
K_0 &= \bar{X} \\
J_1 &= Q_0 \\
K_1 &= Q_0 \\
J_2 &= Q_0X + Q_1X + Q_1Q_0 \\
K_2 &= Q_0X + Q_1X + Q_1Q_0
\end{aligned}
$$

(f) Finally, the circuit is given in Figure 9.

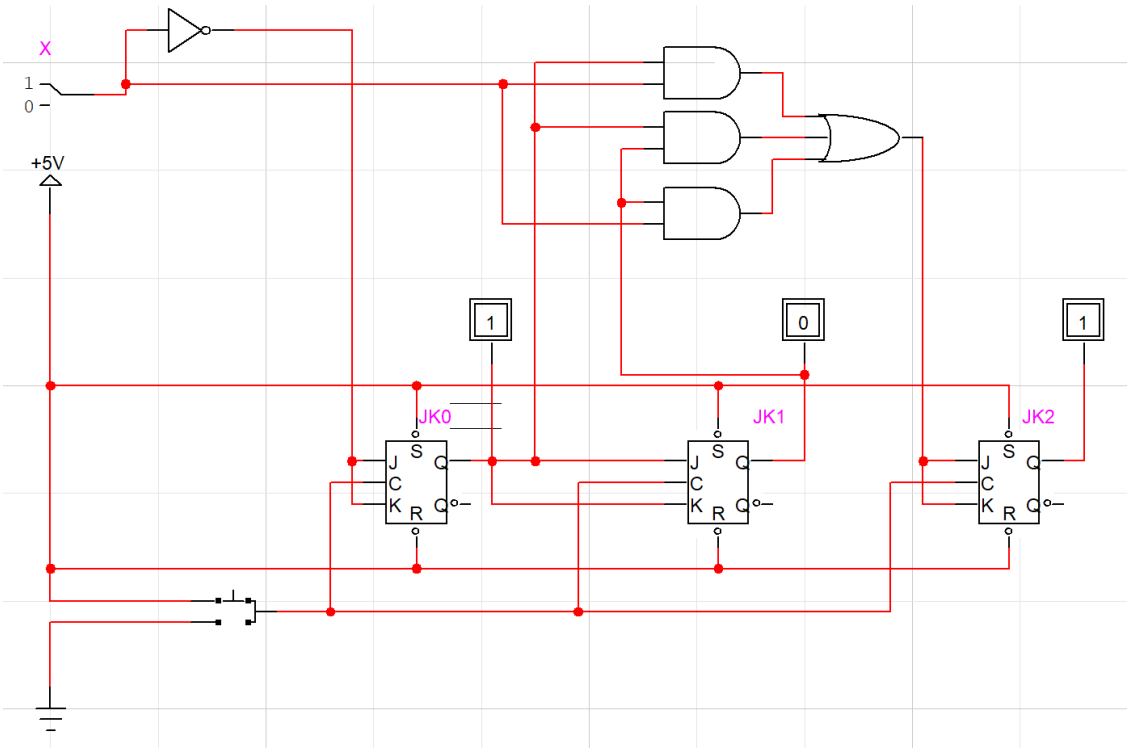


Figure 9: Problem 5(f) Solution.

You do not need to specify PRE or CLR.

6. Elevator *(30 points)*

Design a simple elevator controller using D flip-flops. Suppose the elevator can be in one of four states, depending on whether it is on the 1st or 2nd floor, and whether its door is closed or open. It can take in two inputs, one for the close/open door button, and the other for the up/down button.

- Let S_1 represent the floor that the elevator is on, either 1st ($S_1 = 0$) or 2nd ($S_1 = 1$). Let S_0 represent whether the door is closed ($S_0 = 0$) or open ($S_0 = 1$).
  - For example, $S_1S_0 = 01$ is the state in which the elevator is open on the 1st floor.
- Let I_1 represent the button to go either down (0) or up (1). Let I_0 represent the close (0) or open (1) door button. I_1 takes action before I_0.
  - For example, $I_1I_0 = 11$ tells the elevator to go up a floor and open the door.
- If we try to go up from the 2nd floor or go down from the 1st floor, the elevator does not move.
- The elevator can only move if its door is closed ($S_0 = 0$). If we try to move the elevator while the door is open, it stays in the same floor (but the I_0 will be applied).
  - For example, if the elevator is on the 1st floor and door is opened, with $I_1 = 1$ (up) and $I_0 = 0$ (close), the elevator will stay on the 1st floor but the door will be closed.

(a) Draw the state diagram with all four states S_1S_0 and all possible inputs I_1I_0 for each state. *(5 points)*

(b) Fill the next-state table. *(5 points)*

(c) Draw the D flip-flop transition table. *(5 points)*

(d) Draw the Karnaugh maps of D_0 and D_1. *(5 points)*

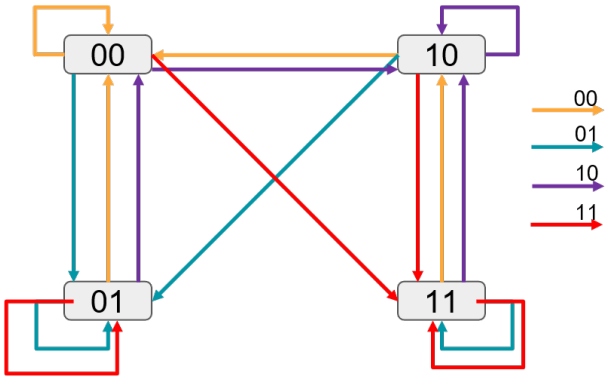
(e) Show the logic expressions for D_0 and D_1 in minimum SOP forms. *(5 points)*

(f) Implement the elevator using two D flip-flops and logic gates. *(5 points)*
You do not need to specify SET or RESET of flip flops.

Solution:

(a) The state diagram is given in Figure 10.

Figure 10: Problem 6(a) Solution.



(b) The next-state table is given in Table 4.

S_1	S_0	I_1	I_0	S_1	S_0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	1	1

Table 4: Problem 6(b) Solution

(c) The state transition table is given in Table 5.

$Q_N \rightarrow Q_{N+1}$	D
$0 \rightarrow 0$	0
$0 \rightarrow 1$	1
$1 \rightarrow 0$	0
$1 \rightarrow 1$	1

Table 5: Problem 6(c) Solution

(d) K-maps are given in Figure 11.

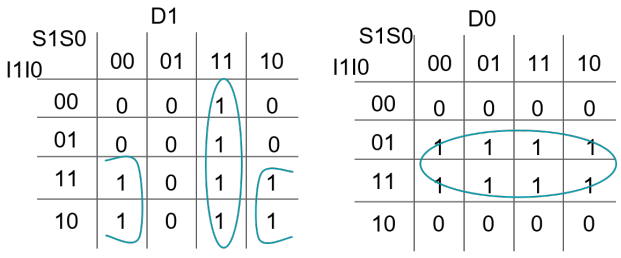


Figure 11: Solution 6(d)

(e) Then, the logic expressions are

$$D_0 = I_0$$
$$D_1 = S_0 S_1 + \bar{S}_0 I_1$$

(f) Finally, the circuit is given in Figure 12.

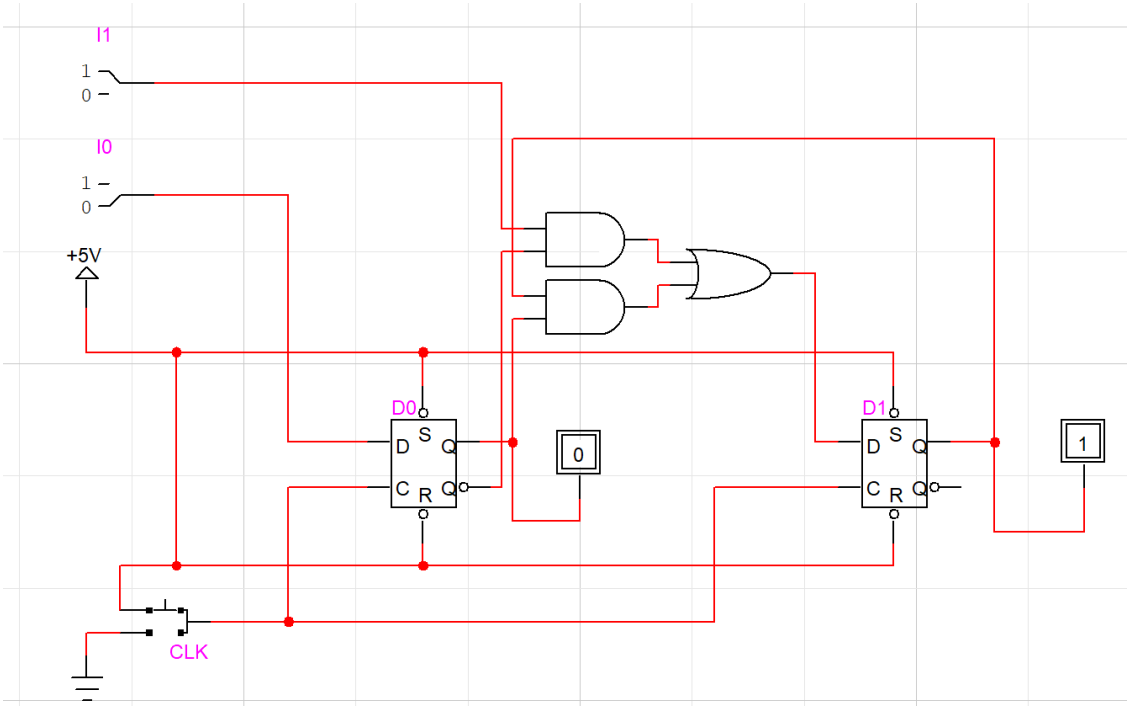


Figure 12: Problem 6(f) Solution.