Digital Circuits: Homeworks #4

Due on Friday, May 26, 2017

Note: Late homework is not accepted. Good luck.

1. **Gated S-R Latch.**
   For a gated S-R latch, draw the Q and $\bar{Q}$ outputs for the inputs in Figure 1. Show them in proper relation to the enable input. Assume that Q starts LOW.

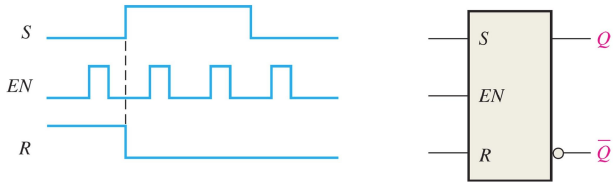

Figure 1: Input Waveform.

2. **Gated D Latch.**
   Determine the output of a gated D latch for the inputs in Figure 2. Assume that Q starts LOW.

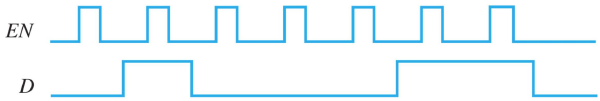

Figure 2: Input Waveform.

3. **J-K Flip-Flops.**
   Two edge-triggered J-K flip-flps are shown in Figure 3. If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. Assume that flip-flops are initially RESET.

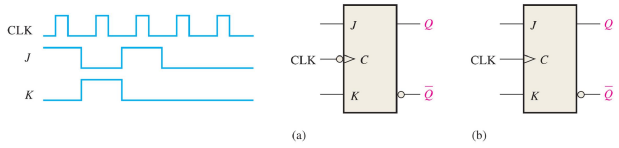

Figure 3: Input Waveform.

4. **D Flip-Flops.**
   A D flip-flop is connected as shown in Figure 4. Draw the Q output in relation to the clock when the flip-flop is initially RESET. What specific function does this device perform?

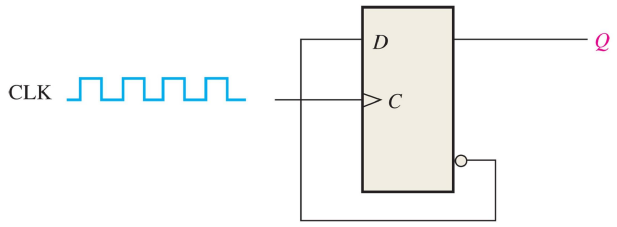

Figure 4: Input Waveform.