Digital Fundamentals

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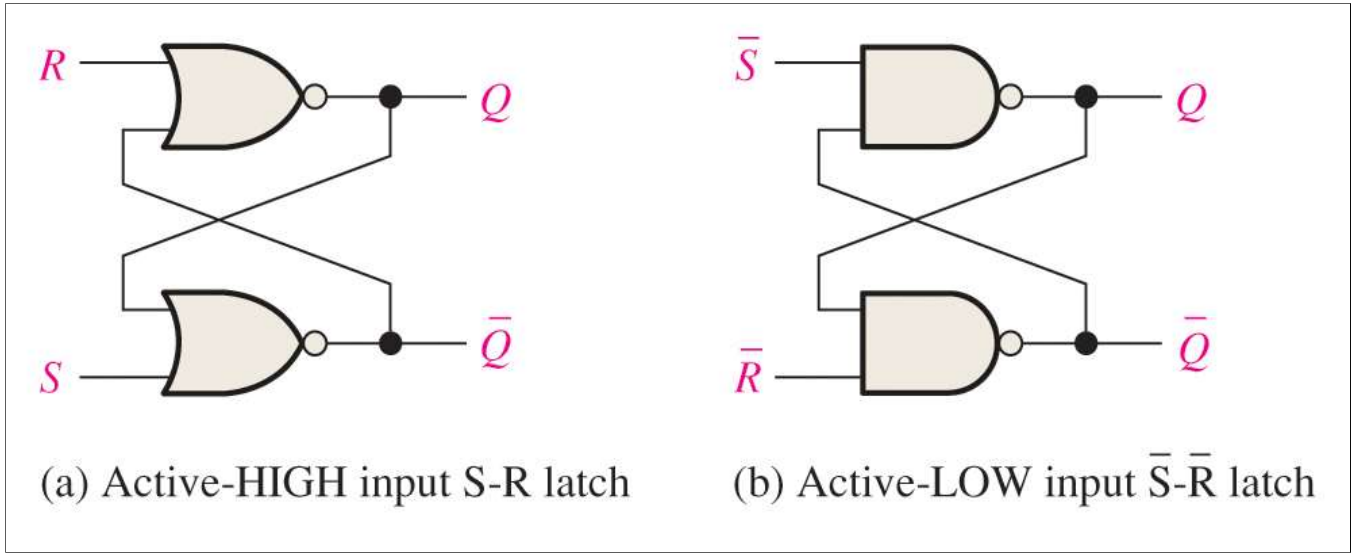
Latches, Flip-Flops, and Timers
Chapter 7

Latches

A **latch** is a temporary storage device that has two stable states (bistable). It is a basic form of memory.



(a) Active-HIGH input S-R latch (b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

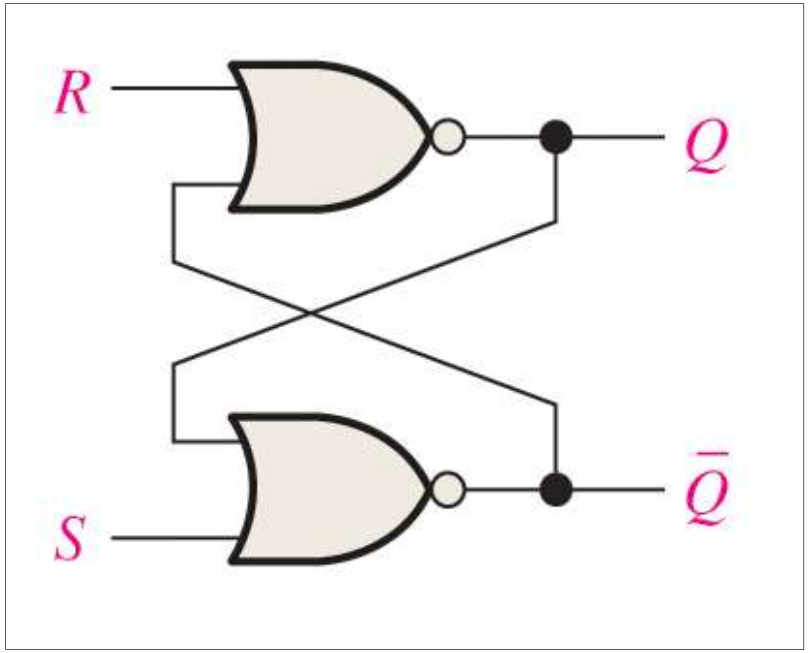
The S-R (Set-Reset) latch is the most basic type. It can be constructed from NOR gates or NAND gates. With NOR gates, the latch responds to active-HIGH inputs; with NAND gates, it responds to active-LOW inputs.

Latches

The active-HIGH *S*-*R* latch is in a stable (latched) condition when both inputs are LOW.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (0). To SET the latch ($Q = 1$), a momentary HIGH signal is applied to the *S* input while the *R* remains LOW.

To RESET the latch ($Q = 0$), a momentary HIGH signal is applied to the *R* input while the *S* remains LOW.

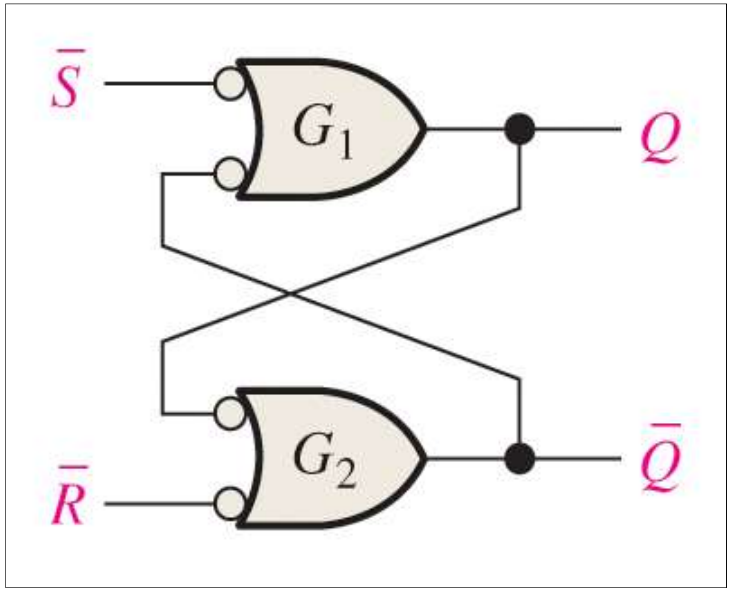


Latches

The active-LOW $\overline{S}$-$\overline{R}$ latch is in a stable (latched) condition when both inputs are HIGH.

Assume the latch is initially RESET (Q = 0) and the inputs are at their inactive level (1). To SET the latch (Q = 1), a momentary LOW signal is applied to the $\overline{S}$ input while the $\overline{R}$ remains HIGH.

To RESET the latch a momentary LOW is applied to the $\overline{R}$ input while $\overline{S}$ is HIGH.



Never apply an active set and reset at the same time (invalid).

Latches

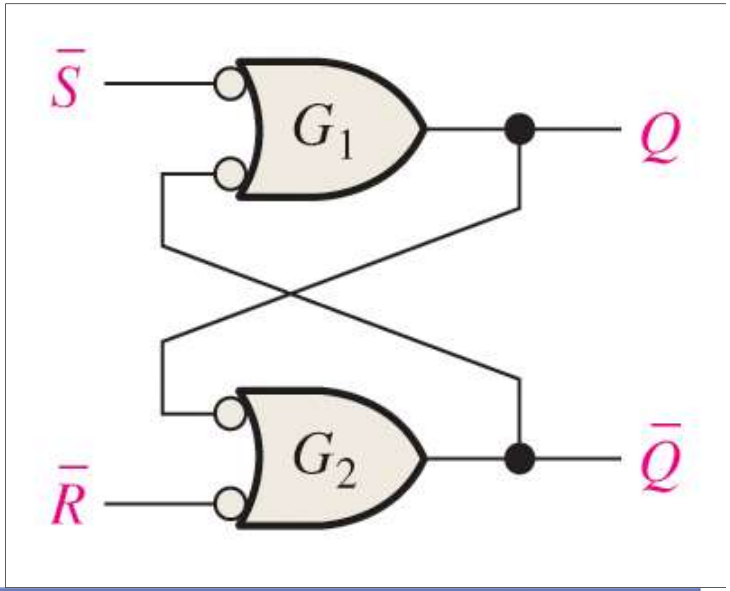


TABLE 7–1

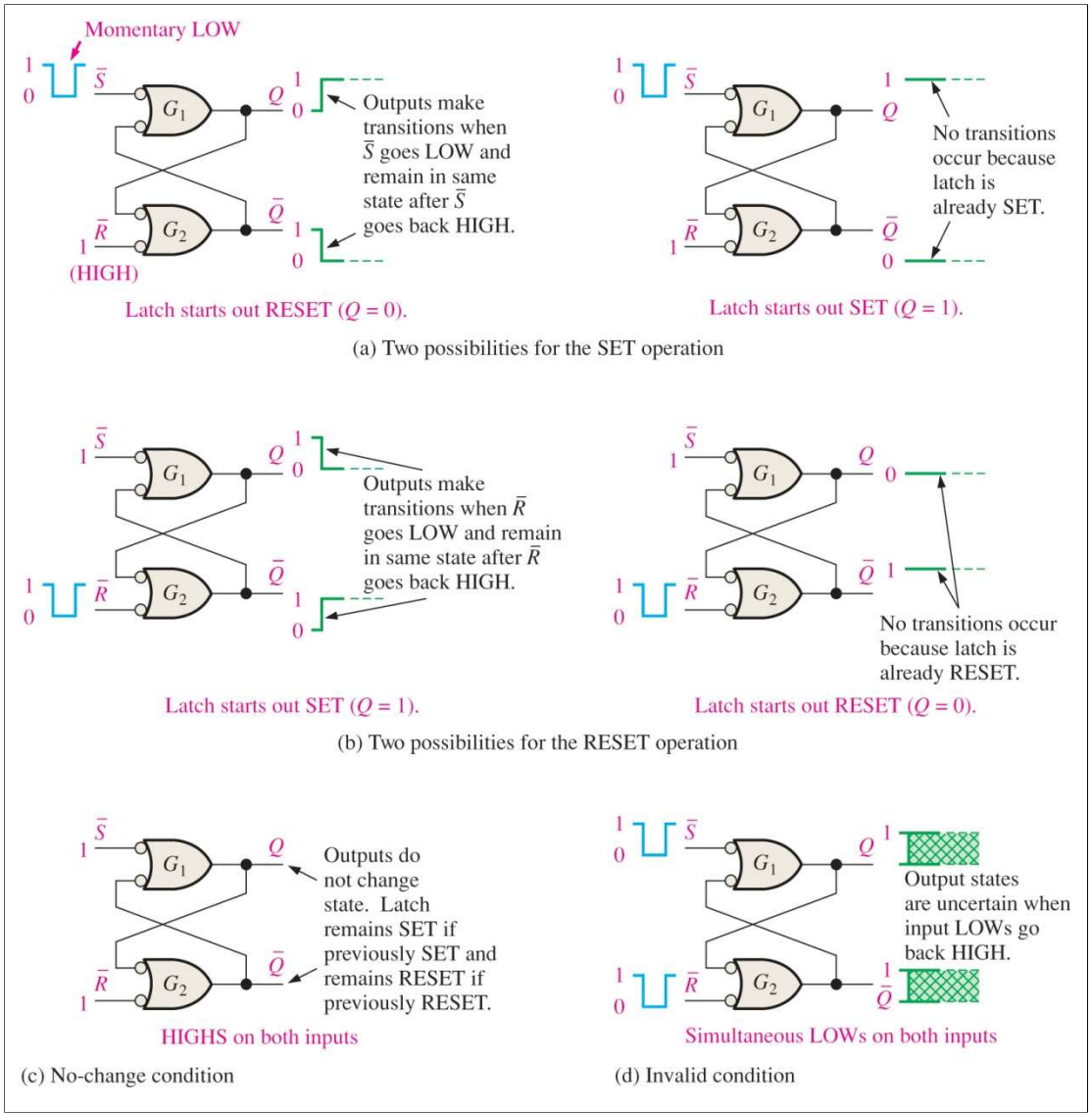
Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

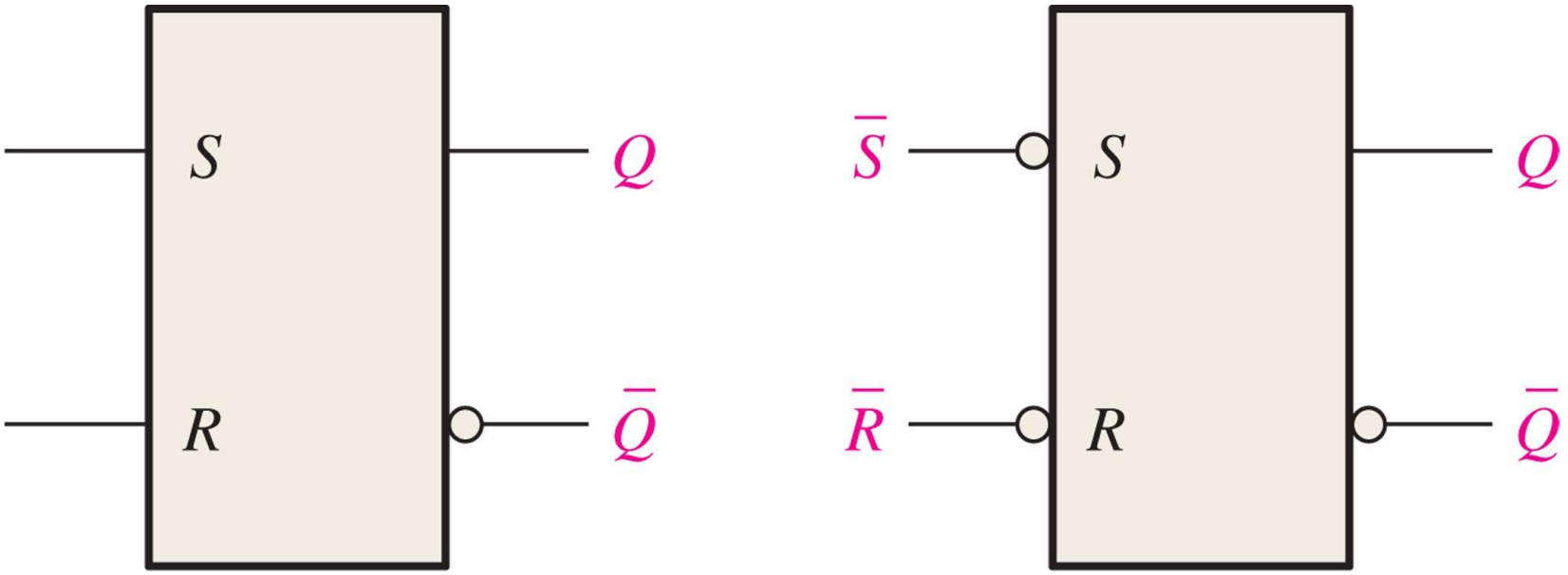
Ch.7 Summary

Latches

The three modes of basic S-R operation



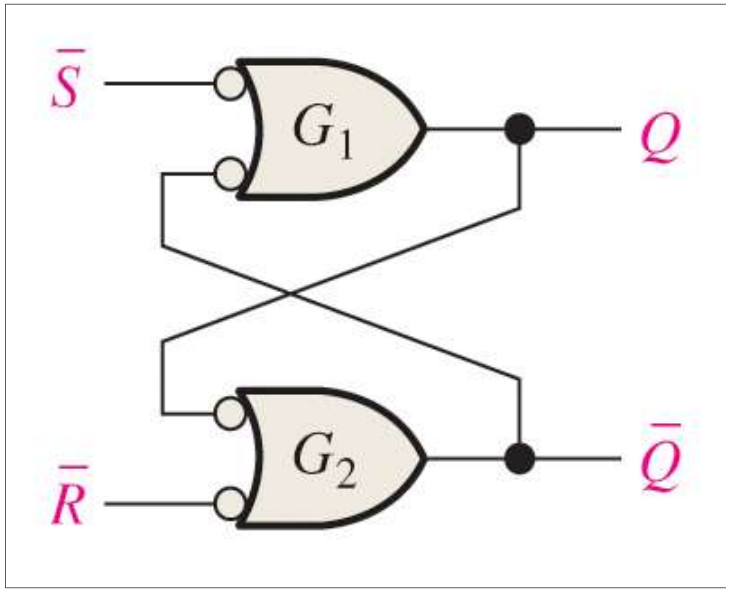
Latches

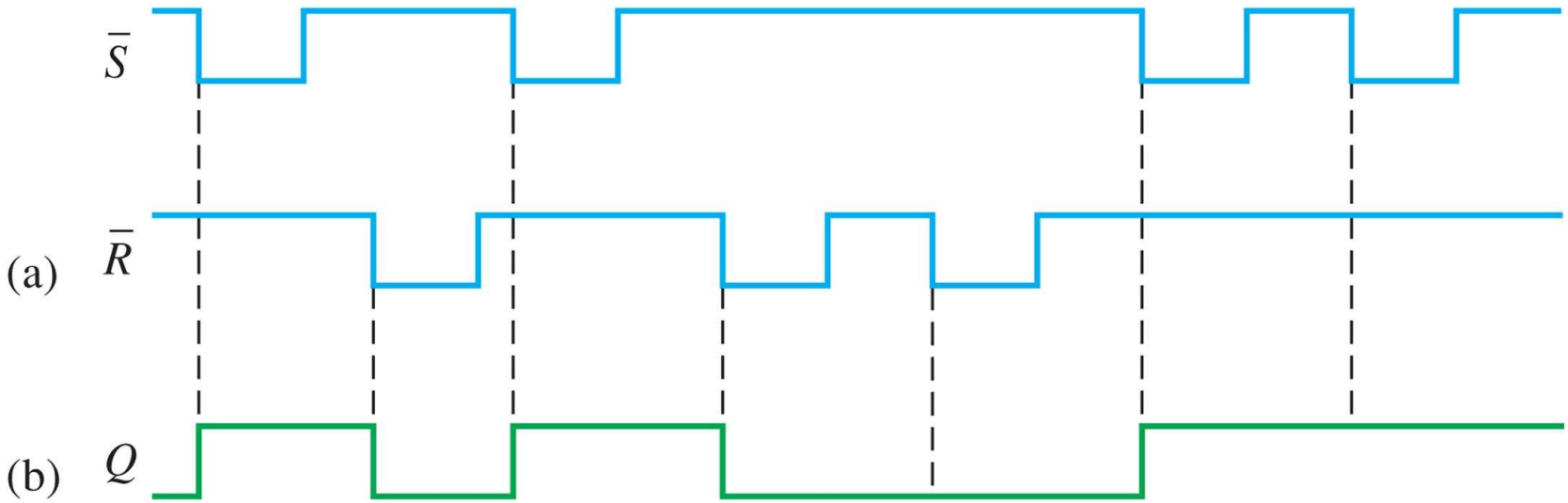


(a) Active-HIGH input S-R latch

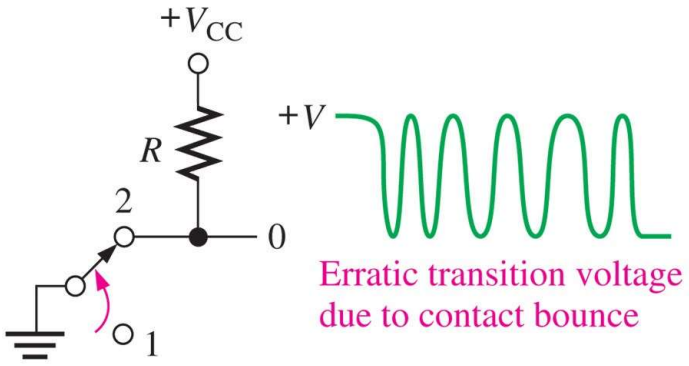
(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

Latches

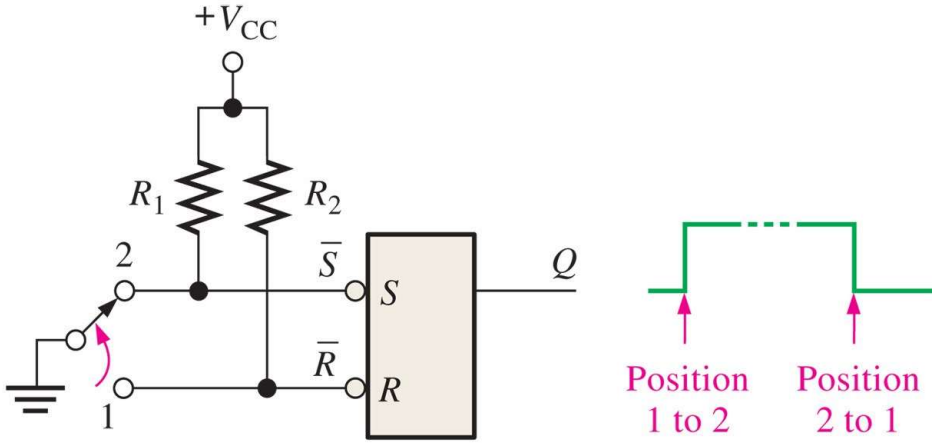




Latches: Applications



(a) Switch contact bounce

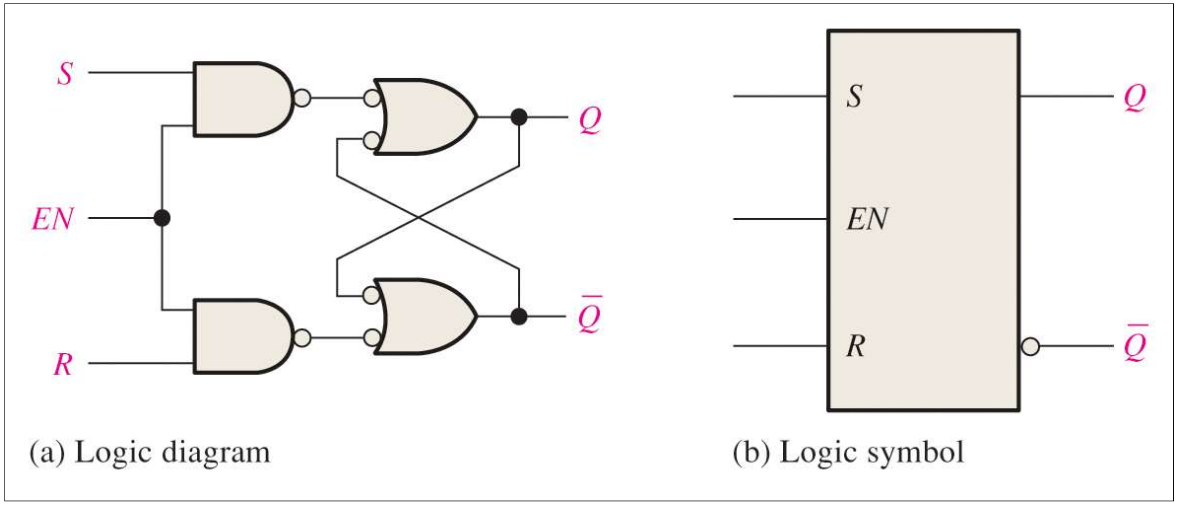


(b) Contact-bounce eliminator circuit

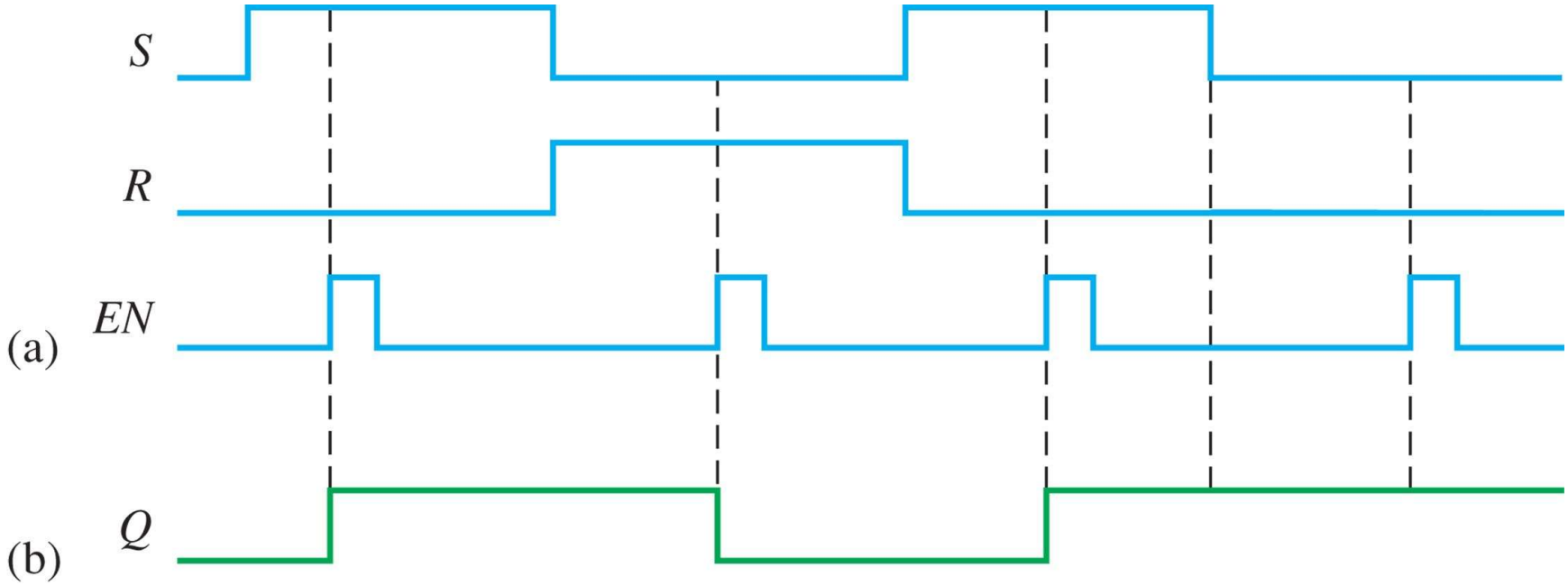
Gated S-R Latch

A gated latch is a variation on the basic latch.

The gated latch has an additional input, called enable (*EN*) that must be HIGH in order for the latch to respond to the *S* and *R* inputs.

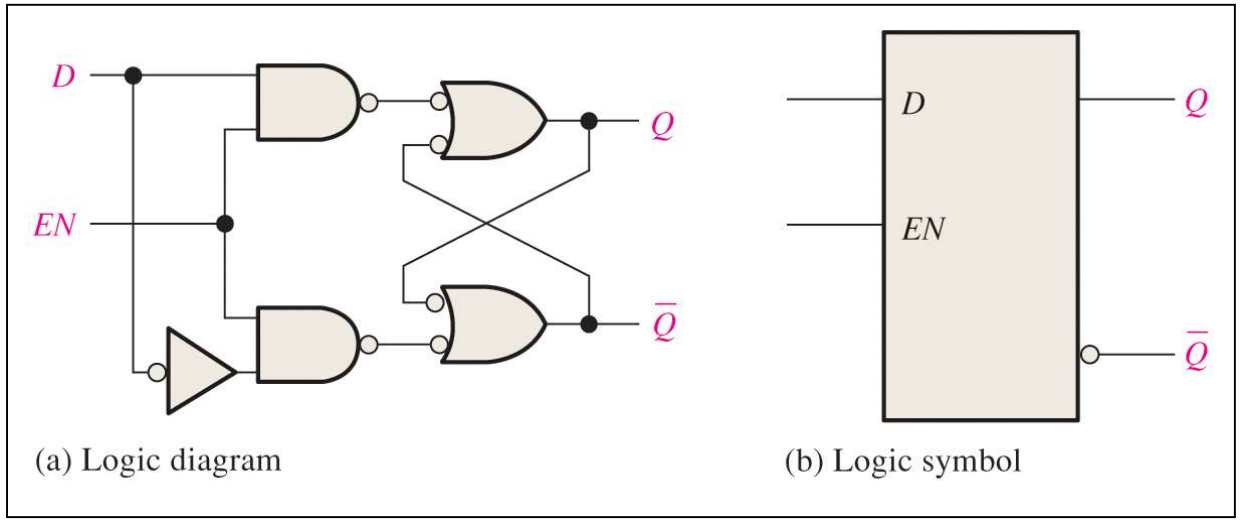


Gated S-R Latch



Gated D Latch

The *D* latch is an variation of the *S*-*R* latch but combines the *S* and *R* inputs into a single *D* input as shown:



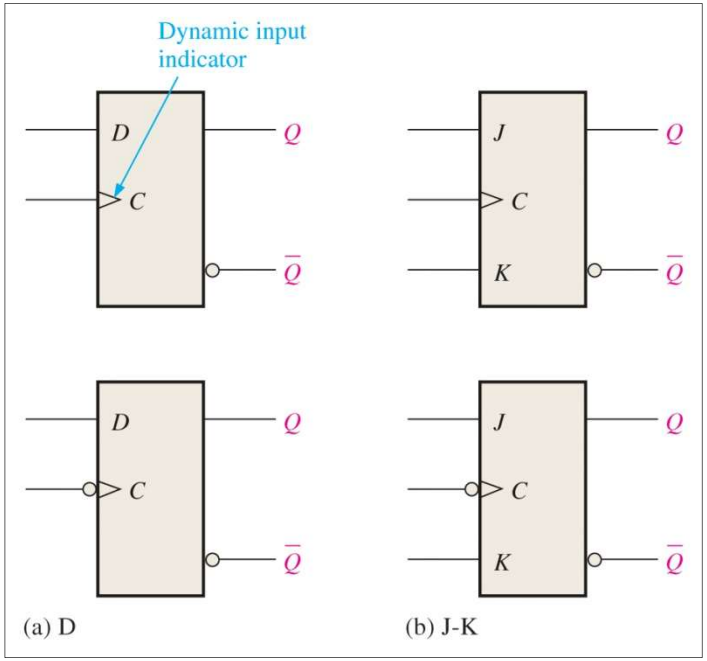
A simple rule for the *D* latch is:

Q follows *D* when the EN is active.

Flip-flops

A flip-flop differs from a latch in the manner it changes states. A flip-flop is a clocked device, in which only the clock edge determines when a new bit is entered.

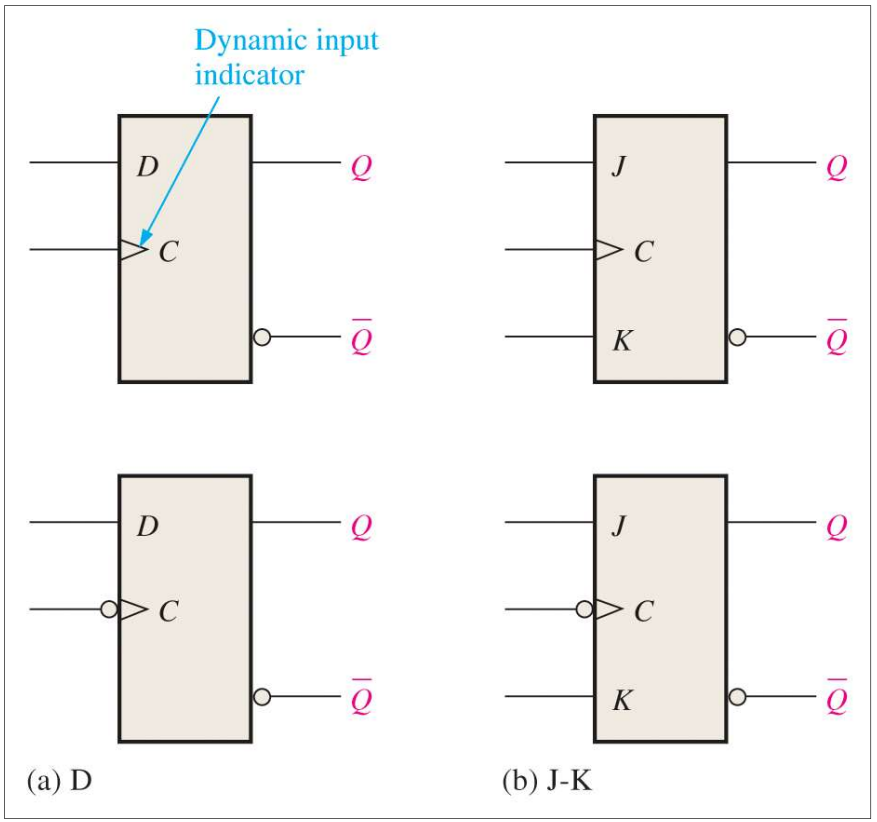
The active edge can be positive or negative.



Edge-Triggered Flip-flops

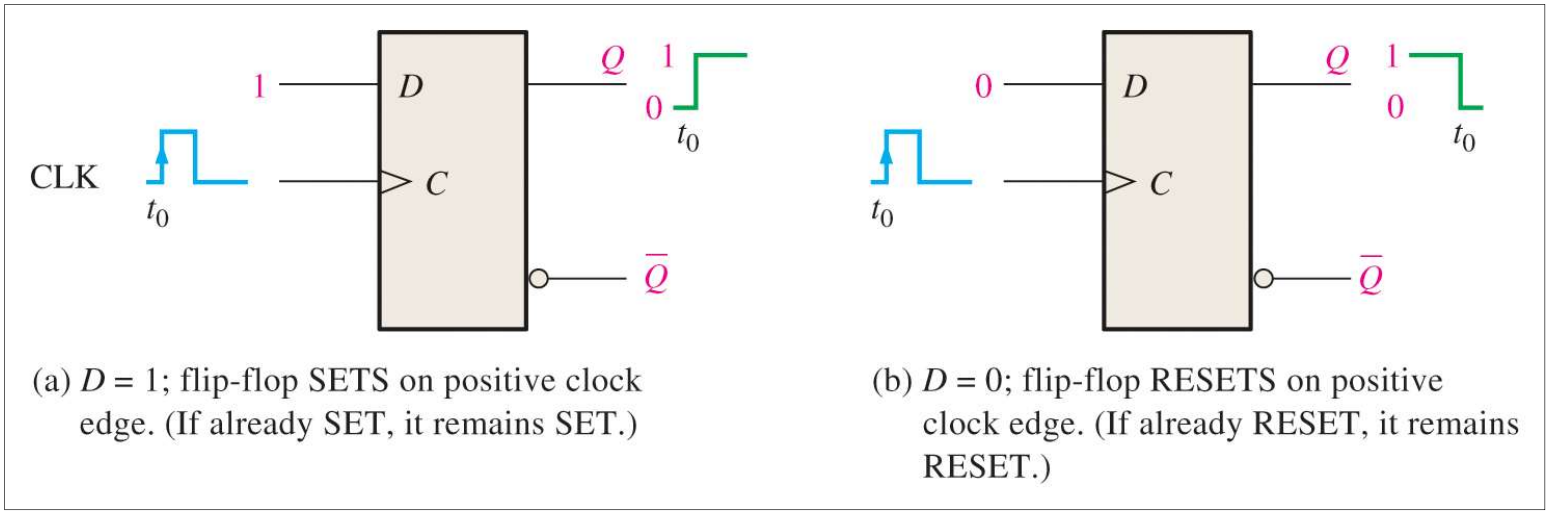
The output from an edge-triggered flip-flop changes on the positive-going or negative-going edge of its clock signal.

A bubble on the clock input indicates that it is a negative-edge triggered flip-flop.



Edge-Triggered D Flip-flops

The data bit at the D-input is transferred to the component output on the edge of the clock signal.

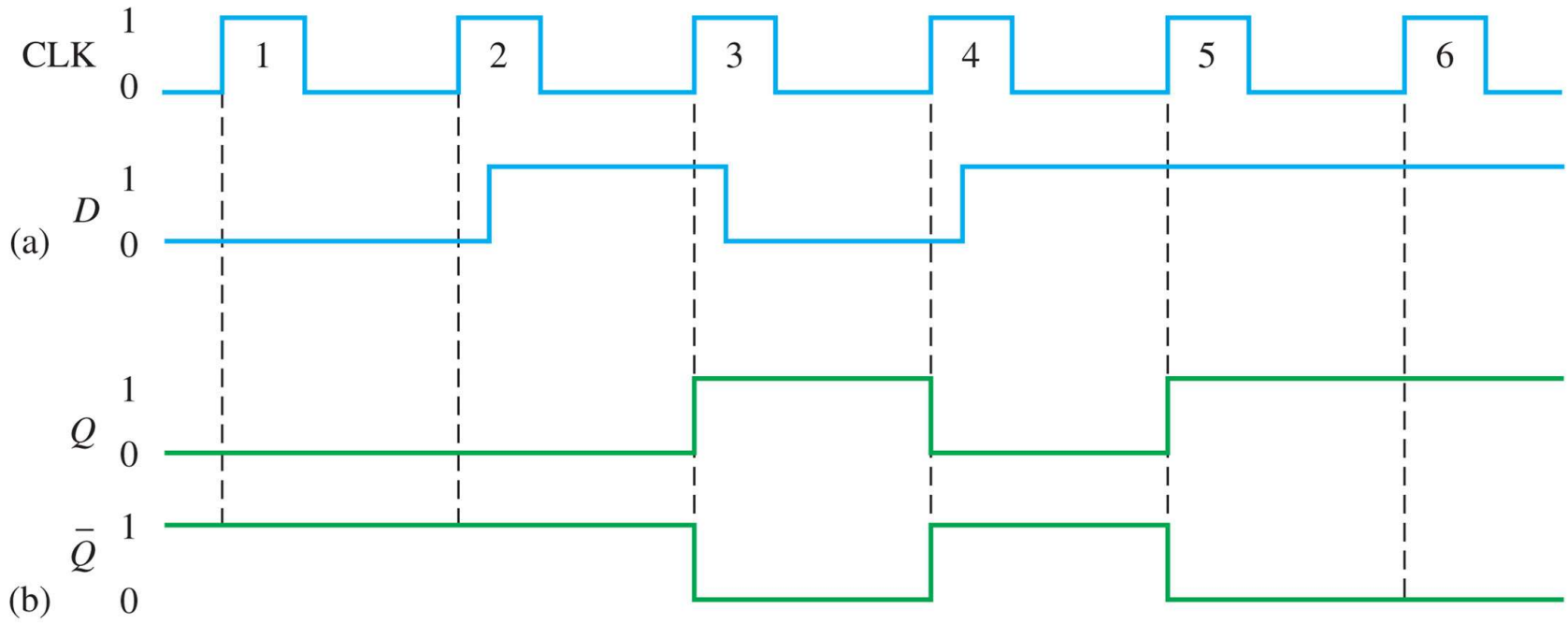


(a) $D = 1$; flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$; flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

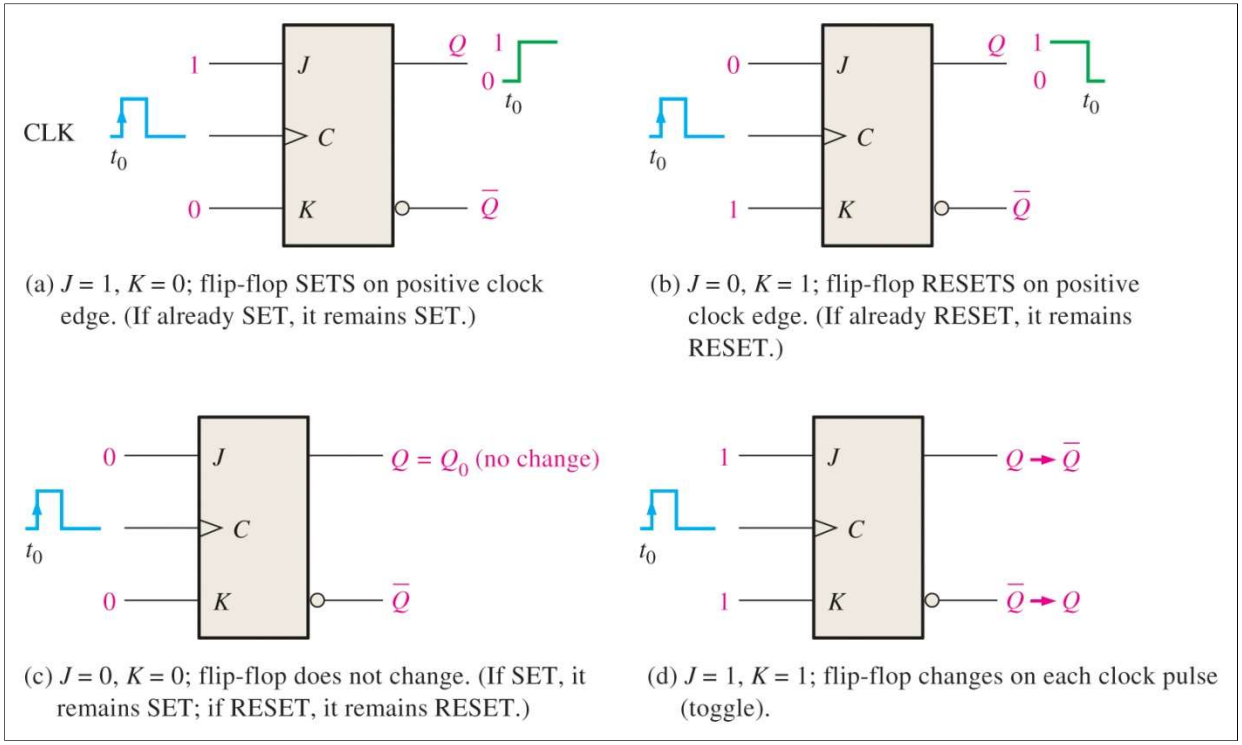
Once triggered, the output (Q) equals the last value at the D input until a new value is triggered in.

Edge-Triggered D Flip-flops



J-K Flip-flops

The values at the J and K inputs to a J-K flip-flop determine its output state. The results of the four possible input combinations of J and K are shown.



(a) $J = 1$, $K = 0$; flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $J = 0$, $K = 1$; flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

(c) $J = 0$, $K = 0$; flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

(d) $J = 1$, $K = 1$; flip-flop changes on each clock pulse (toggle).

J-K Flip-flops

TABLE 7–3

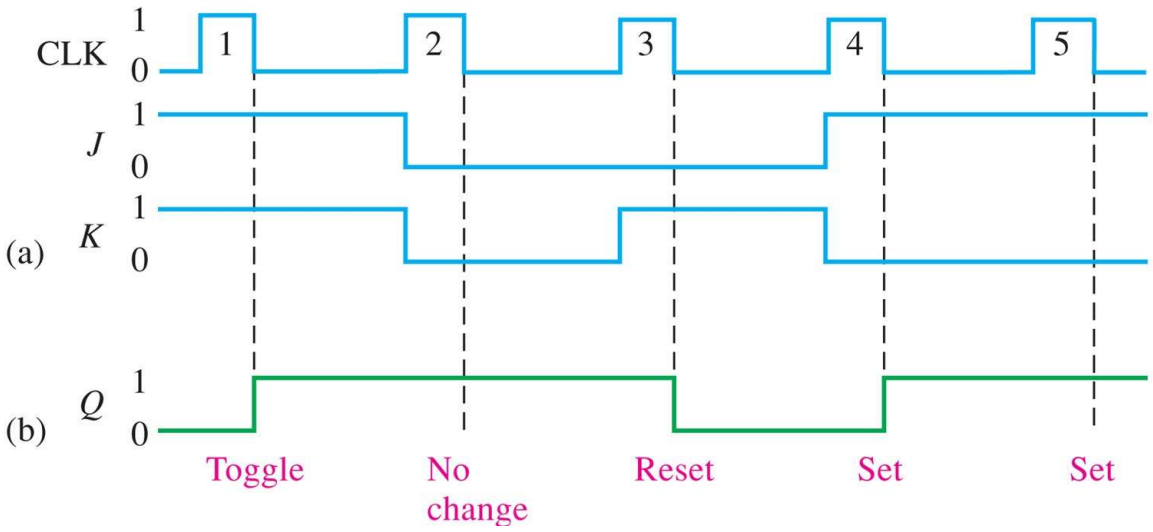
Truth table for a positive edge-triggered J-K flip-flop.

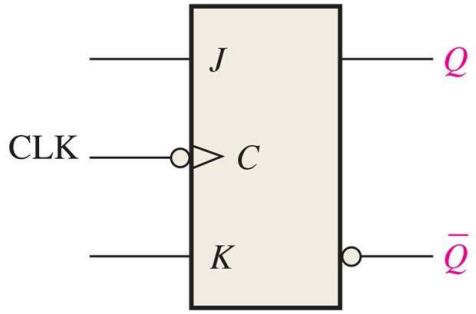
Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

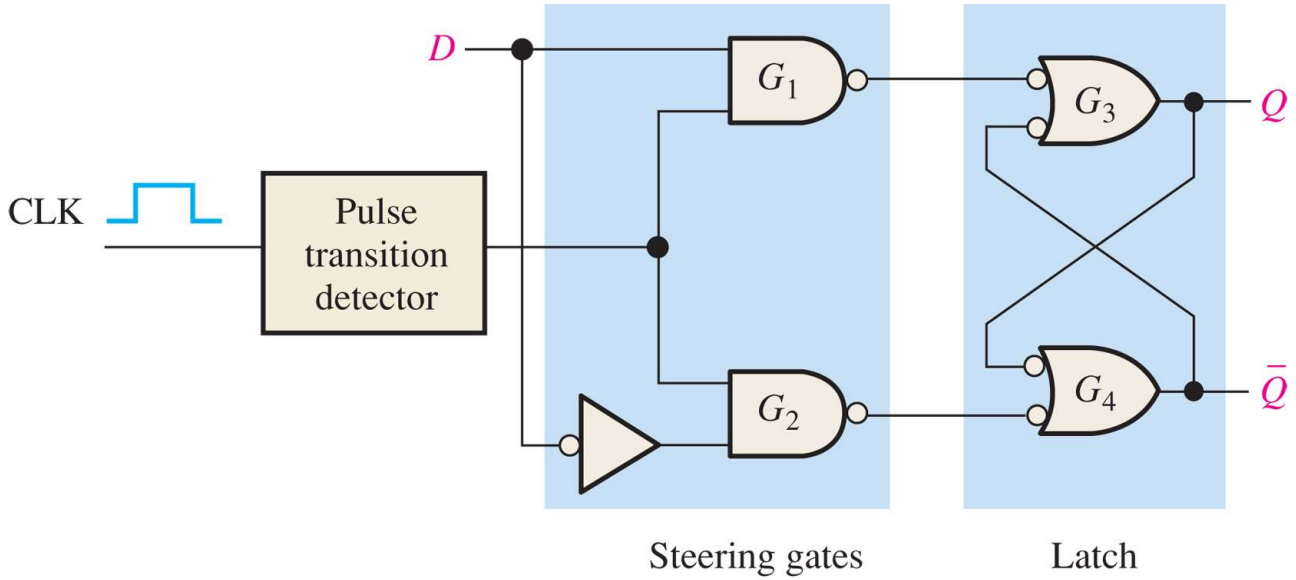
Q_0 = output level prior to clock transition

J-K Flip-flops

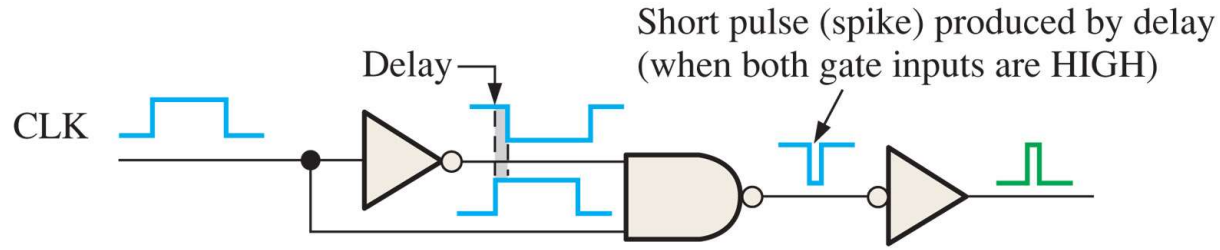




Edge Triggered Operation

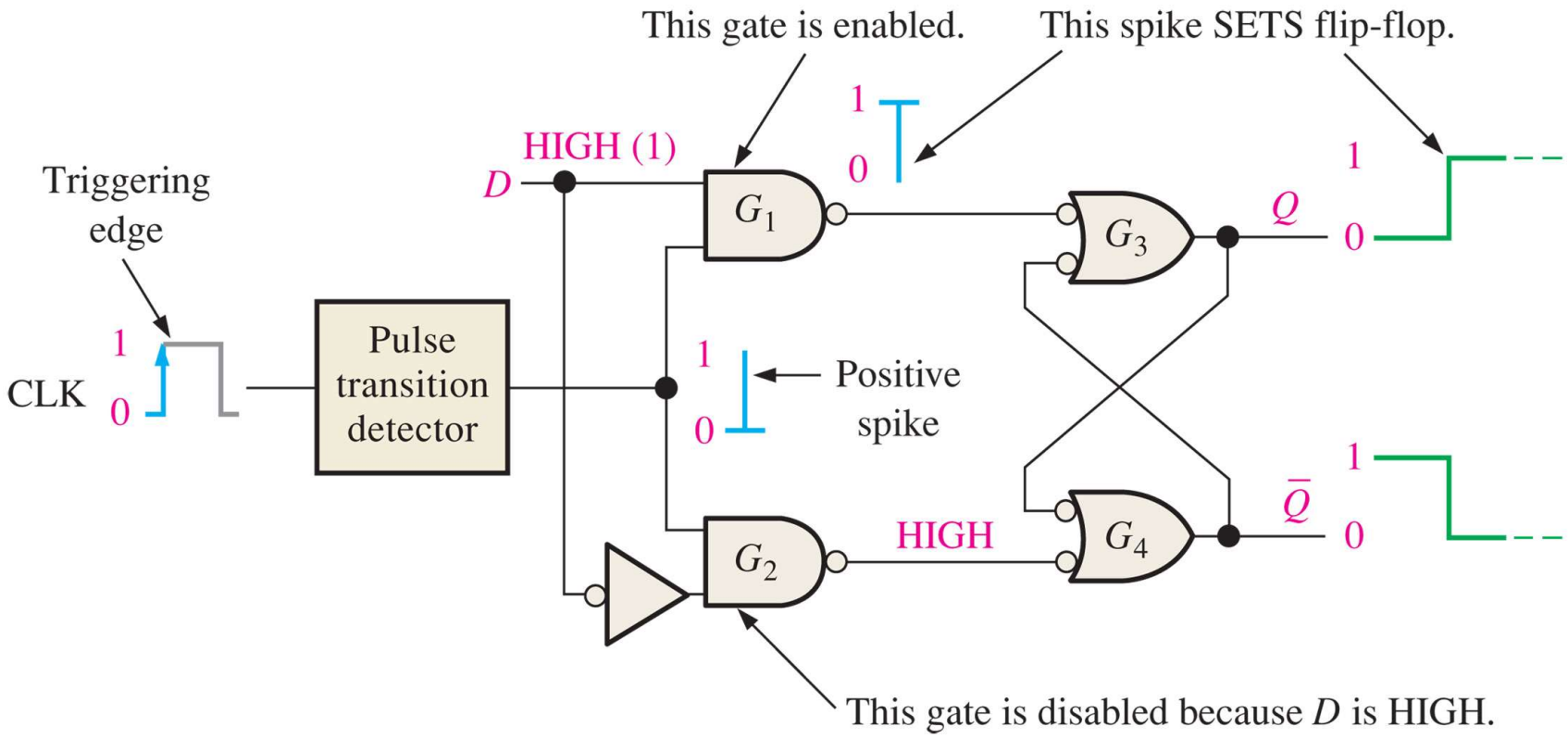


(a) A simplified logic diagram for a positive edge-triggered D flip-flop

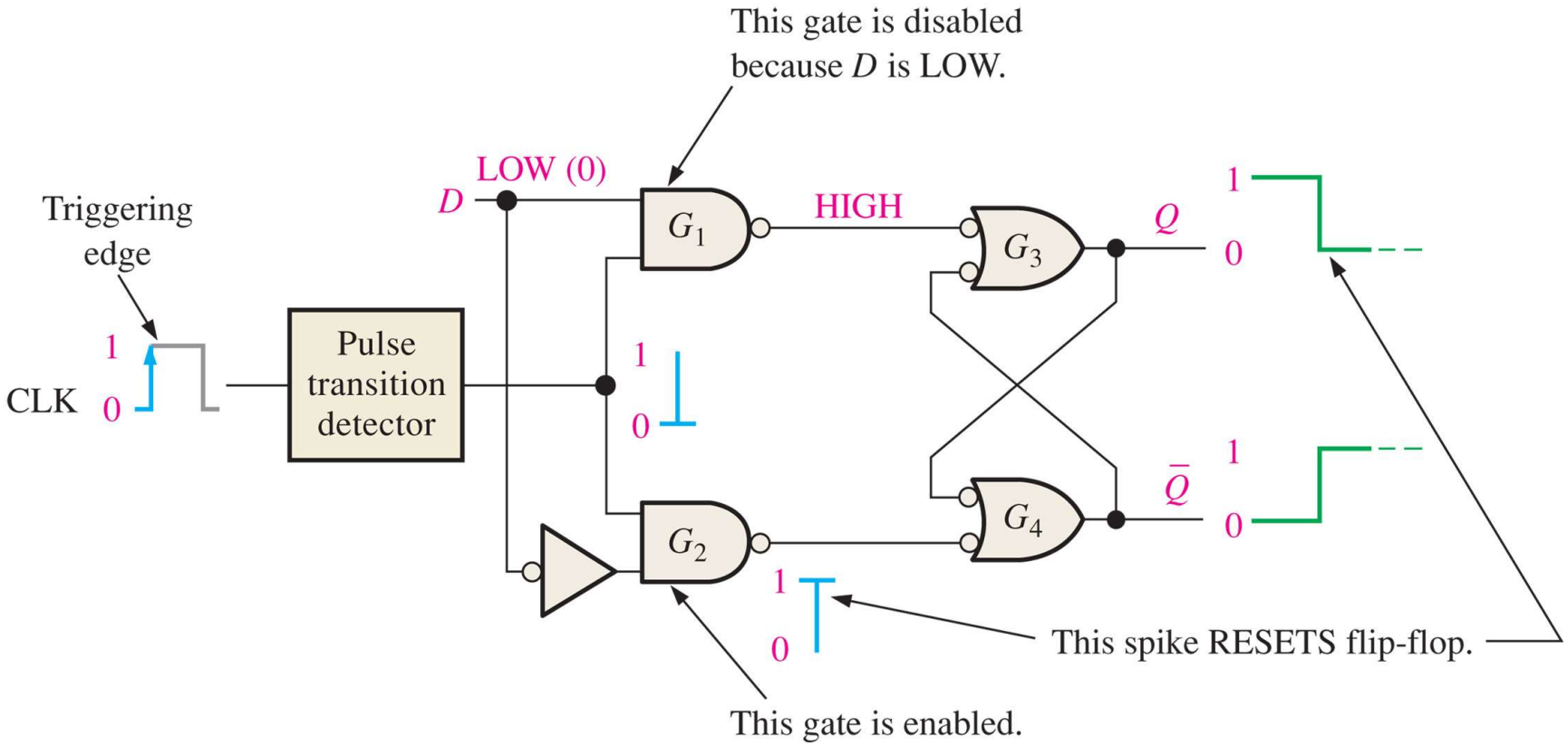


(b) A type of pulse transition detector

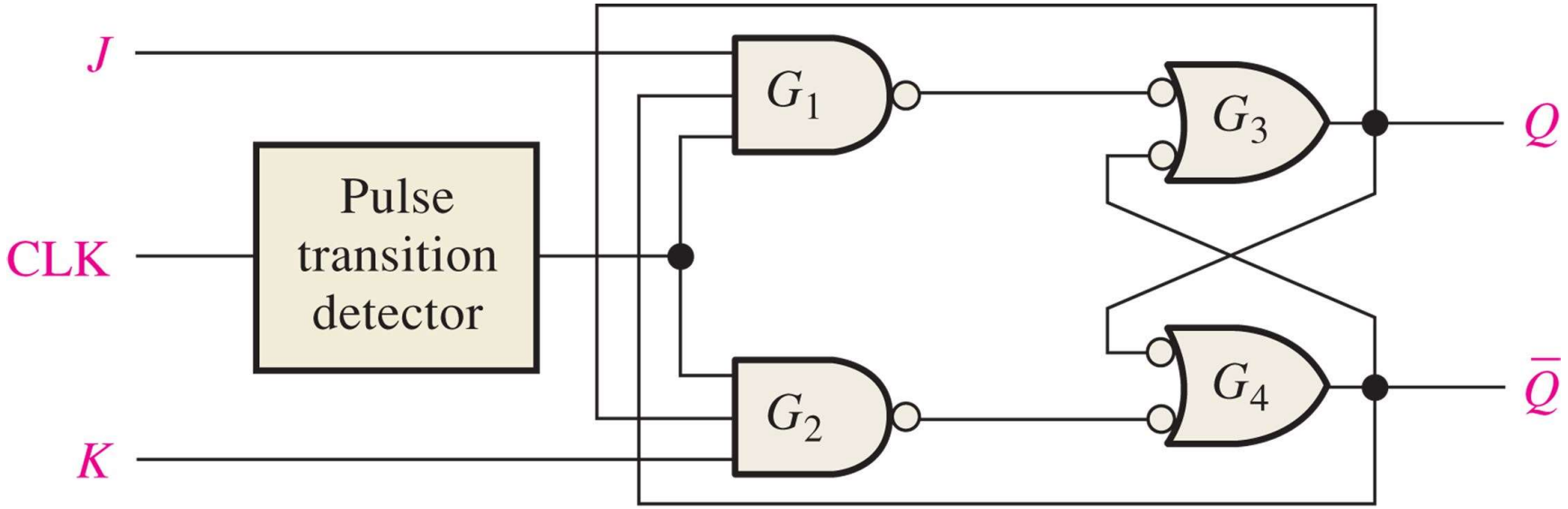
D Flip-flops


This gate is enabled.
This spike SETS flip-flop.
Triggering edge
CLK
1
0
Pulse transition detector
D
HIGH (1)
G_1
G_2
G_3
G_4
1
0
Positive spike
HIGH
Q
$\bar{Q}$
This gate is disabled because D is HIGH.

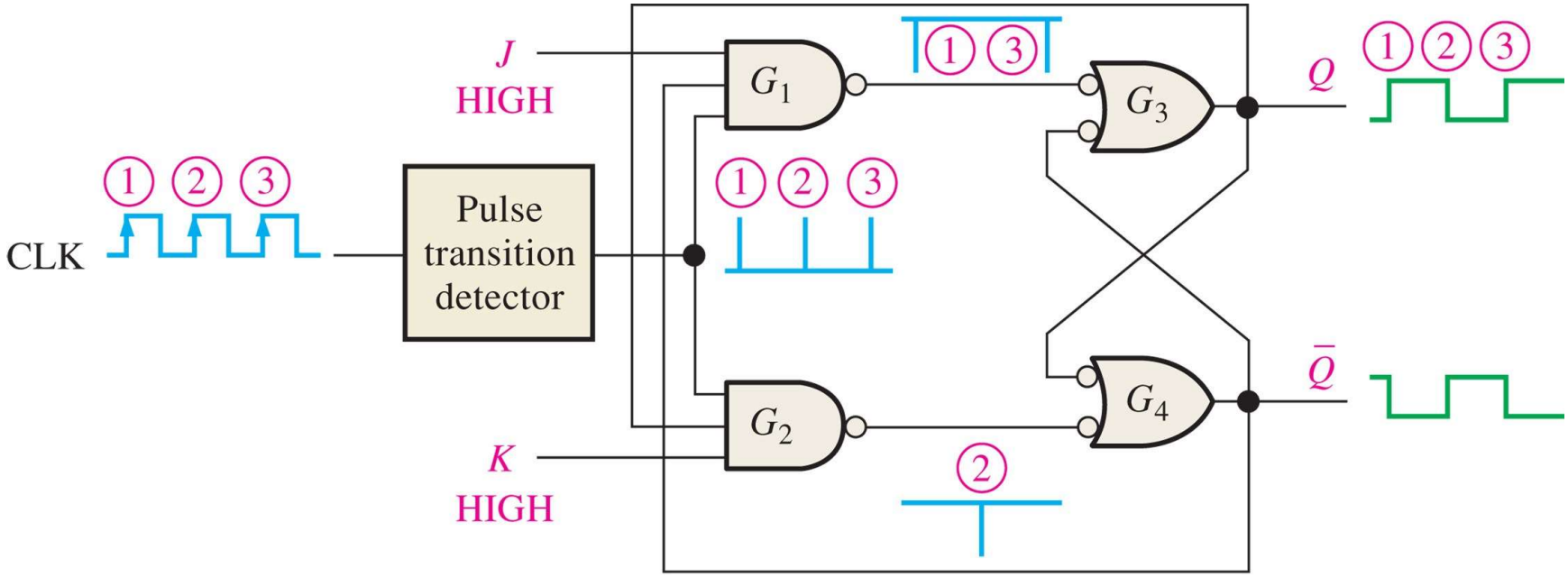
D Flip-flops


This gate is disabled
because D is LOW.
LOW (0)
D
Triggering
edge
1
CLK
0
Pulse
transition
detector
G1
HIGH
G3
Q
1
0
1
0
G2
G4
Q̄
1
0
1
0
1
0
This spike RESETS flip-flop.
This gate is enabled.

J-K Flip-flops



J-K Flip-flops

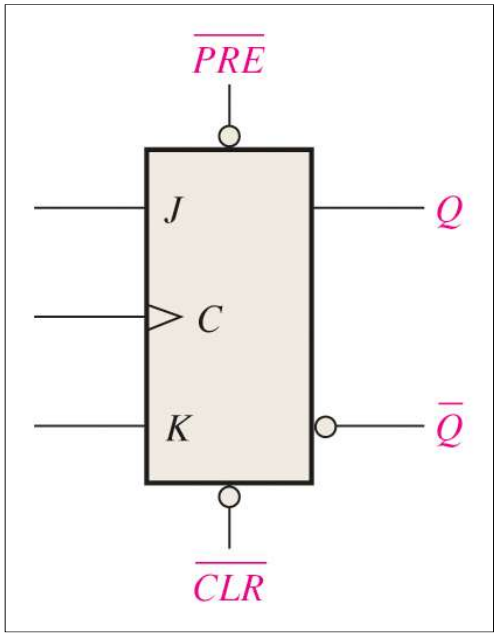


Flip-flop Asynchronous Inputs

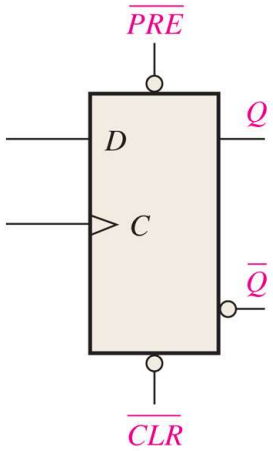
Synchronous (clocked) inputs are transferred on the triggering edge of the clock. Most flip-flops have other inputs that are **asynchronous**, meaning they operate independently of the clock.

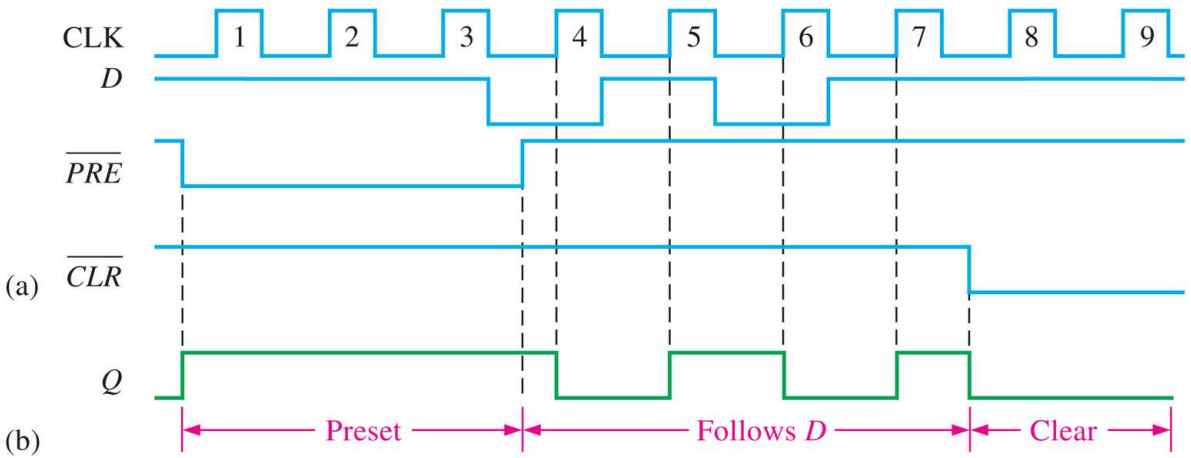
Asynchronous flip-flop inputs are normally labeled preset (*PRE*) and clear (*CLR*). These inputs are usually active LOW. A J-K flip flop with active LOW preset and CLR is shown.

Note that the asynchronous inputs always override the synchronous inputs.



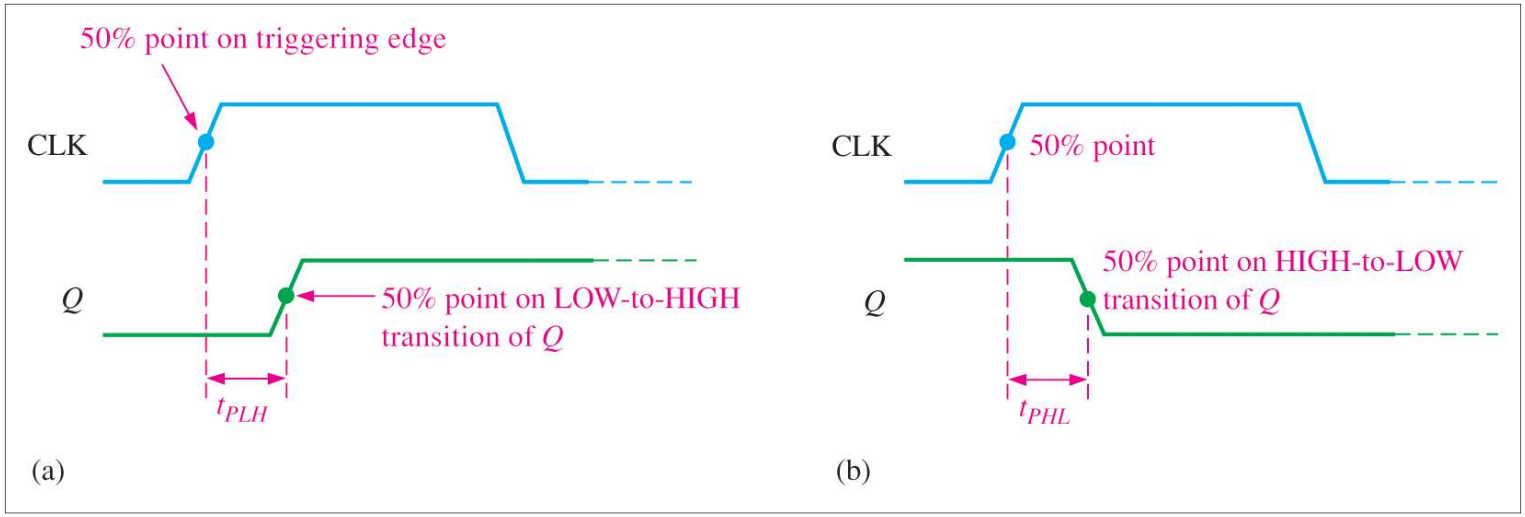
Flip-flop Asynchronous Inputs





Flip-Flop Propagation Delay

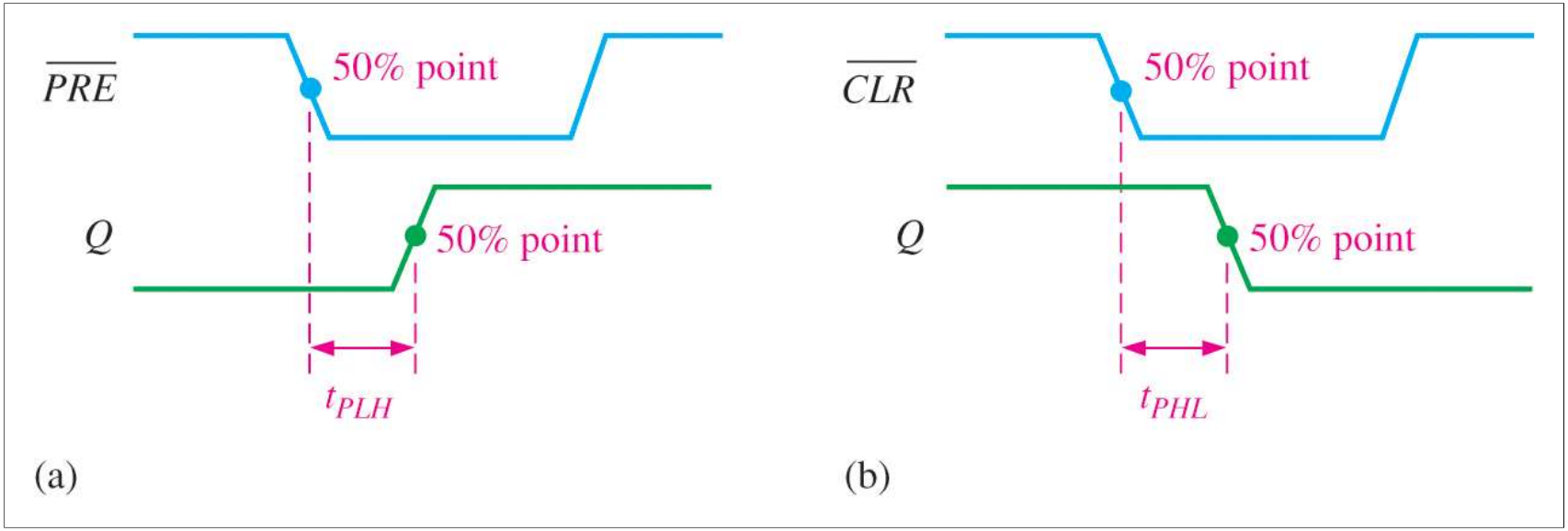
Propagation delay time is specified for the rising and falling outputs. It is measured between the 50% level of the clock to the 50% level of the output transition.



Propagation delay (t_{PLH}) is measured as shown in (a). Propagation delay (t_{PHL}) is measured as shown in (b).

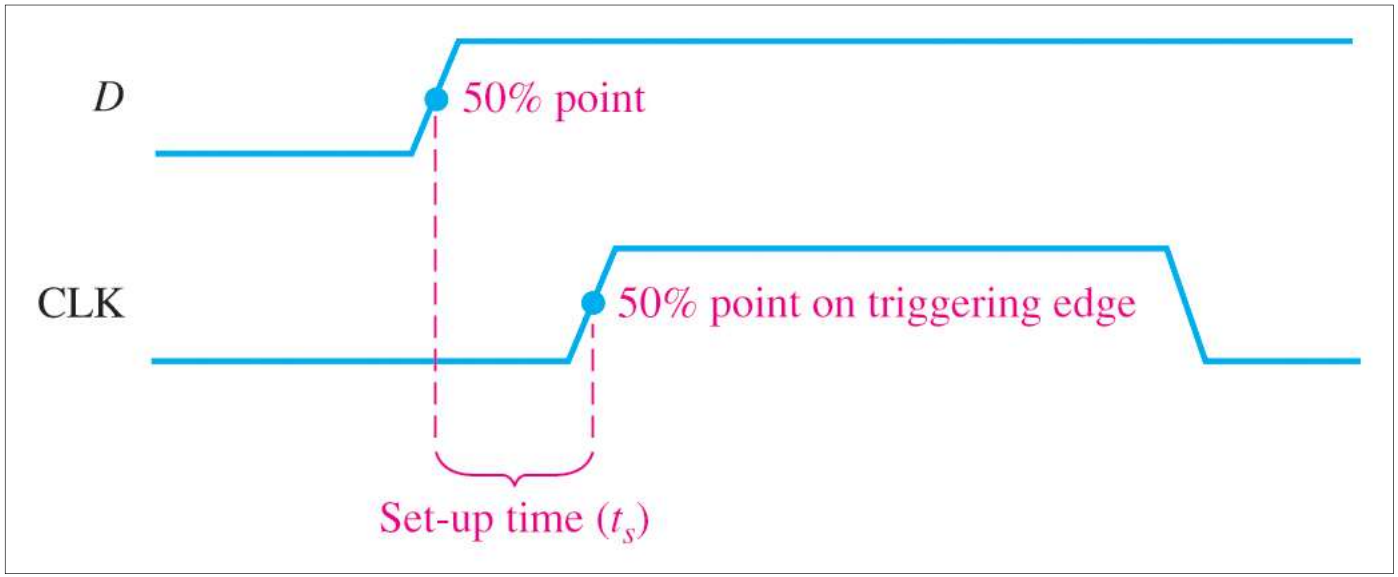
Flip-flop Propagation Delay

Another **propagation delay time** specification is the time required for an *asynchronous input* to cause a change in the output. Again it is measured from the 50% levels.



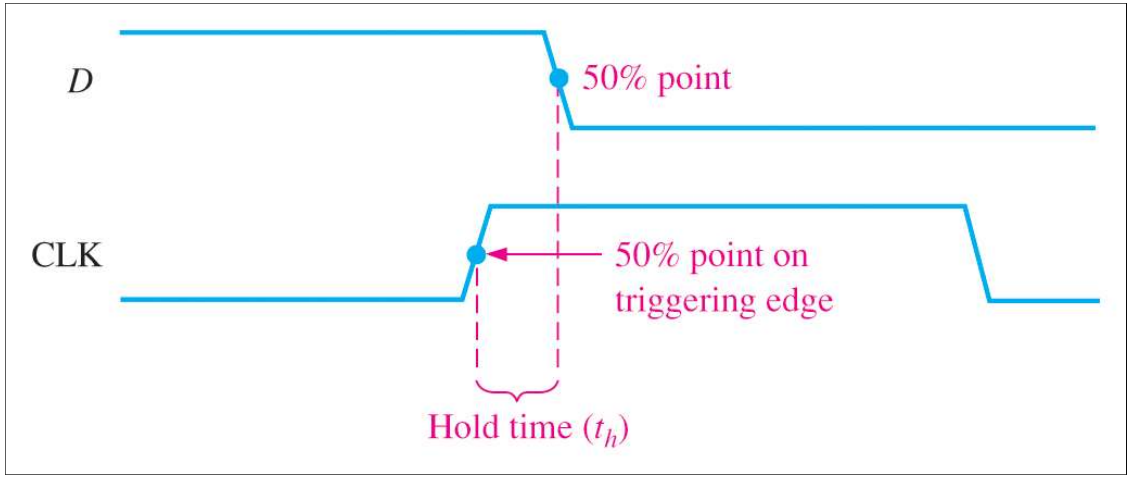
Flip-flop Set-up Time

Another time-related specification is flip-flop **set-up time**. This is the minimum time between the arrival of an input to the D (or J-K) flip-flop and the CLK signal.



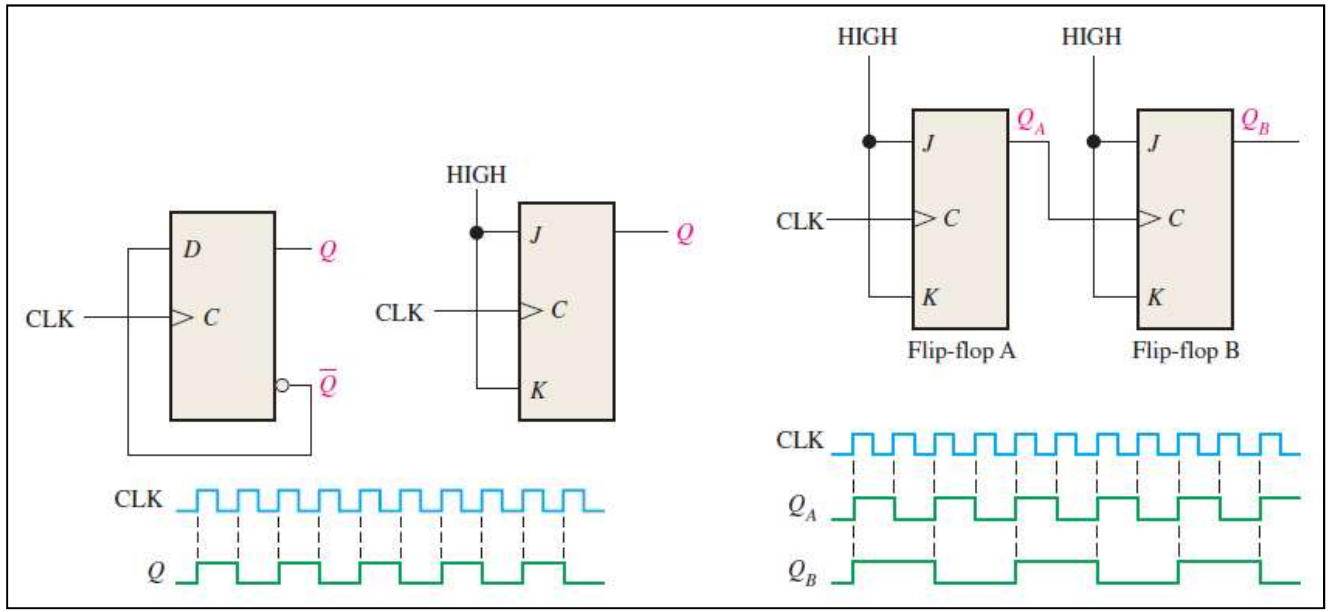
Flip-flop Hold Time

Another time-related specification is flip-flop **hold time**. This is the minimum time over which the input to the D (or J-K) flip-flop must remain stable *after* the arrival of the CLK input for reliable triggering.



Flip-Flop Frequency Division

Flip-flops can be used as frequency dividers, as shown below.



The D and J-K flip flops on the left are wired as “divide-by-2” circuits.

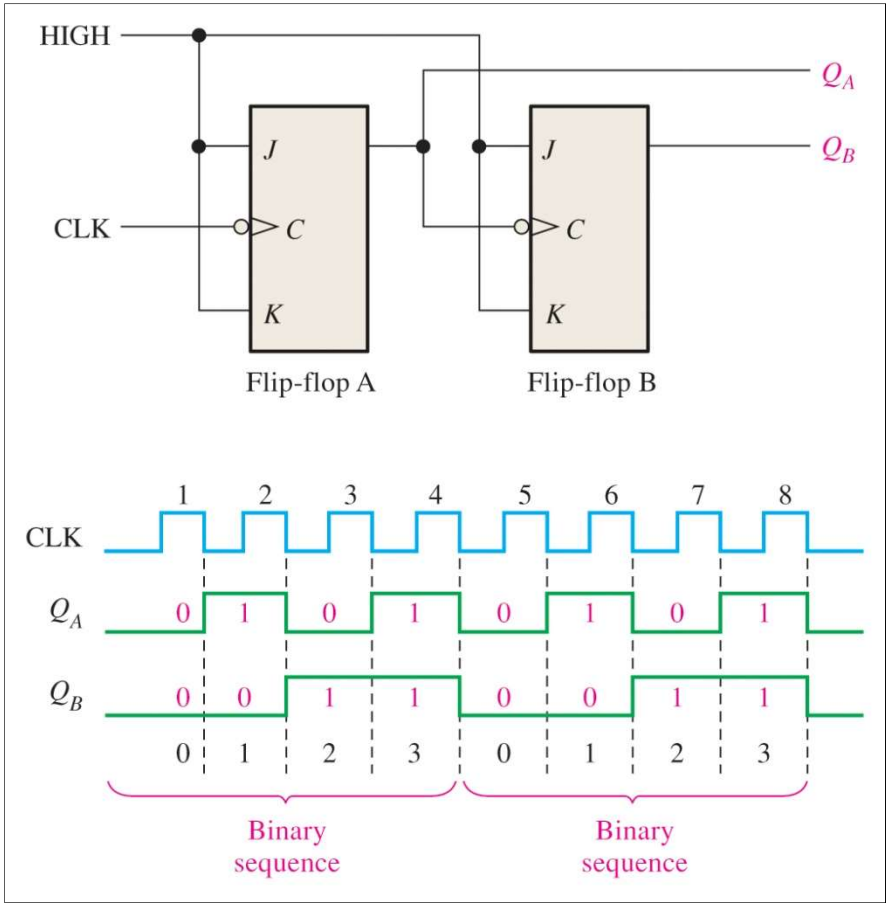
The J-K flip-flops on the right are cascaded to form a “divide-by-4” circuit.

Flip-Flop Counters

Flip-flops can be used to count the number of clock signals they receive as shown here.

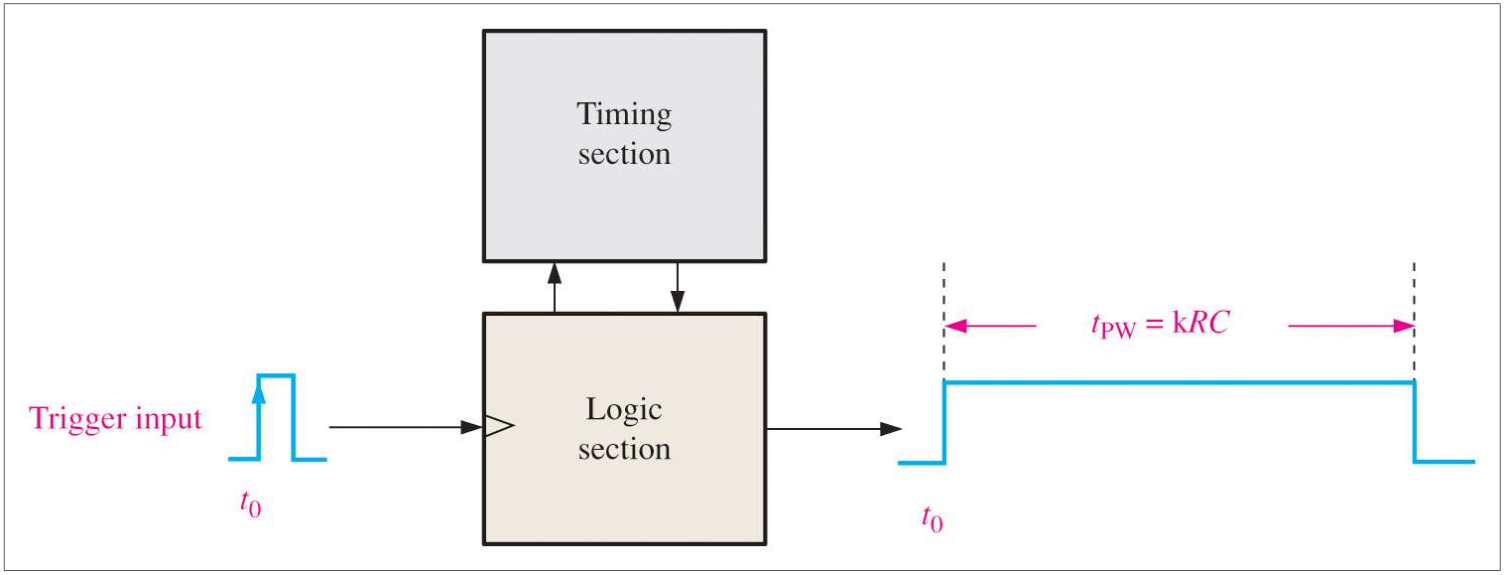
Each CLK input triggers the flip-flops, which are wired to toggle whenever triggered.

The Q_A and Q_B outputs indicate the number of CLK inputs received.



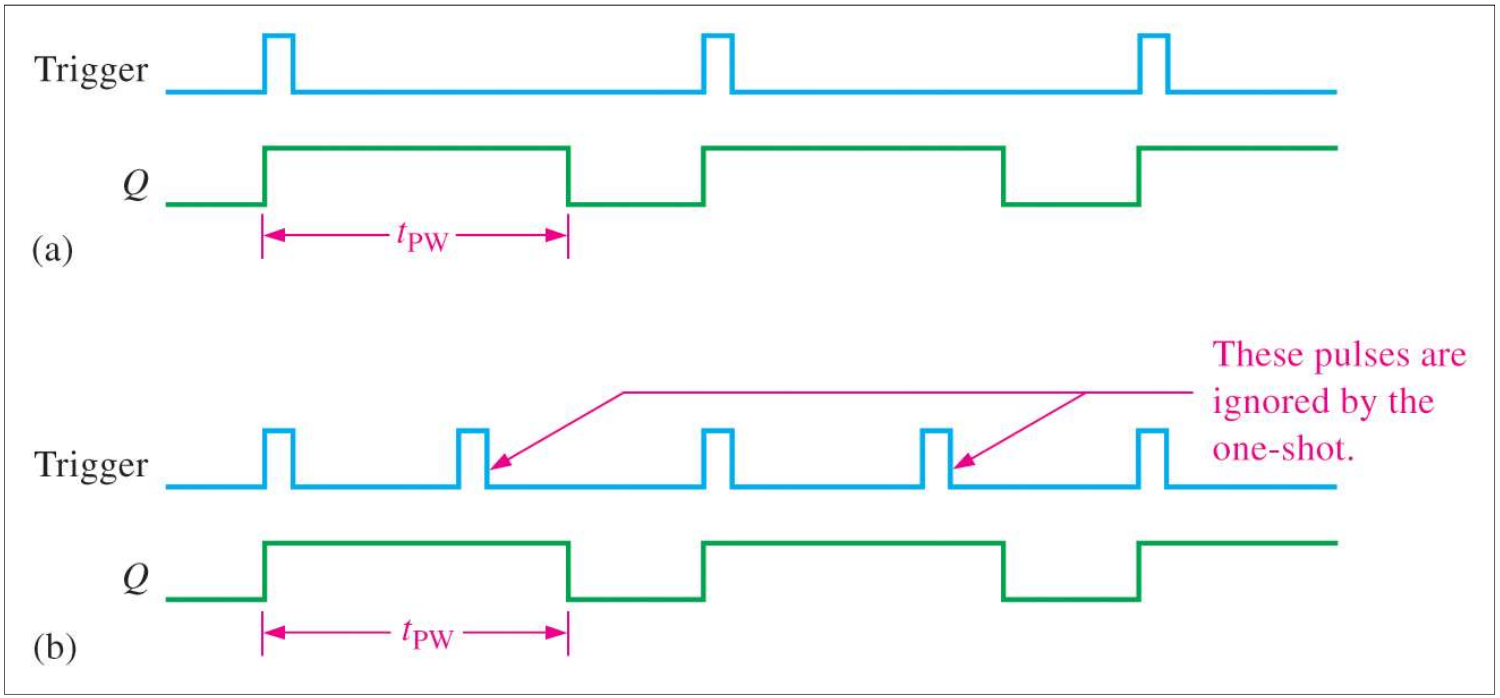
One-Shots

The **one-shot** or **monostable multivibrator** is a device with only one stable state. When triggered, it goes to its unstable state for a predetermined length of time, then returns to its stable state.



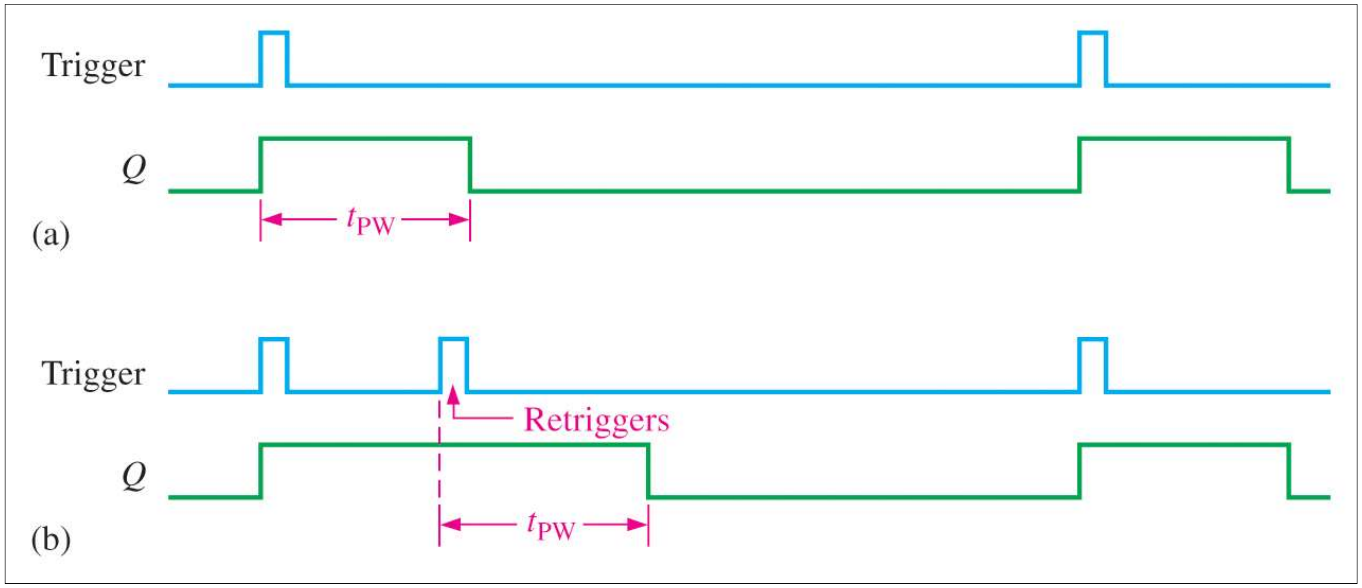
Nonretriggerable One-Shots

A **nonretriggerable** one-shot does not respond to any triggers that occur while in its unstable state, as shown here.



Retriggerable One-Shots

Retriggerable one-shots respond to any trigger, even if it occurs while the component is in its unstable state. If it occurs during the unstable state, the state is extended by an amount equal to its normal output pulse width.



A One-Shot Sequential Timer

One-shots can be wired (as shown) to form a sequential timer; a circuit that can set up a sequence of actions, such as lighting a group of lights in a particular order.