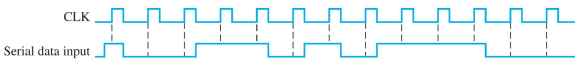
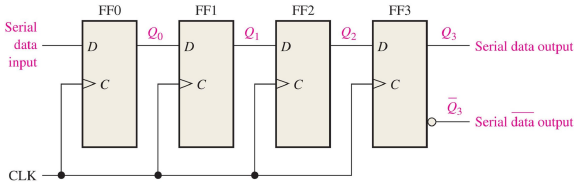
Digital Circuits: Homeworks #5 Solutions

1. **Shift Register Data I/Os.**
For the data input and clock in Figure 1a, determine the states of each flip-flop in the shift register of Figure 1b and show the Q waveforms. Assume that the register contains all 1s initially.



(a) Input Waveform.



(b) Serial In/Serial Out Shift Register.

Figure 1: Input Waveform and Serial In/Serial Out Shift Register.

Solution: Shift Register Data I/Os
All the Q values are being shifted to right and Q_0 takes the serial data input at every clock. Figure 2 shows the Q waveforms.

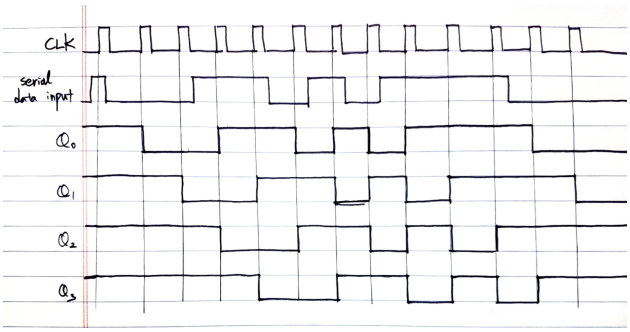
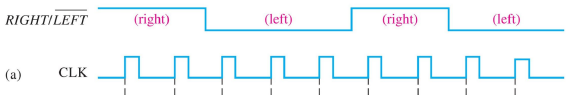


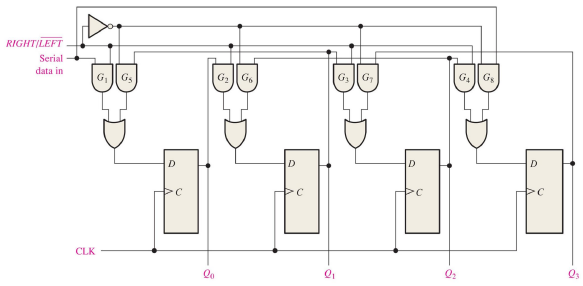
Figure 2: Output Waveform.

2. **Bidirectional Shift Registers.**
Determine the state of the shift register of Figure 3b after each clock pulse for the given $RIGHT/\overline{LEFT}$ control input waveform in Figure 3a. Assume that $Q_0 = 0$, $Q_1 = 1$, $Q_2 = 1$, $Q_3 = 0$, and that the serial data-input line is HIGH.

Solution: Bidirectional Shift Registers.
If $RIGHT/\overline{LEFT} = 1$, all the Q values are being shifted to right and Q_0 takes the serial data input at every clock. If $RIGHT/\overline{LEFT} = 0$, all the Q values are being shifted to left and Q_3 takes the serial data input at every clock. Figure 2 shows the Q waveforms.



(a) Input Waveform.



(b) 4-bit Bidirectional Shift Register.

Figure 3: 4-bit Bidirectional Shift Register and Input Waveform.

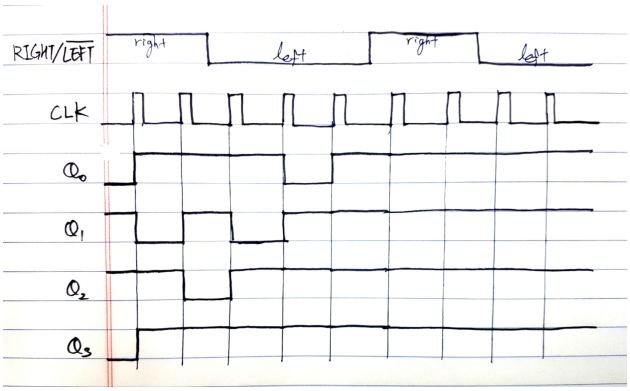


Figure 4: Output Waveform.

3. **Synchronous Counters.**
Determine the sequence of the counter in Figure 5. Show the complete timing diagram of Q_0, Q_1, and Q_2 waveforms for 10 clock pulses. Begin with the counter cleared.

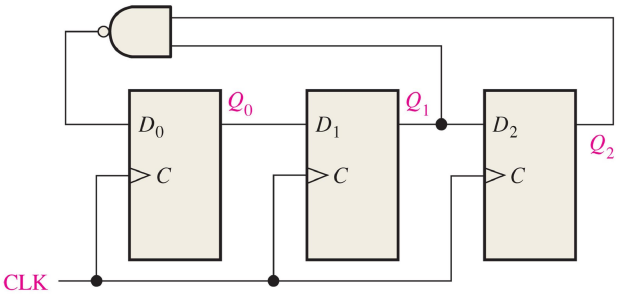


Figure 5: Synchronous Counter.

Solution: Synchronous Counters.
Since the counter is cleared initially, the initial state is $Q_0 = Q_1 = Q_2 = 0$. Q_0 will be 0 if $Q_1 = Q_2 = 1$, and Q_0 will be 1 for all other cases. Thus, we have

$$000 \to 001 \to 011 \to 111 \to 110 \to 100 \to 001 \to 011 \to 111 \to 110 \to 100 \to \cdots$$

Note that we wrote the number in $Q_2Q_1Q_0$ form.

Q waveforms are described in Figure 6. Interestingly, state 000 never appears again.

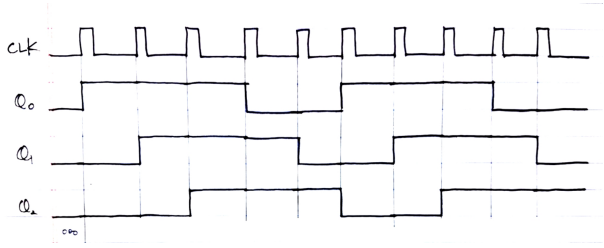


Figure 6: Output Waveform.

The state diagram of this counter is described in Figure 7

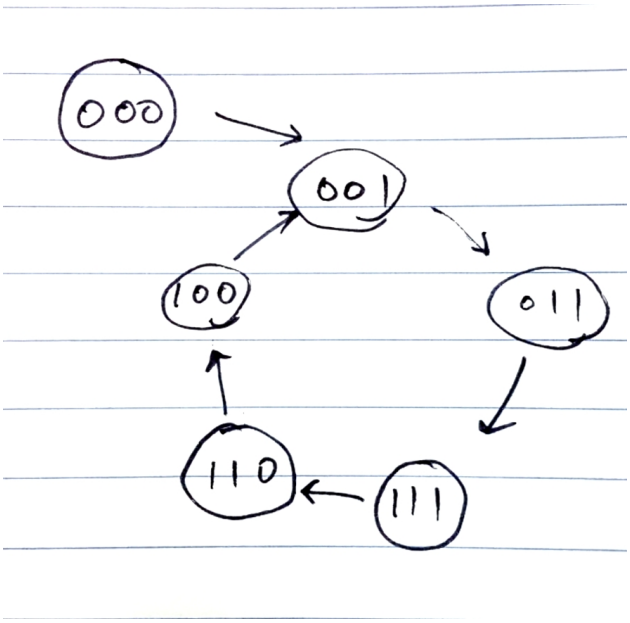


Figure 7: State Diagram.

4. **Design of Synchronous Counters.**
Design a counter to produce the following binary sequence using J-K flip-flops.

$$1, 4, 3, 5, 7, 6, 2, 1, 4, 3, 5, \ldots.$$

Please follow 6 steps to design the counter.
(Hint: We have 7 states from 001 to 111. You can start from drawing the state diagram.)
(Hint2: Use don't care when the present state is 000.)

Solution: Design of Synchronous Counters.
The first step is drawing the state diagram. Note that we are using binary numbers (for example, 001 for 1, 010 for 2, etc). The state diagram is given in Figure 8a.

Then, the step 2 is filling the next-state table. This is given in Table 1.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	x	x	x
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	1	1	0

Table 1: Step 2.

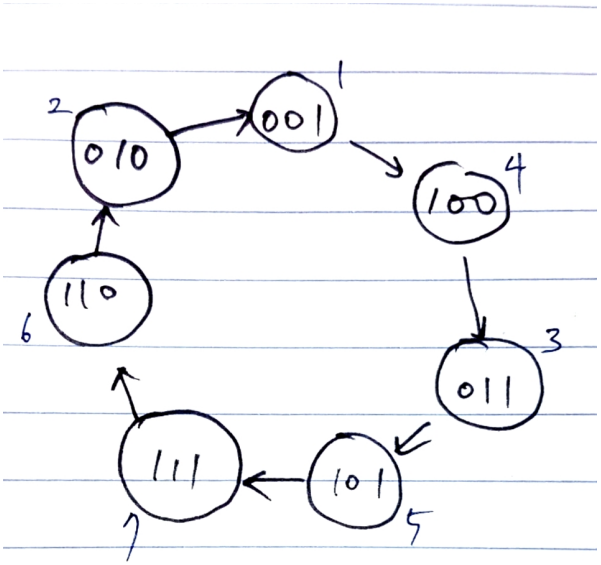
The step 3 is flip-flop transition table. Transition table of J-K flip-flop is given in Figure 8b.

The step 4 is Karnaugh maps. These are given in Figure 8c.

The step 5 is Logic expressions. According to Karnaugh maps, we have

$$J_0 = \bar{Q}_1 + \bar{Q}_2 \tag{1}$$
$$K_0 = \bar{Q}_2\bar{Q}_1 + Q_2Q_1 = Q_2 \text{ XNOR } Q_1 \tag{2}$$
$$J_1 = Q_2 \tag{3}$$
$$K_1 = \bar{Q}_2 \tag{4}$$
$$J_2 = Q_0 \tag{5}$$
$$K_2 = \bar{Q}_0. \tag{6}$$

The final step (step 6) is counter implementation which is given in Figure 8d.



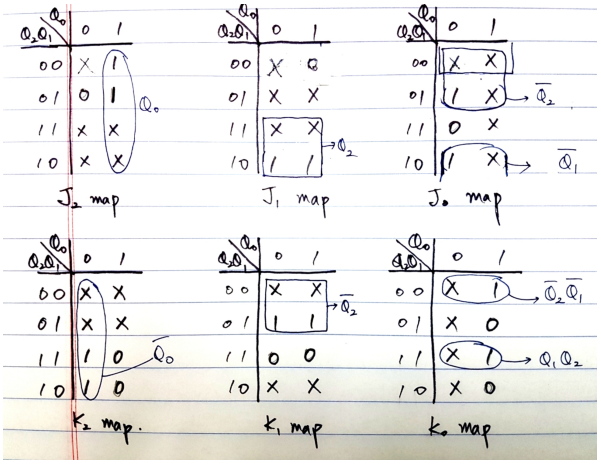
(a) Step 1.

Transition table for a J-K flip-flop.

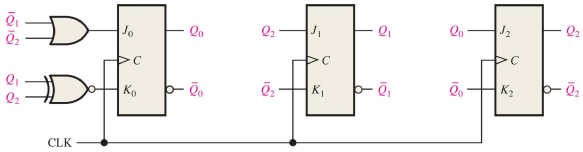
Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Q_N: present state
Q_{N+1}: next state
X: "don't care"

(b) Step 3.



(c) Step 4.



(d) Step 6.