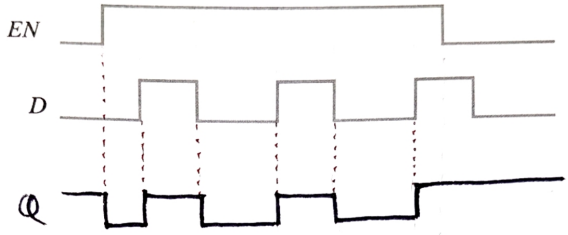
Digital Circuits
Final Solutions

1. Mix of Questions *(30 points)*

Answer the following 6 questions. Drawing waveform is enough for problem (a) to (e) (reasoning is not required). Each of them worth 5 points.

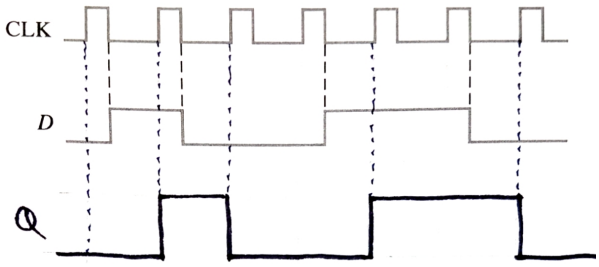
(a) Draw the output of a gated D latch for the inputs in Figure 1. Assume Q is initially HIGH
Solution:

Figure 1: Problem 1(a) Solution.



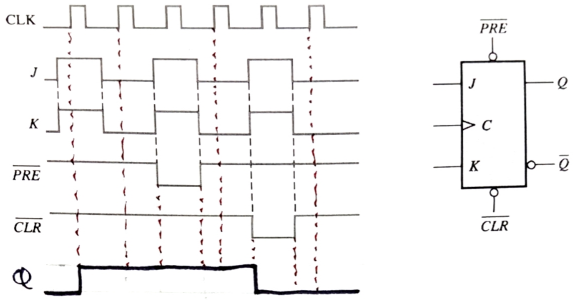
(b) Draw the Q output relative to the clock for a positive edge-triggering D flip-flop with the inputs in Figure 2. Assume Q is initially LOW.
Solution:

Figure 2: Problem 1(b) Solution.



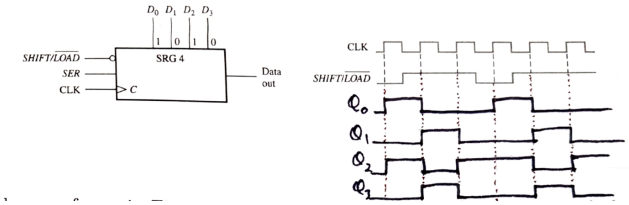
(c) Draw the Q output relative to the clock for a positive edge-triggering J-K flip-flop with the inputs in Figure 3. Assume Q is initially LOW.
Solution:

Figure 3: Problem 1(c) Solution.



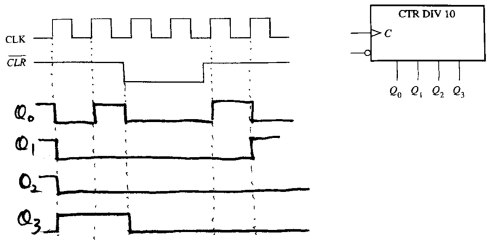
(d) The shift register in Figure 4 has $SHIFT/\overline{LOAD}$ and CLK inputs. The parallel data inputs are $D_0 = 1$, $D_1 = 0$, $D_2 = 1$, and $D_3 = 0$ as shown. Assume the register is cleared intially, and the serial data input (SER) is a 0. Draw the data-output waveform in relation to the inputs.
Solution: Draw Q_3 is enough!

Figure 4: Problem 1(d) Solution.



(e) A BCD decade counter is shown in Figure 5. The waveforms are applied to the clock and clear inputs as indicated. Draw the counter output waveforms (Q_0, Q_1, Q_2, and Q_3) in proper relation to these inputs. The clear input is asynchronous and the counter is initially in the binary 0111 state ($Q_3 = 0$, $Q_2 = Q_1 = Q_0 = 1$).
Solution:

Figure 5: Problem 1(e) Solution.



(f) For the cascaded counter in Figure 6, determine the frequency of the waveform at each point inticated by circled number.

Figure 6: Problem 1(f).

Solution:

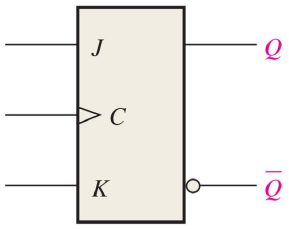
- ① : $100kHz/10 = 10kHz$
- ② : $10kHz/10 = 1kHz$
- ③ : $1kHz/10 = 100Hz$
- ④ : $100Hz/2 = 50Hz$

2. Design Problems *(30 points)*

(a) Design an asynchronous counter using four D flip-flops that counts from 0000 to 1110 (that has 15 states). *(10 points)*

(b) Design 4-bit serial in/serial out shift register with four J-K flip-flops. Specify how your shift register takes data input and CLK. Also specify how your shift register outputs the data. You are NOT allowed to use D flip-flops. *(10 points)*

Figure 7: J-K flip-flop.

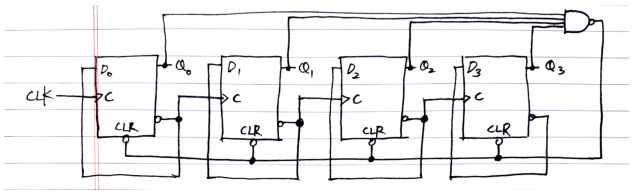


(c) Design 4-bit Johnson counter with four J-K flip-flops. You are NOT allowed to use D flip-flops. *(10 points)*

Solution: Shift Register.

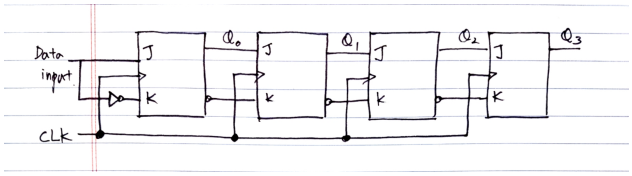
(a) Asynchronous counter is given in Figure 8

Figure 8: Asynchronous Counter.



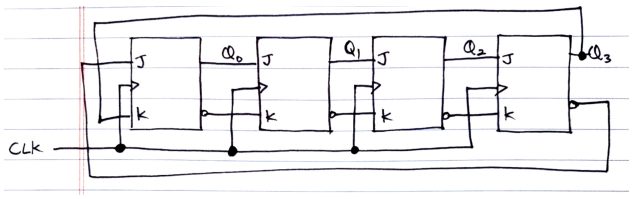
(b) Serial in/serial out shift register using four J-K flip-flops is given in Figure 9

Figure 9: 4-bit Shift Register.



(c) 4-bit Johnson counter using four J-K flip-flops is given in Figure 10

Figure 10: 4-bit Johnson Counter.



3. Design of Synchronous Counters. *(40 points)*
Design a counter to produce the following binary sequence using J-K flip-flops.

$$0, 2, 4, 6, 1, 3, 5, 0, 2, 4, 6, 1, 3, 5, \ldots.$$

Please follow 6 steps to design the counter.

(a) Draw a state diagram. *(5 points)*
(Hint: We have 7 states from 000 to 110)

(b) Fill the next-state table. *(10 points)*
(Hint: Use don't care when the present state is 111)

(c) Draw the flip-flop transition table. *(5 points)*

(d) Draw the Karnaugh maps. *(10 points)*

(e) Show the logic expressions. *(5 points)*

(f) Implement the counter (draw the circuit with flip-flops). *(5 points)*

Solution: Design of Synchronous Counters.

(a) The first step is drawing the state diagram. Note that we are using binary numbers (for example, 001 for 1, 010 for 2, etc). The state diagram is given in Figure 11a.

(b) Then, the step 2 is filling the next-state table. This is given in Table 1.

(c) The step 3 is flip-flop transition table. Transition table of J-K flip-flop is given in Figure 11b.

(d) The step 4 is Karnaugh maps. These are given in Figure 11c.

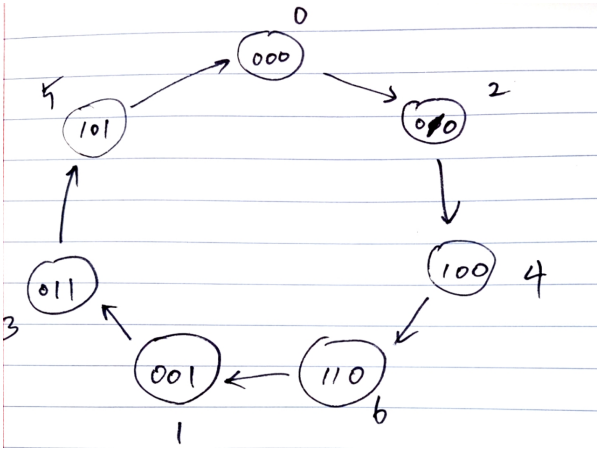
(e) The step 5 is Logic expressions. According to Karnaugh maps, we have

$$J_0 = Q_2 Q_1 \tag{1}$$
$$K_0 = Q_2 \tag{2}$$
$$J_1 = \bar{Q}_0 + \bar{Q}_2 \tag{3}$$
$$K_1 = 1 \tag{4}$$
$$J_2 = Q_1 \tag{5}$$
$$K_2 = Q_0 + Q_1. \tag{6}$$

(f) The final step (step 6) is counter implementation which is given in Figure 11d.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	0	0	1
1	1	1	x	x	x

Table 1: Step 2.



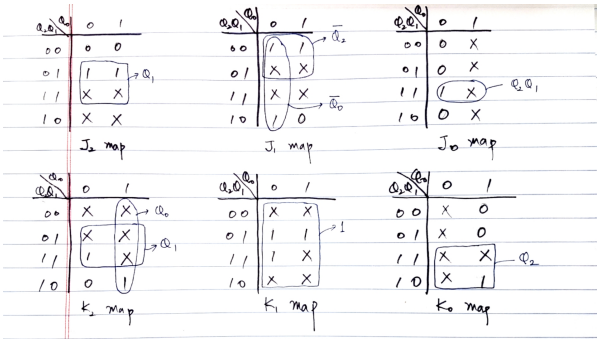
(a) Step 1.

Transition table for a J-K flip-flop.

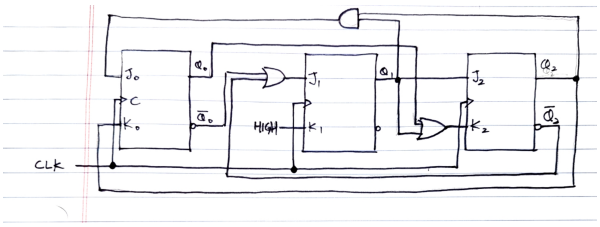
Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Q_N: present state
Q_{N+1}: next state
X: "don't care"

(b) Step 3.



(c) Step 4.



(d) Step 6.