Digital Fundamentals

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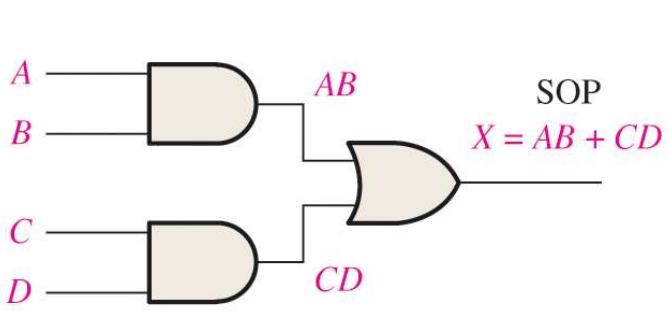
Combinational Logic Analysis

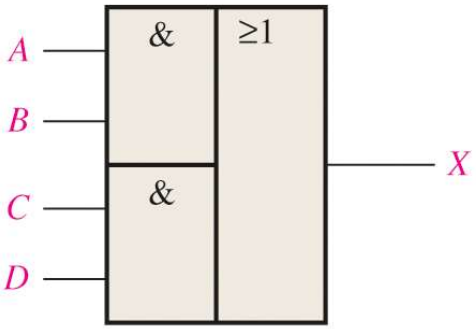
Chapter 5

Combinational Logic Circuits

In Sum-of-Products (SOP) form, basic combinational circuits can be directly implemented with AND-OR combinations if the necessary complement terms are available.



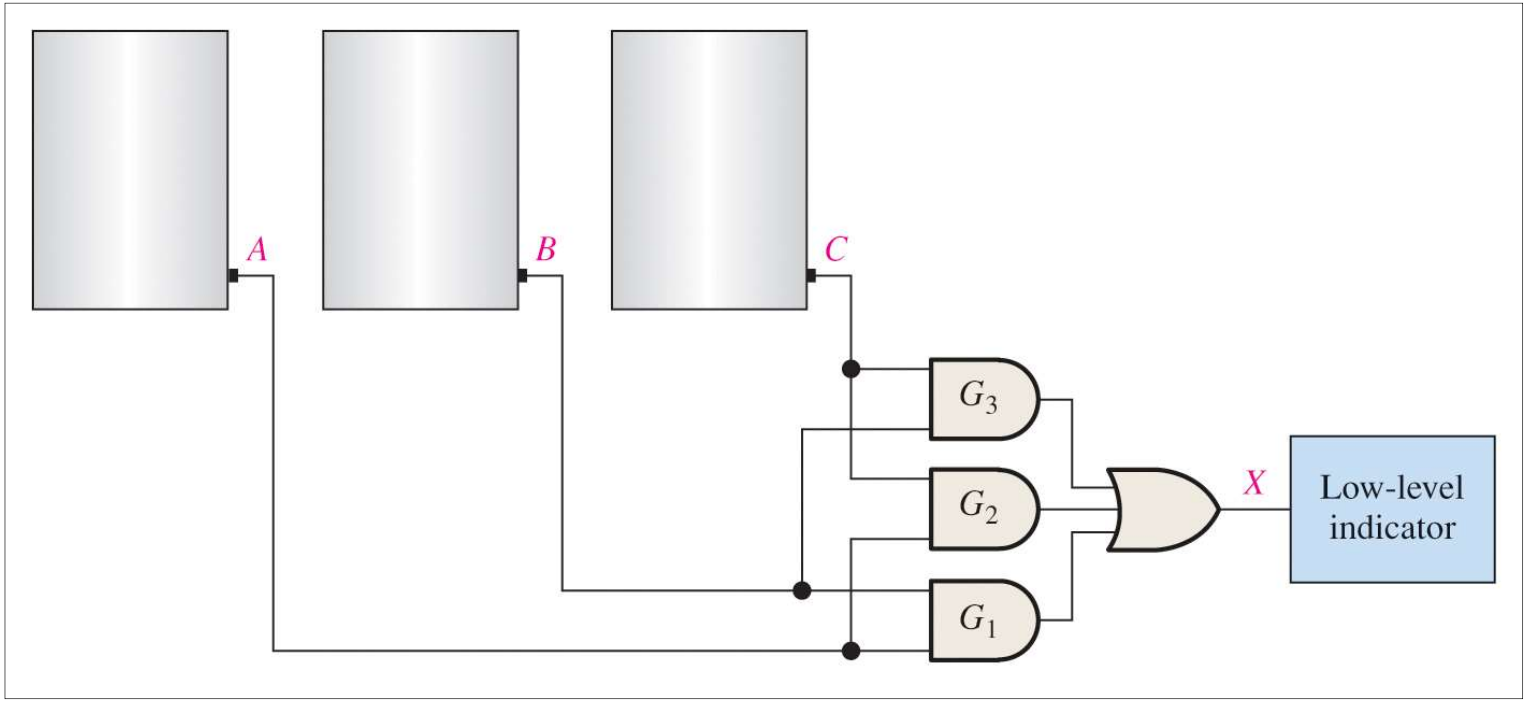
(a) Logic diagram (ANSI standard distinctive shape symbols)



(b) ANSI standard rectangular outline symbol

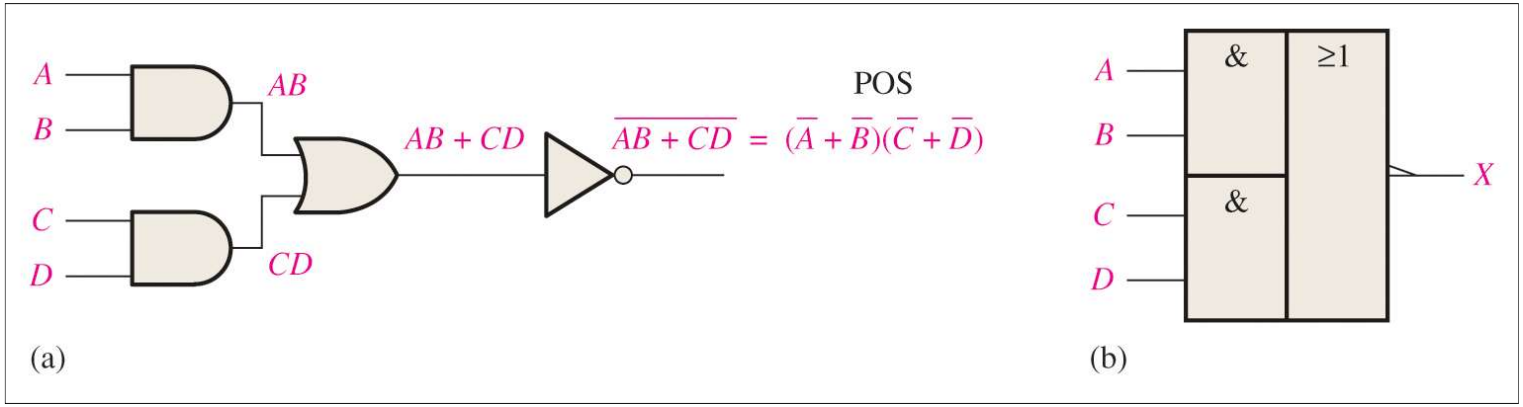
Combinational Logic Circuit Application

A storage tank monitor



AND-OR-Invert Logic

When the output of a SOP form is inverted, the circuit is called an AND-OR-Invert circuit. The AOI configuration lends itself to product-of-sums (POS) implementation.



The output from an AND-OR-Invert logic circuit is LOW whenever A and B are HIGH, or C and D are HIGH.

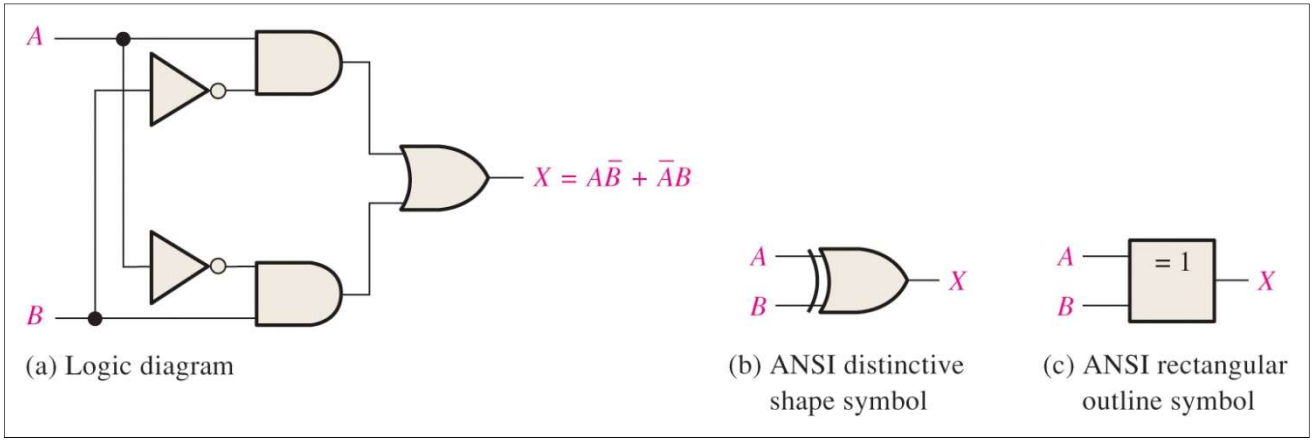
Exclusive-OR Logic

The truth table for an exclusive-OR gate is shown (right). Note that the output is HIGH whenever A and B are unequal.

The Boolean expression is $X = \bar{A}B + A\bar{B}$

TABLE 4–2 • Truth table for an exclusive-OR.

A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0



(a) Logic diagram

(b) ANSI distinctive shape symbol

(c) ANSI rectangular outline symbol

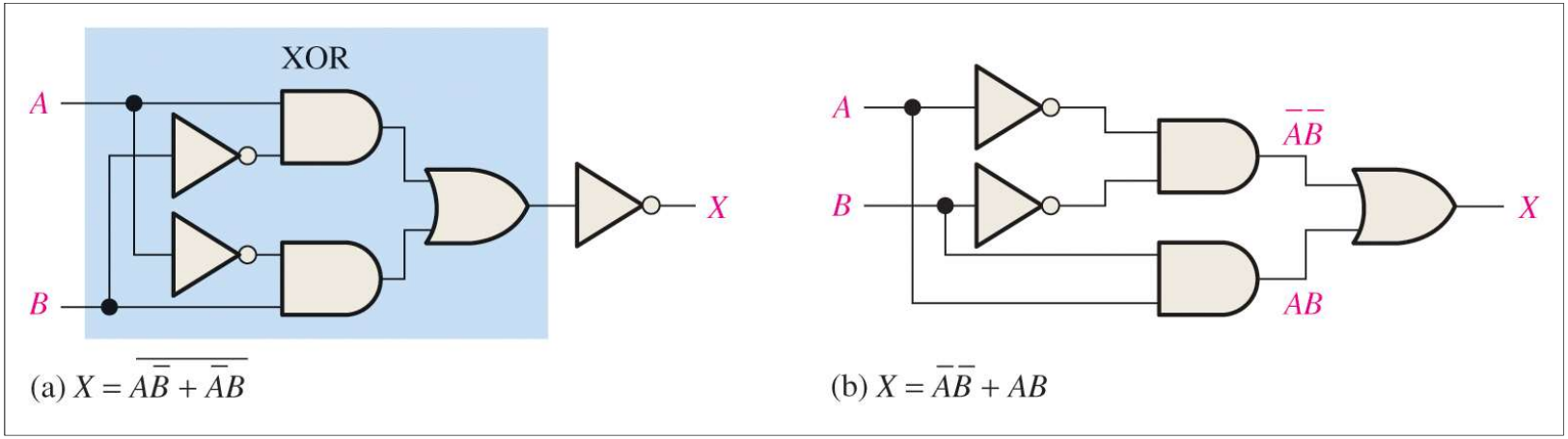
Exclusive-NOR Logic

The truth table for an exclusive-NOR gate is shown (right). Note that the output is HIGH whenever A and B are equal.

The Boolean expression is $X = \overline{A}\overline{B} + AB$

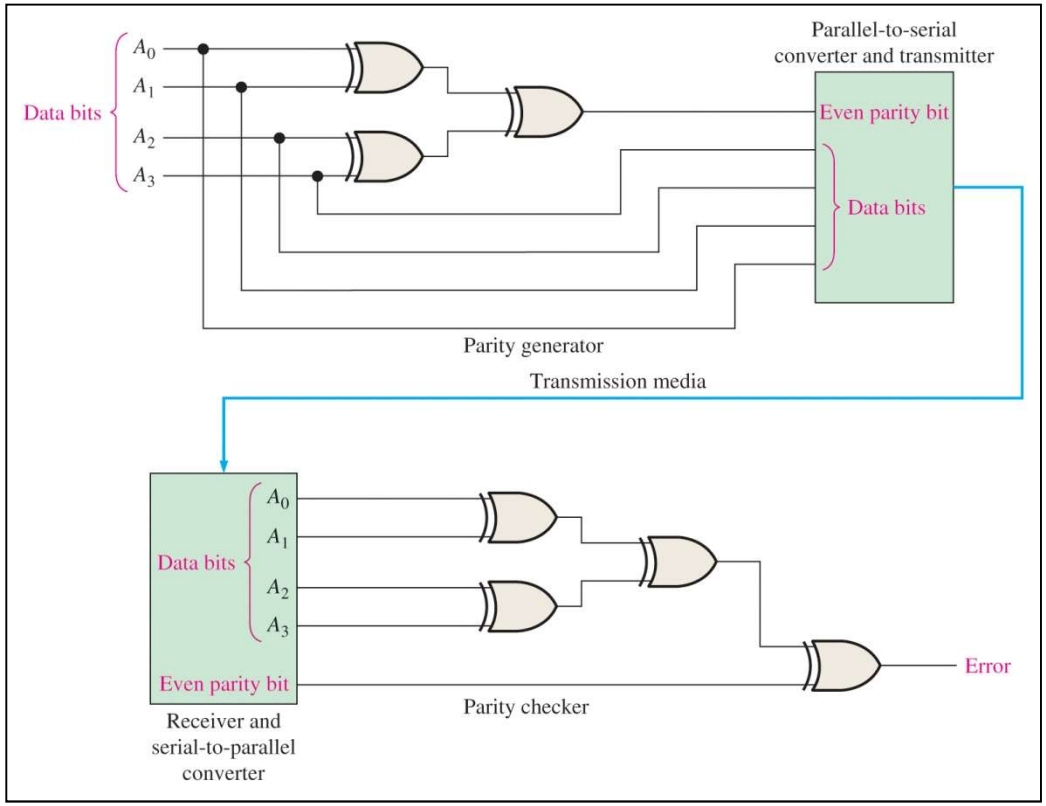
TABLE 3–16 • Truth table for an exclusive-NOR gate.

INPUTS		OUTPUT
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	1



An Exclusive-OR Logic Application

Data transmission with error detection

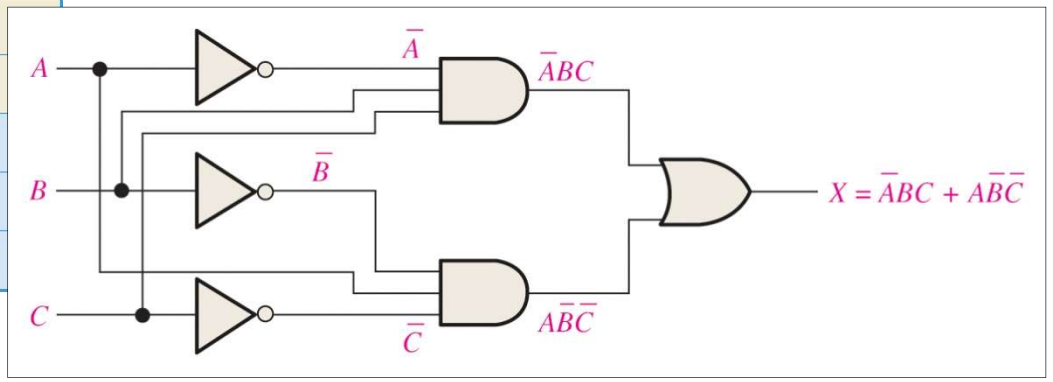


Implementing Combinational Logic

Implementing a SOP expression is done by first forming the AND terms; then the terms are ORed together.

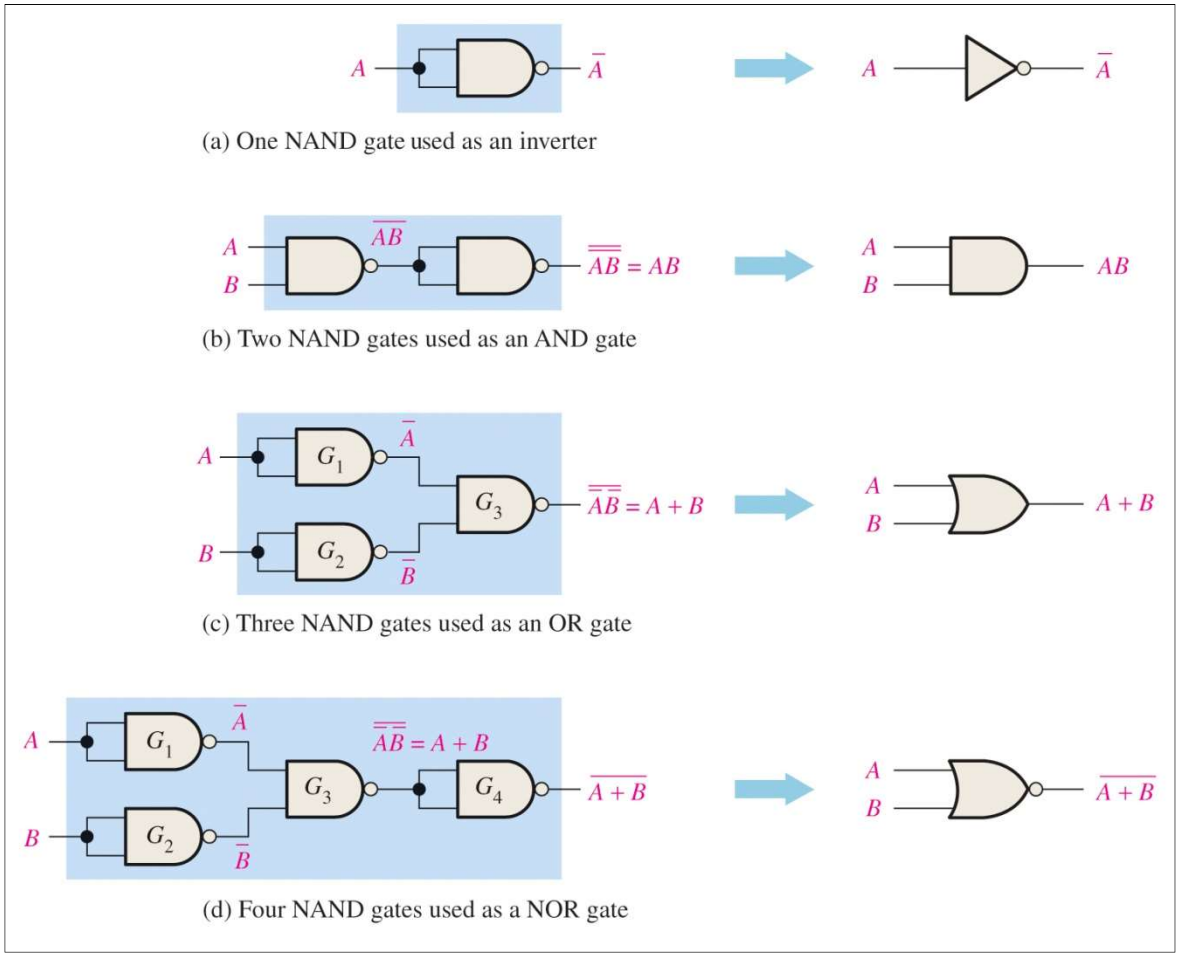
TABLE 4–3

INPUTS A	B	C	OUTPUT X	PRODUCT TERM
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\overline{A}BC$
1	0	0	1	$A\overline{B}\,\overline{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	

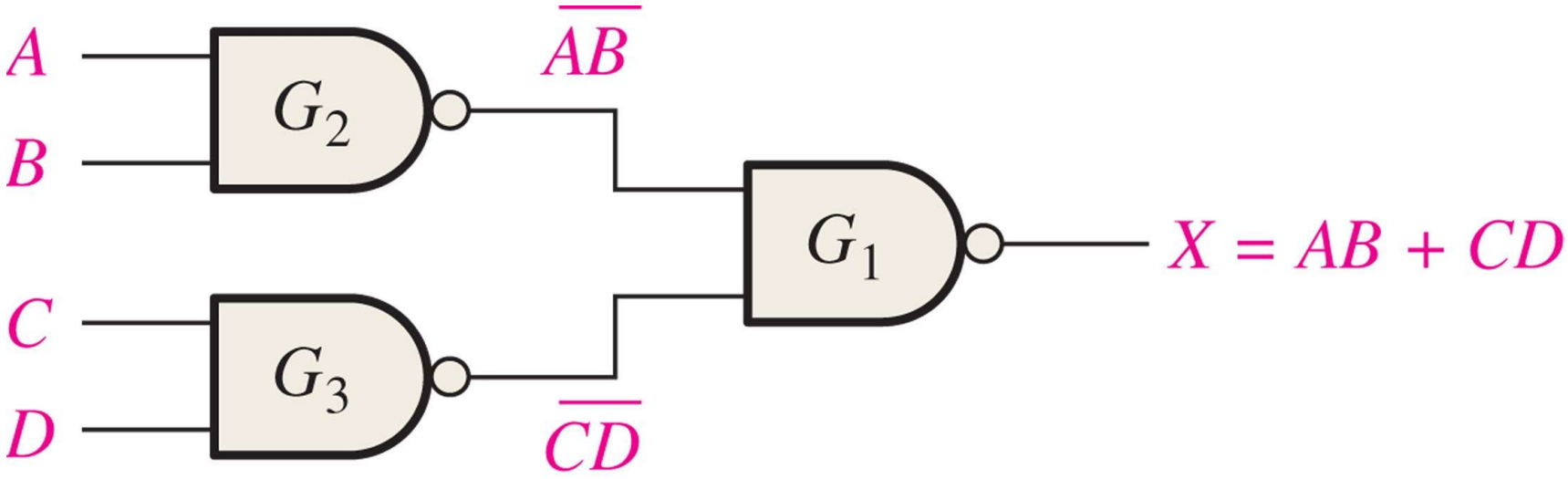


Universal Gates

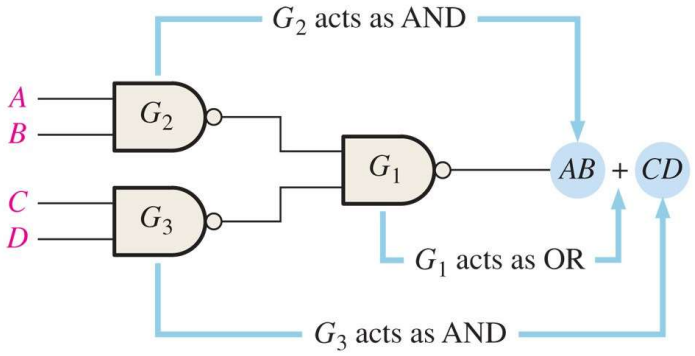
NAND gates are sometimes called **universal gates** because they can be used to produce the other basic Boolean functions.



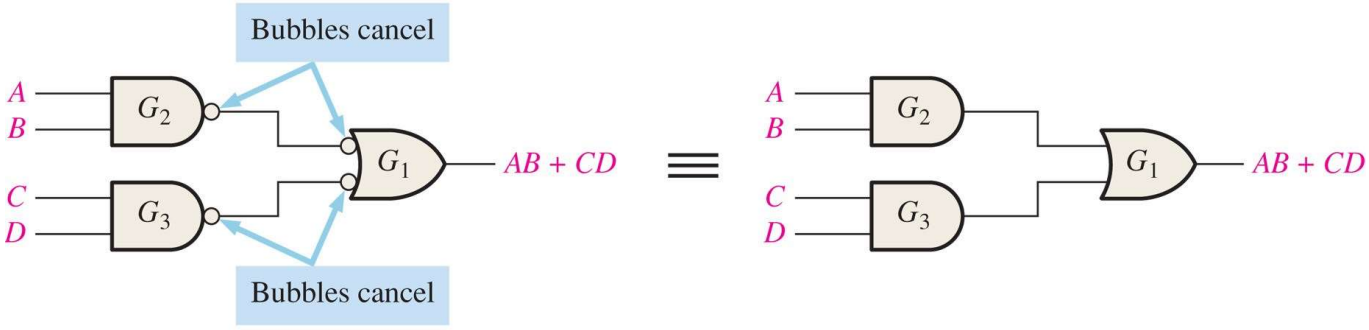
NAND Logic for AB+CD



NAND Logic for AB+CD



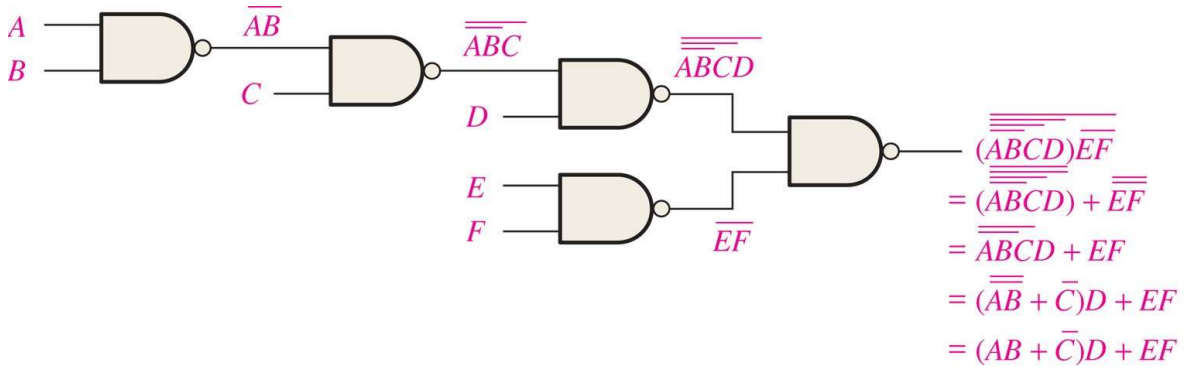
(a) Original NAND logic diagram showing effective gate operation relative to the output expression



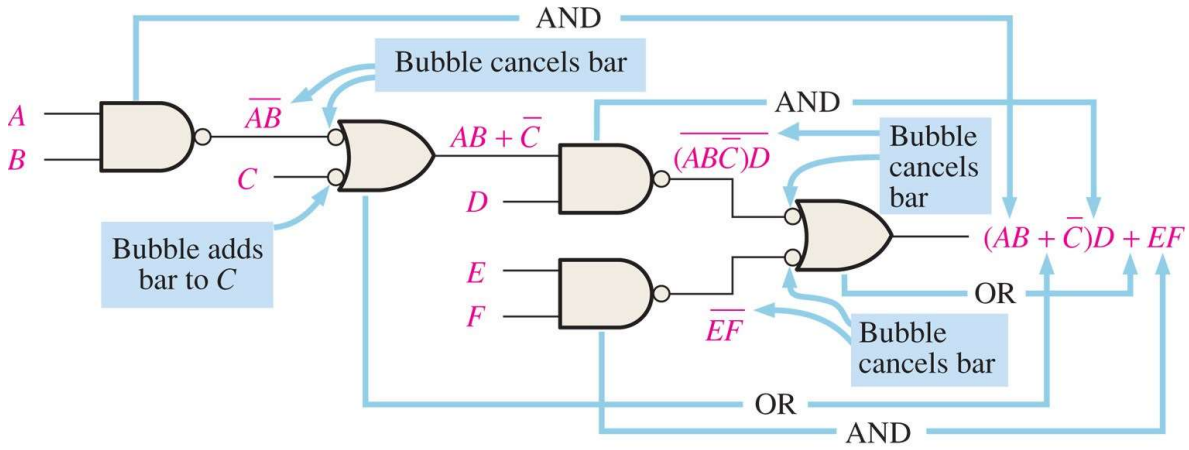
(b) Equivalent NAND/Negative-OR logic diagram

(c) AND-OR equivalent

NAND Logic Diagram



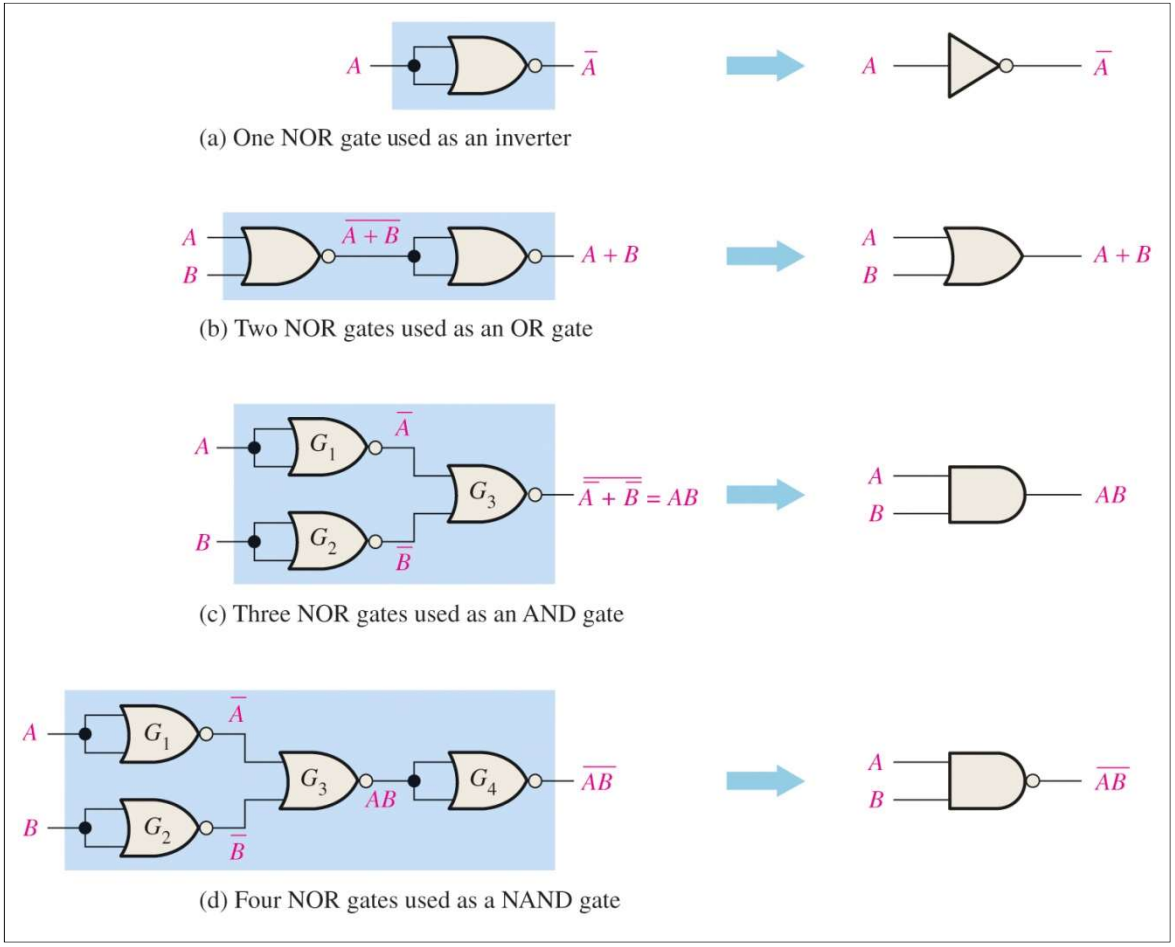
(a) Several Boolean steps are required to arrive at final output expression.



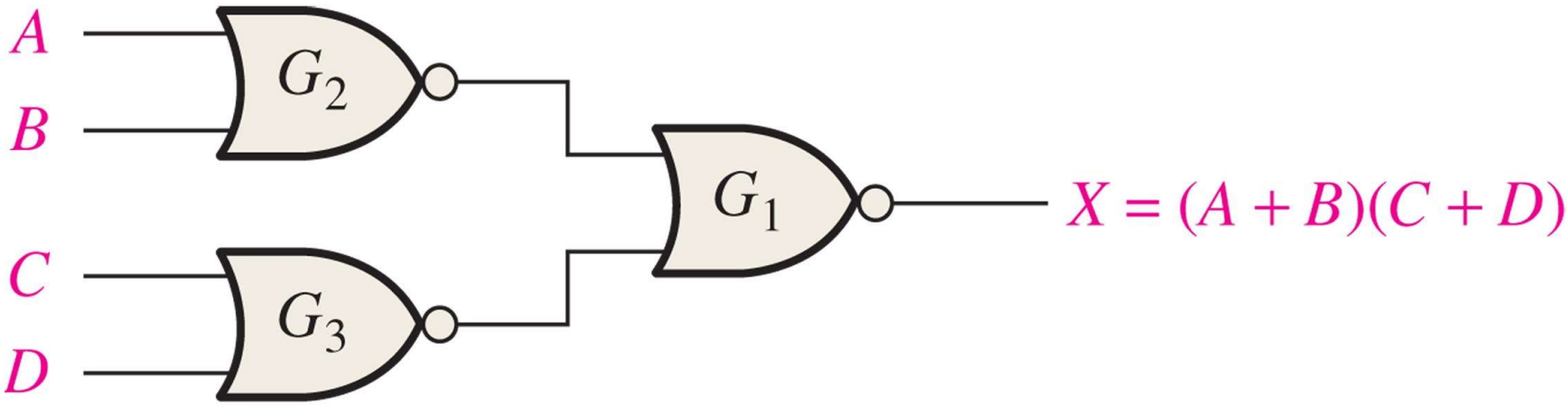
(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

Universal Gates

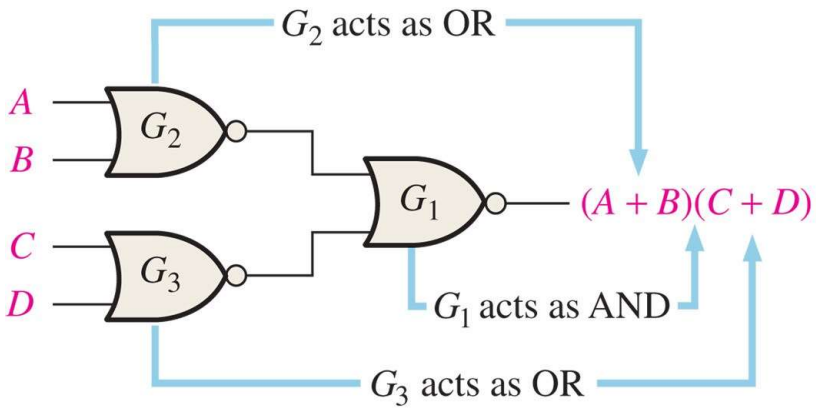
NOR gates are also called **universal gates** because they can be used to produce the other basic Boolean functions.



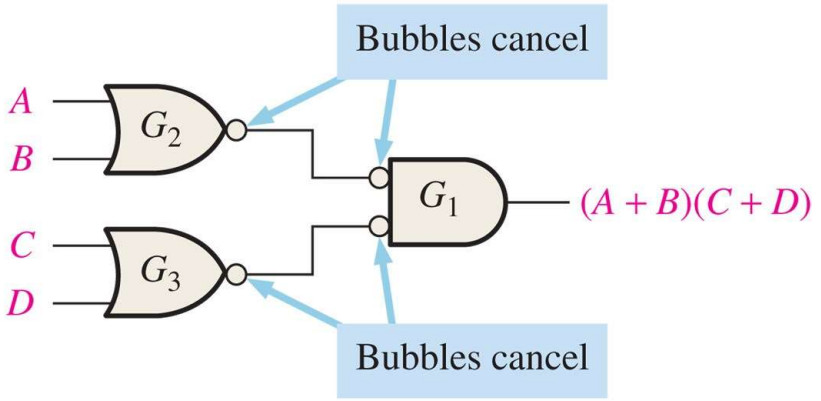
NOR Logic for (A+B)(C+D)



NOR Logic for (A+B)(C+D)

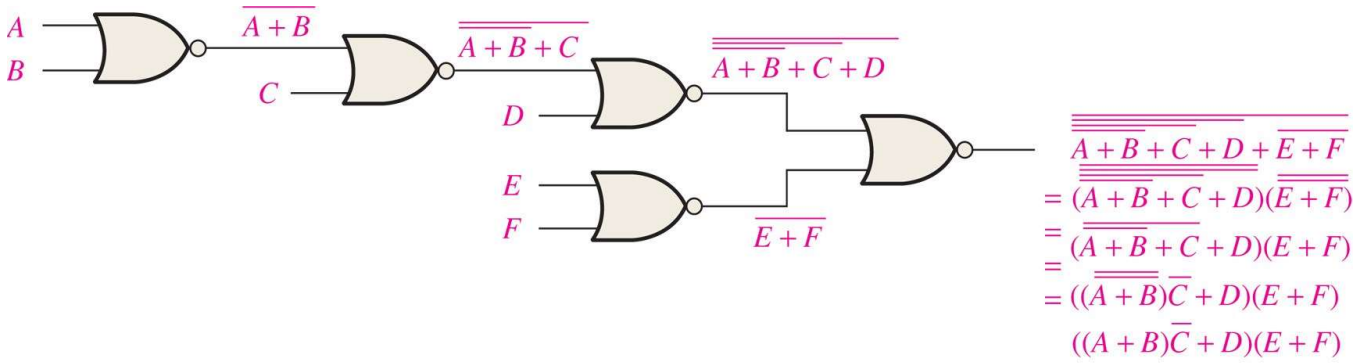


(a)

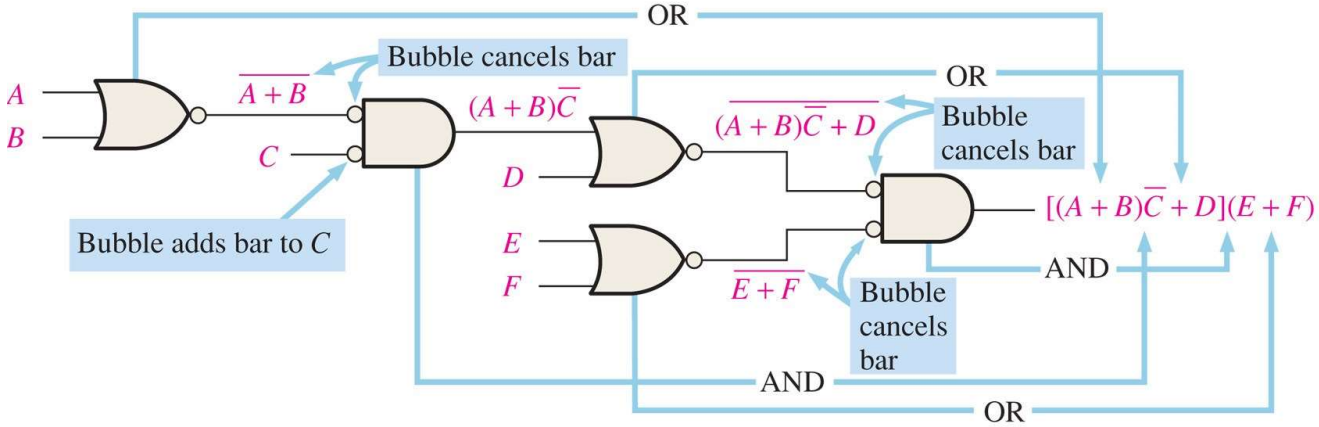


(b)

NOR Logic Diagram

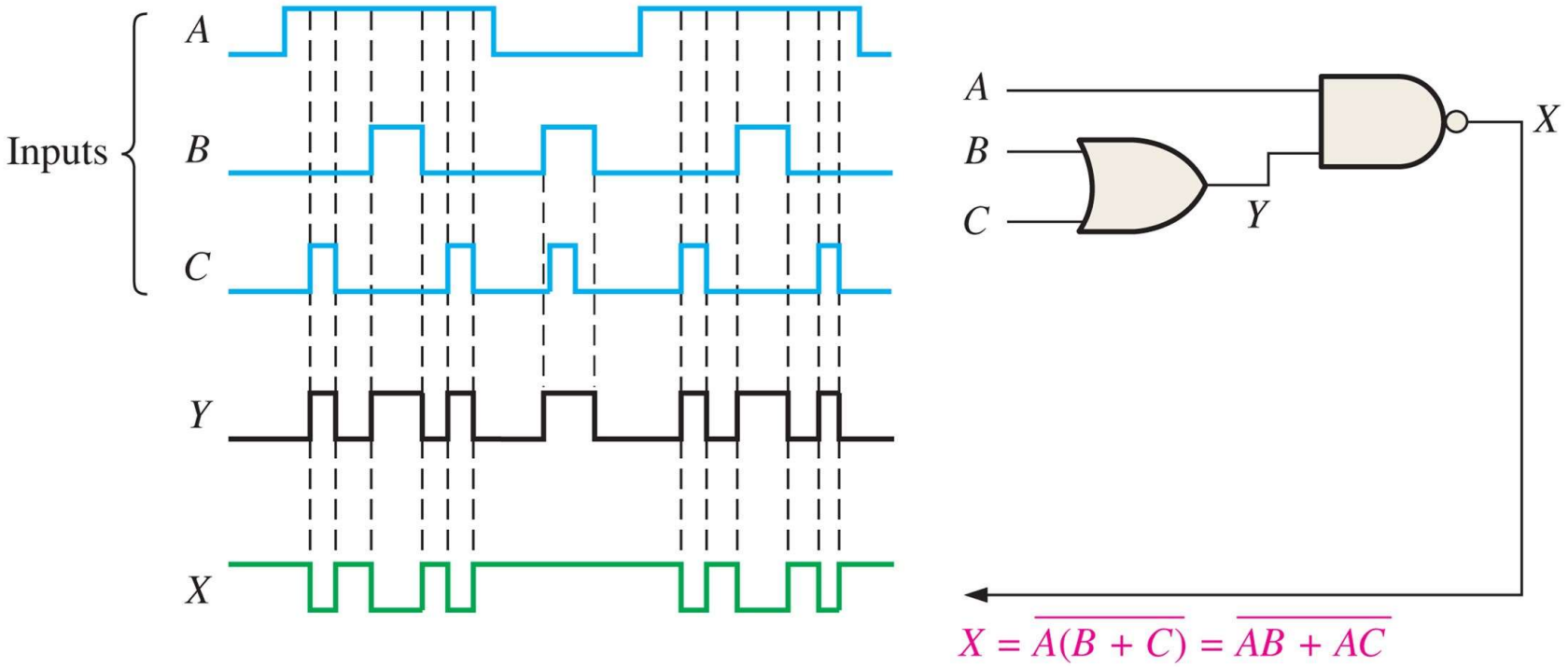


(a) Final output expression is obtained after several Boolean steps.

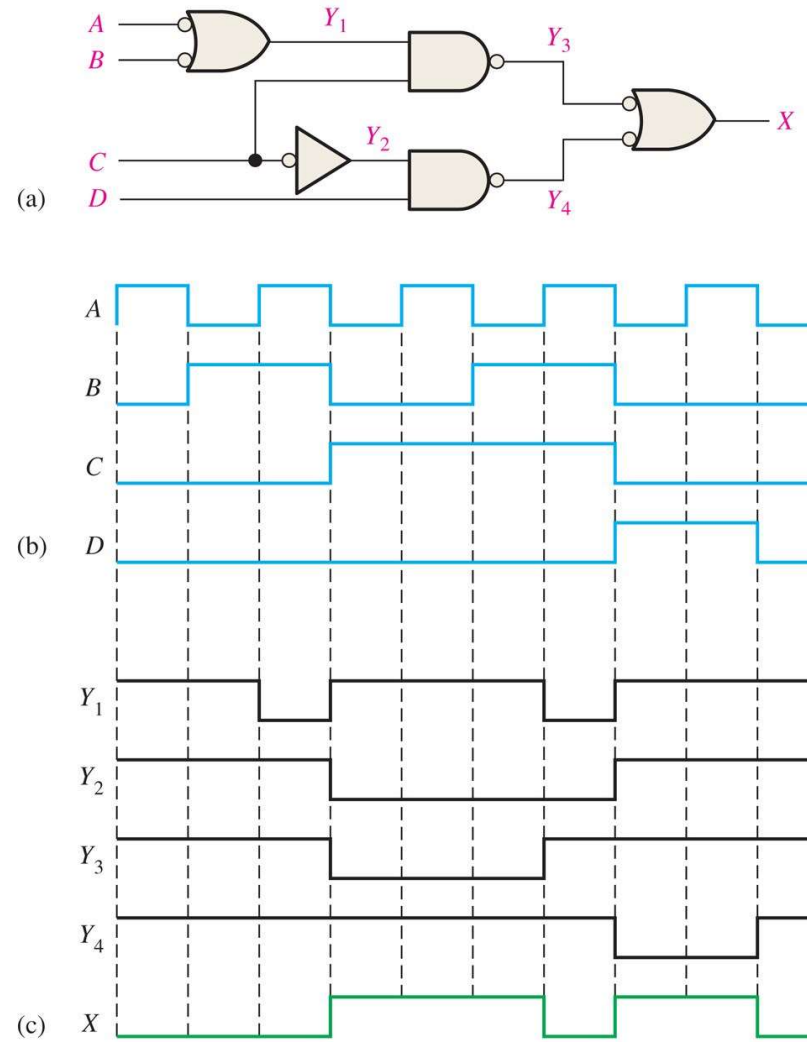


(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

Pulse Waveform Operation



Pulse Waveform Operation



Pulse Waveform Operation