[AX208-SP-101-EN]

AX208
Product Specification

Preliminary Rev 1.0.1

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AX208 8 bit CMOS Microcontroller

High Performance 8-bit RISC MCU

- Maximum 96 MIPS
- Compatible with 8051

Memory

- 12K Bytes IRAM
- 2K Bytes PRAM
- 1K Bytes DRAM

Interrupt Features

- External interrupt on 3 GPIO and USB PHY.
- 2-level interrupt priority

General I/O

- 37 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up selectable individually
- CMOS/TTL level Schmitt triggered input

Digital Peripheral Features

- Two 8-bit timers
- Two 16-bit timers
- One IRTCC
- One Watchdog timer
- Two SPI interface
- Two UART interface
- One SD Card host controller
- One JPEG decode accelerator
- One 8080 compatible LCD interface
- One full speed USB 2.0 host/device

Analog Peripheral Features

- One 32 KHz oscillator
- One 96 MHz RC oscillator
- One BOR
- Two 3.3V to 1.8V LDO
- One 3.3V to 2.8V LDO
- One full speed USB 2.0 PHY
- One 10-bit ADC with 8 channels
- Three Power Gates

Program and Debug support

- OTP programmer

Packages

- LQFP48 (7mm x 7mm)

Operating Temperature

- -40 ℃ to 85 ℃

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Chapter 1 PRODUCT OVERVIEW

1.1 Description

AX208 is an 8051 Compatible high performance mixed signal 8-bit micro controller. It integrates advanced digital and analog peripherals to suit for a variety of applications. For digital peripherals, it supports a variety of digital interfaces including UART, LCD, SPI, SDC, RTCC, Watchdog timer and four general timers. One USB 2.0 full speed device/host controller and one JPEG decode accelerator are provided. For analog peripherals, it integrates ADC, PLL, Power Gate, XOSC and LDO. The micro controller employs an advanced architecture and compatible with standard 8051 with throughput of up to 96 MIPS. All instructions are single-cycled except program branching.

AX208 has 12K-byte (6K x 16) IRAM, 1024-byte (1024 x 8) DRAM and 2K-byte (1K x 16) PRAM. The USB FIFO is shared with IRAM.

Flexible I/O with different programmable capabilities like pull-up, pull-down or wake-up allows AX208 to suit different I/O requirements in the market.

In order to support portable applications and reduce power consumption, three low-power saving modes are added: IDLE mode, HOLD mode and SLEEP mode.

1.2 System Architecture

Chapter 2 PIN Definitions

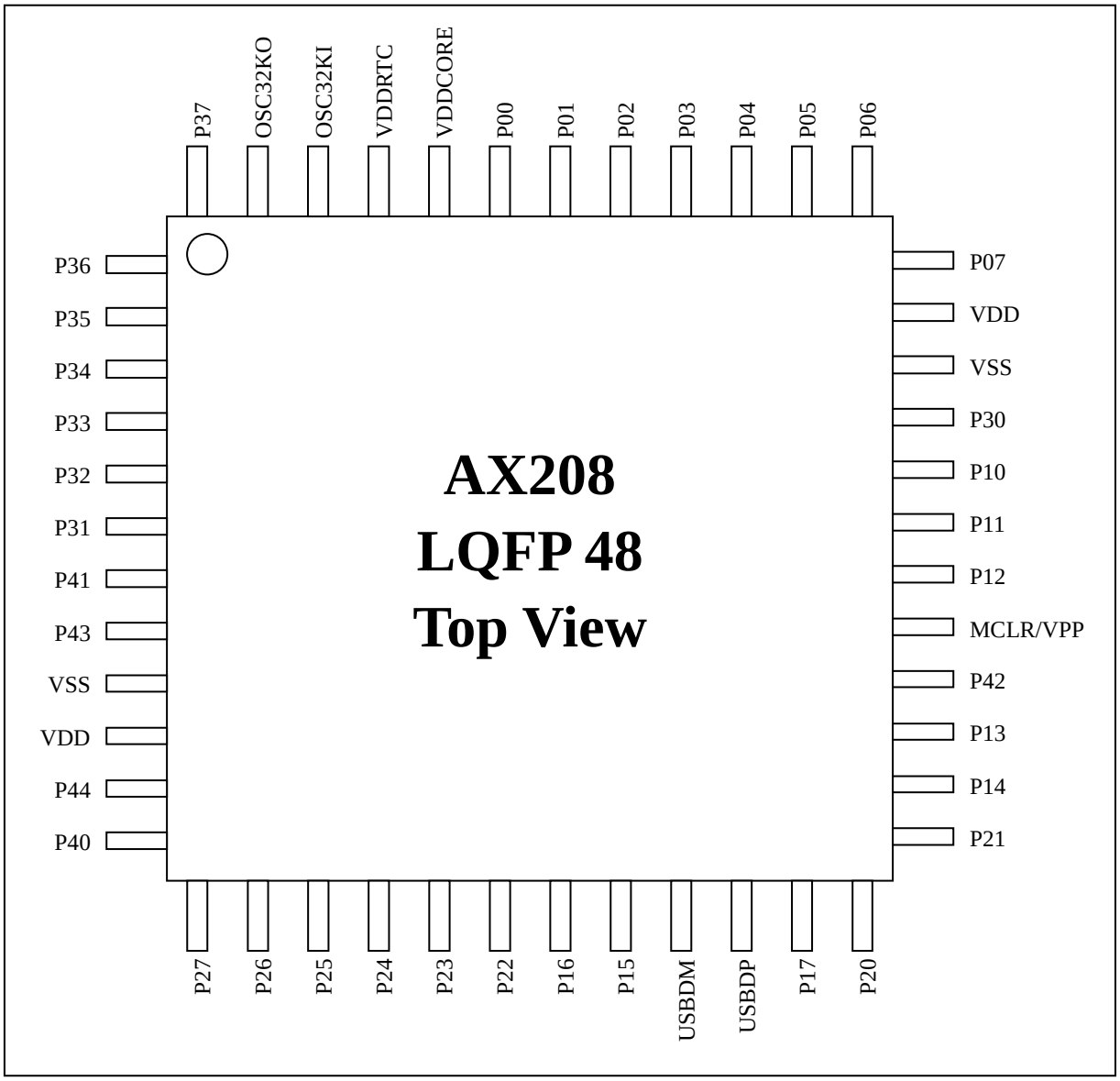
2.1 Part Numbering

AX208

2.2 Packages

LQFP48

2.3 Pin Assignment



Pin assignment for LQFP48

2.4 Pin Descriptions

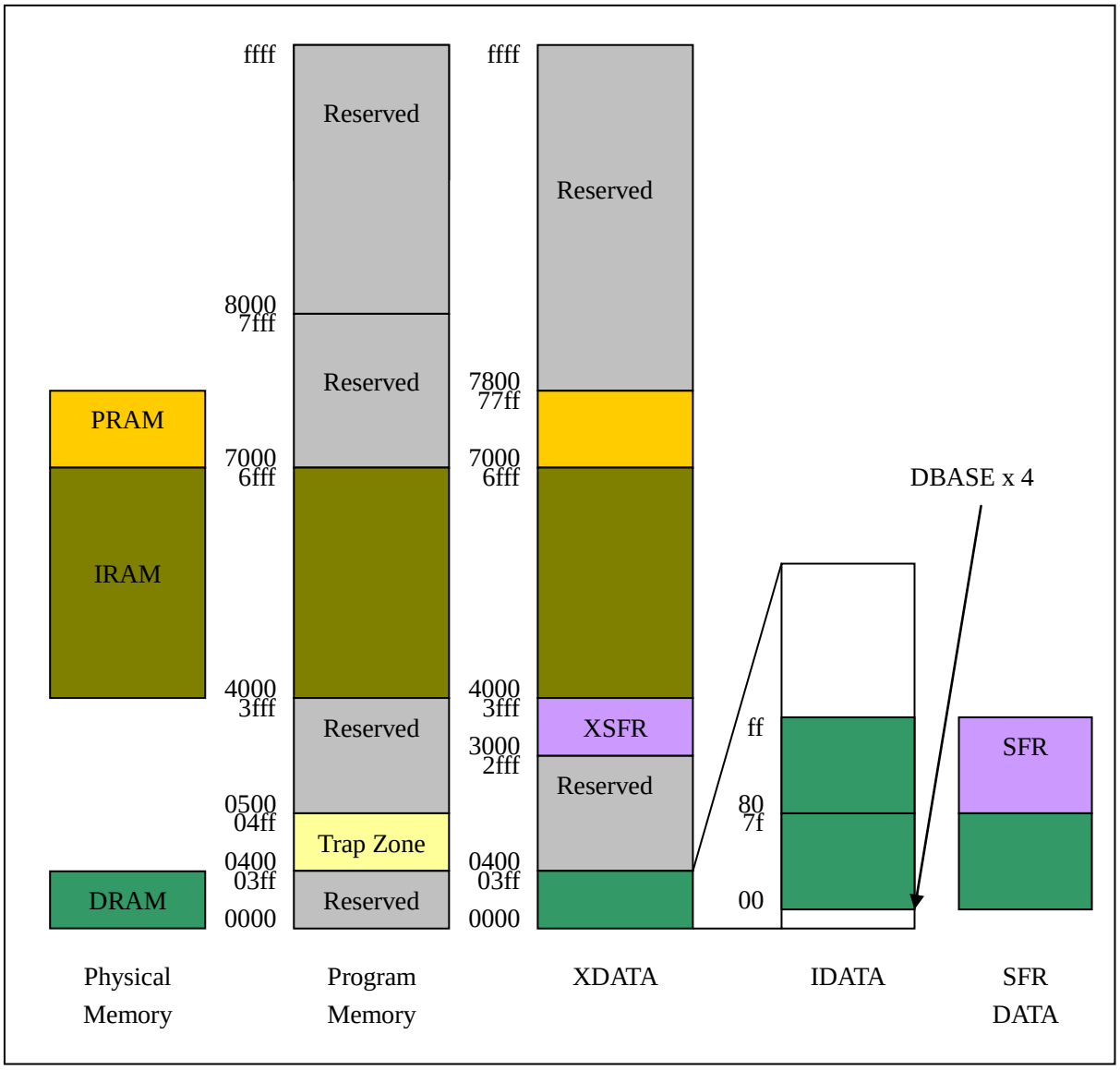
PIN	Symbol	Direct	Description
1	P36	I/O	GPIO
2	P35	I/O	GPIO
3	P34	I/O	GPIO
4	P33	I/O	GPIO

5	P32	I/O	GPIO
6	P31	I/O	GPIO
7	P41	I/O	GPIO
8	P43	I/O	GPIO
9	VSS	Ground	General ground
10	VDD	3.3V Power	3.3V Power
11	P44	I/O	GPIO
12	P40	I/O	GPIO
13	P27	I/O	GPIO
14	P26	I/O	GPIO
15	P25	I/O	GPIO
16	P24	I/O	GPIO
17	P23	I/O	GPIO
18	P22	I/O	GPIO
19	P16	I/O	GPIO
20	P15	I/O	GPIO
21	USBDM	I/O	USB DM
22	USBDP	I/O	USB DP
23	P17	I/O	GPIO
24	P20	I/O	GPIO
25	P21	I/O	GPIO
26	P14	I/O	GPIO
27	P13	I/O	GPIO
28	P42	I/O	GPIO
29	MCLR/VPP	I	MCLR reset input VPP voltage input
30	P12	I/O	GPIO
31	P11	I/O	GPIO
32	P10	I/O	GPIO
33	P30	I/O	GPIO
34	VSS	Ground	General ground
35	VDD	3.3V Power	3.3V Power
36	P07	I/O	GPIO
37	P06	I/O	GPIO
38	P05	I/O	GPIO
39	P04	I/O	GPIO
40	P03	I/O	GPIO
41	P02	I/O	GPIO
42	P01	I/O	GPIO
43	P00	I/O	GPIO
44	VDDCORE	1.8V Power	1.8V Power for core

45	VDDRTCC	1.8V Power	1.8V Power for RTCC
46	OSC32KI	I	32K oscillator input GPIO
47	OSC32KO	O	32K oscillator output GPIO
48	P37	I/O	GPIO

Chapter 3 Memory Organizations

AX208 has three different on-chip memory areas: Program Memory, DATA/IDATA and XDATA. AX208 implements 4 physical memory blocks. They are IRAM, PRAM and DRAM.
AX208 also has 4-Bytes OTP for special use.



3.1 DRAM

AX208's Data/IData can map to some 256B DRAM by setting SFR DBASE. Changing DBASE affects access of Data, IData, Rn, Bit, and Stack.
After changing DBASE, the four pairs of R0 and R1 still retain old value. But the corresponding DATA,

0x00, 0x01, 0x08, 0x09, 0x10, 0x11, 0x18, and 0x19 have new value. So it needs to synchronize Ri and DATA using instructions like "mov 0x00, 0x00".

DRAM is also mapped to XDATA, but the four pairs of R0 and R1 not. So changing the corresponding XDATA of the pairs using movx instructions will need synchronization too.

SFR 3-1 DBASE Register

DBASE (0x9B)

DRAM Base Address Register

	7	6	5	4	3	2	1	0
Name	DBASE							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		DRAM Base Address / 4

3.2 XRAM Memory Accessing and Data Pointer

The data pointers (DPTR0 and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location. Two pointers are useful when moving data from one memory area to another. The user can select the active pointer through a dedicated SFR bit (DPSEL: DPCON.0), or can activate an automatic toggling feature for altering the pointer selection (DPTSL: DPCON.2). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

Data pointer increment/decrement bits DPID0 (DPCON.5) and DPID1 (DPCON.4) define how the INC DPTR instruction functions in relation to the active DPTR.

The AX208 offers a programmable option that allows any instructions related to data pointer to toggle the DPSEL bit automatically. This option is enabled by setting the toggle-select-enable bit (DPTSL) to logic 1. Once enabled, the DPSEL bit is automatically toggled after the execution of one of the following 5 DPTR related instructions:

MOVC A, @A+DPTR

MOVX A, @DPTR

MOVX @DPTR, A

INC DPTR

MOV DPTR, #data16

AX208 also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 after the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent on the setting of the DPAID bits. This option is enabled by setting the automatic increment/decrement enable (DPAID: DPCON.3) to a logic 1 and is affected by one of the following 3 DPTR-related instructions.

DPTR-related instructions are:

MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A

SFR 3-2 DPCON Register

DPCON (0x86)
Data Pointer Configure Register

	7	6	5	4	3	2	1	0
Name	IA		DPID0	DPID1	DPAID	DPTSL	-	DPSEL
Reset	1	0	0	0	0	0	-	0
POR	1	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W

Bit Number	Bit Mnemonic	Description
7-6	IA	**Select Interrupt Vector's Base Address** 01b: Base address is 0x4003 10b: Base address is 0x8003 00b/11b: Reserved
5	DPID0	**DPTR0 increase direction control** 0: DPTR0 increase 1: DPTR0 decrease
4	DPID1	**DPTR1 increase direction control** 0: DPTR1 increase 1: DPTR1 decrease
3	DPAID	**DPTR auto increase enable** 0: disable auto increment 1: enable auto increment
2	DPTSL	**DPSEL toggle enable** 0: DPSEL toggle disable 1: DPSEL toggle enable
0	DPSEL	**DPTR Select** 0: activate DPTR0 1: activate DPTR1

3.3 Stack

AX208's Stack shares the IData. So, DBASE effects the access of Stack. The actual offset to DRAM is SP + DBASE*4.

SFR 3-3 Stack Pointer

SP (0x81)
Stack Pointer

	7	6	5	4	3	2	1	0
Name	SP							
Reset	0	0	0	0	0	1	1	1
POR	0	0	0	0	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		Stack Pointer

3.4 Special Function Registers

The Special Function Registers (SFR) used by the CPU and Peripheral Modules for controlling the desired operation. The Special Function Registers can be classified into two sets: core and peripheral.
Some SFRs are mapped to XDATA space, named XSFR.

SFR 3-4 PSW Register

PSW (0xD0)
Processor Status Word

	7	6	5	4	3	2	1	0
Name	CY	AC	EC	RS1	RS0	OV	EZ	P
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	CY	**Carry Flag** Carry out from bit 1 of ALU operands.
6	AC	**Auxiliary Carry Flag** Carry out from bit 1 of addition operands
5	EC	**Extend Carry Flag** Carry out from extend 16-bits instruction.
4-3	RS1:0	**Register Bank Select Bits** 00b: Select Register Bank 0 01b: Select Register Bank 1 10b: Select Register Bank 2 11b: Select Register Bank 3
2	OV	**Overflow Flag** Overflow set by arithmetic operations.
1	EZ	**Extend Zero Flag** Zero flag of extend 16-bits instruction.

0	P	**Parity Bit** 0: ACC contains an even number of 1's. 1: ACC contains an odd number of 1's.

SFR 3-5 General Purpose Registers

GPR0:7 (0xA1:0xA4, 0xB1:0xB3, 0xB5)

General Purpose Registers

	7	6	5	4	3	2	1	0
Name	GPR0:7							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**General Purpose Register** While running OS, DATA is local to task. General Purpose Registers can be used as global variables.

3.5 Special Function Registers File Map

3.6 Special Function Registers Details

Chapter 4 AXC51-CORE INSTRUCTION SET

The AXC51-CORE of AX208 is fully compatible with the MCS-51™ instruction set. AX208 reset address is 0x8000. Two interrupt entrances are provided: 0x4003 and 0x8003.
AX208 also offers a 16-bits instruction set.

4.1 Performance Overview

The AXC51-CORE employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12 MHz. By contrast, the AXC51-CORE executes most of its instructions in 1 system clock cycle. With system clock running at 96MHz, it has a peak throughput of 96MIPS running in on-chip SRAM area.

4.2 Instruction Set

The instruction set of the AXC51-CORE is fully compatible with the standard MCS-51™ instruction set; standard 8051 development tools can be used to develop software for the AXC51-CORE. All instructions of AXC51-CORE are the binary and functional equivalent of their MCS-51™ counterparts, including op-codes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

Number of Bytes	Mnemonic	Operands	Clock Cycles (running in IRAM)
1	NOP		1
2	AJMP	Code addr	3
3	LJMP	Code addr	3
1	RR	A	1
1	INC	A	1
1	INC	Data addr	1
1	INC	@Ri	1
1	INC	Rn	1
3	JBC	Bit addr, Code addr	1 or 3
2	ACALL	Code addr	3
3	LCALL	Code addr	3
1	RRC	A	1
1	DEC	A	1

2	DEC	Data addr	1
1	DEC	@Ri	1
1	DEC	Rn	1
3	JB	Bit addr, Code addr	1 or 3
1	RET		4
1	RL	A	1
2	ADD	A, #data	1
2	ADD	A, Data addr	1
1	ADD	A, @Ri	1
1	ADD	A, Rn	1
3	JNB	Bit addr, Code addr	1 or 3
1	RETI		4
1	RLC	A	1
2	ADDC	A, #data	1
2	ADDC	A, Data addr	1
1	ADDC	A, @Ri	1
1	ADDC	A, Rn	1
2	JC	Code addr	1 or 3
2	ORL	Data addr, A	1
3	ORL	Data addr, #data	1
2	ORL	A, #data	1
2	ORL	A, Data addr	1
1	ORL	A, @Ri	1
1	ORL	A, Rn	1
2	JNC	Code addr	1 or 3
2	ANL	Data addr, A	1
2	ANL	Data addr, #data	1
1	ANL	A, @Ri	1
1	ANL	A, Rn	1
2	JZ	Code addr	1 or 3
2	XRL	Data addr, A	1
3	XRL	Data addr, #data	1
2	XRL	A, #data	1
2	XRL	A, Data addr	1
1	XRL	A, @Ri	1
1	XRL	A, Rn	1
2	JNZ	Code addr	1 or 3
2	ORL	C, Bit addr	1
1	JMP	@A+DPTR	3
2	MOV	A, #data	1
3	MOV	Data addr, #data	1

2	MOV	@Ri, #data	1
2	MOV	Rn, #data	1
2	SJMP	Code addr	3
2	ANL	C, Bit addr	1
1	MOVC	A, @A+PC	1
1	DIV	AB	1
3	MOV	Data addr, Data addr	1
2	MOV	Data addr, @Ri	1
2	MOV	Data addr, Rn	1
3	MOV	DPTR, #data	1
2	MOV	Bit addr, C	1
1	MOVC	A, @A+DPTR	2
2	SUBB	A, #data	1
2	SUBB	A, Data addr	1
1	SUBB	A, @Ri	1
1	SUBB	A, Rn	1
2	ORL	C, Bit addr	1
2	MOV	C, Bit addr	1
1	INC	DPTR	1
1	MUL	AB	1
2	MOV	@Ri, Data addr	1
2	MOV	Rn, Data addr	1
2	ANL	C, Bit addr	1
2	CPL	Bit addr	1
2	CPL	C	1
3	CJNE	A, #data, Code addr	1 or 3
3	CJNE	A, Data addr, Code addr	1 or 3
3	CJNE	@Ri, #data, Code addr	1 or 3
3	CJNE	Rn, #data, Code addr	1 or 3
2	PUSH	Data addr	1
2	CLR	Bit addr	1
1	CLR	C	1
1	SWAP	A	1
2	XCH	A, Data addr	1
1	XCH	A, @Ri	1
1	XCH	A, Rn	1
2	POP	Data addr	1
2	SETB	Bit addr	1
1	SETB	C	1
1	DA	A	1
3	DJNZ	Data addr, Code addr	1 or 3

1	XCHD	A, @Ri	1
2	DJNZ	Rn, Code addr	1 or 3
1	MOVX	A, @DPTR	2
1	MOVX	A, @Ri	2
1	CLR	A	1
2	MOV	A, Data addr	1
1	MOV	A, @Ri	1
1	MOV	A, Rn	1
1	MOVX	@DPTR, A	1
1	MOVX	@Ri, A	1
1	CPL	A	1
2	MOV	Data addr, A	1
1	MOV	@Ri, A	1
1	MOV	Rn, A	1

Extend 16-bits operation instruction

Mnemonic	Operands	Description	Flags
INCDPi		DPTR = DPTR + 1	
DECDPi		DPTR = DPTR – 1	
ADDDPi		DPTR = DPTR + {R8, B}	
SUBDPi		DPTR = DPTR – {R8, B}	
INC2DPi		DPTR = DPTR + 2	
DEC2DPi		DPTR = DPTR – 2	
ROTR8	EACC, ER8	Rotate Right ACC R8[2:0] Bit	
ROTL8	EACC, ER8	Rotate Left ACC R8[2:0] Bit	
ADD16	ERp, EDPi, ERn	ERp = XRAM + ERn + EC	EZ, EC
	EDPi, ERn, ERp	XRAM = ERn + ERp + EC	
	ERp, ERn, ERm	ERp = ERn + ERm + EC	
SUB16	ERp, EDPi, ERn	ERp = XRAM – ERn – EC	EZ, EC
	EDPi, ERn, ERp	XRAM = ERn – ERp – EC	
	ERp, ERn, ERm	ERp = ERn – ERm – EC	
NOT16	ERn	ERn = ~ERn	
CLR16	ERn	ERn = 0	
INC16	ERn	ERn = ERn + 1	EZ
DEC16	ERn	ERn = ERn – 1	EZ
ANL16	ERn, EDPi	ERn = XRAM & ERn	EZ
	EDPi, ERn	XRAM = XRAM & ERn	
	ERn, ERm	ERn = ERn & ERm	
ORL16	ERn, EDPi	ERn = XRAM | ERn	EZ
	EDPi, ERn	XRAM = XRAM | ERn	
	ERn, ERm	ERn = ERn | ERm	
XRL16	ERn, EDPi	ERn = XRAM ^ ERn	EZ

	EDPi, ERn	XRAM = XRAM ^ ERn	
	ERn, ERm	ERn = ERn ^ ERm	
MOV16	ERn, EDPi	ERn = XRAM	EZ
	EDPi, ERn	XRAM = ERn	
	ERn, ERm	ERn = ERm	
MUL16	ERn, ERm	{ERn, Erm} = ERn * Erm (signed mul)	
MULS16	ERn, ERm	{ERn, Erm} = ERn * Erm (signed mul, saturate)	
ROTR16	ERn, ER8	Rotate Right ERn ER8[3:0] Bit	
ROTL16	ERn, ER8	Rotate Left ERn ER8[3:0] Bit	
SHIFTL	ERn, ER8	ERn = ERn >> ER8[3:0] (logic shift)	
SHIFTR	ERn, ER8	ERn = ERn >> ER8[3:0] (arithmetic shift)	
ADD16 (saturate)	ERp, EDPi, ERn	ERp = XRAM + ERn + EC	EZ, EC
	EDPi, ERn, ERp	XRAM = ERn + ERp + EC	
	ERp, ERn, ERm	ERp = ERn + ERm + EC	
SUB16 (saturate)	ERp, EDPi, ERn	ERp = XRAM – ERn – EC	EZ, EC
	EDPi, ERn, ERp	XRAM = ERn – ERp – EC	
	ERp, ERn, ERm	ERp = ERn – ERm – EC	
SWAP16	ERn	{ERn[7:0], ERn[15:8]} = ERn	

Notes:

ERn, ERm, ERp:	16-bit register ER0-ER3, n=m=p is allowed
ERni, ERmj:	8-bit SFR R00, R01, R10, R11, R20, R21, R30, R31, ni=mj is allowed
EDPi:	XRAM addressing pointer DPTR0 or DPTR1
ER8:	8-bit SFR R8 when using Extend 16-bits instructions
EACC:	8-bit SFR ACC when using Extend 16-bits instructions

4.3 Extend 16-bits instruction's registers

Extend 16-bits instruction use some registers.

ER0, ER1, ER2, and ER3 are 16-bits registers. They can also be used as eight 8-bits SFRs by normal instructions. When using as 8-bits SFRs, Their names are ER00, ER01, ER10, ER11, ER20, ER21, ER30, ER31.

ER8 is an 8-bits registers. It can also be used as an SFR by normal instructions. When using as SFR, It's named R8.

Two instructions use EACC as operand. The EACC is actually register A.

Most instructions use EDP0 or EDP1. They are actually DPTR0 and DPTR1.

SFR 4-1 Extend Registers

ERnm, ER8 (0xE6-0xEE)

Extend 16-bits instruction's registers

	7	6	5	4	3	2	1	0
Name	ERnm, ER8							

Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Extend 16-bits instruction's Registers** Used by 16-bits.instructions.

Chapter 5 INTERRUPT

5.1 Interrupt Sources and Vectors

AX208 provides 16 interrupt sources. All interrupts are controlled by a series combination of individual enable bits and a global enable (EA) in the interrupt-enable register (IE0.7). Setting EA to logic 1 allows individual interrupts to be enabled. Setting EA to logic 0 disables all interrupts regardless of the individual interrupt-enable settings. The interrupt enables and priorities are functionally identical to those of the 80C52.

AX208 provides 2 sets of vectors entry addresses, starting from 0x4003 and 0x8003. The vector base address is set by IA.

5.2 Interrupt Priority

There are 2 levels of interrupt priority: Level 1 to 0. All interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 1 to 0. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 5-1. (except that Soft_interrupt is the highest.)

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled.

Interrupt Sources	Interrupt Vector	No.	Interrupt Flag	Interrupt Enable Bit	Priority Control Bit
Timer0	BASE + 0x03	0		IE0.0	IP0.0
Timer1	BASE + 0x03	1		IE0.1	IP0.1
Timer2	BASE + 0x03	2		IE0.2	IP0.2
Timer3	BASE + 0x03	3		IE0.3	IP0.3
USB	BASE + 0x03	4		IE0.4	IP0.4

SPI	BASE + 0x03	5		IE0.5	IP0.5
SDC	BASE + 0x03	6		IE0.6	IP0.6
Soft_interrupt	BASE + 0x03	7		IE2.4	IP0.7
Huffbuf_empty	BASE + 0x03	8		IE1.0	IP1.0
IDCT	BASE + 0x03	9		IE1.1	IP1.1
BuffOut/Huff	BASE + 0x03	10		IE1.2	IP1.2
PORT	BASE + 0x03	11		IE1.3	IP1.3
WDT LVD	BASE + 0x03	12		IE2.5 IE1.4	IP1.4
IRTCC UART	BASE + 0x03	13		IE1.5	IP1.5
DAC	BASE + 0x03	14		IE1.6	IP1.6
Sfs_int	BASE + 0x03	15		IE1.7	IP1.7

5.3 Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 4 system clock cycles: 1 clock cycle to detect the interrupt and 3 clock cycles to complete the LCALL to the ISR. Additional clock cycles will be required if the CPU is executing branch instructions (e.g.: ACALL, LJMP, JZ...). If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

5.4 Interrupt Registers

SFR 5-1 IE0

IE0 (0xA8)

Interrupt Enable 0

	7	6	5	4	3	2	1	0
Name	EA	IE_SDC	IE_SPI	IE_USB	IE_TM3	IE_TM2	IE_TM1	IE_TM0
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	EA	**Global Interrupt Enable Bit** 0: All interrupts are disabled. 1: All interrupts can be enabled.

6	IE_SDC	**SDC Interrupt Enable Bit** 0: SDC interrupt is disabled. 1: SDC interrupt is enabled if EA=1.
5	IE_SPI	**SPI Interrupt Enable Bit** 0: SPI interrupt is disabled. 1: SPI interrupt is enabled if EA=1.
4	IE_USB	**USB Interrupt Enable Bit** 0: USB interrupt is disabled. 1: USB interrupt is enabled if EA=1.
3	IE_TM3	**Timer 3 Interrupt Enable Bit** 0: Timer 3 interrupt is disabled. 1: Timer 3 interrupt is enabled if EA=1.
2	IE_TM2	**Timer 2 Interrupt Enable Bit** 0: Timer 2 interrupt is disabled. 1: Timer 2 interrupt is enabled if EA=1.
1	IE_TM1	**Timer 1 Interrupt Enable Bit** 0: Timer 1 interrupt is disabled. 1: Timer 1 interrupt is enabled if EA=1.
0	IE_TM0	**Timer 0 Interrupt Enable Bit** 0: Timer 0 interrupt is disabled. 1: Timer 0 interrupt is enabled if EA=1.

SFR 5-2 IE1

IE1 (0xA9)

Interrupt Enable 1

	7	6	5	4	3	2	1	0
Name	IE_SFS	IE_DAC	IE_RTCU	IE_WDLV	IE_PORT	IE_HRGB	IE_IDCT	IE_HBE
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7		
6	IE_DAC	**DAC Interrupt Enable Bit** 0: DAC interrupt is disabled. 1: DAC interrupt is enabled if EA=1.
5	IE_RTCU	**RTC and UART Interrupt Enable Bit** 0: RTC and UART interrupts are disabled. 1: RTC and UART interrupts are enabled if EA=1.
4	IE_WDLV	**WDT and LVD Interrupts Enable Bit** 0: WDT and LVD interrupts are disabled. 1: WDT and LVD interrupts are enabled if EA=1.

3	IE_PORT	**PORT Interrupt Enable Bit** 0: PORT interrupt is disabled. 1: PORT interrupt is enabled if EA=1.
2	IE_HRGB	**Huffman and YUV2RGB Interrupts Enable Bit** 0: Huffman and YUV2RGB interrupts are disabled. 1: Huffman and YUV2RGB interrupts are enabled if EA=1.
1	IE_IDCT	**IDCT Interrupt Enable Bit** 0: IDCT interrupt is disabled. 1: IDCT interrupt is enabled if EA=1.
0	IE_HBE	**Huffman Buffer Empty Interrupt Enable Bit** 0: Huffman Buffer Empty interrupt is disabled. 1: Huffman Buffer Empty interrupt is enabled if EA=1.

SFR 5-3 IE2

IE2 (0x95)

Interrupt Enable 2

	7	6	5	4	3	2	1	0
Name	-	-	IE2_WDT	IE2_SOFT	-	-	-	-
Reset	-	-	0	0	-	-	-	-
POR	-	-	0	0	-	-	-	-
Access	-	-	R/W	R/W	-	-	-	-

Bit Number	Bit Mnemonic	Description
5	IE2_WDT	**Watch Dog Timer Interrupt Enable Bit** 0: Watch Dog Timer interrupt is disabled. 1: Watch Dog Timer interrupt is enabled if EA=1.
4	IE2_SOFT	**Soft Interrupt Enable Bit** 0: Soft interrupt is disabled. 1: Soft interrupt is enabled if EA=1.

SFR 5-4 IP0

IP0 (0xB8)

Interrupt Priority 0

	7	6	5	4	3	2	1	0
Name	IP_SOFT	IP_SDC	IP_SPI	IP_USB	IP_TM3	IP_TM2	IP_TM1	IP_TM0
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	IP_SOFT	**Soft Interrupt Priority Bit** 0: Soft interrupt priority is low.

		1: Soft interrupt priority is high.
6	IP_SDC	**SDC Interrupt Priority Bit** 0: SDC interrupt priority is low. 1: SDC interrupt priority is high.
5	IP_SPI	**SPI Interrupt Priority Bit** 0: SPI interrupt priority is low. 1: SPI interrupt priority is high.
4	IP_USB	**USB Interrupt Priority Bit** 0: USB interrupt priority is low. 1: USB interrupt priority is high.
3	IP_TM3	**Timer 3 Interrupt Priority Bit** 0: Timer 3 interrupt priority is low. 1: Timer 3 interrupt priority is high.
2	IP_TM2	**Timer 2 Interrupt Priority Bit** 0: Timer 2 interrupt priority is low. 1: Timer 2 interrupt priority is high.
1	IP_TM1	**Timer 1 Interrupt Priority Bit** 0: Timer 1 interrupt priority is low. 1: Timer 1 interrupt priority is high.
0	IP_TM0	**Timer 0 Interrupt Priority Bit** 0: Timer 0 interrupt priority is low. 1: Timer 0 interrupt priority is high.

SFR 5-5 IP1

IP1 (0xB9)

Interrupt Priority 1

	7	6	5	4	3	2	1	0
Name	IP_SFS	IP_DAC	IP_RTCU	IP_WDLV	IP_PORT	IP_HRGB	IP_IDCT	IP_HBE
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	IP_SFS	**SOF Frequency Synthesizer Interrupt Priority Bit** 0: SOF Frequency Synthesizer interrupt priority is low. 1: SOF Frequency Synthesizer interrupt priority is high.
6	IP_DAC	**DAC Interrupt Priority Bit** 0: DAC interrupt priority is disabled. 1: DAC interrupt priority is high.
5	IP_RTCU	**RTC and UART Interrupt Priority Bit** 0: RTC and UART interrupts priority is low. 1: RTC and UART interrupts priority is high.

4	IP_WDLV	**WDT and LVD Interrupts Priority Bit** 0: WDT and LVD interrupts priority is low. 1: WDT and LVD interrupts priority is high.
3	IP_PORT	**PORT Interrupt Priority Bit** 0: PORT interrupt priority is low. 1: PORT interrupt priority is high.
2	IP_HRGB	**Huffman and YUV2RGB Interrupts Priority Bit** 0: Huffman and YUV2RGB interrupts priority is low. 1: Huffman and YUV2RGB interrupts priority is high.
1	IP_IDCT	**IDCT Interrupt Priority Bit** 0: IDCT interrupt priority is low. 1: IDCT interrupt priority is is high.
0	IP_HBE	**Huffman Buffer Empty Interrupt Priority Bit** 0: Huffman Buffer Empty interrupt priority is low. 1: Huffman Buffer Empty interrupt priority is high.

Chapter 6 CLOCK AND RESET

6.1 Clock System

6.1.1 Clock Control

AX208 support three Clock source, XOSC32K, RC32K, and internal RC96M. Each of them can drive core working. IRTCC needs XOSC32K or RC32K. So, the external crystal is optional.

AX208 embeds one internal oscillator circuits XOSC 32K. External crystal is needed to generate a clock source. One internal programmable PLL can generate a high frequency clock (480MHz) from the crystal clock source. One internal RC oscillator is also embedded.

To make sure the USB module operate properly, the USB clock must set to be 48MHz. In this case, system clock must be 48MHz or 96 MHz.

SFR 6-1 PCON0

PCON0 (0x87)

Power control 0

	7	6	5	4	3	2	1	0
Name	IROMCEN	IRAMCEN	PRAMCEN	DRAMCEN		IDLE	HOLD	-
Reset	0	0	0	0	-	0	0	-
POR	0	0	0	0	-	0	0	-
Access	R/W	R/W	R/W	R/W	-	R/W	R/W	-

Bit	Bit	

Number	Mnemonic	Description
7	IROMCEN	**IROM clock gate** 0: Enable IROM clock. 1: Disable IROM clock.
6	IRAMCEN	**IRAM clock gate** 0: Enable IRAM clock. 1: Disable IRAM clock.
5	PRAMCEN	**PRAM clock gate** 0: Enable PRAM clock. 1: Disable PRAM clock.
4	DRAMCEN	**DRAM clock gate** 0: Enable DRAM clock. 1: Disable DRAM clock.
3		
2	IDLE	**IDLE mode bit** Write 0: No response. Write 1: Enter IDLE mode. Reading from this bit always return 0.
1	HOLD	**HOLD mode bit** Write 0: No response. Write 1: Enter HOLD mode. Reading from this bit always return 0.

SFR 6-2 PCON1

PCON1 (0x9C)

Power control 1

	7	6	5	4	3	2	1	0
Name	DACCEN	ADCCEN	USBCEN	TMRCEN	UARTCEN	SDCCEN	JPEGCEN	SPICEN
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	DACCEN	**DAC clock gate** 0: Enable DAC clock. 1: Disable DAC clock.
6	ADCCEN	**ADC clock gate** 0: Enable ADC clock. 1: Disable ADC clock.
5	USBCEN	**USB clock gate** 0: Enable USB clock. 1: Disable USB clock.

4	TMRCEN	**TIMER clock gate** 0: Enable TIMER clock. 1: Disable TIMER clock.
3	UARTCEN	**UART clock gate** 0: Enable UART clock. 1: Disable UART clock.
2	SDCCEN	**SDC mode bit** 0: Enable SDC clock. 1: Disable SDC clock.
1	JPEGCEN	**JPEG mode bit** 0: Enable JPEG clock. 1: Disable JPEG clock.
0	SPICEN	**SPI clock gate** 0: Enable SPI clock. 1: Disable SPI clock.

SFR 6-3 PCON2

PCON2 (0xD3)

Power control 2

	7	6	5	4	3	2	1	0
Name	RC96MEN	USBDIV2SEL		-	-		RTCCEN	WDTCEN
Reset	1	0		-	-		0	0
POR	1	0		-	-		0	0
Access	R/W	R/W		-	-		R/W	R/W

Bit Number	Bit Mnemonic	Description
7	RC96MEN	**Internal RC Oscillator Enable Bit** 0: Disable Internal RC Oscillator. 1: Enable Internal RC Oscillator.
6	USBDIV2SEL	**USB Clock Divide 2 Select Bit** 0: Disable USB Divide 2. 1: Enable USB Divide 2.
5		
2		
1	RTCCEN	**RTC clock gate** 0: Enable RTC clock. 1: Disable RTC clock.
0	WDTCEN	**WDT clock gate** 0: Enable WDT clock. 1: Disable WDT clock.

SFR 6-4 CLKCON

CLKCON (0xDB)

Clock control

	7	6	5	4	3	2	1	0
Name	RCTRIM				SC32KSEL	SCSEL	RCFSEL	
Reset	0	0	0	0	0	0	1	0
POR	0	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-4	RCTRIM	**96M RC trimming bit**
3	SC32KSEL	**Sys32k_clk source select** 0: 32K div from 96M RC. 1: RTC32K.
2	SCSEL	**System clock select** 0: From RC clock. 1: From PLL.
1-0	RCFSEL	**RC frequency select** 00: 32K 01: 24M 10: 48M, default 11: 96M

6.1.2 Clock Gating

AX208 provides comprehensive clock gating options for eliminating power-wasting activities. System clock supplies clock signals. Every clock can be gated. It allows the user to shut down the clock signal when the function is not needed.

6.1.3 Phase Lock Loop (PLL)

AX208 provides one on-chip programmable Phase Locked Loop (PLL) clock generators for flexible system clock multiplication. The PLL has reference clock from crystal oscillator to provide a stable reference clock and the reference clock is multiplied to provide the final system clock. The PLL can generate 480 MHz output clocks for system and USB PHY.

SFR 6-5 PLLCON

PLLCON (0xB7)

PLL Configuration

	7	6	5	4	3	2	1	0
Name	PLL_LOCK	PLLOSEL			-	-	PLLINSEL	PLLEN
Reset	0	0	0	0	-	-	0	0

POR	0	0	0	0	-	-	0	0
Access	RO	R/W	R/W	R/W	-	-	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	PLL_LOCK	**PLL lock flag** 0: not lock 1: lock **Note: When PLLINSEL=0, this bit is always 0. After about 200ms, PLL is OK.**
6-4	PLLOSEL	**PLL output frequency select** 000: 24MHz 001: 30MHz 010: 48MHz 011: 60MHz 100: 80MHz 101: 96MHz Others: Reserved
1	PLLINSEL	**PLL input clock select** 0: select RTC32K 1: select 1MHz clock
0	PLLEN	**PLL enable** 0: Disable 1: Enable

6.2 Reset

6.2.1 Reset Sources

AX208 has 6 sources of reset.

Internal reset 4 sources include:

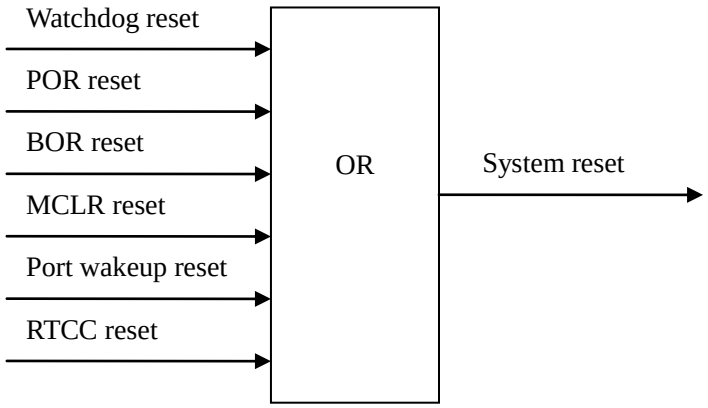
- Watchdog reset
- RTCC reset
- POR reset
- BOR reset

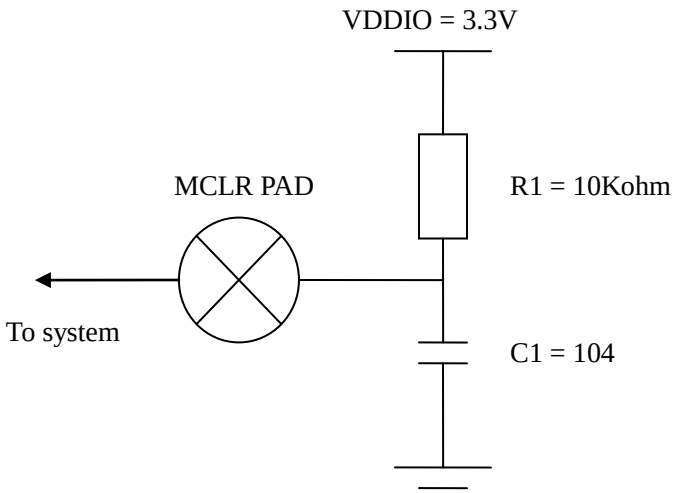
External reset 2 sources include:

- Port wakeup reset
- MCLR reset

6.2.2 System Reset Generation

All reset signals are OR'ed together inside the device to generate an overall system reset to reset the chip. Once reset, the program memory address is reset to 8000h, which is the start address of the Normal Mode.





6.2.3 Power-on Reset (POR)

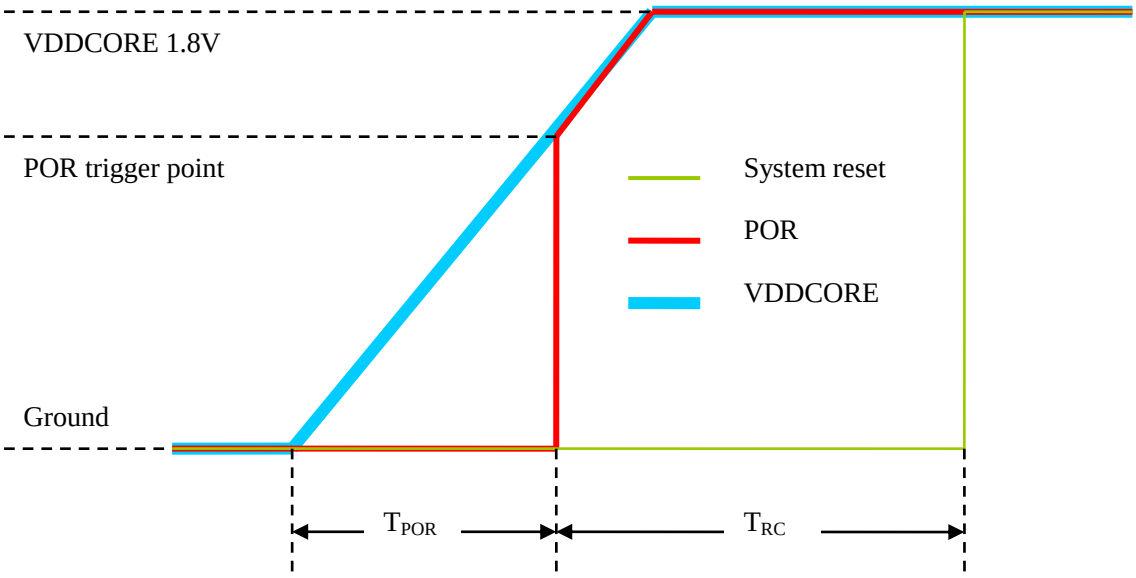
AX208 provides an on-chip Power-On-Reset (POR) circuit to detect power-on and to reset internal logic before VDD reaches the pre-determined POR threshold voltage. Under VDD=1.8V, the POR threshold voltage is set to be about 1.2V-1.3V.

Sometimes, when the VDD is power-off and quickly power-on again, there might be cases that the POR will work improperly and internal reset might not be generated. For this reason, AX208 POR circuit incorporates an internal self-reset module to discharge PORB output during power-off to ensure each

power cycle will work properly.

However, it is also highly recommended user should have a long time between power-off and next power-on to ensure proper start-up. The time depends on actual system board environment and how much decoupling capacitors between power and ground. User has to take into account this effect during board level design.

Figure 6-5 illustrates the power-on and reset signals waveform during proper power-on. Internally, there is TPOR and TRC time for both the POR circuit and the internal counter. TPOR is the time for the POR circuit to stay at zero voltage until it reaches VPOR and the time varies for different VDD rise-up time. It can be assumed to be about 2/3 of the VDD rise-up time. TRC is the time for internal counter to count 4ms using internal RC-oscillator when the counter sees a high logic from PORB signal. As a result, the overall internal reset time is the sum of TPOR and TRC. Such a long time is required to ensure the Power is stable for system use. It also ensures all internal logics are properly reset.



Chapter 7 LOW POWER MANAGEMENT

AX208 device has the low power management mode that can help reducing power consumption when the device does not require intensive CPU resources and speed. There are three low power modes available: SLEEP mode, Hold mode and IDLE mode.

7.1 SLEEP mode

SLEEP mode is an ultimate power reduction mode that will disable power supply to 1.8V logics. I/O status will be keep after 1.8V logics are power down. Before entering SLEEP mode, all analog modules must be disabled.
SLEEP mode can be wake up by RTCC and PORT.
After waken up from SLEEP mode, AX208 will be reset.

7.2 HOLD mode

HOLD mode will stop the clock from entering to system. The system clock is gated with the HOLD mode control. Once enter HOLD mode, clock to the system logic halts. Therefore, there will be no clock switching entering the system logic so that power consumption is minimized due to no AC switching. However, the clock sources are not disabled and they are still running. This allows the clock to be resumed in real time without waiting for the PLL to lock again. Watchdog interrupt, RTCC interrupt, Port interrupt and all reset event will cause system to exit HOLD mode. TO enter HOLD mode, user need to write a '1' to HOLD register (Bit1 of PCON0).
When wakeup from HOLD Mode by port or RTCC, if interrupt is enabled, AX208 enters corresponding interrupt service subroutine (ISR), else AX208 will execute the instruction following HOLD.
When wakeup from HOLD Mode by watchdog, if watchdog interrupt is enabled, AX208 will enter watchdog's ISR, else AX208 will be reset.

7.3 IDLE mode

IDLE mode will stop the clock from entering to the CPU. The CPU clock is gated with the IDLE mode control. Once enter IDLE mode, clock to the CPU logic halts. Therefore, there will be no clock switching entering the CPU logic so CPU power consumption is minimized. All interrupt events will cause system to exit IDLE mode, which include all peripheral interrupt.
TO enter IDLE mode, user need to write a '1' to IDLE register (Bit2 of PCON0).
When exit IDLE mode, AX208 will enter interrupt service subroutine.

7.4 LDO

AX208 provides three on-chip low drop-out regulators (LDO_0, LDO_1 and LDO_2) to convert from 3.3V to 1.8V or 3.3V to 2.8V for internal core power use. It is there to provide high power supply noise rejection and also to minimize power consumption.

- LDO_0 3.3V to 1.8V for RTCC, always enable, working current <= 5uA, output driving 1mA, 1uF CAP
- LDO_1 3.3V to 1.8V for core, can be disabled by CPU, output driving 50mA, 1uF CAP
- LDO_2 3.3V to 2.8V (stable and exact voltage selected: 2.6V, 2.8V, 3.0V) for LCD, can be disabled by CPU, output driving 20mA .

Chapter 8 PORT

AX208 provides five ports (Port 0/1/2/3/4) for user to develop applications. Inputs are all Schmitt triggered with about 400-500mV hysteresis level to filter input voltage fluctuations. Each port pin can be independently set as input or output. Most of the port pins are built-in slew-rate controlled to reduce output bouncing noise. There is one internal 20KΩ pull-up and one 10KΩ pull-down resistor selectable for each input port pin.

8.1 Data Direction configuration

There are five port data direction registers: P0DIR, P1DIR, P2DIR, P3DIR and P4DIR. All port pins are defined as "output" when it is set as "0" and as "input" when it is set as "1". Table 8-1 illustrates the configuration.

Register	Set bit "x" of PxDIR as "1"	Clear bit "x" of PxDIR as "0"	Initial value
P0DIR	Inputs	Outputs	FFh
P1DIR	Inputs	Outputs	FFh
P2DIR	Inputs	Outputs	FFh
P3DIR	Inputs	Outputs	FFh
P4DIR	Inputs	Outputs	7Fh

8.2 Port Data configuration

There are five port data registers: P0, P1, P2, P3 and P4. The port data value is stored as "0" when Px register is set to "0" and as "1" when Px register is set to "1". Table 8-2 illustrates the configuration.

Register	Set bit "x" of Px as "1"	Clear bit "x" of Px as "0"	Initial value
P0	Store "1"	Store "0"	xx
P1	Store "1"	Store "0"	xx
P2	Store "1"	Store "0"	xx
P3	Store "1"	Store "0"	xx
P4	Store "1"	Store "0"	xx

8.3 Pull-up and Pull-down configuration

There are five data pull-up registers: PUP0, PUP1, PUP2, PUP3 and PUP4. The port pin will be pull-up disabled when PUPx register is set to "0" or the pin is set as output, and pull-up enabled when it is set to "1" and the pin is set as input.

There are five data pull-down registers: PDN0, PDN1, PDN2, PDN3 and PDN4. The port pin will be

pull-down disabled when PDNx register is set to "0" or the pin is set as output, and pull-down enabled when it is set to "1" and the pin is set as input.

Register	Set bit "x" of PUPx as "1"	Clear bit "x" of PUPx as "0"	Initial value
PUP0	Enable pull-up	Disable pull-up	00h
PUP1	Enable pull-up	Disable pull-up	00h
PUP2	Enable pull-up	Disable pull-up	00h
PUP3	Enable pull-up	Disable pull-up	00h
PUP4	Enable pull-up	Disable pull-up	00h

Register	Set bit "x" of PDNx as "1"	Clear bit "x" of PDNx as "0"	Initial value
PDN0	Enable pull-down	Disable pull-down	00h
PDN1	Enable pull-down	Disable pull-down	00h
PDN2	Enable pull-down	Disable pull-down	00h
PDN3	Enable pull-down	Disable pull-down	00h
PDN4	Enable pull-down	Disable pull-down	04h

8.4 Digital input enable

There is two digital input enable register: PIE0 and PIE1. There are several I/O MUXed with analog module. I/O digital input and output must be disabled when Analog Module is enabled.

SFR 8-1 PIE

PIE (0x9A)

Port digital input enable control 0

	7	6	5	4	3	2	1	0
Name	PIE07	PIE06	PIE05	PIE04	PIE03	PIE02	PIE01	PIE00
Reset	1	1	1	1	1	1	1	1
POR	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	PIE07	**P13 digital input enable bit (Far ADC7)** 0: P13 digital Input Disabled 1: P13 digital Input Enabled
6	PIE06	**P12 digital input enable bit (Far ADC6)** 0: P12 digital Input Disabled 1: P12 digital Input Enabled
5	PIE05	**P11 digital input enable bit (Far ADC5)** 0: P11 digital Input Disabled 1: P11 digital Input Enabled
4	PIE04	**P04 digital input enable bit (Far ADC4)**

		0: P04 digital Input Disabled 1: P04 digital Input Enabled
3	PIE03	**P03 digital input enable bit (Far ADC3)** 0: P03 digital Input Disabled 1: P03 digital Input Enabled
2	PIE02	**P02 digital input enable bit (Far ADC2)** 0: P02 digital Input Disabled 1: P02 digital Input Enabled
1	PIE01	**P43 digital input enable bit (Far PGATE0_Flash)** 0: P43 digital Input Disabled 1: P43 digital Input Enabled
0	PIE00	**P00 digital input enable bit (Far LDO_LCD)** 0: P00 digital Input Disabled 1: P00 digital Input Enabled

SFR 8-2 PIE1

PIE (0x9D)

Port digital input enable control 1

	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	PIE11	PIE10
Reset	-	-	-	-	-	-	1	1
POR	-	-	-	-	-	-	1	1
Access	-	-	-	-	-	-	R/W	R/W

Bit Number	Bit Mnemonic	Description
1	PIE11	**P44 digital input enable bit (Far PGATE2_SD)** 0: P44 digital Input Disabled 1: P44 digital Input Enabled
0	PIE10	**P23 digital input enable bit (Far PGATE1_LCD)** 0: P23 digital Input Disabled 1: P23 digital Input Enabled

8.5 Peripherals MUXed with Ports

In order to provide more flexible port functions and to minimize pin counts, some of the ports are multiplexed with other peripherals or functions. Table 8-5 illustrates the “Ports MUXed mapping”.

Table 8-5: Port Mapping

8.6 Read and Write Ports

Port 0 to Port 4 are memory-mapped into the Data Memory addressing space. Writing to a port data register sets the voltage levels of the corresponding port pins that have been configured to operate as outputs. Reading from a data register reads the voltage levels of the corresponding port pins.

As illustrated in Figure 8-1, there are major differences reading the port values when the port is set as input and output. When the port is set as output, the CPU will read the port value from Px register instead of the port pin value. When the port is set as input, the CPU will read the value from port pin directly instead of the port value from Px register. As a result, the user should be very careful when using Read-then-Write instructions to access the ports.

PxDIR should be changed after writing the output value to Px when using port as output. For example:

Code assembler:

```
MOV P0, #01h
ANL P0DIR, #0FEH
```

Code C51:

```
P0 = 0x01;
P0DIR &= 0xFE;
```

The first instruction in this example writes the Port 0 data register (P0), which controls the output levels of the Port 0 pins, P00 through P07, and then configures P00 as output. Figure 8-1 shows the internal hardware structure and configuration registers for each pin of Port 0~4.

8.7 Wakeup

8.7.1 Wakeup through external port0

The PWKEN registers (Wakeup Enable Register) allow P0.5, P0.6, P0.7, USB DP and USB DM to cause wakeup.

Clearing bit0-2 in the PWKEN register enables wakeup on corresponding pin of P0.5, P0.6 and P0.7. The trigger condition on the selected pin can be either rising edge or falling edge. The WKED register (Wakeup Edge Select) selects the desired transition edge. Setting a bit in WKED register selects the falling edge of the corresponding P0.5, P0.6 and P0.7 pin. Resetting the bit selects the rising edge. The PWKEN registers are set to 0Fh upon reset.

Once a valid transition occurs on the selected pin, the WKPND (PWKEN.7~PWKEN.5) register (Wakeup Pending Register) latches the transition in the corresponding bit position. Logic ‘1’ indicates the occurrence of the selected trigger edge on the corresponding Port pins. Upon reset, logic ‘0’ is set to all bits of WKPND.

Note:

1. Port 0 wakeup initialization. To avoid any false signaling to port, the followings would be a recommended procedure for Wakeup initialization:

- Configure the edge select of Port 0 pins on WKEDG register,

- Clear the corresponding bits on WKPND Wakeup Pending Register
- Clear the corresponding bits in the PWKEN registers to enable the wakeup on the corresponding port pins

2. Upon exiting the sleep down mode, the Multi-Input Wakeup logic causes full chip reset.

8.7.2 Wakeup registers

SFR 8-3 PWKEN

PWKEN (0x97)

Port wakeup enable

	7	6	5	4	3	2	1	0
Name				PWKEN4	PWKEN3	PWKEN2	PWKEN1	PWKEN0
Reset	-	-	-	1	1	1	1	1
POR	-	-	-	1	1	1	1	1
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
4	PWKEN4	**USB DP wakeup enable bit** 1: USB DP wakeup Disabled 0: USB DP wakeup Enabled
3	PWKEN3	**USB DM wakeup enable bit** 1: USB DM wakeup Disabled 0: USB DM wakeup Enabled
2	PWKEN2	**P07 wakeup enable bit** 1: P07 wakeup Disabled 0: P07 wakeup Enabled
1	PWKEN1	**P06 wakeup enable bit** 1: P06 wakeup Disabled 0: P06 wakeup Enabled
0	PWKEN0	**P05 wakeup enable bit** 1: P05 wakeup Disabled 0: P05 wakeup Enabled

SFR 8-4 PWKPND

PWKPND (0x98)

Port wakeup PND flag

	7	6	5	4	3	2	1	0
Name				PWKPND4	PWKPND3	PWKPND2	PWKPND1	PWKPND0
Reset	-	-	-	0	0	0	0	0
POR	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
4	PWKPND4	**USB DP wakeup PND flag** 0: no USB DP wakeup event occurred 1: USB DP wakeup event occurred
3	PWKPND3	**USB DM wakeup PND flag** 0: no USB DM wakeup event occurred 1: USB DM wakeup event occurred
2	PWKPND2	**P07 wakeup PND flag** 0: no P07 wakeup event occurred 1: P07 wakeup event occurred
1	PWKPND1	**P06 wakeup PND flag** 0: no P06 wakeup event occurred 1: P06 wakeup event occurred
0	PWKPND0	**P05 wakeup PND flag** 0: no P05 wakeup event occurred 1: P05 wakeup event occurred

SFR 8-5 PWKEDGE

PWKEDGE (0x99)

Port wakeup Edge select

	7	6	5	4	3	2	1	0
Name				PWKEDGE4	PWKEDGE3	PWKEDGE2	PWKEDGE1	PWKEDGE0
Reset	-	-	-	x	x	x	x	x
POR	-	-	-	x	x	x	x	x
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
4	PWKEDGE4	**USB DP wakeup Edge select** 0: select USB DP rising edge as wakeup event 1: select USB DP falling edge as wakeup event
3	PWKEDGE3	**USB DM wakeup Edge select** 0: select USB DM rising edge as wakeup event 1: select USB DM falling edge as wakeup event
2	PWKEDGE2	**P07 wakeup Edge select** 0: select P07 rising edge as wakeup event 1: select P07 falling edge as wakeup event
1	PWKEDGE1	**P06 wakeup Edge select** 0: select P06 rising edge as wakeup event 1: select P06 falling edge as wakeup event
0	PWKEDGE0	**P05 wakeup Edge select** 0: select P05 rising edge as wakeup event

		1: select P05 falling edge as wakeup event

Note:

1. Enable P0x Wakeup is a condition of P0x wakeup events occurred.
2. To enable PWKPNDx, set PWKENx to '0'
3. To clear PWKPNDx, write '0' to PWKPNDx. PWKPNDx will be '0' 2 clocks later after write '0' to PWKPNDx.
4. PWKPNDx is cleared when PWKENx is '1'.

Chapter 9 TIMERS

9.1 Timer0

Timer0 is a 8-bit timer/counter with a 7-bit pre-scaler. It can be configured as a timer or a counter.

9.1.1 Timer0 SFR

SFR 9-1 TMR0CON

TMR0CON (0xF8)

Timer0 control

	7	6	5	4	3	2	1	0
Name	T0PND	-	-	-	T0OS	T0CS	T0SE	T0EN
Reset	0	-	-	-	0	0	0	0
POR	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	T0PND	**Timer0 Pending Flag** 0: Not Pending 1: Pending
3	T0OS	**Timer0 external increase source** 0: select P21 1: select Sys32k_clk , if core clock run at 32k, it's not permit to select this option
2	T0CS	**Timer0 incuease source** 0: select system clock Sys_clk 1: select external increase source
1	T0SE	**Timer0 external increase source edge select**

		0: Rising Edge 1: Falling Edge
0	T0EN	**Timer0 enable** 0: Disable 1: Enable

SFR 9-2 TMR0CNT

TMR0CNT (0xF9)

Timer0 Counter

	7	6	5	4	3	2	1	0
Name	TMR0CNT							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer0 Counter** Timer0 will increase in proper condition while it is enable. It overflows when TMR0CNT=TMR0PR, TMR0CNT will be cleared to 0x00 when overflow occurs, and the interrupt flag will be set '1' by hardware.

SFR 9-3 TMR0PR

TMR0PR (0xFA)

Timer0 Period

	7	6	5	4	3	2	1	0
Name	TMR0PR							
Reset	1	1	1	1	1	1	1	1
POR	1	1	1	1	1	1	1	1
Access	W	W	W	W	W	W	W	W

Bit Number	Bit Mnemonic	Description
7-0		**Timer0 Period** The overflow period of the times is: Tinc-source * TMR0PSR * (TMR0PR+1)

SFR 9-4 TMR0PSR

TMR0PSR (0xFB)

Timer0 pre-scalar select

	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	PSR		
Reset	-	-	-	-	-	x	x	x
POR	-	-	-	-	-	x	x	x
Access	-	-	-	-	-	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
2-0	TMR0PSR	**Timer0 pre-scalar select** 000: div 1 001: div 2 010: div 4 011: div 8 100: div 16 101: div 32 110: div 64 111: div 128

9.2 Timer1

Timer1 is a 16-bit timer/counter. It can be configured as a timer, a counter or a PWM generator.

9.2.1 Timer1 SFR

SFR 9-5 TMR1CON

TMR1CON (0xE1)

Timer1 control

	7	6	5	4	3	2	1	0
Name	T1PWMOS1	T1PWMOS0	T1S		T1PND	T1OD	T1POEN	T1EN
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	T1PWMOS1	**PWM output select P40** 0: Not select 1: select
6	T1PWMOS0	**PWM output select P23** 0: Not select 1: select
5-4	T1S	**Timer1 clock source select** 00: select system clock 01: select external pin rising edge (P20) 10: select external pin falling edge (P20) 11: select Sys32k_clk
3	T1PND	**Timer1 Pending Flag**

		0: Not Pending 1: Pending
2	T1OD	**Timer1 PWM open-drain output** 0: normal output 1: open-drain output, the associate I/O must set as input
1	T1POEN	**Timer1 PWM output enable** 0: disable 1: enable
0	T1EN	**Timer1 enable** 0: Disable 1: Enable

SFR 9-6 TMR1CNTH/ TMR1CNTL

TMR1CNTH/ TMR1CNTL (0x3021/0x3020)

Timer1 Counter

	7	6	5	4	3	2	1	0
Name	TMR1CNTH/ TMR1CNTL							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer1 Counter** Timer1 will increase in proper condition while it is enable. It overflows when TMR1CNT=TMR1PR, TMR1CNT will be cleared to 0x0000 when overflow, and the interrupt flag will be set '1' by hardware.

SFR 9-7 TMR1PRH/ TMR1PRL

TMR1PRH/ TMR1PRL (0x3023/0x3022)

Timer1 Period

	7	6	5	4	3	2	1	0
Name	TMR1PRH/ TMR1PRL							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer1 Period** The overflow period of the times is: Tinc-source * (TMR1PR+1)

SFR 9-8 TMR1PWMH/ TMR1PWML

TMR1PWMH/ TMR1PWML (0x3025/0x3024)

Timer1 PWM duty

	7	6	5	4	3	2	1	0

Name	TMR1PWMH/ TMR1PWML							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer1 PWM duty** TMR1PWM is reserved in timer/counter mode. In PWM mode, it is used as duty cycle setting.

9.3 Timer2

Timer2 is a 16-bit timer/counter with a 7-bit pre-scaler. It can be configured as a timer, a counter or a PWM generator.

9.3.1 Timer2 SFR

SFR 9-9 TMR2CON

TMR2CON (0xC1)

Timer2 control

	7	6	5	4	3	2	1	0
Name	T2PWMOS1	T2PWMOS0	T2S	T2PND	T2PSR			T2EN
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	T2PWMOS1	**PWM output select P41** 0: Not select 1: select
6	T2PWMOS0	**PWM output select P26** 0: Not select 1: select
5	T2S	**Timer2 clock source select** 0: select system clock 1: select Sys32k_clk rising edge
4	T2PND	**Timer2 Pending Flag** 0: Not Pending 1: Pending

3-1	T2PSR	**Timer2 pre-scaler** 000: div 1 001: div 2 010: div 4 011: div 8 100: div 16 101: div 32 110: div 64 111: div 128
0	T2EN	**Timer2 enable** 0: Disable 1: Enable

SFR 9-10 TMR2CNTH/ TMR2CNTL

TMR2CNTH/ TMR2CNTL (0x3031/0x3030)

Timer2 Counter

	7	6	5	4	3	2	1	0
Name	TMR2CNTH/ TMR2CNTL							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer2 Counter** Timer2 will increase in proper condition while it is enable. It overflows when TMR2CNT=TMR2PR, TMR2CNT will be cleared to 0x0000 when overflow, and the interrupt flag will be set '1' by hardware.

SFR 9-11 TMR2PRH/ TMR2PRL

TMR2PRH/ TMR2PRL (0x3033/0x3032)

Timer2 Period

	7	6	5	4	3	2	1	0
Name	TMR2PRH/ TMR2PRL							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer2 Period** The overflow period of the times is: Tinc-source * TMR2PSR * (TMR2PR+1)

SFR 9-12 TMR2PWMH/ TMR2PWML

TMR2PWMH/ TMR2PWML (0x3035/0x3034)

Timer2 PWM duty

	7	6	5	4	3	2	1	0
Name	TMR2PWMH/ TMR2PWML							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer2 PWM duty** TMR2PWM is reserved in timer/counter mode. In PWM mode, it is used as duty cycle setting.

9.4 Timer3

Timer3 is a 8-bit timer/counter with a 7-bit pre-scaler. It can be configured as a timer or a counter.

9.4.1 Timer3 SFR

SFR 9-13 TMR3CON

TMR3CON (0xAC)

Timer3 control

	7	6	5	4	3	2	1	0
Name	T3PND	-	-	-	T3OS	T3CS	T3SE	T3EN
Reset	0	-	-	-	0	0	0	0
POR	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	T3PND	**Timer3 Pending Flag** 0: Not Pending 1: Pending
3	T3OS	**Timer3 external increase source** 0: select P14 1: select Sys32k_clk , if core clock run at 32k, it's not permit to select this option
2	T3CS	**Timer3 increase source** 0: select system clock Sys_clk 1: select external increase source
1	T3SE	**Timer3 external increase source edge select**

		0: Rising Edge 1: Falling Edge
0	T3EN	**Timer3 enable** 0: Disable 1: Enable

SFR 9-14 TMR3CNT

TMR3CNT (0xAD)

Timer0 Counter

	7	6	5	4	3	2	1	0
Name	TMR3CNT							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer3 Counter** Timer3 will increase in proper condition while it is enable. It overflows when TMR3CNT=TMR3PR, TMR3CNT will be cleared to 0x00 when overflow occurs, and the interrupt flag will be set '1' by hardware.

SFR 9-15 TMR3PR

TMR3PR (0xAE)

Timer0 Period

	7	6	5	4	3	2	1	0
Name	TMR3PR							
Reset	1	1	1	1	1	1	1	1
POR	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		**Timer3 Period** The overflow period of the times is: Tinc-source * TMR3PSR * (TMR3PR+1)

SFR 9-16 TMR3PSR

TMR3PSR (0xAF)

Timer3 pre-scalar select

	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	PSR		
Reset	-	-	-	-	-	x	x	x
POR	-	-	-	-	-	x	x	x
Access	-	-	-	-	-	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
2-0	TMR3PSR	**Timer3 pre-scalar select** 000: div 1 001: div 2 010: div 4 011: div 8 100: div 16 101: div 32 110: div 64 111: div 128

9.5 Watchdog

The Watchdog Timer (WDT) logic consists of a 20bit Watchdog Timer. The Watchdog Timer is clocked by internal RC oscillator running at 32KHz or SYS32K_CLK. When device resets, the WDT is disabled and user should enable the WDT if it is needed.

In the default configuration, WDT overflows in 2 ms. The application program needs to write a '1' into WDTCON[5] at least once 2 ms to prevent WDT time out. The lower 3 bits of the WDTCON register control the selection of overflow time period. Figure 9-5 shows the WDT block diagram.

Watchdog SFR

SFR 9-17 WDTCON

WDTCON (0xF7)

Watchdog control

	7	6	5	4	3	2	1	0
Name	WDTPD	WDTTO	CLRWDT	WDTEN	RSTEN	WDTPS		
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	WDTPD	**Watchdog Flag** 0: Before hold operation 1: After hold operation
6	WDTTO	**Watchdog Time Out** 0: After clear Watchdog or Power up 1: After Watchdog time out
5	CLRWDT	**Clear WDT counter** 0: No action 1: Write to clear WDT counter
4	WDTEN	**WDT enable bit**

		0: Disable the Watchdog timer 1: Enable the Watchdog timer
3	RSTEN	**WDT reset enable bit** 0: Disable the Watchdog reset 1: Enable the Watchdog reset
2-0	WDTPS	**WDT time out period setting** 000: 2ms 001: 8ms 010: 32ms 011: 128ms 100: 512ms 101: 2048ms 110: 8192ms 111: 32768ms

Watchdog Wake up

There are 2 modes for wake up operation: wake up without reset and wake up with reset. It determines by RSTEN bit (WDTCON[3]). When RSTEN sets to 0, the watchdog will generate a non-reset wake up after counter overflows. Only in HOLD Mode, non-reset wake up can wakeup AX208 and it will continue to execute next instruction. When RSTEN sets to 1, the watchdog will generate a reset wakeup after counter overflows. During HOLD Mode, watchdog reset can wake up the chip, and then, AX208 goes back to the initial state.

9.6 IRTCC

IRTCC offers a real time clock with alarm. It also offers:

- Two alternative 32kHz clock sources, XOSC32K and RC32K
- Two signals, alarm and second
- Seven wake-up sources
- And 64-Bytes RAM

There are some configure registers, one 4-Bytes second-counter register, and one 4-Bytes alarm setting register in the IRTCC. The registers and the RAM can be accessed by core through the communication channels.

The second signal can work as interrupt by setting the IRTIE bit. When IRTCC works and IRTIE = 1, IRTCC second interrupt will be generated every 1 second by setting IRTPND to 1. IRTPND can be cleared by software by writing 0 to IRTPND bit.

The alarm signal can work as interrupt by setting the IRTALIE bit. When IRTCC works and IRTALIE = 1, IRTCC alarm interrupt will be generated when the current time is equal to the preset time by setting IRTALPND to 1. IRTALPND can be cleared by software by writing 0 to IRTALPND bit.

Alarm signal can also work as a wake-up source.

9.6.1 Communication with IRTCC

IRTCC offers some commands for core to access the registers and RAM.

9.6.1.1Command list

Symbol	value	Addr	Op	Data	Function
Rtc_alm_rd	0x52	0B	R	4B	Read alarm register
Rtc_alm_wr	0x53	0B	W	4B	Write alarm register
Rtc_ram_rd	0x56	1B	R	Up to 64B	Read RAM
Rtc_ram_wr	0x57	1B	W	Up to 64B	Write RAM
Rtc_cfg_rd	0x54	0B	R	1B	Read configure register
Rtc_cfg_wr	0x55	0B	W	1B	Write configure register
Rtc_cfg1_rd	0x58	0B	R	1B	Read configure 1 register
Rtc_cfg1_wr	0x59	0B	W	1B	Write configure 1 register
Rtc_cfg2_rd	0x5A	0B	R	1B	Read configure 2 register
Rtc_cfg2_wr	0x5B	0B	W	1B	Write configure 2 register
Rtc_cfg3_rd	0x60	0B	R	1B	Read configure 3 register
Rtc_cfg3_wr	0x61	0B	W	1B	Write configure 3 register
Rtc_cnt_rd	0xE0	0B	R	4B	Read second counter register
Rtc_cnt_wr	0xF0	0B	W	4B	Write second counter register

9.6.1.2Command procedure

Read from IRTCC:

1. IRTCON.EN = 1
2. IRTDATA = cmd
3. Wait for IRTCON.DONE = 0
4. IRTDATA = xx
5. Wait for IRTCON.DONE = 0
6. Get value of IRTDATA
7. Repeat to 4, till last byte
8. IRTCON.EN = 0

Write to IRTCC:

1. IRTCON.EN = 1
2. IRTDATA = cmd
3. Wait for IRTCON.DONE = 0
4. IRTDATA = data
5. Wait for IRTCON.DONE = 0

6. Repeat to 4, till last byte
7. IRTCON.EN = 0

9.6.2 IRTCC timer

IRTCC timer can be power independently. It can work even other logic in AX208 is power off. In IRTCC timer, there are one 8-bit configure register, one 32-bit real time counter, one 32-bit alarm register and 64-byte user RAM. All of these can be access (read or write) by several command sets through the IRTCC control.

There is 6-bit valid address for the 64-byte user RAM. So the upper 2-bit of address in the Write_RAM or Read_RAM command are ignored. After one byte write/read, the internal address can increase automatically, this characteristic provide a burst mode to write/read the RAM. If the internal address increase greater than 63, it will roll back to 0.

9.6.3 IRTCC SFR

SFR 9-18 IRTCON

IRTCON (0x9F)

IRTCC control

	7	6	5	4	3	2	1	0
Name	-	-	IRTALPND	IRTALIE	IRTPND	IRTIE	DONE	EN
Reset	-	-	x	x	x	x	x	x
POR	-	-	x	x	x	x	x	x
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	IRTRSTEN	**IRTCC second reset enable pending** 0: Not Pending (Write 0 to clear pending) 1: Pending
5	IRTALPND	**IRTCC alarm pending** 0: Not Pending (Write 0 to clear pending) 1: Pending
4	IRTALIE	**IRTCC alarm interrupt enable** 0: Disable 1: Enable
3	IRTPND	**IRTCC second pending** 0: Not Pending (Write 0 to clear pending) 1: Pending
2	IRTIE	**IRTCC second interrupt enable** 0: Disable

		1: Enable Must be '1' if IRTCC second is used to wake up system.
1	DONE	**Communication done flag** 0: done 1: not done
0	EN	**IRTCC communications enable** 0: Disable 1: Enable

SFR 9-19 IRTDATA

IRTDATA (0x9E)

IRTCC communication data

	7	6	5	4	3	2	1	0
Name	IRTDATA							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		Write to IRTDATA will start IRTCC communication and set DONE flag to 1. After DONE flag back to 0, read IRTDATA will return IRTCC data.

9.6.4 Configure Registers

IRTCC timer configure register

	7	6	5	4	3	2	1	0
Name	OSCEN	ALMEN	PDFLAG	TSMODE	F1HZEN	F32KHZEN	CLK32KSEL	ALMOT
Reset	0	0	1	0	0	0	0	x
POR	0	0	1	0	0	0	0	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	OSCEN	**XOSC32K enable** 0: Disable 1: Enable
6	ALMEN	**Alarm function enable** 0: Disable 1: Enable
5	PDFLAG	**IRTCC timer power down flag** 0: RTCC timer is working 1: RTCC timer is just power on

4	TSMODE	
3	F1HZEN	**1Hz/2Hz signal output enable** 0: Disable 1: Enable
2	F32KHZEN	**32KHz signal output enable** 0: Disable 1: Enable
1	CLK32KSEL	**RTCC timer clock source select** 0: RTCC timer works with RC32K 1: RTCC timer works with XOSC32K
0	ALMOT	**Alarm match flag** 0: No alarm match happen 1: Alarm match This flag is set to '1' by hardware when alarm register match real timer counter. It can be clear to '0' of ALMEN is set to '0' or 'Write_ALM' is detected.

IRTCC timer configure 1 register

	7	6	5	4	3	2	1	0
Name	-	-	-	F2HZSEL	RC32KEN	PMIX	PDOWN	CORELDOEN
Reset	-	-	-	x	1	1	0	1
POR	-	-	-	x	1	1	0	1
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
4	F2HZSEL	**Select output frequency** 0: output 1Hz 1: output 2Hz
3	RC32KEN	**RTC internal 32K RC OSC enable** 0: Disable 1: Enable
2	PMIX	**RTC VDD and CORE VDD power mix** 0: Disable 1: Enable
1	PDOWN	**Power down latch** 0: Disable 1: Enable latch
0	CORELDOEN	**CORE LDO enable** 0: Disable 1: Enable

IRTCC timer configure 2 register

	7	6	5	4	3	2	1	0

Name	-	ALMWKEN	MCLRWKEN	USBDPWKEN	USBDMWKEN	WK2EN	WK1EN	WK0EN
Reset	-	x	0	0	0	0	0	0
POR	-	x	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
6	ALMWKEN	**Alarm wake up enable** 0: Disable 1: Enable
5	MCLRWKEN	**MCLR wake up enable** 0: Disable 1: Enable
4	USBDPWKEN	**USB DP wake up enable** 0: Disable 1: Enable
3	USBDMWKEN	**USB DM wake up enable** 0: Disable 1: Enable
2	WK2EN	**P07 wake up enable** 0: Disable 1: Enable
1	WK1EN	**P06 wake up enable** 0: Disable 1: Enable
0	WK0EN	**P05 wake up enable** 0: Disable 1: Enable

IRTCC timer configure 3 register

	7	6	5	4	3	2	1	0
Name	-	-	MCLRWKEG	USBDPWKEG	USBDMWKEG	WK2EG	WK1EG	WK0EG
Reset	-	-	0	0	0	0	0	0
POR	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
5	MCLRWKEG	**MCLR wake up edge** 0: Disable 1: Enable
4	USBDPWKEG	**USB DP wake up edge** 0: rising 1: falling

3	USBDMWKEG	**USB DM wake up edge** 0: rising 1: falling
2	WK2EG	**P07 wake up edge** 0: rising 1: falling
1	WK1EG	**P06 wake up edge** 0: rising 1: falling
0	WK0EG	**P05 wake up edge** 0: rising 1: falling

Chapter 10 UART

UART is a serial port capable of asynchronous transmission. The UART can function in full duplex mode. Receive data is buffered in a holding register. This allows the UART to start reception of a second incoming data byte before software has finished reading the previous data byte.

10.1 Control registers

SFR 10-1 UARTCON

UARTCON (0xFD)

UART control

	7	6	5	4	3	2	1	0
Name	UTSBS	UTTXNB	NBITEN	UTEN	UTTXINV	UTRXINV	TXIE	RXIE
Reset	0	1	x	x	x	x	x	x
POR	0	1	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	UTSBS	**Stop Bit Select** 0: 1 bit as Stop Bit 1: 2 bits as Stop Bit
6	UTTXNB	**The ninth bit data** The ninth bit data of transmitter buffer. Write the ninth bit into this location that you want to transmit.
5	NBITEN	**Nine-Bit mode Enable Bit** 0: Eight-bit mode 1: Nine-bit mode
4	UTEN	**UART Enable Bit** 0: Disable UART module 1: Enable UART module
3	UTTXINV	**Transmit Invert Selection Bit** 0: Transmitter output without inverted 1: Transmitter output inverted
2	UTRXINV	**Receive Invert Selection Bit** 0: Receiver input without inverted 1: Receiver input inverted
1	TXIE	**Transmit Interrupt Enable** 0: Transmit interrupt disable

		1: Transmit interrupt enable
0	RXIE	**Receive Interrupt Enable** 0: Receive interrupt disable 1: Receive interrupt enable

SFR 10-2 UARTSTA

UARTSTA (0xFC)

UART status

	7	6	5	4	3	2	1	0
Name	UTRXNB	FEF	RXIF	TXIF				PSEL
Reset	x	x	0	1	-	-	-	0
POR	x	x	0	1	-	-	-	0
Access	R/W	R/W	R/W	R/W	-	-	-	R/W

Bit Number	Bit Mnemonic	Description
7	UTRXNB	**The ninth bit data** The ninth bit data of receive buffer
6	FEF	**Frame Error Flag** 0: the stop bit is '1' in the last received frame 1: the stop bit is '0' in the last received frame
5	RXIF	**UART RX Interrupt Flag** 0: UART receive not done 1: UART receive done
4	TXIF	**UART TX Interrupt Flag** 0: UART transmit not done 1: UART transmit done Writing data to UARTDATA or '0' to TXIF to clear this flag.
0	PSEL	**UART Port Select** 0: P25 as receive pin and P27 as transmit pin 1: P40 as receive pin and P07 as transmit pin

SFR 10-3 UARTBAUDH/UARTBAUD

UARTBAUDH/UARTBAUD (0x96/0xFE)

UART communication data

	7	6	5	4	3	2	1	0
Name	UARTBAUDH/UARTBAUD							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		Baud = {UARTBAUDH, UARTBAUD} Baud Rate = Fsysclock / [8 * (Baud+1)]

SFR 10-4 UARTDATA

UARTDATA (0xFF)

UART communication data

	7	6	5	4	3	2	1	0
Name	UARTDATA							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		Write this location will load the data to transmitter buffer. And read this location will read the data from the receiver buffer.

Chapter 11 SPI

SPI can serve as master or slave.
SPI uses 2 pins for 2-wire mode:

	SPI Group 0	SPI Group 1
Serial Data (SPIDIDO)	P16	P22
Serial Clock (SPICLK)	P17	P24

SPI uses pins for 3-wire mode:

	SPI Group 0	SPI Group 1
Serial Data In (SPIDI)	P15	P25
Serial Data Out (SPIDO)	P16	P22
Serial Clock (SPICLK)	P17	P24

11.1 SPI Registers

SFR 11-1 SPICON

SPICON (0xD8)
SPI control

	7	6	5	4	3	2	1	0
Name	SPIPND	SPISM	SPIRT	SPIWS	SPIGSEL	SPIEDGE	SPIIDST	SPIEN
Reset	1	0	0	0	0	0	0	0
POR	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	SPIPDN	**SPI Pending bit** 0: Transmission is not finish 1: Transmission finish Read only, writing SPIBUF will clear this bit.
6	SPISM	**SPI mode selection** 0: Master mode 1: Slave mode
5	SPIRT	**SPI RX/TX select bit in 2-wire mode or DMA mode** 0: TX 1: RX In 3-wire mode, SPI can both Transmit and Receive at he same time. But if use DMA mode or 2-wire mode, just one direction (TX or RX) is allowed. Use this bit to select TX or RX.
4	SPIWS	**SPI 2-wire/3-wire mode select bit**

		0: 3-wire mode 1: 2-wire mode
3	SPIGSEL	**SPI Group select bit** 0: Group 0 1: Group 1
2	SPIEDGE	**SPI sampling edge select bit** When SPIIDST = 0: 0: sample at falling edge 1: sample at rising edge When SPIIDST = 1: 0: sample at rising edge 1: sample at falling edge
1	SPIIDST	**SPI clock signal idle state** 0: Clock signal stay at 0 when idle 1: Clock signal stay at 1 when idle
0	SPIEN	**SPI enable bit** 0: SPI disable 1: SPI enable

SFR 11-2 SPIBAUD

SPIBAUD (0xDA)

SPI Baud Rate

	7	6	5	4	3	2	1	0
Name	SPIBAUD							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		Baud rate – Fsysclock / [2 * (SPIBAUD+1)]

SFR 11-3 SPIBUF

SPIBUF (0xD9)

SPI Data Buffer

	7	6	5	4	3	2	1	0
Name	SPIBUF							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		Write this location will load the data to transmitter buffer. And read this location will read the data from the receiver buffer.

SFR 11-4 SPIDMACNT

SPIDMACNT (0xD7)

SPI DMA counter

	7	6	5	4	3	2	1	0
Name	SPIDMACNT							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		SPI DMA Byte = (SPIDMACNT+1) * 2 Writing this register will kick start one DMA process

SFR 11-5 SPIDMAADDR

SPIDMAADDR (0xD6)

SPI DMA Start Address

	7	6	5	4	3	2	1	0
Name	SPIDMAADDR							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7-0		In order to initial SPIDMAADDR, you should write this register twice. First write the high byte, then the low byte. SPI DMA Start Address should be at even address.

11.2 Operation Guide

11.2.1 SPI Normal Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPIRT in 2-wire mode or 3 wire mode
3. Select master mode or slave mode
4. Configure clock frequency when step 3 selected master mode
5. Select one of the four timing mode
6. Enable SPI module by set SPIEN ‘1’
7. Write data to SPIBUF(SPI1BUF0 if SPI1 used) to kick-start a process
8. Wait for SPIPND change to ‘1’, or wait for interrupt
9. Read received data from SPIBUF if need

10. Go to Step 7 to start another process if need or turn off SPI by clearing SPIEN

11.2.2 SPI DMA Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPIRT for DMA direction
3. Select master mode or slave mode
4. Configure clock frequency when step 3 selected master mode
5. Select one of the four timing mode
6. Enable SPI module by set SPIEN ‘1’
7. Write the start address to SPIDMAADR
8. Write data to SPIDMACNT to kick-start a DMA process.
9. Wait for SPIPND change to ‘1’, or wait for interrupt
10. Go to Step 7 to start another DMA process if need or turn off SPI by clearing SPIEN

Chapter 12 SARADC

AX208 provides an eight-channel moderate conversion speed and a moderate resolution 10-bit successive approximated register Analog to Digital Converter (SARADC) for users to develop applications in the following areas:

- Voice grade applications
- Audio applications requiring moderate performance
- Measurement requiring moderate performance and speed

12.1 Pins used

ADC Signal	Pin
ADC7	P13/MIC
ADC6	P12
ADC5	P11
ADC4	P04
ADC3	P03
ADC2	P02
ADC1	1/2 AVDD
ADC0	BG

12.2 SARADC Registers

SFR 12-1 ADCCON

ADCCON (0xD2)

SARADC control

	7	6	5	4	3	2	1	0
Name	ADCGO	EOC	TMREN	ADCTL	ADCEN	ADCSEL		
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	ADCGO	**ADC Conversion Start** When read: 0: conversion finished 1: conversion not finished

		When write: 0: N/A 1: start conversion
6	EOC	**Check if end of conversion** 0: finish 1: not finish
5	TMREN	**Timer Input Enable** 0: disable 1: enable
4	ADCTL	**Timer Source Select** 0: Timer0 1: Timer1
3	ADCEN	**ADC Module Enable** 0: disable 1: enable
2-0	ADCSEL	**ADC Channel Select** 000: ADC0 001: ADC1 010: ADC2 011: ADC3 100: ADC4 101: ADC5 110: ADC6 111: ADC7

SFR 12-2 MICCON

MICCON (0xCF)

MIC control

	7	6	5	4	3	2	1	0
Name	-	ADCLDOEN	ADCHOLD	MICEN	ADC7LINS	MFTEN	MGAIN	
Reset	-	0	0	0	0	0	0	0
POR	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
6	ADCLDOEN	**ADC LDO enable** 0: disable 1: enable
5	ADCHOLD	**ADC analog signal hold control** 0: not hold 1: hold
4	MICEN	**MIC enable**

		0: disable 1: enable
3	ADC7LINS	**ADC7 line in select, bypass mic control** 0: MIC IN 1: bypass MIC IN
2	MFTEN	**MIC filter enable** 0: disable filter 1: enable filter
1-0	MGAIN	**MIC line buffer gain control** 00: 01: 10: 11:

SFR 12-3 ADCBAUD

ADCBAUD (0x3040)

SD host control register 1

	7	6	5	4	3	2	1	0
Name	-	-	BAUD					
Reset	-	-	x	x	x	x	x	x
POR	-	-	x	x	x	x	x	x
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
5-0	BAUD	ADC conversion baud rate

SFR 12-4 ADCDATAL

ADCDATAL (0xD4)

SARADC Buffer low byte control

	7	6	5	4	3	2	1	0
Name	ADCDATAL		-	-	-	-	-	-
Reset	x	x	-	-	-	-	-	-
POR	x	x	-	-	-	-	-	-
Access	RO	RO	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7-6	ADCDATAL	SARADC Buffer low byte

SFR 12-5 ADCDATAH

ADCDATAH (0xD5)

SARADC Buffer high byte control

	7	6	5	4	3	2	1	0
Name	ADCDATAH							

Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	RO	RO	RO	RO	RO	RO	RO	RO

Bit Number	Bit Mnemonic	Description
7-0	ADCDATAH	SARADC Buffer high byte

12.3 Operation Guide

For ADC conversion, a general procedure can be like in the following:

- Configure ADCCON register by

1. Select the channel to use (ADCCON[2:0])
2. Enable ADCEN (ADCCON.0=1)
3. Enable ADCGO (ADCCON.7=1)

- Configure ADCBAUD register by

4. Select the ADC trigger mode either manual or timer-trigger(ADCBAUD.7)
5. Select the Timer to use(ADCBAUD.6)
6. Set ADC conversion Clock Frequency(ADCBAUD[5:0])

- Kick-start the ADC conversion by selecting which timer0/1 under timer-trigger mode or selecting ADCGO under manual mode
- During conversion, ADCGO bit will keep as 1 and after each conversion, ADCGO bit will change to 0. The ADC done pending bit will change to 1 after each ADC conversion finish.

Chapter 13 LCD Interface

AX208 provides an 8080 compatible LCD interface to generate WR and CS signals to LCD panel.
Port 3 is the default LCD data port for LCD interface. Port 3 must be set as output by setting P3DIR to 0x00 when Port 3 is used as LCD data.
CS signal will output to P2.1. P2.1 must be set as output by writing 0 to P2DIR[1] when P2.1 is used as CS.
WR signal will output to P1.1. P1.1 must be set as output by writing 0 to P1DIR[1] when P1.1 is used as WR.
LCD interface can be kicked started by two ways when LCDEN = 1 :

1. Kick start automatically by hardware when MODE = 0.
2. Kick start by writing data to P3 when MODE = 1.

13.1 LCD Control Registers

SFR 13-1 LCDCON

LCDCON (0xB6)

LCD control register

	7	6	5	4	3	2	1	0
Name	LCDLDOEN	LCDTRIM			MODE	WRP	CSP	LCDEN
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	LCDLDOEN	**LCD LDO enable bit** 0: disable 1: enable
6-4	LCDTRIM	**LCD LDO Trimming** 000: LDO output 2.6V … 100: LDO output 2.8V … 111: LDO output 3.0V
3	MODE	**LCD kick start mode select** 0: kick start automatically 1: kick start by writing to P3
2	WRP	**WR signal parity**

		0: WR active high 1: WR active low
1	CSP	**CS signal parity** 0: CS active high 1: CS active low
0	LCDEN	**LCD interface enable** 0: LCD interface disable 1: LCD interface enable

SFR 13-2 LCDPR

LCDPR (0xC7)

LCD CS pulse width Register

	7	6	5	4	3	2	1	0
Name	-	-	BUSY	LCDPR				
Reset	-	-	0	0	0	0	0	0
POR	-	-	0	0	0	0	0	0
Access	-	-	R	W	W	W	W	W

Bit Number	Bit Mnemonic	Description
5	BUSY	**LCD interface state** 0: LCD interface is ready 1: LCD interface is busy
4-0	LCDPR	**LCD CS pulse width** 00000: 1 system clock 00001: 2 system clocks 00010: 3 system clocks 00011: 4 system clocks … 11101: 30 system clocks 11110: 31 system clocks 11111: 32 system clocks
3	CPCLR	**Command interrupt pending clear bit** 0: inactive 1: clear pending
2	DPCLR	**Data interrupt pending clear bit** 0: inactive 1: clear pending
1	8CKE	**Send eight SD clocks after command or data** 0: disable 1: enable
0	ORISE	**Edge selection for sending data and command** 0: falling

		1: rising

SFR 13-3 LCDTCON

LCDTCON (0xC8)

LCD WR pulse timing control Register

	7	6	5	4	3	2	1	0
Name	WR_ACTIVE			WR_DEACTIVE				
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	W	W	W	W	W	W	W	W

Bit Number	Bit Mnemonic	Description
7-5	WR_ACTIVE	**LCD WR pulse start point** 000: 1 system clock after CS active 001: 2 system clocks after CS active … 110: 7 system clocks after CS active 111: 8 system clocks after CS active
4-0	WR_DEACTIVE	**LCD WR pulse end point** 00000: 1 system clock after CS active 00001: 2 system clocks after CS active … 11110: 31 system clocks after CS active 11111: 32 system clocks after CS active

Chapter 14 Audio DAC

DAC module enable if LCHEN or RCHEN is enabled.
DAC left channel will be output to P2.6 when left channel is enabled by LCHEN.
DAC right channel will be output to P4.1 when right channel is enabled by RCHEN.

14.1 Control Registers

SFR 14-1 DACCON

DACCON (0xA5)
DAC control register

	7	6	5	4	3	2	1	0
Name	PND	PCLR	LCHEN	RCHEN	SRSET			
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	RO	WO	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	PND	**DAC pending** 0: Not pending 1: Pending, request data
6	PCLR	**Clear DAC pending** Write '1' to clear DAC pending
5	LCHEN	**Left channel output enables** 0: Disable 1: Enable
4	RCHEN	**Right channel output enables** 0: Disable 1: Enable
3-0	SRSET	**Sample rate setting** 0000: 48KHz 0001: 44.1KHz 0010: 32KHz 0100: 24KHz 0101: 22.05KHz 0110: 16KHz 1000: 12KHz 1001: 11.025KHz 1010: 8KHz

		Others: reserved, never write this values into SRSET

SFR 14-2 DACRCH

DACRCH (0xA7)

DAC right channel

	7	6	5	4	3	2	1	0
Name	DACRCH							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Bit Number	Bit Mnemonic	Description
7-0		Software should write twice to complete the whole value, first the upper byte, then the lower byte.

SFR 14-3 DACLCH

DACLCH (0xA6)

DAC left channel

	7	6	5	4	3	2	1	0
Name	DACLCH							
Reset	x	x	x	x	x	x	x	x
POR	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Bit Number	Bit Mnemonic	Description
7-0		Software should write twice to complete the whole value, first the upper byte, then the lower byte.

SFR 14-4 DACPTR

DACPTR (0x3070)

DAC DMA pointer

	7	6	5	4	3	2	1	0
Name	DACPTR							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	WO	WO	WO	WO	WO	WO	WO	WO

Bit Number	Bit Mnemonic	Description
7-0		DMA pointer is the start address of audio samples transmit to DAC in a DMA process, it can point to IRAM only (0x4000~0x6FFF). And because of the 16-bit address, software should write twice to complete the address, first the upper byte, then the lower byte. The address must be align to 2-byte.

SFR 14-5 DACCNT

DACCNT (0x3071)

DAC DMA counter

	7	6	5	4	3	2	1	0
Name	DACCNT							
Reset	0	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0
Access	WO	WO	WO	WO	WO	WO	WO	WO

Bit Number	Bit Mnemonic	Description
7-0		DMA counter is the number of audio samples transmit to DAC in a DMA process. Write this location will kick start DMA. For example, if you want to transmit 7 left channel audio samples (14 bytes) and 7 right channel audio samples (14 bytes) to DAC in DMA mode, than you should write a value of '7' into DACCNT.

14.2 Demo Code

Polling the pending in normal mode:

```
While(1)
{
    while(!(DACCON & BIT(7))); //wait pending
    DACCON |= BIT(6); //clear pending
    DACLCH = 0x00; //left data upper byte
    DACLCH = 0x00; //left data lower byte
    DACRCH = 0x00; //right data upper byte
    DACRCH = 0x00; //right data lower byte
}
```

Polling the pending in DMA mode:

```
While(1)
{
    while(!(DACCON & BIT(7))); //wait pending
    DACCON |= BIT(6); //clear pending
    DACPTR = 0x40; //dma start address upper byte
    DACPTR = 0x16; //dma start address lower byte
    DACCNT = 7; //7 samples to left and 7 samples to right in a DMA process
    //kick start DMA
}
```

Chapter 15 Power Gate and LVD

15.1 Power Gate

AX208 integrate three power gates:

Name	Purpose	Driving (mA)
PGATE0	For SPI Flash	50
PGATE1	For LCD back light	50
PGATE2	For SDC	100

SFR 15-1 PGCON

PGCON (0xD1)

Power Gate control register

	7	6	5	4	3	2	1	0
Name	-	-	-	PG1TSEL	PG1ENSEL	PG2EN	PG1EN	PG0EN
Reset	-	-	-	0	0	0	0	0
POR	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
4	PG1TSEL	**PGATE1 trigger timer select** 0: Timer1 1: Timer2
3	PG1ENSEL	**PGATE1 output enable control select, active when PG1EN = 1.** 0: Control by PG1EN 1: Control by timer PWM
2	PG2EN	**PGATE2 enable** 0: Disable 1: Enable
1	PG1EN	**PGATE1 enable** 0: Disable 1: Enable
0	PG0EN	**PGATE0 enable** 0: Disable 1: Enable

15.2 LVD

SFR 15-2 LVDCON

LVDCON (0xBF)

LVD control register

	7	6	5	4	3	2	1	0
Name	LVDIF	LVDINTEN	LVDRSTEN	-	LVD_LV		LVDOE	LVDEN
Reset	0	0	0	-	0	0	0	0
POR	0	0	0	-	0	0	0	0
Access	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Bit Number	Bit Mnemonic	Description
7	LVDIF	**LVD interrupt pending bit.** 0: When LVD threshold not detect. Cleared by writing '0' to it 1: When LVD threshold is detected
6	LVDINTEN	**LVD interrupt enable bit.** 0: LVD interrupt is disabled 1: LVD interrupt is enabled
5	LVDRSTEN	**LVD Reset enable bit.** 0: LVD Reset is disabled 1: LVD is enabled
3-2	LVD_LV	**LVD voltage detect select** 00: 2.2V 01: 2.3V 10: 2.5V 11: 2.7V
1	LVDOE	**LVD output enable bit.** 0: LVD output is enabled 1: LVD output is disabled
0	LVDEN	**LVD enable bit** 0: LVD is enabled 1: LVD is disabled

Chapter 16 Characteristics

16.1 LDO for LCD DC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Vin	Input voltage	-	3.3.	-	V	
Vout	Output voltage	-	2.6/2.8/3.0	-	V	Output 3bit trim (default value = 3'100, Vout = 2.8V)
Ileak	Leak current	0	-		uA	Disable
Iout	Output current	-	-	20	mA	

16.2 Power Gate for FLASH DC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Vin	Input voltage	3.2	3.3.	3.4	V	
Iout	Output current	-	-	50	mA	
Vdrop	Output voltage drop	-	-	0.3	V	50 mA driving

16.3 Power Gate for SDC DC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Vin	Input voltage	3.2	3.3.	3.4	V	
Iout	Output current	-	-	100	mA	
Vdrop	Output voltage drop	-	-	0.3	V	100 mA driving

16.4 Power Gate for LCD DC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Vin	Input voltage	3.2	3.3	3.4	V	
Iout	Output current	-	-	50	mA	
Vdrop	Output voltage drop	-	-	0.3	V	50 mA driving

16.5 XOSC DC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Fin	Frequency input		32		KHz	
Fout	Frequency output	-	32	-	KHz	
I	current	0			uA	Disable

16.6 PLL DC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Fin	Frequency input		32/1000		KHz	Fin select 32k or 1M
Fout	Frequency output	-	60/80/96	-	MHz	
I	current	0			uA	Disable

16.7 I/O Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VIL	Low-Level input voltage	-	-	30% * VDDIO	V	VDDIO = 3.3V
VIH	High-level input voltage	70% * VDDIO	-	-	V	VDDIO = 3.3V
RPUP	Internal pull-up resister		10		KΩ	
RPDN	Internal pull-down resister		10		KΩ	

16.8 Audio DAC Parameters

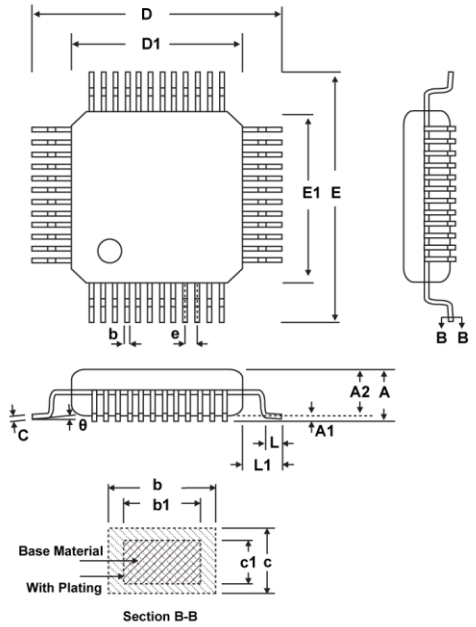
Sym	Characteristics	Min	Typ	Max	Unit	Conditions
SNR		-	53	-	dB	20k low pass fillter + Aweighted fillter, 100K loading
SNDR		-	52	-	dB	

16.9 SARADC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
SNR		-	33	-	dB	MIC IN with X48 internal amplifier
THD+N		-	-55	-	dB	

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
SNR		-	40	-	dB	MIC IN with X48 external amplifier
THD+N		-	-58	-	dB	

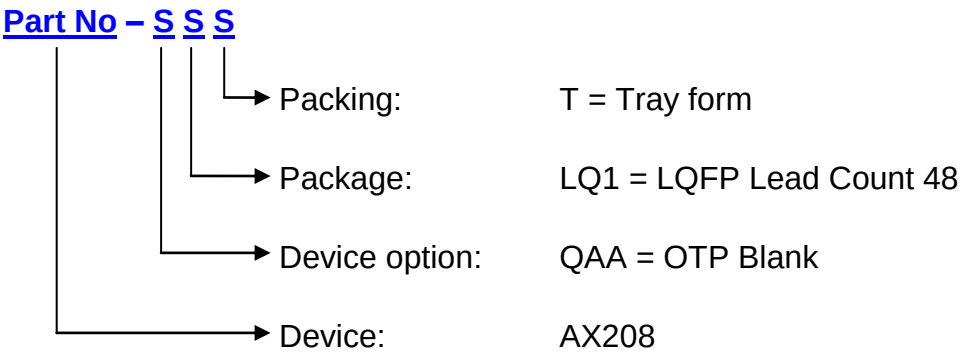
Chapter 17 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	___	___	1.60
A1	0.10	___	0.20
A2	1.30	1.40	1.50
b	0.20	___	0.25
b1	0.20	___	0.30
c	0.107	___	0.197
c1	0.107	___	0.147
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e	0.50 BSC		
L	0.50	___	0.70
L1	1.00 BSC		
θ	0	___	7°

LQFP48 (7mm x 7mm)

Chapter 18 Ordering Code



Ordering Code	Brief Description
AX208-QAALQ1T	**SOP14**

Please contact sales office (sales@appotech.com) for ordering procedures.

Appendix I Revision History

Date	***Version***	***Comment***	***Revised by***
2011.01.06	1.0.0	First release version	Liu Zhuzhan
2011.01.14	1.0.1	Revised version	Liu Zhuzhan