Interfacing the Intel® PXA27x Processor Family to 802.11 Companion Chips

Application Note

Document Order Number: 280009-001

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1.0 Introduction

The wireless industry has expressed significant interest in providing WLAN capability for handheld devices and mobile phones. The Intel® PXA27x Processor Family (PXA27x processor) offers many peripheral interfaces that allow for a WLAN connection without sacrificing functionality commonly used in handheld devices and mobile phones.

Common interfaces available for connecting WLAN to the PXA27x processor include:

- CF (Compact flash)
- SDIO (Secure Digital* I/O)
- USB (Universal Serial Bus)
- SSP (Synchronous Serial Port)
- MSL (Mobile Scalable Link)
- VLIO (Variable Latency I/O)

This document addresses the trade-offs that designers must be consider when selecting the optimal interface for connecting Wi-Fi companion chips to the PXA27x processor such as bus utilization and I/O power.

Designers must also consider power and performance (or bus/controller utilization) when choosing an optimal interface. Throughout this application note, the lowest possible power mode for an operating system going into idle mode is referred to as *OS idle*. PXA27x-specific power modes are referred to by the power-mode name followed by the word mode (that is, *standby mode* refers to the PXA27x standby power mode). The standby mode is the lowest PXA27x power mode that can be considered for OS idle. Some companion chips may not be able to use some of the interfaces described in this application note, instead having to go into standby during OS idle because standby requires an external wake-up source.

Power consumption from a WLAN solution (baseband, transceiver, and power amplifier) can vary greatly across vendors. Power consumption also depends on such factors as operating mode, distance from access point, and network traffic moving across the access point. Choosing an interface with the lowest possible IO voltage ranges (from 1.8 to 3.3 volts) can also result in power savings, depending on the interface.

2.0 Related Documents

Table 1 lists available PXA27x processor supplemental documentation. Contact an Intel representative for the latest version of Intel documents without order numbers.

Table 1. Supplemental Documentation (Sheet 1 of 2)

Title
Intel® PXA27x Processor Family Developer's Manual (Order No. 280000)
Intel® PXA27x Processor Family Design Guide (Order No. 280001)
Intel® PXA27x Processor Family Electrical, Mechanical, and Thermal Specification (Order No. 280002)

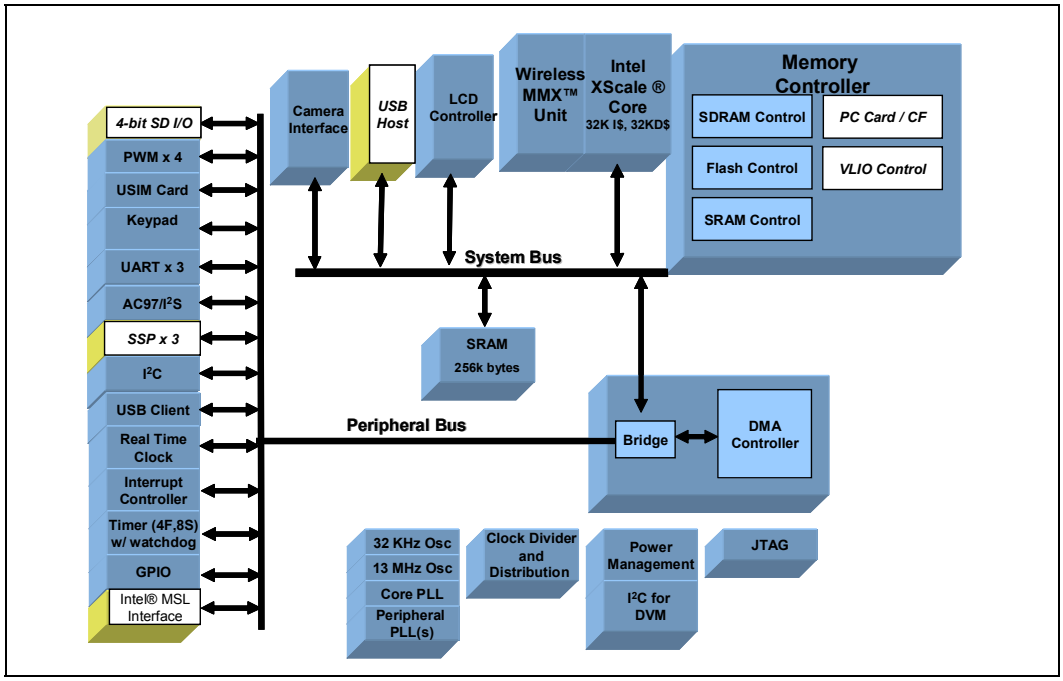
Table 1. Supplemental Documentation (Sheet 2 of 2)

Title
Intel® PXA270 Processor Electrical, Mechanical, and Thermal Specification (Order No. 280003)
Mobile Scalable Link Specification
CF+ and CompactFlash Specification Revision 1.4
Universal Serial Bus Specification Revision 1.1
SD Memory Card Specification Version 1.0
SDIO Card Specification Version 1.0 (Draft 4)

3.0 System Overview

Figure 1 is a block diagram of the PXA27x processor. White blocks with text in italics indicate controllers commonly used for interfacing to Wi-Fi companion chips. As shown in Figure 1 the USB host and memory controller interface directly to the PXA27x internal system bus. The Intel® MSL interface, SDIO and SSP controller interfaces use the peripheral bus before data is transferred to the system bus.

Figure 1. Intel® PXA27x Family Processor Block Diagram



4.0 System Considerations and Power/Performance Trade-Off

Information in this section describes the potential trade-offs when selecting the optimal interface for connecting Wi-Fi companion chips to the PXA27x processor. See Section 5.0 for general power considerations.

4.1 PC Card / Compact Flash

When interfacing to the memory controller, the Wi-Fi companion chip must have an external signal connecting to a GPIO input signal to wake up the PXA27x processor while in standby mode.

PC Card / CF specifies the I/O voltage to be either 3.3V or 5.0V. The PXA27x processor supports VCC_MEM (I/O voltage for CF) at 1.8V, 2.5V, and 3.3V. Therefore, 3.3V must be used to comply with the CF specification.

The trade-off occurs now for power versus cost (real estate and expense). The following is a list of options interfacing CF to the PXA27x memory controller:

- To reduce I/O power during transfers to other devices on the memory bus, VCC_MEM can be set to 1.8V. Setting VCC_MEM to 1.8V requires external voltage translators to support CF at 3.3 volts.
- Otherwise, if the 802.11 companion chip supports 1.8V CF I/O, voltage translators are not required if VCC_MEM equals 1.8V. This results in power savings during data transfers through the CF interface.

The following is an example of memory bus performance calculations that can be used (and modified) to determine if using the Wi-Fi companion chip on the CF interface will have any impact to the design. The memory bus utilization calculations are based on transfers to/from 32-bit SDRAM. To calculate the reduced throughput, use...

- tfr1 (transfer rate 1) = 11 Mbps maximum 802.11b transfer rate (actual data rate is less)
- tfr2 = 32 Mbps maximum best case CF (I/O transfers, with a maximum wait of 423ns)

  The memory bus is shared between the CF and SDRAM memory. Therefore, transfers to CF devices reduce potential throughput to the SDRAM. The estimated calculation for reduced throughput to SDRAM is as follows:
- bu1 (bus utilization 1) = tf1/tf2 = 11 / 32 = 34.3% maximum bus utilization of the CF controller with Wi-Fi.
- tfr3 = 1422 Mbps maximum SDRAM data rate (SDCLKx = 100MHz @ 32 bits, 18 SDCLKx per 8-beat burst, assuming pages always closed)
- tfr4 = tfr3 * bu1 = 1422 Mbps * 34.3% = 487.9 Mbps (61 MB/s)
- tfr5 = tfr3 - tfr4 = 934.5 Mbps maximum available SDRAM transfer rate with Wi-Fi on CF

  LCD refresh is one example designers must calculate as part of the required data rate if the LCD frame buffer resides within SDRAM
- tfr6 = 295 Mbps data rate for VGA(640x480) x 16 bits x 60 fps
- bu2 = (tfr4 + tfr6) / tfr3 = (487.9 Mbps + 295 Mbps) / 1422 Mbps = 55% maximum memory controller utilization with VGA and Wi-Fi interfacing to CF.

System bus utilization is considered nominal between interfaces because all data must pass through the system bus no matter which interface connects to the Wi-Fi companion chip.

4.2 SDIO

Designers can create a system using a PXA27x processor with either 3.0 or 3.3V on VCC_IO. If the Wi-Fi companion chip uses SDIO to interface to the PXA27x processor, VCC_IO must be set to 3.3V to meet the SD/SDIO voltage requirements of 3.1 - 3.5V V_{ih}. If the Wi-Fi companion chip V_{oh} (max) exceeds VCC_IO, use a quick switch to prevent exceeding the V_{ih} (max) PXA27x requirements.

The data-transfer rates for SDIO can be up to 78 Mbps. This transfer rate is not necessarily a problem if only one SDIO interface is being used to support Wi-Fi. However, if the PXA27x processor is designed in a system using two different SDIO cards where one is the Wi-Fi, the maximum transfer rate of the Wi-Fi might not be attainable, depending on possible coexisting transfers to the other SDIO card. Systems must be configured to use SPI mode when supporting two different SDIO cards. See the *Intel® PXA27x Processor Family Design Guide* for additional information how to interface to SDIO cards.

4.3 USB Host

USB interfaces have become very popular. Wi-Fi companion chips are available with USB as an option for interfacing to the Wi-Fi baseband. The PXA27x processor provides a dedicated power domain for USB host and client separating them from all other peripherals. However, designers must evaluate some performance considerations.

The PXA27x VCC_USB voltage domain supports either 3.0V or 3.3V nominal. The USB power supply must be +5.0 V (per the USB specification), yet the PXA27x processor does not have 5.0V-tolerant inputs. An external device is needed to interface the USBHPEN0 and USBHPWR0 pins to the power supply and over-current detection circuits. See the *Intel® PXA27x Processor Family Design Guide* for additional information.

Regarding performance, the USB maximum transfer rate for version 1.1 is 12 Mbps. The USB effective data rate can range from anywhere from 3.2 Mbps to 8.8 Mbps. Actual data rate varies depending on system implementation and the OS ability to maximize data transfers. Using the best-case estimated data rate and assuming no additional loss of data rate due to the operating system, the maximum possible transfer is 80% of the 11 Mbps 802.11b potential.

tfrp (transfer rate percentage) = 8.8 Mbps / 11 Mbps = 80%

The USB host controller has direct access to the system bus. System bus utilization is considered nominal between different interfaces because all data must pass through the system bus no matter which interface connects to the Wi-Fi companion chip. See the section entitled “Latency of Accesses on the System Bus” in the System Bus Arbiter chapter of the *Intel® PXA27x Processor Family Developer’s Manual* for additional information on how to optimize performance on the system bus.

4.4 SSP (Using SPI Protocol)

The PXA27x SSP I/O is powered by VCC_IO, which can be designed with either 3.0V or 3.3V. Most SPI devices use 3.3V for the I/O voltage. Therefore, use 3.3V to comply with the SPI specifications, which requires all other devices on the VCC_IO run at 3.3V, consuming maximum I/O power.

SSP maximum transfer rate is 13 Mbps. The effective data rate is approximately 80%. Therefore, the maximum possible transfer rate for the Wi-Fi device interface using SSP is 10.4 Mbps (13Mbps * 0.8), down from the original 11 Mbps possible transfer rate.

4.5 MSL

The MSL interface has its own dedicated power domain (VCC_BB) of 1.8V, 2.5V, or 3.3V nominal supplies. Having the dedicated power domain does eliminate the requirement for other devices in the system to match the same I/O voltage used on the Wi-Fi companion chip interfacing to MSL. The recommendation for greater power savings is to use 1.8V VCC_BB during data transfers.

The MSL transfer rate per link can be up to 192 Mbps at 48 MHz using a 4-bit bus. The single-bit MSL interface transfer rate can be up to 48 Mbps. Systems requiring CF support in addition to Wi-Fi interfacing to MSL must use the single bit MSL interface. See the MSL chapter in the *Intel® PXA27x Processor Family Design Guide* for additional information.

The MSL controller connects to the peripheral bus similar to SDIO and SSP controllers. Once data is transferred through the peripheral bus to system bus bridge, it contends only with requests made on the system bus. Performance improvement on the peripheral bus is realized by using the bus split transactions, DPCSR[BRGSPLIT], if programmed I/O is used over the DMA bridge. See the DMA chapter in the *Intel® PXA27x Processor Family Developer's Manual* for additional information.

System bus utilization is consider nominal between different interfaces because all data must pass through the system bus no matter which interface connects to the Wi-Fi companion chip. See the section entitled “Latency of Accesses on the System Bus” in the System Bus Arbiter chapter of the *Intel® PXA27x Processor Family Developer's Manual* for additional information on how to optimize performance on the system bus.

Another consideration when using MSL is that Intel basebands also use the MSL interface. MSL 1.0 does not.

4.6 VLIO

When interfacing to the memory controller, the Wi-Fi companion chip must have an external signal connecting to a GPIO input signal to wake up the PXA27x processor while in standby mode.

All system memory connections to PXA27x processor share the same VCC_MEM power domain. When interfacing memory using the VLIO interface without a voltage level shifter, the I/O voltage must be the same as the system memory such as flash and SDRAM. VCC_MEM has the flexibility to accept 1.8V, 2.5V, and 3.3V.

Memory controller utilization calculations are similar to those shown in Section 4.1. Note that VLIO wait signals have no maximum requirements; therefore, VLIO with excessive wait cycles have a significant impact on the SDRAM data rate.

System bus utilization is considered nominal between interfaces because all data must pass through the system bus no matter which interface connects to the Wi-Fi companion chip.

5.0 Power Considerations

Use standby mode while in OS idle for greater power savings. All processor activity stops in standby mode, except for the real-time clock (RTC), some OST, and the clocks and power manager. Because internal activity has stopped, recovery from standby mode must be through an external or RTC event. If the Wi-Fi can wake up the PXA27x processor using an external source, consider standby mode to achieve lowest power during OS idle. Otherwise, the system can be designed such that the Wi-Fi would not be required to wake up the PXA27x processor, thus allowing standby mode to be used during OS idle.

Systems requiring Wi-Fi to wake up the PXA27x processor but do not have an external wake-up signal must use idle mode for OS idle. 13M / idle is the lowest possible idle mode using the least amount of power. Ensure that the peripheral can still operate at 13 MHz or can supply its own clock into the PXA27x processor. Otherwise, the lowest idle mode depends on the peripheral chosen and the lowest clock speed that allows it to continue to operate.

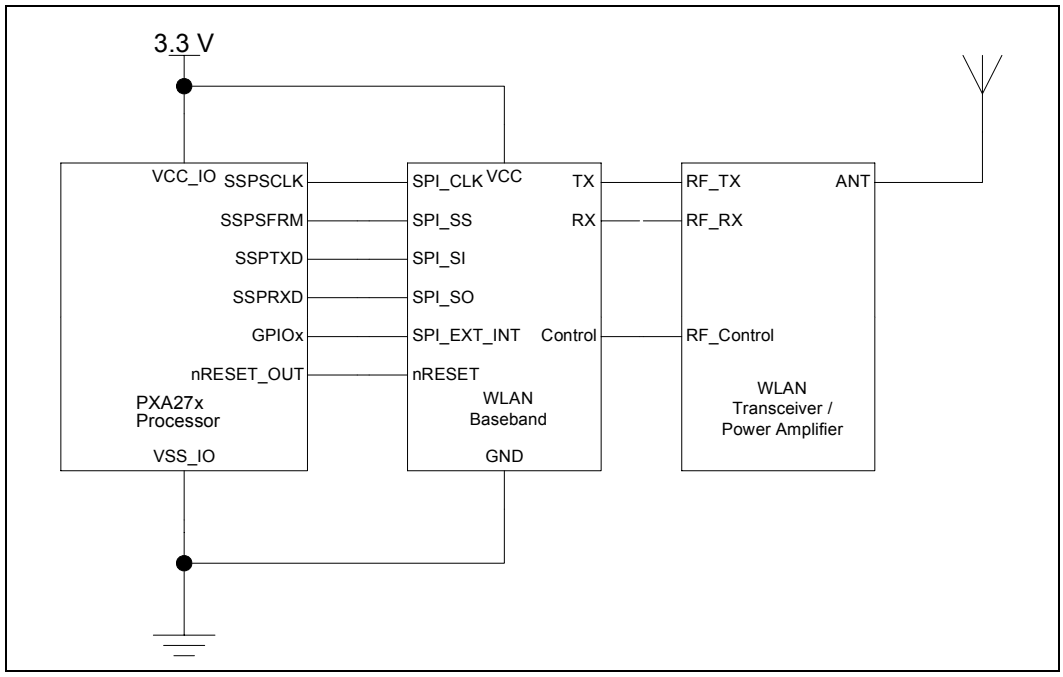
For maximum power savings, the Wi-Fi should exist on its own independent power domain, thus enabling the Wi-Fi system to be powered down completely when it is not in use. Having WiFi on its own domain is ideal when a communicator is in standby awaiting a call and no transfers are expected through the Wi-Fi. A design allowing users to turn on or off the Wi-Fi system could take advantage of the independent power domain by removing all power when the users has turned off Wi-Fi.

6.0 Example Schematic

The schematic in Figure 2 shows interfacing a PXA27x processor to an Wi-Fi companion chip using the SPI interface. The PXA27x symbol shown in Figure 2 shows only a subset of signals that are needed to interface to the Wi-Fi companion chip.

The signal SPI_EXT_INT must be connected to a GPIOx signal that can wake up the PXA27x processor. This would allow PXA27x to go into standby mode and be awakened from an external source. The nRESET_OUT signal holds the Wi-Fi companion chips in reset until the PXA27x processor has powered up and begun fetching instructions.

Figure 2. Intel® PXA27x Family Processor Connecting to an 802.11 Companion Chip



7.0 802.11 Companion Chips

This section lists different vendors who offer low-power Wi-Fi companion chips (at the time of this writing) that are compatible with the PXA27x processor. Because specifications for external components are subject to change, it is the engineer's responsibility to confirm that components used from this list or the bill of materials supplied by either Intel reference or development platforms meet the specifications listed in the latest release of the PXA27x processor EMTS.

However, data is not yet available on the companion chips listed below actually working with the PXA27x processor family.

Table 2. 802.11 Companion Chips

Manufacturers
Agere Systems Inc.
Philips Semiconductor
SyChip Inc.

8.0 Conclusion

The PXA27x processor offers flexible Wi-Fi connections without sacrificing the functionality of other devices commonly used in mobile phones. Power and performance are factors that play a significant role when choosing an optimal interface. The PXA27x processor is built around the Intel XScale® technology that optimizes high performance with minimal power consumption.

Using a PXA27x family processor to connect to 802.11 companion chips offers considerable savings in power consumption and improvement in data throughput over traditional cellular modem technologies such as GSM/GPRS and W-CDMA. Such advantages translate into less air time and lower airtime costs. While all PXA27x interfaces mentioned within this document can be used for 802.11b companion chips, compact flash, SDIO, MSL, and VLIO are more suitable for interfacing to 802.11a and 802.11g companion chips.

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