Group Meeting Report

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Bender How To https://github.com/pulp-platform/bender

What is Bender: a version management for hardware dependencies and file checklist; encoding dependencies version, arrange codefiles, and generating scripts for different EDA. **Deeply used in Pulpissimmo.**

Typical Start Workflow

1. Save *Bender.yml* in root directory (package checklist)

2. First analysis/update source code by `bender update`

3. Check dependency gplot by `bender packages` & `bender sources -f -t vivado`

4. Generating tool scripts to EDA by:
bender script vivado -t vivado   > add_files.tcl
bender script vivado-sim -t simulation   > add_files_sim.tcl

bender script vsim -t simulation   > compile.tcl

bender script verilator -t simulation   > verilate.f

5. Lock a reproducible version and submit to repo with *Bender.lock*

Save *Bender.yml* in root directory (package checklist)

```
albert@localhost:~/Works/pulpissimo> bender update -f
warning: Using config at "/home/albert/Works/pulpissimo/.bender.yml" for overrides.
    Cloning common_cells (https://github.com/pulp-platform/common_cells.git)
    Cloning apb (https://github.com/pulp-platform/apb.git)
    Cloning jtag_pulp (https://github.com/pulp-platform/jtag_pulp.g
    Cloning pulp_soc (https://github.com/pulp-platform/pulp_soc.git
    Cloning tbtools (https://github.com/pulp-platform/tbtools.git)
    Cloning tech_cells_generic (https://github.com/pulp-platform/te
    Cloning register_interface (https://github.com/pulp-platform/re
    Cloning generic_fll (https://github.com/pulp-platform/generic_F
    Cloning apb_fll_if (https://github.com/pulp-platform/apb_fll_if.
    Cloning common_verification (https://github.com/pulp-platform/c
    Cloning adv_dbg_if (https://github.com/pulp-platform/adv_dbg_if.
    Cloning apb2per (https://github.com/pulp-platform/apb2per.git)
    Cloning apb_adv_timer (https://github.com/pulp-platform/apb_adv_
    Cloning apb_interrupt_cntrl (https://github.com/pulp-platform/ap
    Cloning axi (https://github.com/pulp-platform/axi.git)
    Cloning timer_unit (https://github.com/pulp-platform/timer_unit.
    Cloning cluster_interconnect (https://github.com/pulp-platform/c
    Cloning fpnew (https://github.com/pulp-platform/cvfpu.git)
    Cloning cv32e40p (https://github.com/pulp-platform/cv32e40p.git)
    Cloning ibex (https://github.com/pulp-platform/ibex.git)
    Cloning scm (https://github.com/pulp-platform/scm.git)
    Cloning pulp_io (https://github.com/pulp-platform/pulp-io.git)
    Cloning hwpe-mac-engine (https://github.com/pulp-platform/hwpe-mac-engine.git)
    Cloning riscv-dbg (https://github.com/pulp-platform/riscv-dbg.git)
    Cloning fpu_div_sqrt_mvp (https://github.com/pulp-platform/fpu_div_sqrt_mvp.git)
    Cloning udma_uart (https://github.com/pulp-platform/udma_uart.git)
    Cloning udma_core (https://github.com/pulp-platform/udma_core.git)
    Cloning udma_i2c (https://github.com/pulp-platform/udma_i2c.git)
    Cloning udma_sdio (https://github.com/pulp-platform/udma_sdio.git)
    Cloning udma_i2s (https://github.com/pulp-platform/udma_i2s.git)
    Cloning udma_camera (https://github.com/pulp-platform/udma_camera.git)
    Cloning udma_qspi (https://github.com/pulp-platform/udma_qspi.git)
    Cloning udma_filter (https://github.com/pulp-platform/udma_filter.git)
    Cloning udma_hyper (https://github.com/pulp-platform/udma_hyper.git)
    Cloning hwpe-stream (https://github.com/pulp-platform/hwpe-stream.git)
    Cloning hwpe-ctrl (https://github.com/pulp-platform/hwpe-ctrl.git)
   Checkout tech_cells_generic (https://github.com/pulp-platform/tech_cells_generic.git)
   Checkout register_interface (https://github.com/pulp-platform/register_interface.git)
   Checkout apb_fll_if (https://github.com/pulp-platform/apb_fll_if.git)
   Checkout generic_fll (https://github.com/pulp-platform/generic_FLL.git)
   Checkout pulp_soc (https://github.com/pulp-platform/pulp_soc.git)
   Checkout tbtools (https://github.com/pulp-platform/tbtools.git)
   Checkout common_verification (https://github.com/pulp-platform/common_verification.git)
   Checkout common_cells (https://github.com/pulp-platform/common_cells.git)
   Checkout axi (https://github.com/pulp-platform/axi.git)
   Checkout hwpe-stream (https://github.com/pulp-platform/hwpe-stream.git)
   Checkout cluster_interconnect (https://github.com/pulp-platform/cluster_interconnect.git)
   Checkout scm (https://github.com/pulp-platform/scm.git)
```

If encounter Internet issue, maybe return
` *error: Dependency `***` from
`https://github.com/pulp-platform/***.git`
cannot satisfy requirement `^0.*.*` `*, pls try:
```

rm -rf .bender/git/db
bender update -f
```

Check dependency by `bender packages`

```
albert@localhost:~/Works/pulpissimo> bender packages
common_verification
tech_cells_generic
common_cells
apb axi
fpu_div_sqrt_mvp register_interface udma_core
fpnew gpio hwpe-ctrl hwpe-stream udma_camera udma_filter udma_hyper udma_i2c udma_i2s udma_qspi udma_sdio udma_uart
adv_dbg_if apb2per apb_adv_timer apb_interrupt_cntrl cluster_interconnect cv32e40p hwpe-mac-engine ibex jtag_pulp pulp_io riscv-dbg scm timer_unit
apb_fll_if generic_fll pulp_soc pulpissimo_optional_vips pulpissimo_padframe_fpga pulpissimo_padframe_rtl_sim tbtools
```

Check gplot by `bender sources -f -t vivado`

```
    "tech_cells_generic": []
},
"defines": {},
"files": [
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl/qspi_pkg.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl/udma_spim_ctrl.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl/udma_spim_reg_if.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl/udma_spim_txrx.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl/udma_spim_top.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl/udma_qspi_wrap.sv"
],
"dependencies": [
    "udma_core",
    "common_cells",
    "tech_cells_generic"
],
"version": "2.0.0"
},
{
"package": "udma_sdio",
"independent": false,
"target": "all(*, all(*))",
"include_dirs": [],
"export_incdirs": {
    "udma_sdio": [],
    "udma_core": [],
    "common_cells": [
        "/home/albert/Works/pulpissimo/.bender/git/checkouts/common_cells-bdd3ba741800de55/include"
    ],
    "tech_cells_generic": []
},
"defines": {},
"files": [
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/sdio_pkg.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/sdio_crc16.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/sdio_crc7.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/udma_sdio_reg_if.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/sdio_txrx_cmd.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/sdio_txrx_data.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/sdio_txrx.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/udma_sdio_top.sv",
    "/home/albert/Works/pulpissimo/.bender/git/checkouts/udma_sdio-137248d661f5f240/rtl/udma_sdio_wrap.sv"
],
```

<u>Generating tool scripts</u> to EDA by:
```

# bender script <format> -t <target> > <filename>
bender script vivado -t vivado          > add_files.tcl
bender script vivado-sim -t simulation  > add_files_sim.tcl


bender script vsim   -t simulation      > compile.tcl


bender script verilator -t simulation   > verilate.f
```

! Remind to use `bender update` before generating scripts to lock the dependencies version

<u>For Vivado:</u>
```

bender script vivado -t vivado          > add_files.tcl
bender script vivado-sim -t simulation  > add_files_sim.tcl

# in Vivado Console, to add/update files
source add_files.tcl
# in Vivado Source Flow, to add/update files
source add_files_sim.tcl
```

Showcase

```
723    set_property include_dirs [list \
731        $ROOT/.bender/git/checkouts/cv32e40p-703290f15a6e8974/bhv \
732        $ROOT/.bender/git/checkouts/cv32e40p-703290f15a6e8974/rtl/include \
733        $ROOT/.bender/git/checkouts/hwpe-ctrl-e547e392627a22fd/rtl \
734        $ROOT/.bender/git/checkouts/hwpe-mac-engine-db1193857e43071d/rtl \
735        $ROOT/.bender/git/checkouts/hwpe-stream-1004699fca3c87e1/rtl \
736        $ROOT/.bender/git/checkouts/ibex-3d636992cd289cea/rtl \
737        $ROOT/.bender/git/checkouts/ibex-3d636992cd289cea/vendor/lowrisc_ip/ip/pri
738        $ROOT/.bender/git/checkouts/pulp_io-8557a8d559d27a25/inc \
739        $ROOT/.bender/git/checkouts/pulp_soc-b7e7c62781de8fd8/rtl/include \
740        $ROOT/.bender/git/checkouts/register_interface-d81701e89d22e79e/include \
741        $ROOT/.bender/git/checkouts/udma_core-55b32791e708906d/rtl \
742        $ROOT/.bender/git/checkouts/udma_core-55b32791e708906d/rtl/common \
743        $ROOT/.bender/git/checkouts/udma_hyper-25d0d36a772cf85e/udma-hyperbus/src
744        $ROOT/.bender/git/checkouts/udma_i2c-a768c09ae26d9daa/rtl \
745        $ROOT/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl \
746        $ROOT/hw/includes \
747        $ROOT/hw/padframe/pulpissimo_padframe_fpga_autogen/include \
748        $ROOT/hw/padframe/pulpissimo_padframe_rtl_sim_autogen/include \
749    ] [current_fileset -simset]
750
751  ∨ set_property verilog_define [list \
752        TARGET_FPGA \
753        TARGET_SYNTHESIS \
754        TARGET_VIVADO \
755        TARGET_XILINX \
756    ] [current_fileset]
757
758  ∨ set_property verilog_define [list \
759        TARGET_FPGA \
760        TARGET_SYNTHESIS \
761        TARGET_VIVADO \
762        TARGET_XILINX \
763    ] [current_fileset -simset]
764
```

```
830    ] [current_fileset -simset]
813        $ROOT/.bender/git/checkouts/cv32e40p-703290f15a6e8974/rtl/include \
814        $ROOT/.bender/git/checkouts/hwpe-ctrl-e547e392627a22fd/rtl \
815        $ROOT/.bender/git/checkouts/hwpe-mac-engine-db1193857e43071d/rtl \
816        $ROOT/.bender/git/checkouts/hwpe-stream-1004699fca3c87e1/rtl \
817        $ROOT/.bender/git/checkouts/ibex-3d636992cd289cea/rtl \
818        $ROOT/.bender/git/checkouts/ibex-3d636992cd289cea/vendor/lowrisc_ip/ip/prim/rtl \
819        $ROOT/.bender/git/checkouts/pulp_io-8557a8d559d27a25/inc \
820        $ROOT/.bender/git/checkouts/pulp_soc-b7e7c62781de8fd8/rtl/include \
821        $ROOT/.bender/git/checkouts/register_interface-d81701e89d22e79e/include \
822        $ROOT/.bender/git/checkouts/udma_core-55b32791e708906d/rtl \
823        $ROOT/.bender/git/checkouts/udma_core-55b32791e708906d/rtl/common \
824        $ROOT/.bender/git/checkouts/udma_hyper-25d0d36a772cf85e/udma-hyperbus/src \
825        $ROOT/.bender/git/checkouts/udma_i2c-a768c09ae26d9daa/rtl \
826        $ROOT/.bender/git/checkouts/udma_qspi-cdef62325988d740/rtl \
827        $ROOT/hw/includes \
828        $ROOT/hw/padframe/pulpissimo_padframe_fpga_autogen/include \
829        $ROOT/hw/padframe/pulpissimo_padframe_rtl_sim_autogen/include \
830    ] [current_fileset -simset]
831
832    set_property verilog_define [list \
833        TARGET_FPGA \
834        TARGET_SIMULATION \
835        TARGET_VIVADO \
836        TARGET_XILINX \
837    ] [current_fileset]
838
839    set_property verilog_define [list \
840        TARGET_FPGA \
841        TARGET_SIMULATION \
842        TARGET_VIVADO \
843        TARGET_XILINX \
844    ] [current_fileset -simset]
845
846
```

Developing Process

1. Developing in separate ip repo `axi/` or `gpio/`

2. Tag and push (must vX.Y.Z):
git tag -a v1.12.0 -m "axi: release 1.12.0"
git push origin v1.12.0

3. Edit top `Bender.yml` and git push in soc repo:
dependencies:
  axi:
    git: "git@github.com:your-org/axi.git"
    version: "=1.12.0"   # accurate v1.12.0
    # or "~1.12"   # allow 1.12 or near more
    # or ">=1.11,<2.0"   # allow 1.x newest，allow semver

5. `bender update` and `bender checkout`

Localization dependency

```
dependencies:
  common_cells:              { git: "https://github.com/pulp-platform/common_cells.git",       version: 1.21.0 }
  apb:                       { git: "https://github.com/pulp-platform/apb.git",                 version: 0.2.4 }
  jtag_pulp:                 { git: "https://github.com/pulp-platform/jtag_pulp.git",           version: 0.2.0 }
  pulp_soc:                  { git: "https://github.com/pulp-platform/pulp_soc.git",            version: 5.0.1 }
  tbtools:                   { git: "https://github.com/pulp-platform/tbtools.git",             version: 0.2.1 }
  tech_cells_generic:        { git: "https://github.com/pulp-platform/tech_cells_generic.git", version: 0.2.3 }
  pulpissimo_padframe_rtl_sim: { path: "hw/padframe/pulpissimo_padframe_rtl_sim_autogen" }
  pulpissimo_padframe_fpga:  { path: "hw/padframe/pulpissimo_padframe_fpga_autogen" }
  register_interface:        { git: "https://github.com/pulp-platform/register_interface.git", version: 0.4.1 }
  generic_FLL:               { git: "https://github.com/pulp-platform/generic_FLL.git",         version: 0.2.0 }
  apb_fll_if:                { git: "https://github.com/pulp-platform/apb_fll_if.git",          version: 0.2.1 }
```

- Change to GitLab in order to private version management and developing

Next Week

1. Continue Localization dependency
2. Environment Configuration
3. Bender