Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Jan. 4, 14:00

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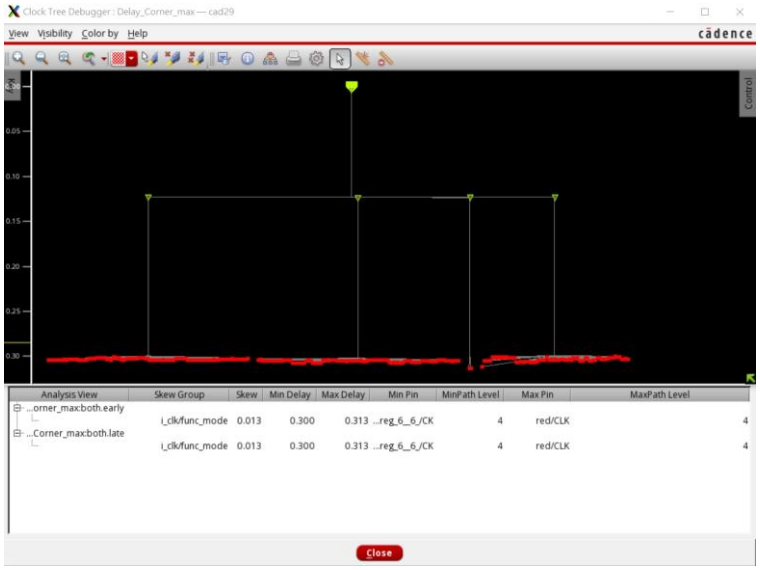
Student Name: 陳昱仁

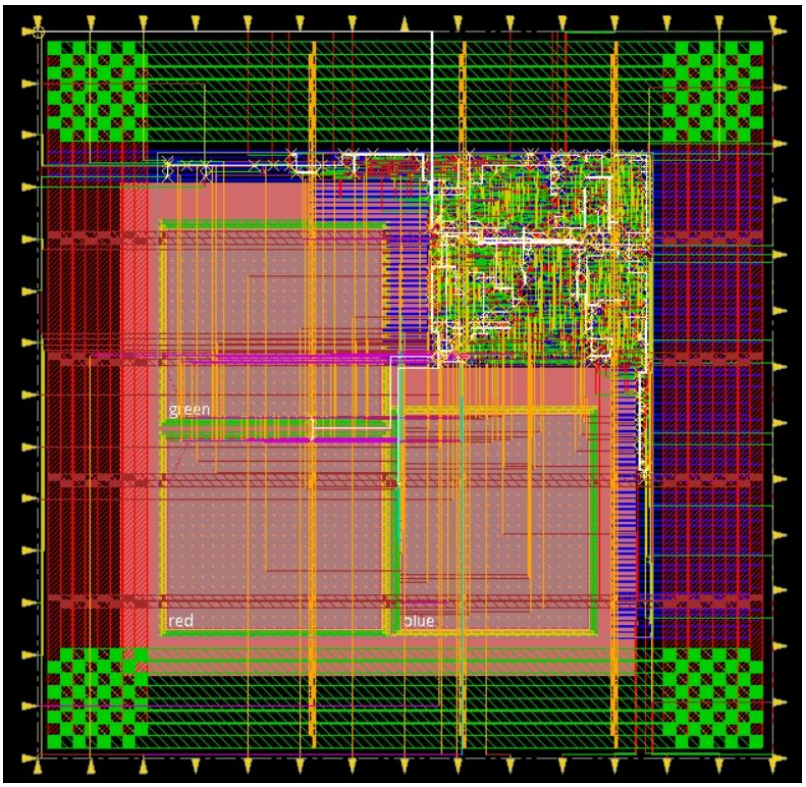
Questions and Discussion

1. Fill in the blanks

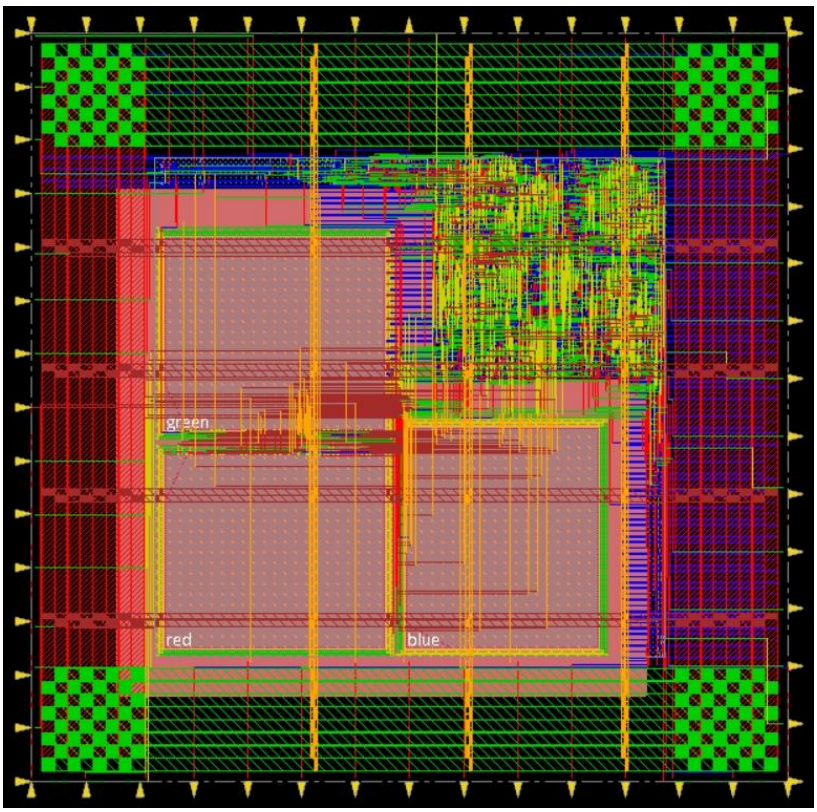
Physical category (10%)		
Design Stage	Description	Value
P&R	Number of DRC violation (ex: 0) (Verify -> Verify Geometry…)	**0**
	Number of LVS violation (ex: 0) (Verify -> Verify Connectivity…)	**0**
	Core area (um^2)	**105143.75**
	Die area (um^2)	**234901.30**
Prost-layout Gate-level Seimulation	Cycle time for Post-layout Simulation (ex. 10ns)	**6.0ns**
N/A	Follow your design in HW3? (If not, write down the student ID of the designer)	**Yes**

2. Attach the snapshot of CCOpt Clock Tree Debugger result, and show the routing result in the layout (10%).





3. Attach the snapshot of your final layout **after adding core filler** (10%).



4. Show one of the critical paths (reg2reg) after post-route optimization (5%)

```
Path 1: MET Setup Check with Pin sorter_sort_G_r_reg_7__2_/CK
Endpoint:   sorter_sort_G_r_reg_7__2_/D (v) checked with  leading edge of 'i_
clk'
Beginpoint: green/Q[5]                  (^) triggered by  leading edge of 'i_
clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.298
- Setup                         0.235
+ Phase Shift                   6.000
+ CPPR Adjustment               0.000
= Required Time                 6.063
- Arrival Time                  5.634
= Slack Time                    0.429
     Clock Rise Edge                     0.000
     + Source Insertion Delay           -0.304
     = Beginpoint Arrival Time          -0.304
     Timing Path:
     +-------------------------------------------------------------------------------------+
     |            Pin             | Edge |  Net   |    Cell    | Delay | Arrival | Required |
     |                            |      |        |            |       |  Time   |   Time   |
     |----------------------------+------+--------+------------+-------+---------+----------|
     | i_clk                      |  ^   | i_clk  |            |       |  -0.304 |    0.125 |
     | CTS_ccl_a_buf_00016/A      |  ^   | i_clk  | CLKBUFX16  | 0.004 |  -0.300 |    0.129 |
     | CTS_ccl_a_buf_00016/Y      |  ^   | CTS_3  | CLKBUFX16  | 0.117 |  -0.183 |    0.246 |
     | CTS_ccl_a_buf_00011/A      |  ^   | CTS_3  | CLKBUFX16  | 0.001 |  -0.182 |    0.247 |
     | CTS_ccl_a_buf_00011/Y      |  ^   | CTS_1  | CLKBUFX16  | 0.177 |  -0.005 |    0.424 |
     | green/CLK                  |  ^   | CTS_1  | sram_256x8 | 0.012 |   0.007 |    0.436 |
     | green/Q[5]                 |  ^   | q_G[5] | sram_256x8 | 1.985 |   1.992 |    2.421 |
     | U1850/A                    |  ^   | q_G[5] | CLKINVX1   | 0.002 |   1.994 |    2.423 |
     | U1850/Y                    |  v   | n1749  | CLKINVX1   | 0.245 |   2.238 |    2.667 |
     | U1938/A                    |  v   | n1749  | NOR2X1     | 0.000 |   2.239 |    2.668 |
     | U1938/Y                    |  ^   | n1000  | NOR2X1     | 0.612 |   2.850 |    3.279 |
     | U1941/A                    |  ^   | n1000  | CLKINVX1   | 0.000 |   2.851 |    3.280 |
     | U1941/Y                    |  v   | n2219  | CLKINVX1   | 0.461 |   3.312 |    3.741 |
     | U1942/A1                   |  v   | n2219  | AO22X1     | 0.000 |   3.312 |    3.741 |
     | U1942/Y                    |  v   | n1005  | AO22X1     | 0.389 |   3.701 |    4.130 |
     | U1943/B0                   |  v   | n1005  | AOI21X1    | 0.000 |   3.701 |    4.130 |
     | U1943/Y                    |  ^   | n1009  | AOI21X1    | 0.132 |   3.833 |    4.262 |
     | FE_RC_2_0/B0               |  ^   | n1009  | OAI2BB2XL  | 0.000 |   3.833 |    4.262 |
     | FE_RC_2_0/Y                |  v   | n1010  | OAI2BB2XL  | 0.128 |   3.961 |    4.390 |
     | U1662/A0                   |  v   | n1010  | OAI21XL    | 0.000 |   3.961 |    4.390 |
     | U1662/Y                    |  ^   | n1584  | OAI21XL    | 0.260 |   4.221 |    4.650 |
     | U1266/B0                   |  ^   | n1584  | OA21XL     | 0.000 |   4.221 |    4.650 |
     | U1266/Y                    |  ^   | n2189  | OA21XL     | 0.448 |   4.669 |    5.098 |
     | U1264/A                    |  ^   | n2189  | CLKINVX1   | 0.000 |   4.669 |    5.098 |
     | U1264/Y                    |  v   | n2210  | CLKINVX1   | 0.339 |   5.008 |    5.437 |
     | U1960/A                    |  v   | n2210  | NAND2X2    | 0.000 |   5.008 |    5.437 |
     | U1960/Y                    |  ^   | n2178  | NAND2X2    | 0.200 |   5.208 |    5.637 |
     | U1169/A                    |  ^   | n2178  | NOR2XL     | 0.000 |   5.208 |    5.637 |
     | U1169/Y                    |  v   | n2179  | NOR2XL     | 0.100 |   5.308 |    5.737 |
     | U1841/B0                   |  v   | n2179  | AOI211X1   | 0.000 |   5.308 |    5.737 |
     | U1841/Y                    |  ^   | n2181  | AOI211X1   | 0.194 |   5.502 |    5.931 |
     | U2610/B0                   |  ^   | n2181  | OAI21XL    | 0.000 |   5.502 |    5.931 |
     | U2610/Y                    |  v   | n876   | OAI21XL    | 0.132 |   5.634 |    6.063 |
     | sorter_sort_G_r_reg_7__2_/D |  v   | n876   | DFFQX1     | 0.000 |   5.634 |    6.063 |
     +-------------------------------------------------------------------------------------+
```

5. Attach the snapshot of timing report for setup time with no timing violation (post-route) (5%).

```
------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.134  |  0.550  |  2.531  |  0.134  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   452   |   322   |   104   |   26    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)       |     0       |      0 (0)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 73.354%
Total number of glitch violations: 0
```

6. Attach the snapshot of timing report for hold time with no timing violation (post-route) (5%).

```
------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.592  |  0.592  |  3.001  |  4.127  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   452   |   322   |   104   |   26    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 73.354%
------------------------------------------------------------
```

7. Attach the snapshot of DRC checking after routing (5%).

```
innovus 11> verify_drc
 *** Starting Verify DRC (MEM: 1684.4) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 163.200 163.200} 1 of 9
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {163.200 0.000 326.400 163.200} 2 of 9
  VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {326.400 0.000 487.600 163.200} 3 of 9
  VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 163.200 163.200 326.400} 4 of 9
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {163.200 163.200 326.400 326.400} 5 of 9
  VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {326.400 163.200 487.600 326.400} 6 of 9
  VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 326.400 163.200 481.750} 7 of 9
  VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {163.200 326.400 326.400 481.750} 8 of 9
  VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {326.400 326.400 487.600 481.750} 9 of 9
  VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.5  ELAPSED TIME: 1.00  MEM: 1.0M) ***
```

8. Attach the snapshot of LVS checking after routing (5%).

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Thu Dec 30 22:21:19 2021

Design Name: ipdc
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (487.6000, 481.7500)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Thu Dec 30 22:21:19 2021
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.000M)
```

9. Attach the snapshot of final area result (5%).

```
************************* Analyze Floorplan **************************
    Die Area(um^2)              : 234901.30
    Core Area(um^2)             : 105143.75
    Chip Density (Counting Std Cells and MACROs and IOs): 34.060%
    Core Density (Counting Std Cells and MACROs): 76.093%
    Average utilization         : 100.000%
    Number of instance(s)       : 3324
    Number of Macro(s)          : 3
    Number of IO Pin(s)         : 59
    Number of Power Domain(s) : 0
************************* Estimation Results *************************
**********************************************************************
```