

Computer-Aided VLSI System Design
Midterm Examination
Nov. 13, 2008

Your Name _____

Student ID Number _____

Instructions

Exams: Consultation during the exam is not permitted. This is not an open book exam. The exam is to be completed in one and half hours. If you need scratch paper, just use the blank parts of these pages; show all of your work on these pages. Before you start writing, please check if you have all 16 pages of the exam.

Regrading Policy: Exams will be accepted for regrading up to two weeks after you get the graded exam. No regrades after two weeks.

Please sign the following statement upon completing this exam:

I certify that I will follow the above instructions. I have neither received nor given unpermitted aid on this examination.

Your signature _____

***** Score Board (to be filled by graders) *****

	Total points
Problem 1	10
Problem 2	15
Problem 3	10
Problem 4	10
Problem 5	10
Problem 6	10
Problem 7	15
Problem 8	20
Total	100

combinational ckt : =

sequential ckt : <

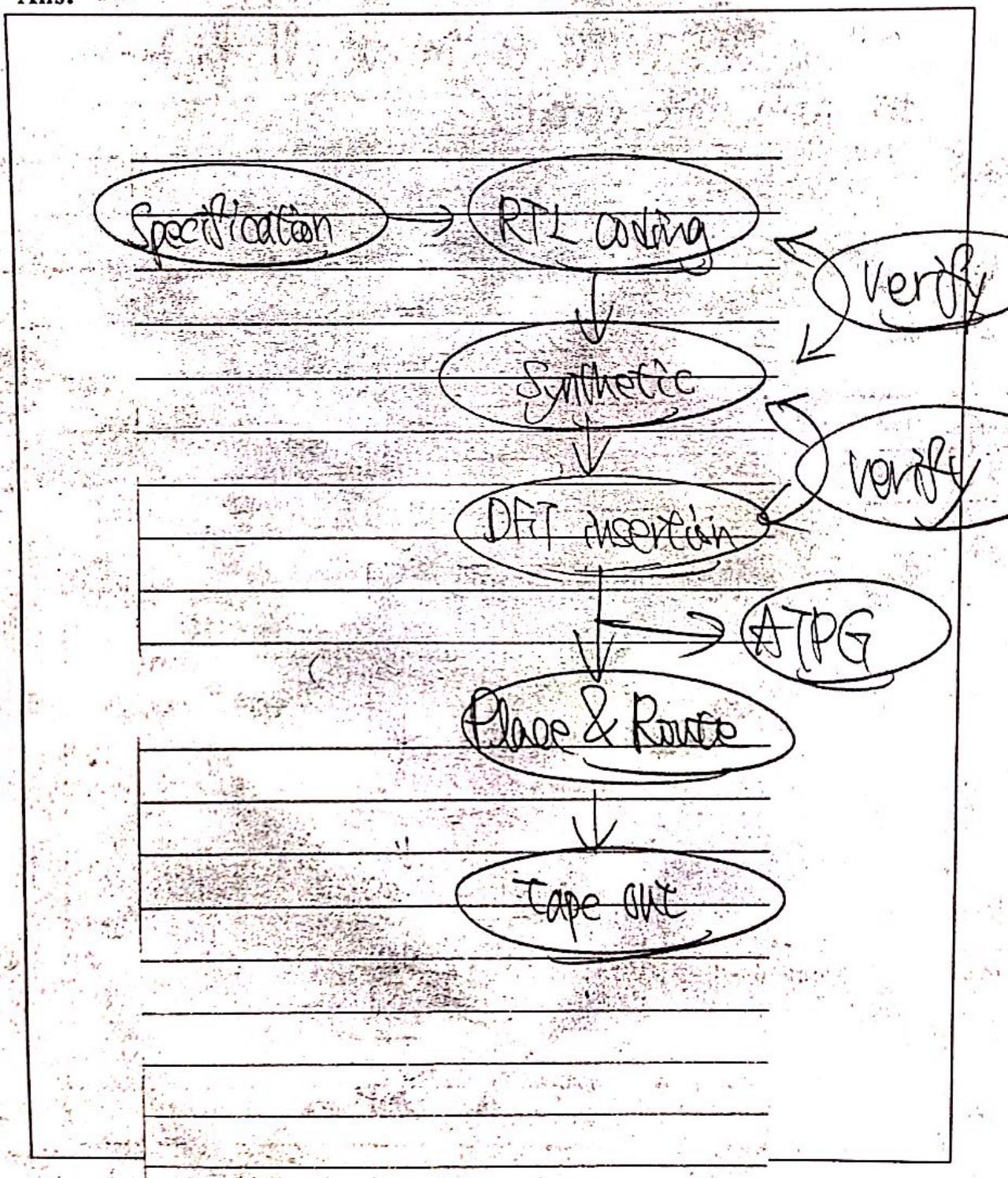
Problem 1 <Design Flow>

(10%) The following items are the steps in the cell-base design flow steps. Please make connections between these steps.

- (a) RTL Coding; (b) Dft Insertion; (c) Tape Out; (d) Specification; (e) Place & Route;
(f) Synthesis; (g) ATPG; (h) Verify

(hint: please draw the flowchart. Some steps may occur in the flowchart more than one times.)

Ans:



Problem 2 <Basic Concept>

A. (6%) Briefly explain the following terms:

- (a) Fault simulation
- (b) Defect level

Ans:

(a) input a test vector, to find out all faults
~~from this vector~~

(b)

Defect level

B. (9%) Briefly describe what new features are included in SVTB.

Ans.

Simula

Synthes

Synth

System: Terrey

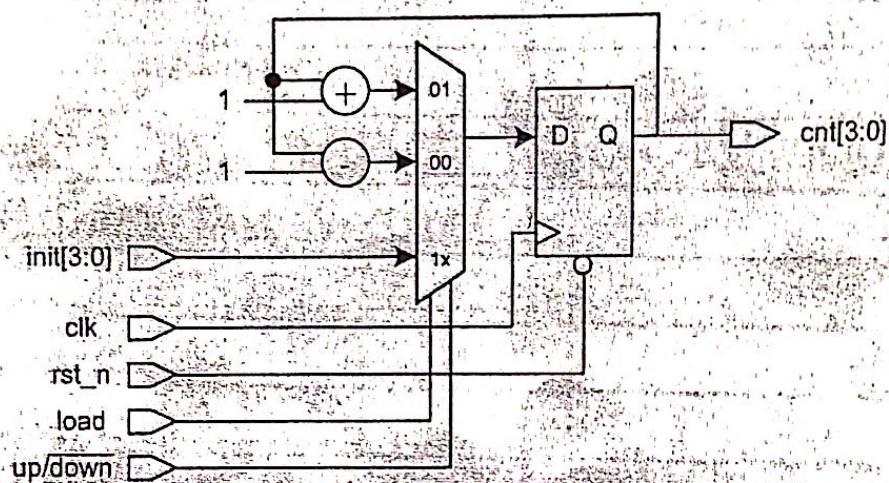
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這看的。

...Orz

Problem 3 <Verilog Debug and Coding>

A counter with synchronized initial value loading and up count/down count function is shown below.



(10%) The following Verilog-RTL code for the counter is not correct. Please write the correct version in the right column.

Verilog code with bugs

```
module counter(clk, rst_n, cnt,
init, load, updown)
```

```
input clk, rst_n;
```

```
output [3:0] cnt;
```

```
input [3:0] init;
```

```
input load;
```

```
wire [3:0] cnt_w;
```

```
reg [3:0] cnt;
```

```
reg [3:0] init;
```

```
wire
```

```
always@(cnt or init)
```

```
begin
```

```
case((load, updown))
```

```
2'b00: cnt_w = cnt - 1'bl;
```

```
2'b01: cnt_w = cnt + 1'bl;
```

```
2'b10: cnt_w = init;
```

```
endcase
```

```
default:
```

```
end
```

```
always@(posedge clk or posedge
```

```
rst_n)
```

```
begin
```

```
if(!rst_n)
```

```
cnt <= 4'd0;
```

```
else
```

```
cnt <= cnt_w;
```

```
end
```

```
endmodule
```

Corrected Code

~~st_n, cnt,~~

~~input updown;~~

~~updown or load~~

~~- 1'bl;~~

~~; + 1'bl;~~

~~init;~~

~~hit;~~

~~or negedge~~

There are totally bugs.

Problem 4 <Verilog 2001>

(10%) Given the following code written with Verilog-2001, please show the outputs if this code is simulated via a Verilog simulator.

```

`timescale 1ns/1ns

module test;
reg signed [7:0] x, a;
reg [7:0] y, b;

initial begin
    x = -8'd6; y=8'd6;
    #5 y=8'd255;
    fork
        #15 a = x >>> (-2'b1);
        #5 b' = x >> (-2'b1);
        begin
            #10 y <= x;
            x <= y;
        end
    join
    #20 x[4 +: 4] = 0;
    #5 $finish;
end

```

$$\begin{array}{r}
 \text{X} = \underline{\underline{11111010}} \\
 \text{b} = \underline{\underline{00001111}} - 3
 \end{array}$$

```
initial begin
```

```
$monitor("%t %d %d %d %d", $time, x, y, a, b);
```

```
end
```

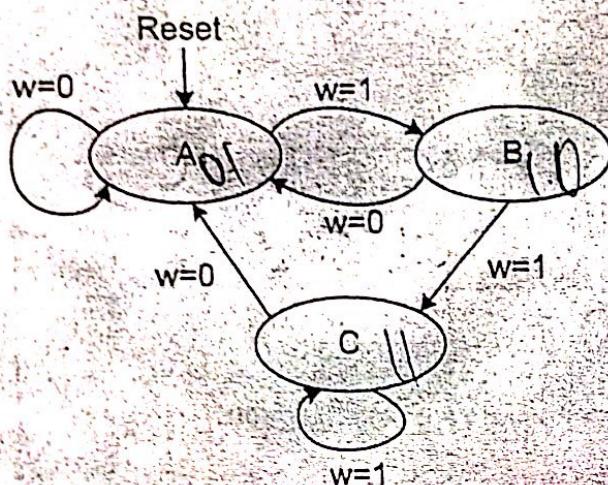
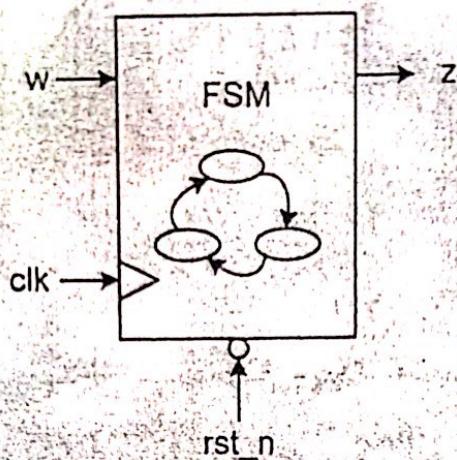
```
endmodule
```

Ans:

	x	y	a	b				
0	6	6	X	X				
5	-6	255	X	X				
10	-6	255	X	3				
15	-7	250	X	31				
20	-4	250	X	31				

Problem 5 <Finite State Machine>

(10%) A state diagram of a finite state machine is shown below.



State	Output z
A	0
B	0
C	1

Please complete the following Verilog code:

~~Ans:~~

```

module FSM(clk, rst_n, z, w);

    input clk, rst_n;
    output z;
    input w;

    parameter A=2'b01, B=2'b10, C=2'b11;

    reg [1:0] state; //current state
    reg [1:0] next_state; //next state logic output
    reg z;

```

```
//next state logic  
always@(rst_n or W or state)  
begin  
    if (!rst_n)  
        next_state = A;  
  
    else begin  
        case (state)  
            A: begin  
                if (W=1)      next_state = B;  
                else          next_state = A;  
                Z = 1'd0;  
            end  
            B: begin  
                if (W=1)      next_state = C;  
                else          next_state = B;  
                Z = 1'd0;  
            end  
            C: begin  
                if (W=0)      next_state = A;  
                else          next_state = C;  
                Z = 1'd1;  
            end  
        endcase  
    end  
end
```

```
begin
    if (~reset)
        state <- A;
    else
        state <- next_state;
end

endmodule
```

Problem 6 <Manually Synthesis from Verilog RTL Code>

(10%) In the following table, the left column show some pieces of Verilog RTL code. Please draw the corresponding circuits in the right column. You can use AND, OR, NAND, NOR, XOR, XNOR, NOT, MUX in the circuit diagram.

Verilog Code	Circuit Diagram
<pre> always @ (a or b or sel) begin if (sel[1]) z = a; else if (sel[0]) z = b; end </pre>	
<pre> always @ (a or b or c) begin for(k=0; k<=2; k=k+1) begin out[k] = a[k] + b[k]; c = (a[k] b[k]) & c; end end </pre>	

$$C = (a[0] \mid b[0]) \& (a[1] \mid b[1]) \& (a[2] \mid b[2]) \& c$$

Problem 7 (15%) <Synthesis Reports>

- A. (5%) The following figure is the area report after synthesis. It sometimes shows "undefined" in total area. Please explain it and describe how to fix it.

```
*****
Report : area
Design : ALU
*****
.
.
.
Number of cells: 90
Number of references: 10
.
.
.
Combinational area: 1939.291626
Noncombinational area: 2049.062256
Net Interconnect area: undefined
.
.
.
Total cell area: 3988.353760
Total area: undefined
```

Ans:

沒有設定 wire-load

所以 total area 會 unknown

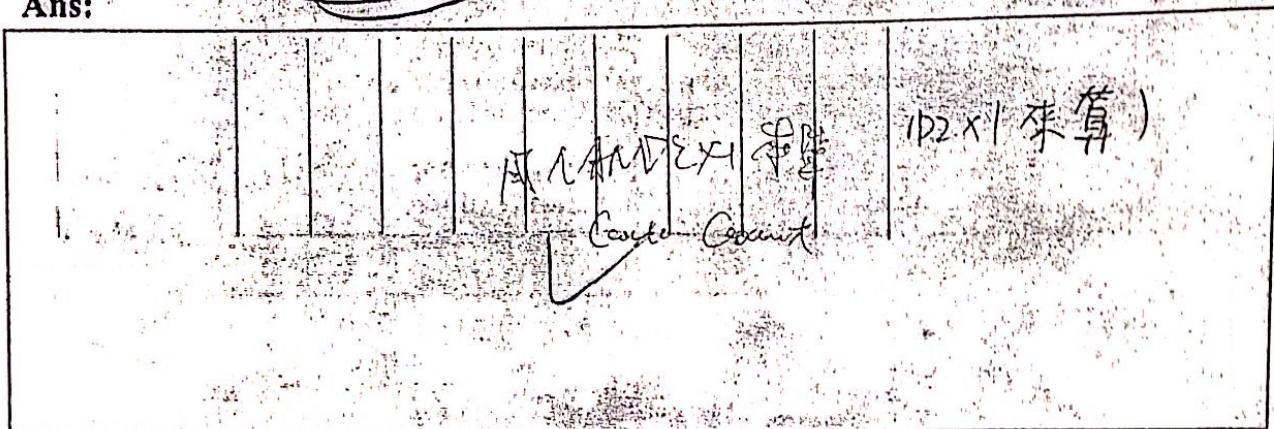
D2 soft 善手

; 由成一個 design file

B. (5%) If the total area is 4134, how many gate counts does it correspond to? You may need the cell table shown below.

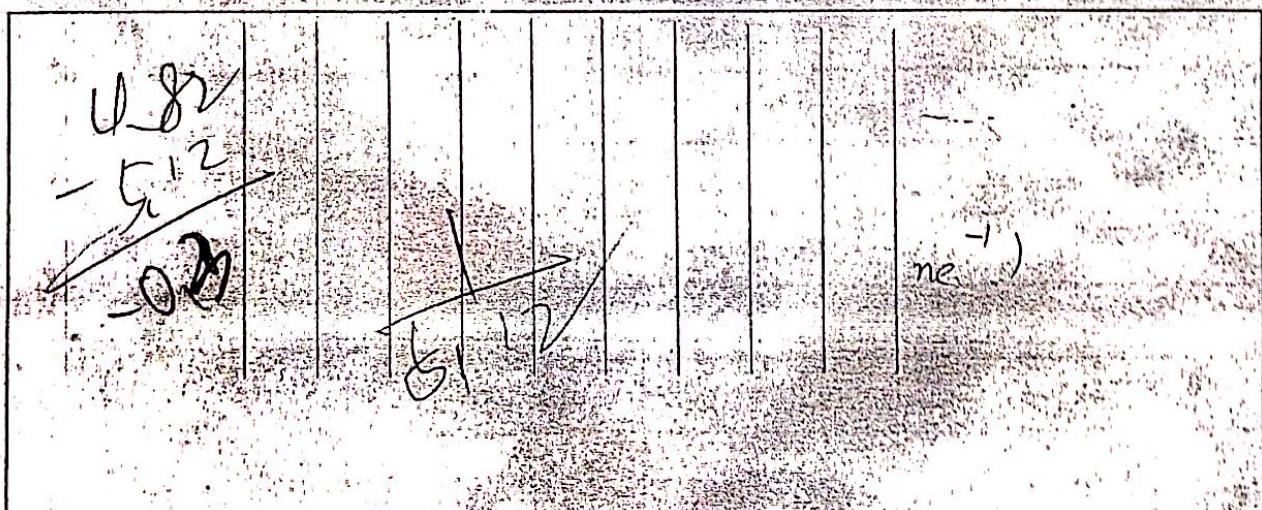
Cell Type	Height(um)	Width(um)
OR2x1	2	2
AND2x1	3	2.5
NOR2x1	2.5	2.5
NAND2x1	3	2

Ans:



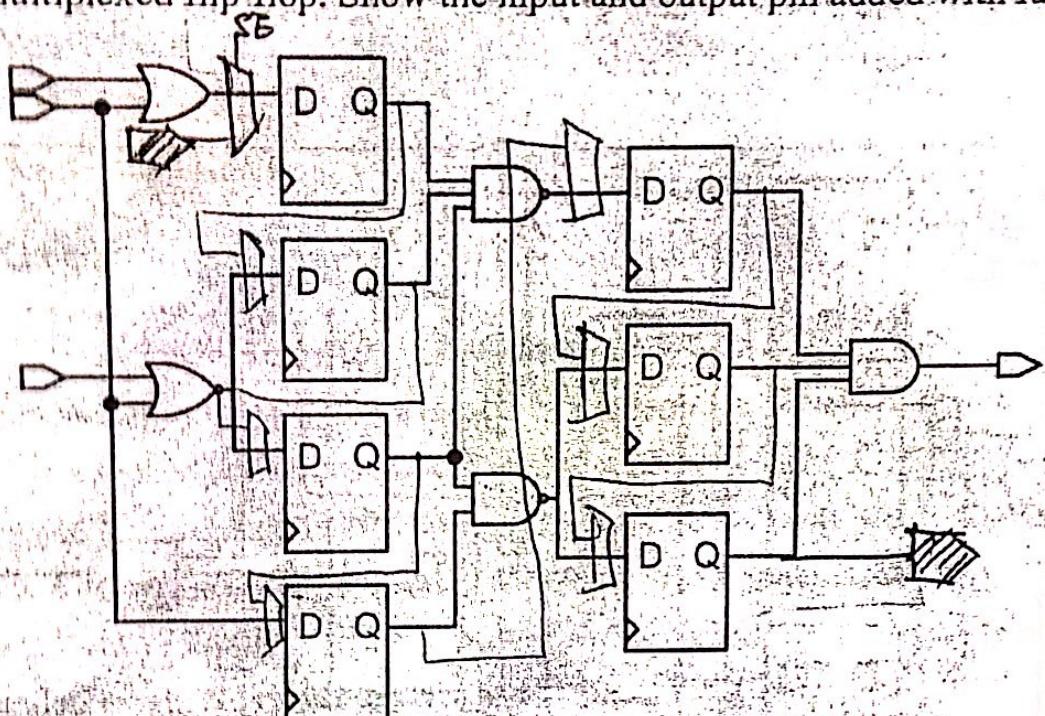
C. (5%) In the timing report, the most important information is the slack value. If the data arrival time is 5.12 and the data required time is 4.82, what is the slack? What is the maximum operation speed of the circuit?

Ans:

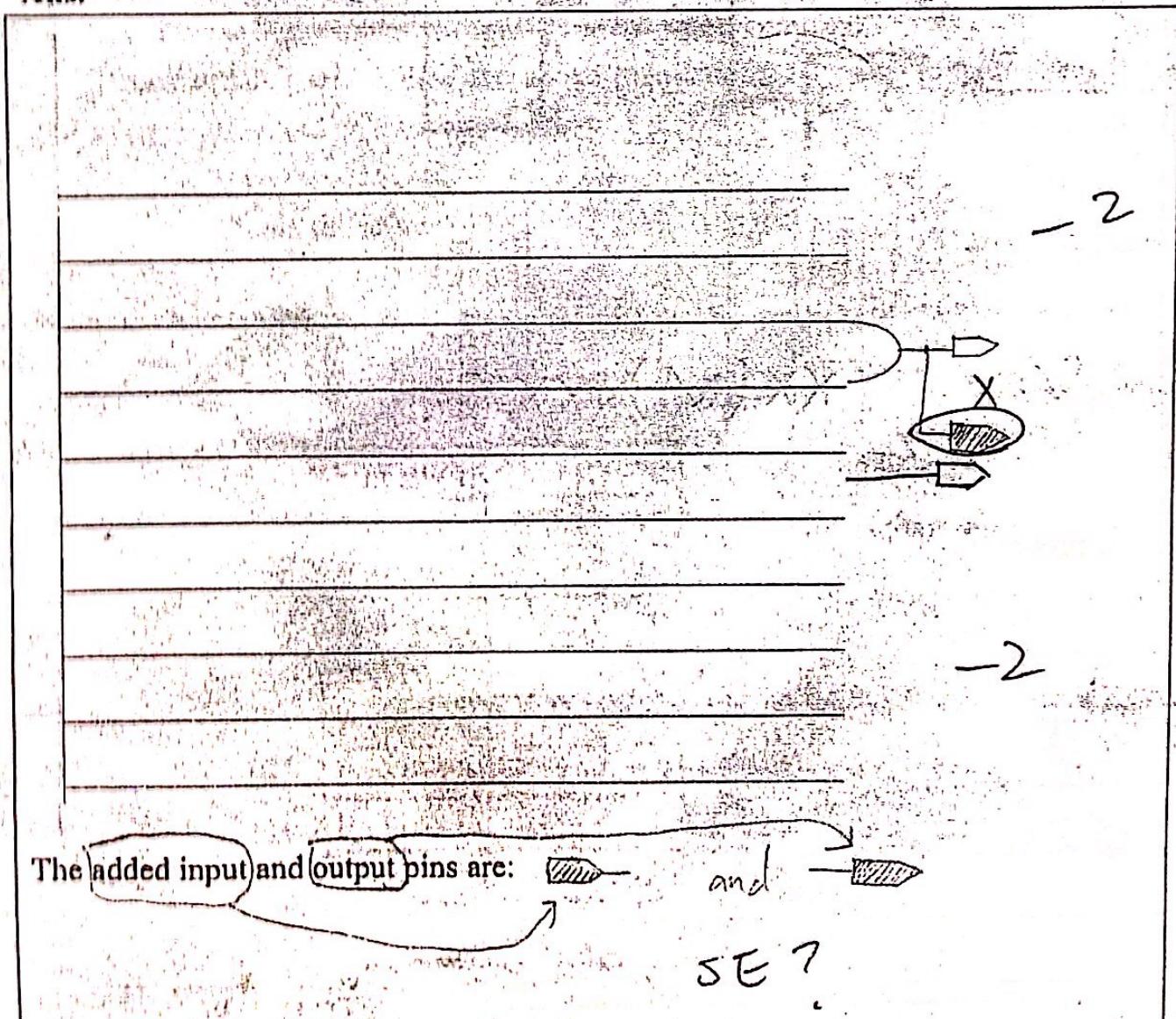


Problem 8 <Design for Testing>

A. (10%) For the following circuits, please draw the associated circuits with full-scan with multiplexed flip-flop. Show the input and output pin added with full-scan.



Ans.



B. (10%) Apply D-algorithm to find out the test pattern for the "stuck-at-1" fault at node A. Show the process of the testing flow using this test pattern. (Note: The process includes the test input vector being shifted into the scan chain and the expected output being shifted out from the scan chain.)

Ans.

