Computer-Aided VLSI System Design
Midterm Examination
Nov. 12, 2009

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Instructions

Exams: Consultation during the exam is not permitted. This is not an open book exam. The exam is to be completed in one and half hours. If you need scratch paper, just use the blank parts of these pages; **show all of your work on these pages.** Before you start writing, please check if you have all 14 pages of the exam.

Regrading Policy: Exams will be accepted for regrading up to two weeks after you get the graded exam. No regrades after two weeks.

Please sign the following statement upon completing this exam:

I certify that I will follow the above instructions. I have neither received nor given unpermitted aid on this examination.

Your signature 余孟璘

********** Score Board (to be filled by graders) **********

	Total points	Your points
Problem 1	10	8+2
Problem 2	15	14
Problem 3	10	5
Problem 4	12	12
Problem 5	12	12
Problem 6	5	5
Problem 7	12	12
Problem 8	14	14
Problem 9	10	10
Total	100	92+2

Problem 1 <Design Flow>

The following items are the steps in the cell-base design flow.

(a) DRC & LVS Verification; (b) DFT Insertion; (c) RTL Coding; (d) Place & Route; (e) Tape Out; (f) Synthesis; (g) Specification.

(6%) A. Please give the correct order of these steps.

6

Ans:

g → c → f → b → d → a → e

4

(4%) B. Besides taping out, which ones belong to the back-end part of the design flow?

Ans:

d, a, e

Problem 2 <Basic Concept>

(4%) A. Give one feature of SystemVerilog for design verification.

Ans:

f

event base simulation ✓

(3%) B. What kind of information does an SDF file give?

Ans:

3

timing information of the circuit ✓

(4%) C. What is a critical path?

Ans:

3

delay time 最長的 combinational path ✓

Input → FF

FF → FF

FF → output

(4%) D. What is setup time violation of a flip-flop?

Ans:

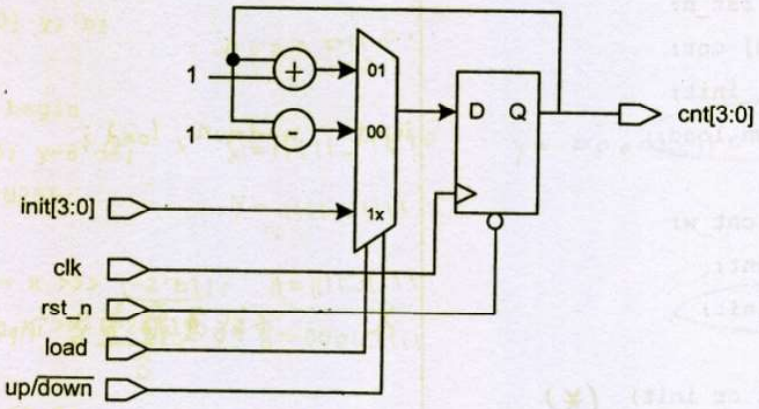
4

在 clk 拉起來之前 (posedge sensitive)

Flip-flop 的 input 沒有在該 FlipFlop 的 setup time 之前穩定

Problem 3 <Verilog Debug and Coding>

A counter with synchronized initial value loading and up count/down count function is shown below.



(10%) The following Verilog-RTL code for the counter is not correct. Please write the correct version in the right column.

Verilog code with bugs

```
module counter(clk, rst_n, cnt,
init, load, updown)

input clk, rst_n;
output [3:0] cnt;
input [3:0] init;
input updown load;

wire [3:0] cnt_w;
reg [3:0] cnt;
reg [3:0] init;

always@(cnt or init)
begin
  case({load, updown})
    2'b00: cnt_w = cnt - 1'b1;
    2'b01: cnt_w = cnt++;
    2'b10: cnt_w = init;
  endcase
end

always@(posedge clk or rst_n)
begin
  if(~rst_n)
    cnt <= 4'd0;
  else
    cnt <= cnt_w;
end

endmodule
```

Corrected Code

```
module counter (clk, rst_n , cnt,
init, load, updown ) ;

input  updown , load ;

X  不能重複宣告 input

2'b01 :  cnt_w = cnt + 1 ;

2'b11 :  cnt_w = init ;
default :  cnt_w = 0 ;
           init

always @ (posedge clk or negedge rst_n)
```

There are totally 5 8 bugs.

Problem 4 <Verilog Simulation>

(12%) Given the following code written with Verilog-2001, please show the outputs if this code is simulated via a Verilog simulator.

```
`timescale 1ns/1ns
module test;
reg signed [7:0] x, a;
reg [7:0] y, b;

initial begin
x= -8'd6; y=8'd6;
#5 y=8'd255;
fork
 #15 a = x >>> (-2'b1);
 #5  b = x >> (-2'b1);
 begin
  #10 y <= x;
      x <= y;
 end
join
#20 x[4 +: 4] = 0;
#5 $finish;
end

initial begin
 $monitor("%t %d %d %d %d",$time, x, y, a, b);
end
endmodule
```

Ans:

0	-6	6	x	x
5	-6	255	x	x
10	-6	255	x	31
15	-1	250	x	31
20	-1	250	-1	31
40	15	250	-1	31

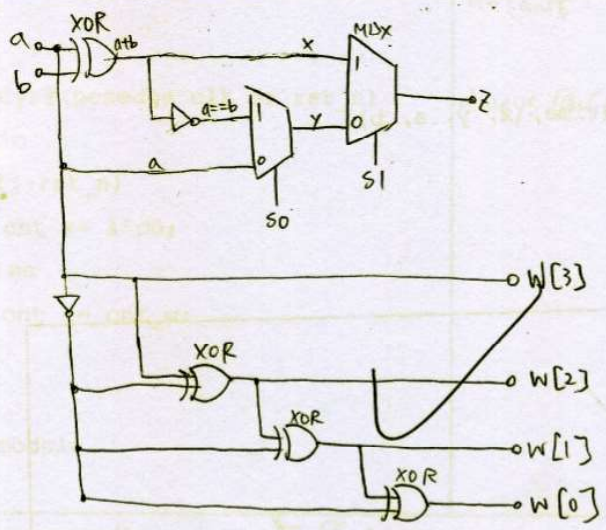
Problem 5 <Manually Synthesis from Verilog RTL Code>

(12%) The following block shows a procedural block of Verilog RTL code. Please draw the corresponding circuits in the bottom block. You can use AND, OR, NAND, NOR, XOR, XNOR, NOT, MUX in the circuit diagram.

Verilog Code

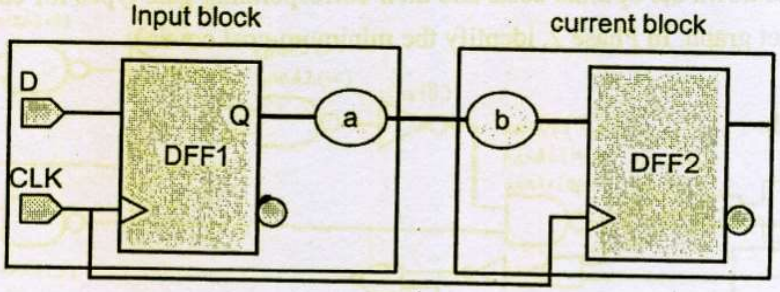
```
wire a, b, s0, s1;
reg [3:0] w;
reg x, y, z;
integer i;
always@(a or b or x or y or s0 or s1)
begin
   z = (s1)? x: y;
   x = a + b;
   y = (s0)? (a==b): a;
   for(i=0; i<3; i=i+1)
   begin
      w[i] = w[i+1] ^~ a;
   end
   w[3] = a;
end
```

Circuit Diagram



Problem 6 <Input Delay>

(5%) B. Please specify the **input delay** of the **current block** in the following circuit.



5

Ans:

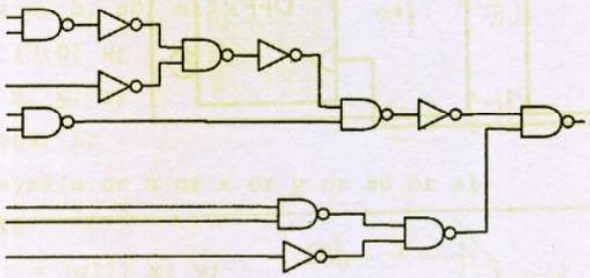
DFF1 的 CLK→Q delay + ⓐ delay

Problem 7 <DAGON algorithm>

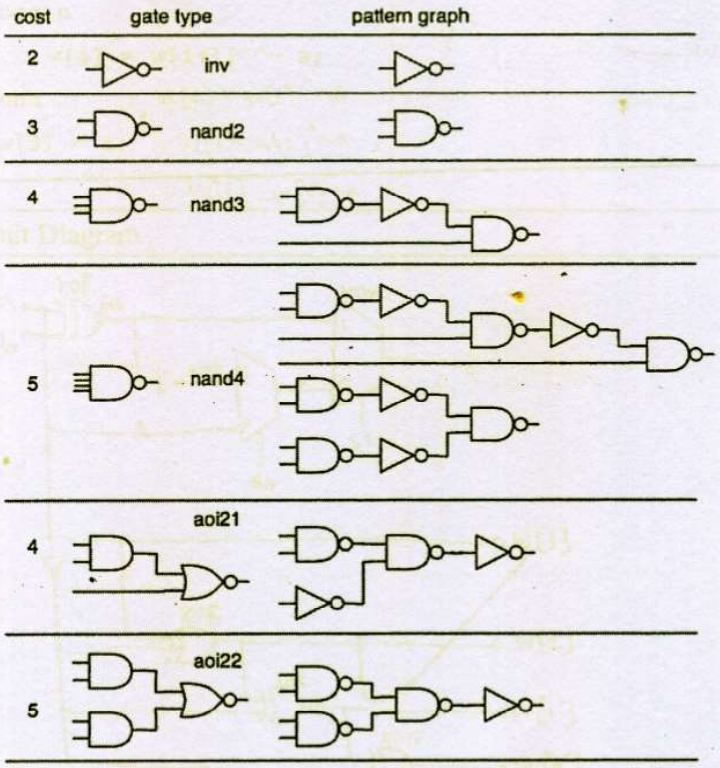
(12%) Perform technology mapping using the DAGON algorithm to compute a *minimum-cost cover* for the following subject graph using the given library.

(In Phase 1, write down the optimal costs and their corresponding gate types for each gate in the subject graph. In Phase 2, identify the minimum-cost cover.)

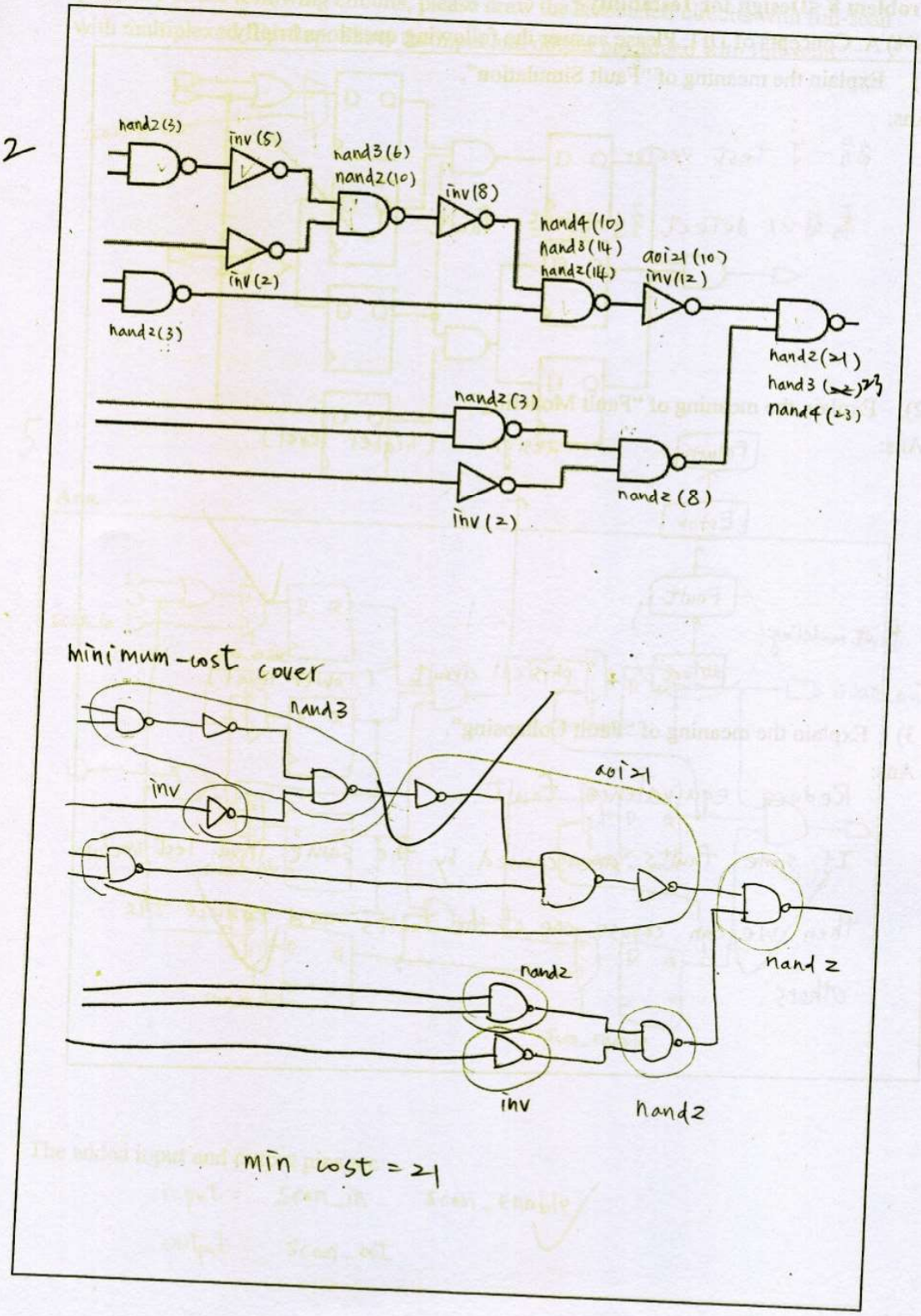
Subject graph:



Library:



Ans:


nand2(3)
inv(5)
nand3(6)
nand2(10)
inv(8)
nand4(10)
nand3(14)
nand2(14)
aoi21(10)
inv(12)
inv(2)
nand2(3)
nand2(21)
nand3(23)
nand4(23)
nand2(3)
nand2(8)
inv(2)
minimum-cost cover
nand3
inv
aoi21
nand2
nand2
inv
nand2
min cost = 21

Problem 8 <Design for Testability>

(9%) A. Concepts of DfT. Please answer the following questions briefly.

1) Explain the meaning of "Fault Simulation".

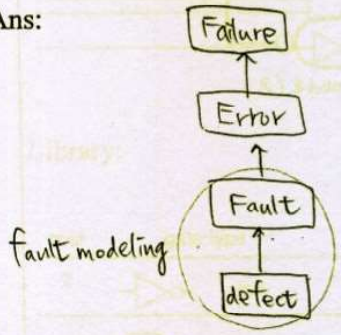
Ans:

給一个 test vector

看可以 detect 到哪些 fault ✓

2) Explain the meaning of "Fault Modeling".

Ans:



design (higher level)

physical circuit (lower level)

✓

3) Explain the meaning of "Fault Collapsing".

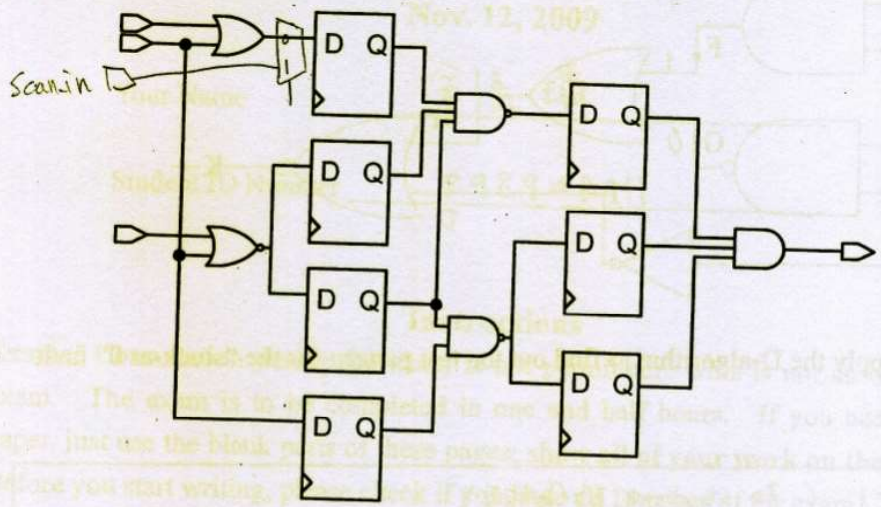
Ans:

Reduce equivalence fault.

If some faults are caused by the same input test vector then we can choose one of the faults and reduce the others. ✓

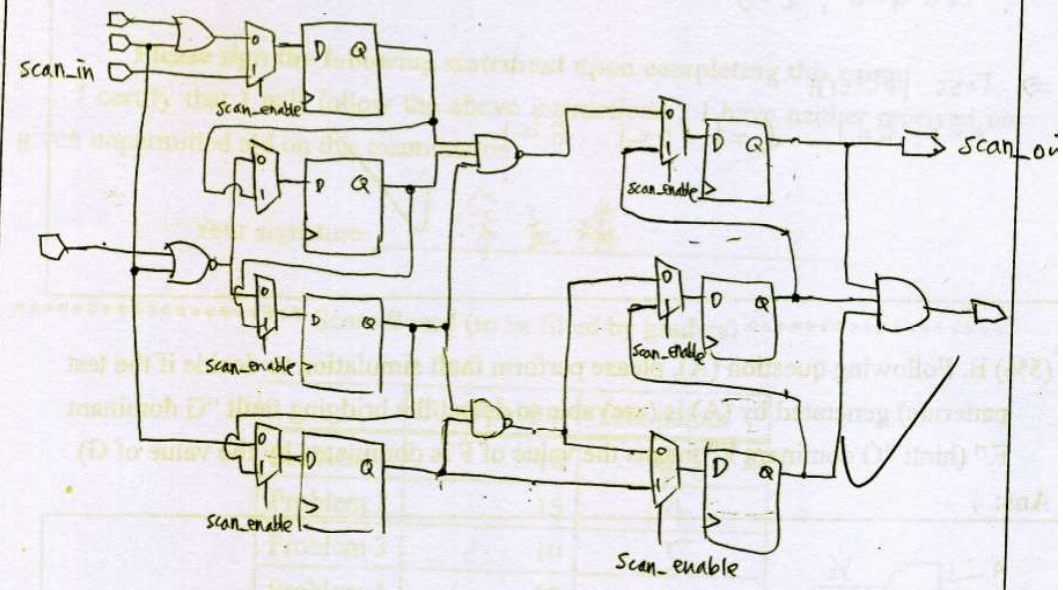
scan_in scan_enable

(5%) B. For the following circuits, please draw the associated circuits with full-scan with multiplexed flip-flop. Show the input and output pin added with full-scan.



5

Ans.

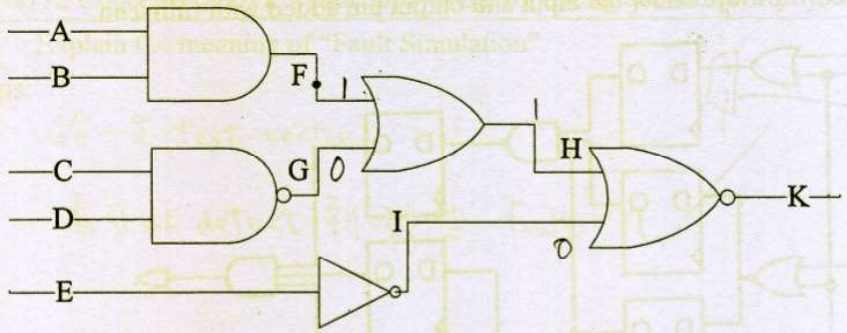


The added input and output pins are:

input : scan_in . scan_enable

output : scan_out

Problem 9 <Fault Simulation & ATPG>



(5%) A. Apply the D-algorithm to find out the test pattern for the "stuck-at 0" fault at net F

Ans:

① Let F = 1 (和 stuck-at 的值相反)

② Let F be sensitive to K

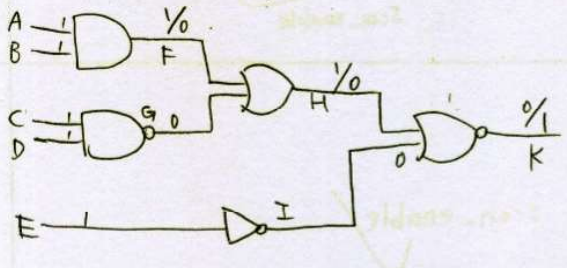
Let G=0 , I=0

⇒ Test pattern

A=1 B=1 C=1 D=1 E=1

(5%) B. Following question (A), please perform fault simulation to decide if the test pattern(s) generated by (A) is (are) able to detect the bridging fault "G dominant F." (hint: "G dominant F" means the value of F is dominated by the value of G)

Ans:



可以 detect this bridging fault