Fabrication and Characterization of a Metal Oxide Semiconductor Capacitor

Alberto Arriaga Felix
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UCR: Bourns College of Engineering

***Abstract*— A MOS capacitor is an important device used in electronic devices. This paper describes the fabrication of a MOS capacitor in the EE136 Lab using a p-type silicon wafer. The fabrication of this device is described in detail, including the steps of photolithography and metal deposition. A brief overview of the theory behind MOS capacitor device operation is given. The fabricated device is tested to demonstrate its Capacitance-Voltage characteristics. These experimental results are compared with simulated results for the same type of device. Overall it was observed that the fabricated device followed the results of the simulation, but the resulting Cfh and Clf did not match.**

I. INTRODUCTION

The metal oxide semiconductor (MOS) capacitor is a two-terminal device consisting of three layers. A metal gate electrode, an insulation layer, and a semiconducting layer body. The structure of a MOS capacitor is shown in figure 1. This structure is obtained by growing a layer of silicon dioxide (SiO2) called the insulation layer, on top of a silicon substrate (p-type or n-type) called the body. Then depositing a layer of polycrystalline silicon (polySi) that acts as the gate, on top of the SiO2. Finally, metal contacts are place on either side, allowing for measurements.

The MOS capacitor is not a widely used device by itself. However, it is a part of the MOS transistor (MOSFET). This transistor is the most widely used semiconductor device in electronic devices. The fabrication of the MOS Capacitor structure is one of the most critical steps when fabricating MOSFETs. This is because of the need for an ideal oxide-semiconductor interface for improved performance in electronics. The basic MOS capacitor lends itself as a diagnostic tool used for determining the quality of the process used in the fabrication of integrated circuits. Knowing the quality and reliability of the gate oxides shows the quality of the semiconductor fabrication process.

This paper will review the fabrication procedure of a MOS capacitor. It will discuss and analyze the Capacitance-Voltage (C-V) characterization of a MOS capacitor fabricated in the EE136 lab. Finally, it will show a comparison of the fabricated MOS capacitor with its simulated model.

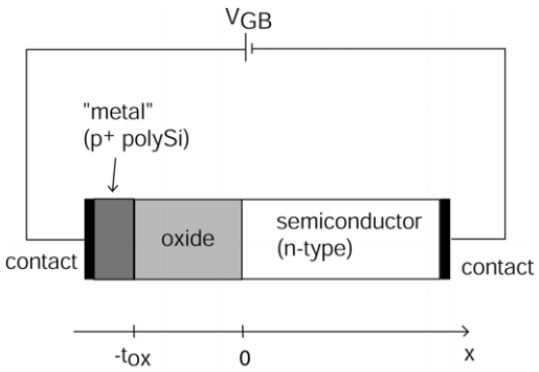

Fig. 1. Metal-oxide-semiconductor structure on n-type silicon.

II. MOS CAPACITOR FABRICATION

The MOS capacitor fabricated in the EE 136 Lab used the techniques of photolithography, and Metal Deposition and Lift-off.

A. Photolithography

1) Cleaning

A small piece of p-type silicon wafer in Fig, 2 was cleaned using Deionized water (DI). DI water is water that has had almost all its mineral ions removed, and helps with removing impurities from the Si surface. After this, the silicon wafer was blow dried using a pump compressor to remove all possible dust particles from the surface.

2) Coating

Then 2 drops of photoresist AZ5214 were placed on the silicon wafer piece. The wafer was then placed on a spin coater, shown in Fig. 3, that allows the photoresist to spread evenly on the surface of the wafer. The spin coater was set to 30 seconds, after that the wafer was removed. The wafer was transferred to a baking plate of Fig. 6, where it was soft baked for 120 secs at 110 ˚C. this step is needed as the solvent can absorb exposing radiation.

3) Align Mask and Expose Pattern

After the wafer cool down, it was placed inside a SUSS MicroTec MA/BA 6 mask and bond aligner machine. A mask of a MOS capacitor structure was placed in the machine (figure 4). The mask is aligned with the wafer using the attached cameras and monitor. The wafer is then exposed inside the machine to high intensity ultraviolet light radiation, through the mask, in the places predetermined by the mask as shown in Fig. 5. The masked use had a 10mm feature size.

4) Develop

After, the masked is removed from the machine it is placed inside a development agent liquid shown in Fig. 6. Any photoresist that has been exposed to the UV light is washed away, leaving the bare silicon dioxide in the exposed areas. The wafer was then cleaned with DI water and blow dried, to remove any traces of developed photoresist. The resulting wafer was examined under a microscope as shown in Fig. 7.

B. Metal Deposition

The metal deposition part of the fabrication was done by the TA, since students did not have access to metal deposition equipment. During this process, a film coating of aluminum was deposited on the silicon wafer, covering the pattering of the wafer.

Fig. 2. Small piece of p-type silicon wafer.

Fig. 3. Spin Coating.

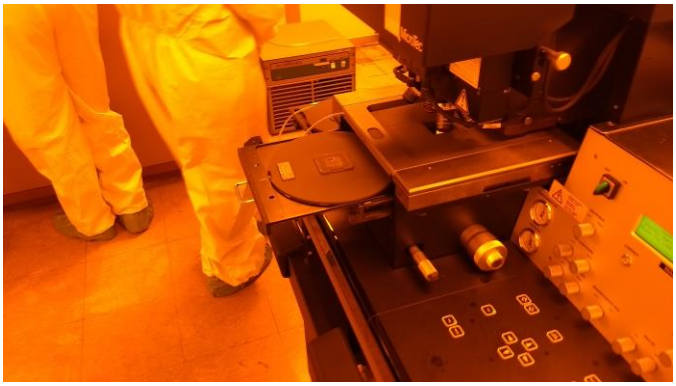

Fig. 4. Align Mask inside SUSS MicroTec MA/BA 6.

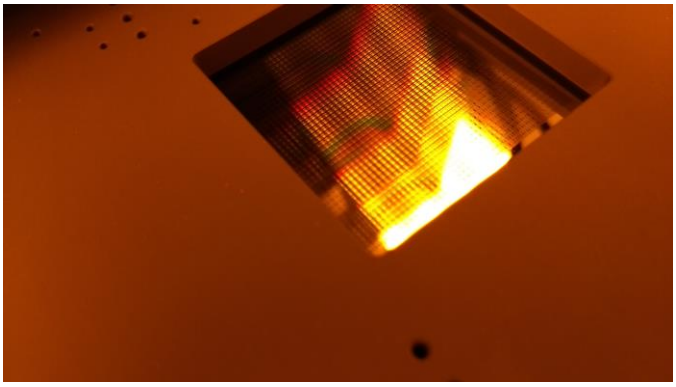

Fig. 5. Before UV exposure, mask pattern visible.

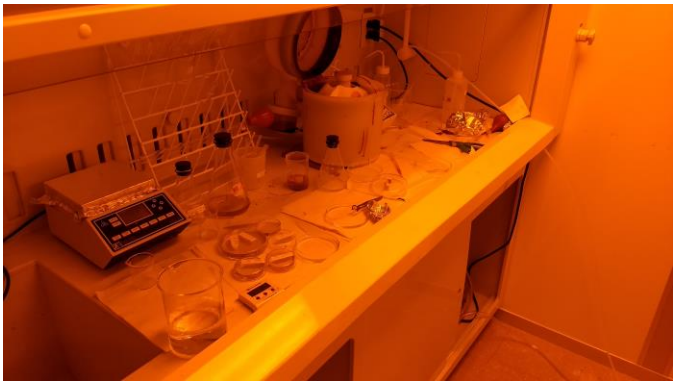

Fig. 6. Development agent and Baking.

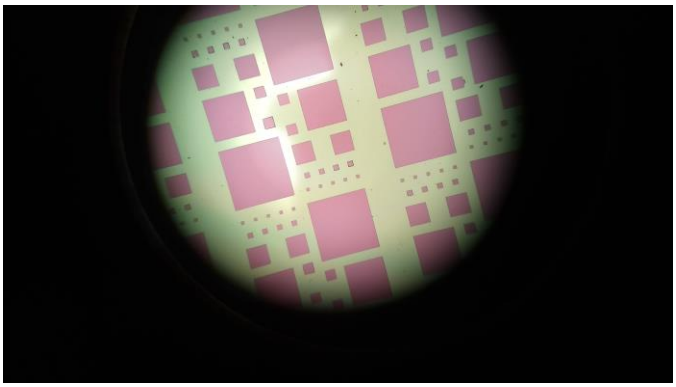

Fig. 7. Result wafer with pattern etched.

III. C-V CHARACTERIZATION

The MOS capacitor was connected to an Agilent 4284 Precision LCR meter via the metal gate and body contact as seen in "Fig. 8".

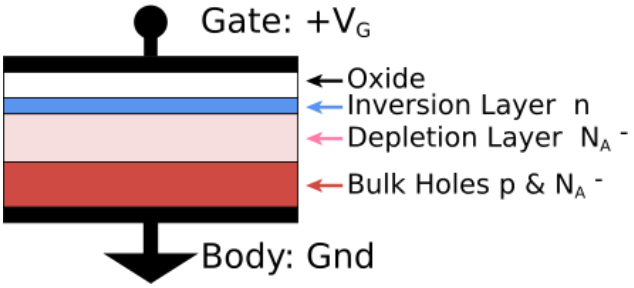

Fig. 8. Diagram of MOS capacitor nodes.

The capacitance depends on the voltage that is applied at the gate. The resulting Capacitance-Voltage (CV) curve shows that there are three regimes of operation separated by two voltages as shown in Fig. 9.

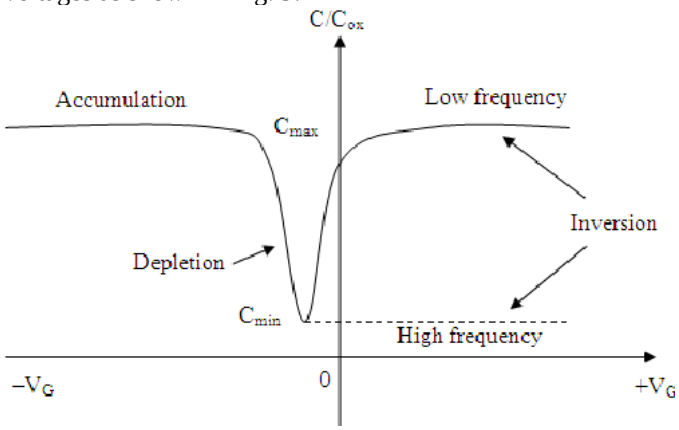

Fig. 9. Capacitance vs Gate Voltage diagram of a MOS Capacitor.

The regions are, Accumulation in which carriers of the same type as the body accumulates at the surface. Depletion in which the surface is devoid of any carriers leaving only a space charge or depletion layer. Inversion in which carriers of the opposite type from the body aggregate at the surface to "invert" the conductivity type. The two voltages that separate these regions are the Flatband Voltage (Vfb) and the Threshold Voltage (Vt).

The Capacitance in the accumulation region is given by (1). While in the depletion region by (2), and in the inversion region by (3).

$$C_{LF} = C_{HF} = C_{ox}, \text{ for } V_G \le V_{FB} \quad (1)$$

$$C_{LF} = C_{HF} = \frac{1}{\frac{1}{C_{ox}} + \frac{x_d}{\varepsilon_s}}, \text{ for } V_{FB} \le V_G \le V_T \quad (2)$$

$$C_{LF} = C_{ox} \text{ and } C_{HF} = \frac{1}{\frac{1}{C_{ox}} + \frac{x_{d,\max}}{\varepsilon_s}}, \text{ for } V_G \ge V_T \quad (3)$$

The MOS Capacitor that was fabricated in the lab showed the CV curves of Figs. 10-12 when the frequency was set to 10MHz, 7KHz, and 1KHz respectively. The reported CV characteristic for the 1MHz is correct and matches the theoretical approximation of Fig. 9. The two measurements obtain for the lower frequencies show unreliable results. The graphs show an uncharacteristic result where the capacitance is linear until it reaches zero. This result could be cause by breakdown of the material in the fabricated MOS capacitor. The high frequency graph of Fig 10 shows a maximum Chf of 0.40 nanoFarads/cm^3 at -3V. While the low frequency graph of Fig 11 shows a Clf of 13 nanoFarads/cm^3 at -3V.

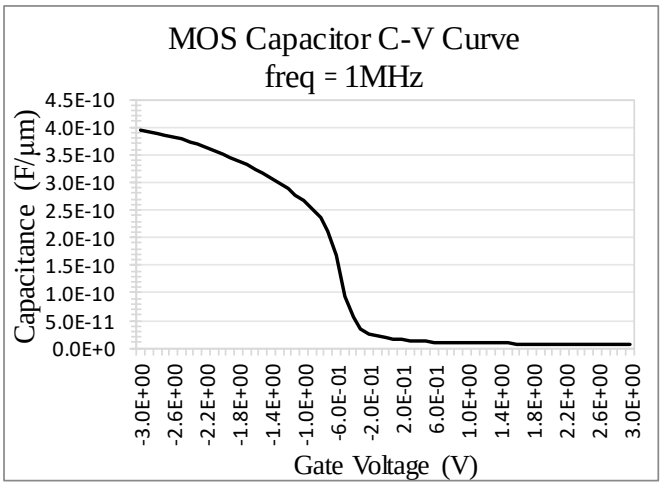

Fig. 10. CV Characteristics at 10MHz with voltage variation from -3V to 3V.

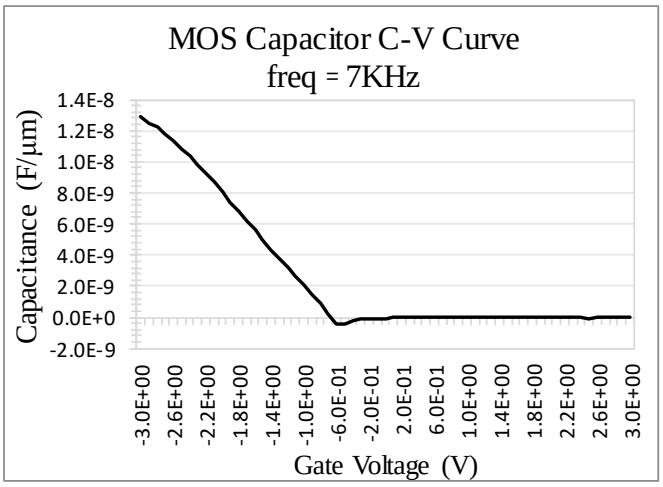

Fig. 11. CV Characteristics at 7KHz with voltage variation from -3V to 3V.

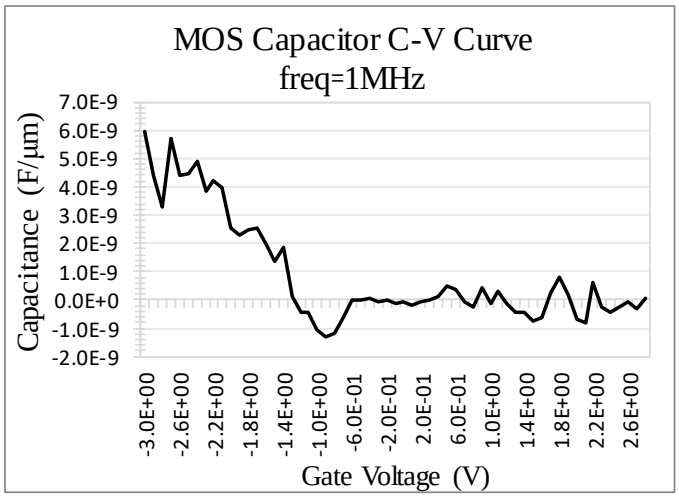

Fig. 12. CV Characteristics at 1KHz with voltage variation from -3V to 3V.

IV. MOS CAPACITOR SIMULATION

A simulation model was done using the MOS CAP simulation tool found at the nanoHUB.org website. The simulation was done using the parameters, Si thickness of 1mm, SiO2 thickness of 20nm, and with an aluminum Gate electrode.

Fig. 13 Shows the resulting CV curve of the simulated MOS capacitor with parameters equal to those of the fabricated MOS capacitor

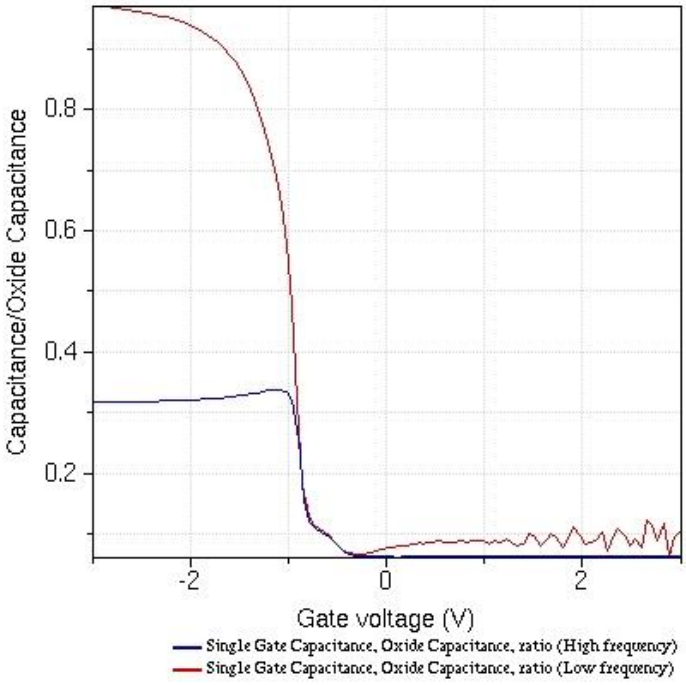

Fig. 13. CV Characteristics of Simulated MOS Capacitor, frequncy range 10Mhz (blue line) to 1KHz (red line), and voltage range -3V to 3V.

The red line of Fig. 13 shows the low frequency simulation, and gives a Clf of 1 Farads/cm^3 at -3V. The blue line of Fig. 13 shows the high frequency simulation and gives a Chf of 0.3 Farads/cm^3 at -3V.

CONCLUSION

The simulation results numbers are not the same as the experimental numbers for the MOS capacitor fabricated in the lab. But the CV Curves show similar characteristics, including the relationship of the low-frequency curve and the high frequency curve.

Overall, this lab showed the processes of fabricating a MOS capacitors. How to understand the theory behind the operation of this device. Provided us with two forms to test the operation of a particular device, through physical fabrication and testing, and simulation.

REFERENCES

[1] Jaeger, Richard C. Introduction to microelectronic fabrication. Reading, Mass:Addison-Wesley, 1993. Print.