MO601 – Project 2

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Objective

- This project studies the *Virtual Memory System*
  - Focus on *Translation Lookaside Buffer* (TLB)

- Two main objectives:
  1. Check the impact of the page size (4kB and 4MB) in the number of memory accesses caused by misses in the TLB;

  2. Check the impact of the absence of the TLB in the number of memory accesses;

- *PIN* used to simulate caches and TLBs;
- *SPEC2006* Benchmarks used for testing;

Page Size and the TLB Overview

- For each miss in the TLB, *n* memory accesses have to be made to translate a virtual address, where *n* is the number of page table levels
  - A 3-level page table was considered for this project
- One TLB for Data and one for Instructions
- Statistics are counted as:

$$Total\ Page\ Table\ Access = 3 * Total\ TLB\ Misses$$

  - Data or Instruction; 3-Level Page table

$$Total\ Memory\ Access = Total\ Page\ Table\ Access + L3\ Cache\ Misses$$

  - Data or Instructions; L3 Misses can be Data or Instruction as well

Page Size and the TLB Implementation

- Uses the Pintool *allcache.cpp* as base

- Modifications:
  - Added functions to print csv and human readable results, along with output file name arguments

  - Split the *Ul2Access* function in *Ul2Access _Data* and *Ul2Access_Ins* functions
    - Required to count the Data and Instruction L3-Misses separately

Page Size and the TLB Results

	I Mem Access		I TLB Misses		I Pg. Table Access		D Mem Access		D TLB Misses		D Pg. Table Access	
BM name	4kB Pg.	4MB Pg.	4kB Pg.	4MB Pg.	4kB Pg.	4MB Pg.	4kB Pg.	4MB Pg.	4kB Pg.	4MB Pg.	4kB Pg.	4MB Pg.
403.gcc << 200.in	279193514	2452045	92318751	3	276956253	9	3694007144	207005239	1165078483	3244405	3495235449	9733215
403.gcc << c-typeck.in	111009769	668114	36747413	3	110242239	9	1872216860	223672250	546909639	1088539	1640728917	3265617
456.hmmer << nph3.hmm	15377140	7708	5123236	4	15369708	12	540301346	58694661	159604263	16	478812789	48
462.libquantum << control	1964	1496	160	4	480	12	56549189182	53774731522	924819841	64	2774459523	192
464.h264ref << foreman	11128567	122818	2798461	4	8395383	12	1611682660	21781459	526048662	16	1578145986	48
501.toy-bm-1	795	679	42	3	126	9	2007	1503	174	6	522	18
502.toy-bm-2	1101	879	78	4	234	12	3076	2459	223	6	669	18

TLB Impact

- Considers a non-existent TLB
  - Each TLB Access (Hit or Miss) becomes 3 memory accesses
- Considers each memory access to take *60ns*
- Count Instruction and Data together
- Considers 4MB pages

BM name	With TLB		Without TLB		Increase Factor
	Pg. Table Access (I and D)	Total Time (s)	Pg. Table Access (I and D)	Total Time (s)	
501.toy-bm-1	27	2.70E-08	120616	1.21E-04	4467.26
502.toy-bm-2	30	3.00E-08	217128	2.17E-04	7237.60
403.gcc << 200.in	9733224	9.73E-03	2130813598	2.13E+00	218.92