Project 2 – Protocol Analysis, Design, and Testing

CIIC 4070 – Computer Networks

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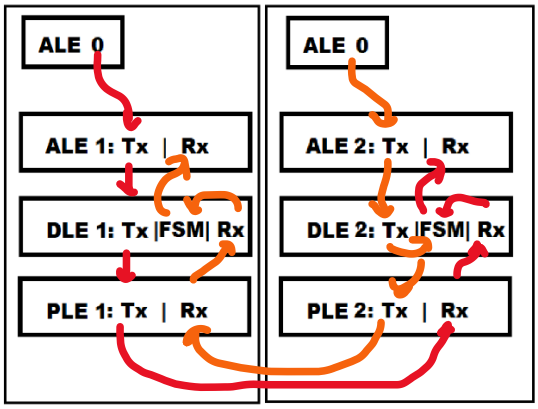
I. Introduction

This paper is a project for the CIIC 4070 course at UPRM. IT will count as a partial exam in which the resulting product of the student's investigative process showcases a developed result that encompasses the topics discussed in class. In it, the student is required to understand the stop-and-wait protocol coded in Python that the professor gave in class and modify it to execute new parameters and to monitor global variables in which several specs of the new implementation will be registered (average delay, loss rate and duplication rate). The student will also make two experiments with different layers to confirm his design and will record himself explaining the project and its development process in detail.

II. The Layer Model used in the given protocol



ALE: Application Layer Entity -> takes in user input and sends to DLE to encode to lower layers

DLE: Data Link Layer Entity -> In charge of synchronizing the ACK procedures and sending direct encoded bit messages to the PLE.

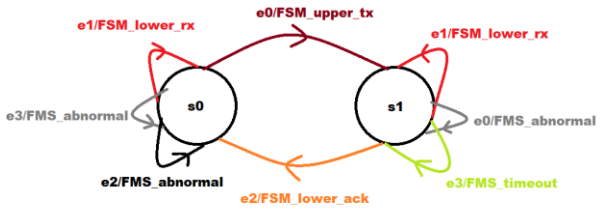
PLE-: Physical Layer Entity -> Coded representation of a independent device that has connected through a network in order to send a receive data.

Tx: Transfer Procedure

Rx: Receiving Procedure

FSM: Finite State Machine : In the DLE this new protocol allows a much more clearer interaction with the states and the severa ACK procedures that the DLE has to deal with

III. The finite state machine in the data layer



The FSM has two states:

- S0 : Ready to Send
- S1: Waiting for ACK

The FSM has 4 events:

- E0 : FSM_upper_tx (transmit info in upper layer)
- E1 :FSM_lower_tx(transmit info to lower layer)
- E2: FSM_lower_ack (receive lower ack sequence)
- E3: timeout (the response from the lower layer has been delayed and retransmission is required)

There are 9 transitions in total. The one involving *E0: FSM_upper_tx* is activated once the upper layer has brought more information to transmit and successfully delivered into the DLE. Both *E1* event driven transitions are related to a repeated signal to request data from the lower layer (being an ack sequence or data). All *FMS_abnormal* sequences refer to wrong signals and invalid instructions. The E2: FSM_lower_ack is the transition of successful ack from lower layer to the DLE. Finally, the E3 in the s1 state refers to a timeout occurring, and it indicates an immediate request to retransmission from source.

IV. The design of a measurement layer

The measurement layer works mostly like an application layer. In fact, most of the details that encompass this layer revolve around the fact that it generates the messages that will be transmitted throughout the whole interaction between the duplex networks. However, it would keep track of various details that are of interest to potential testers (delay rates, loss rates, duplication occurrences).

Constructor

Loop

V. Conclusions

Throughout this project the student understood in a practical environment the requisites of making a layered network system using only software and IDE's. The exchange of ACK procedures and data were visualized in a much more comprehensive perspective and laid the foundation for the expansion of knowledge that the student can acquire in the area of study of network development.

VI. References

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