ECEN 454 Lab 3: Cell Characterization using Spectre

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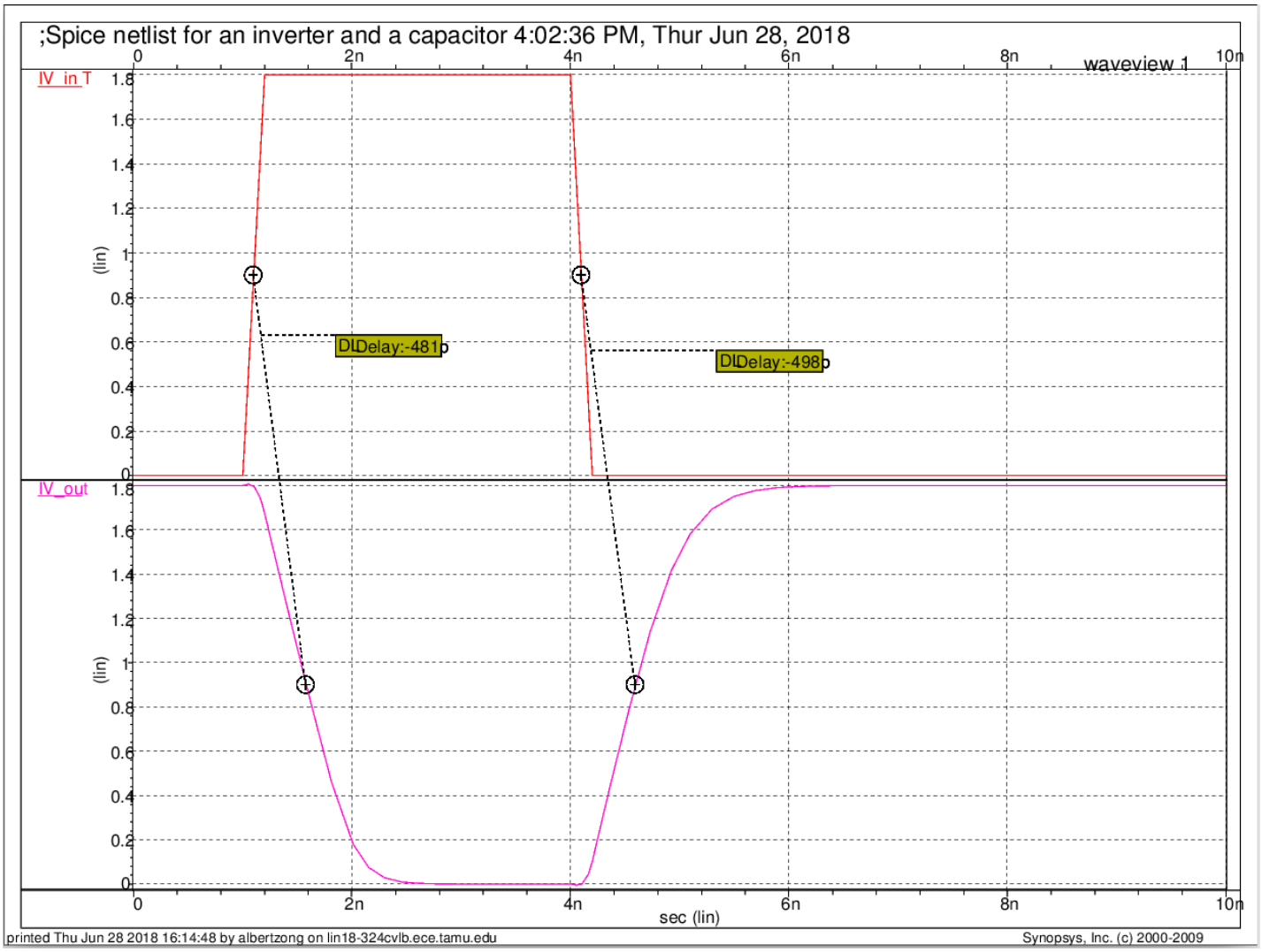
Due Date: June 28, 2018

INVERTER

Rising Delay: 498p
Falling Delay: 481p

Inverter (Delay_Table):

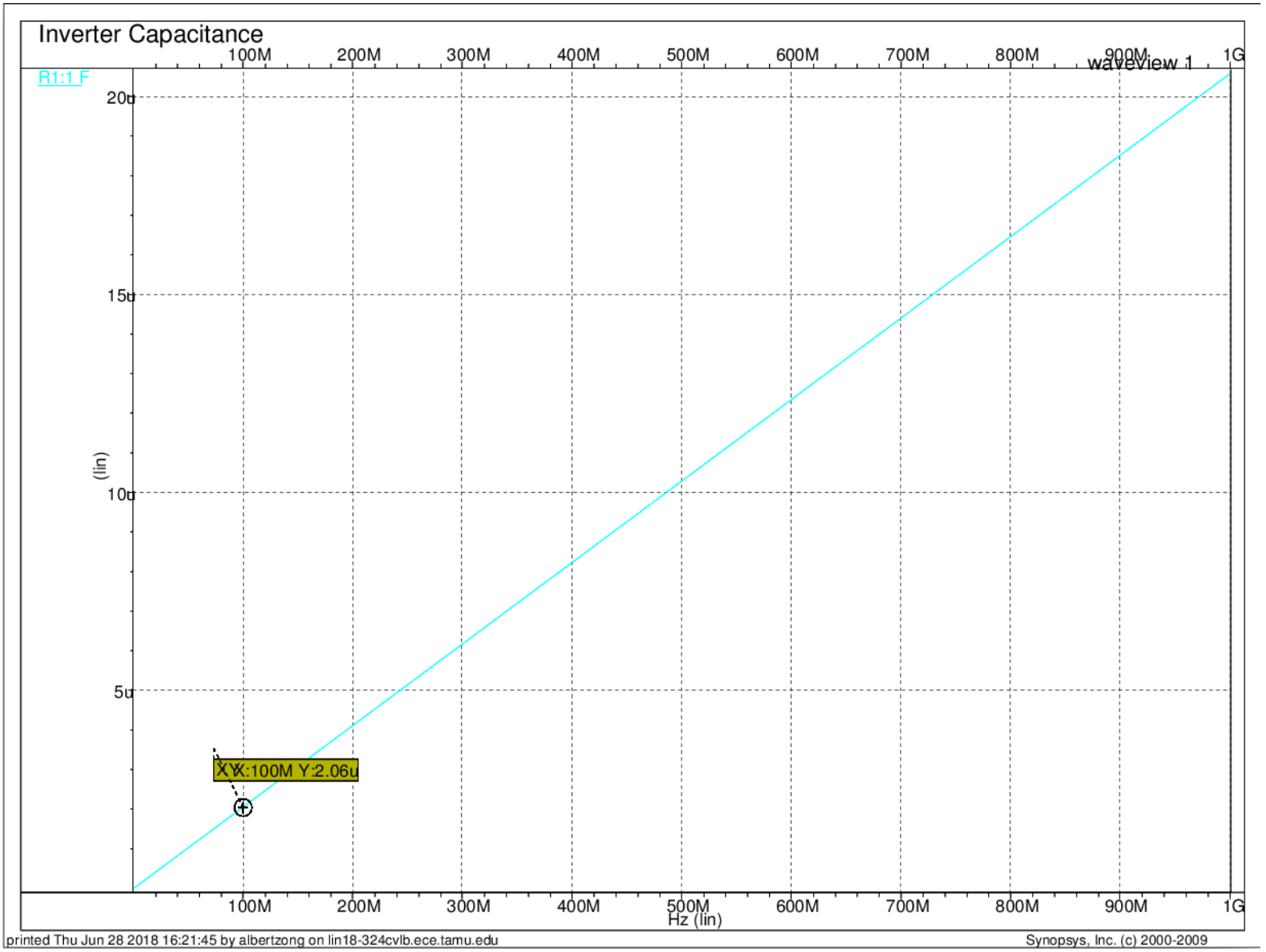
Capacitance	Rising Delay	Falling Delay	% Error
1f	45.2p	27.1p	
10f	101p	85.8p	
20f	144p	131p	
30f	188p	175p	
40f	232p	219p	
50f	277p	262p	
60f	321p	306p	
70f	368p	351p	
80f	410p	393p	
90f	451p	439p	
100f	498p	481p	3.5%



Inverter (Capacitance):

Frequency	Output Current	C = (If)/(2*pi*f)
100 MHz	2.06 uA	3.279 fF
200 MHz	4.11 uA	3.271 fF
300 MHz	6.18 uA	3.279 fF
400 MHz	8.24 uA	3.279 fF
500 MHz	10.3 uA	3.279 fF
600 MHz	12.3 uA	3.263 fF
700 MHz	14.4 uA	3.274 fF
800 MHz	16.5 uA	3.283 fF
900 MHz	18.5 uA	3.272 fF
1 GHz	20.6 uA	3.279 fF

Average Capacitance: 3.2758 fF

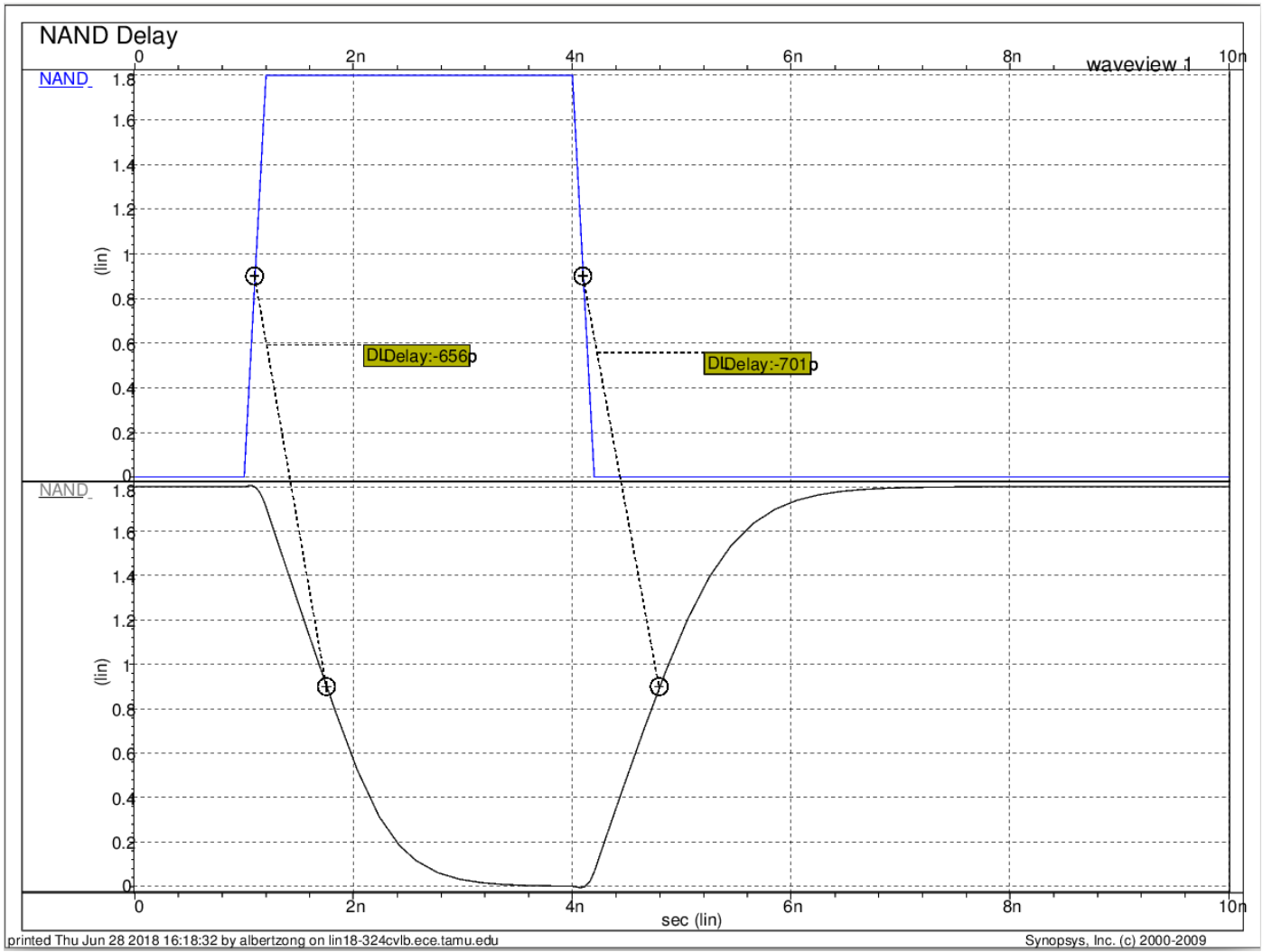


NAND

Rising Delay: 701p
Falling Delay: 656p

NAND (Delay_Table):

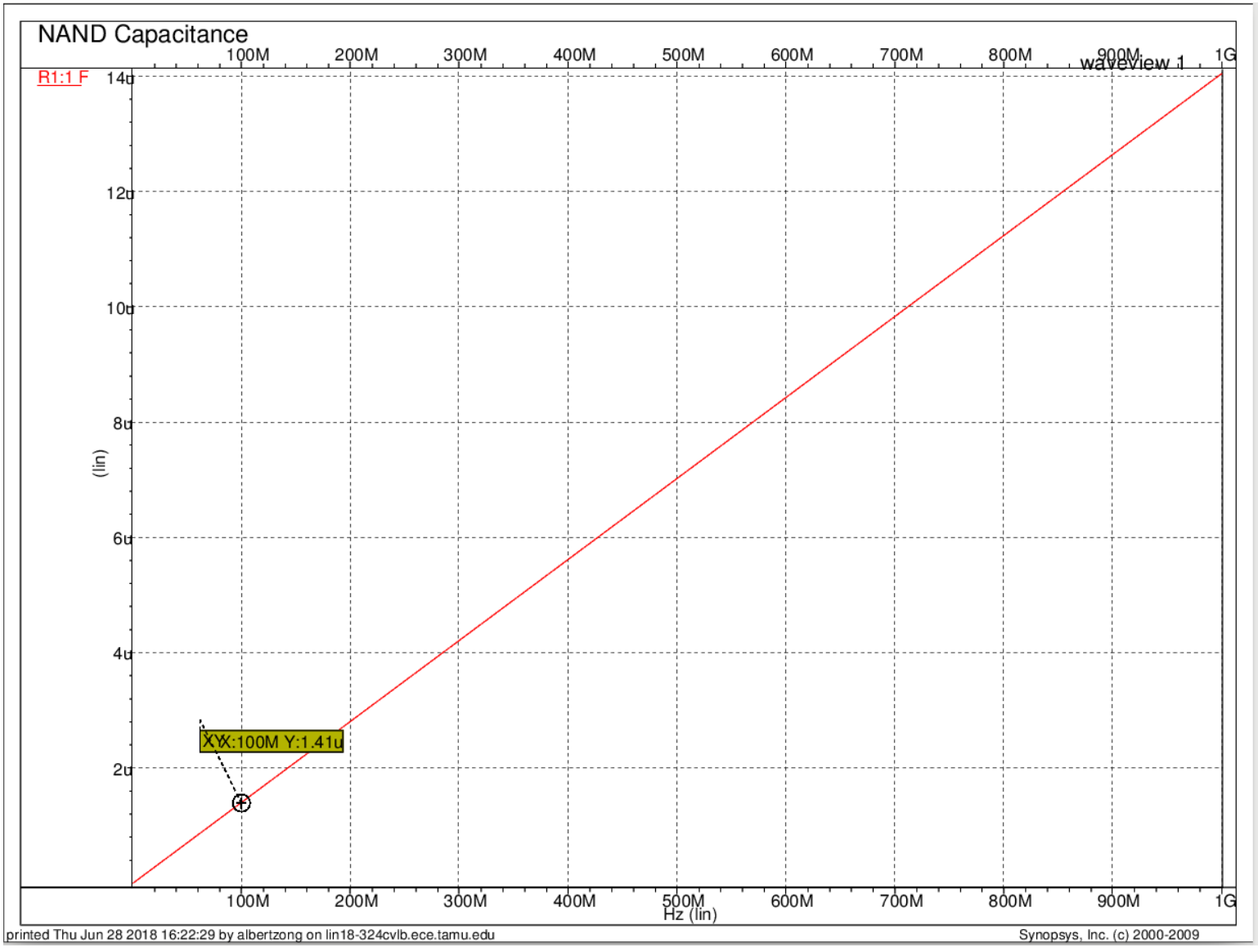
Capacitance	Rising Delay	Falling Delay	% Error
1 f	57.7 p	35.4 p	
10 f	125 p	107 p	
20 f	190 p	168 p	
30 f	254 p	229 p	
40 f	320 p	291 p	
50 f	382 p	351 p	
60 f	447 p	414 p	
70 f	511 p	474 p	
80 f	575 p	533 p	
90 f	637 p	595 p	
100 f	701 p	656 p	6.86 %



NAND (Simcap):

Frequency	Output Current	C = (If)/(2*pi*f)
100 MHz	1.40 uA	2.228 fF
200 MHz	2.81 uA	2.236 fF
300 MHz	4.21 uA	2.335 fF
400 MHz	5.62 uA	2.236 fF
500 MHz	7.02 uA	2.235 fF
600 MHz	8.42 uA	2.233 fF
700 MHz	9.83 uA	2.235 fF
800 MHz	11.2 uA	2.228 fF
900 MHz	12.6 uA	2.228 fF
1 GHz	14.0 uA	2.228 fF

Average Capacitance: 2.2322 fF

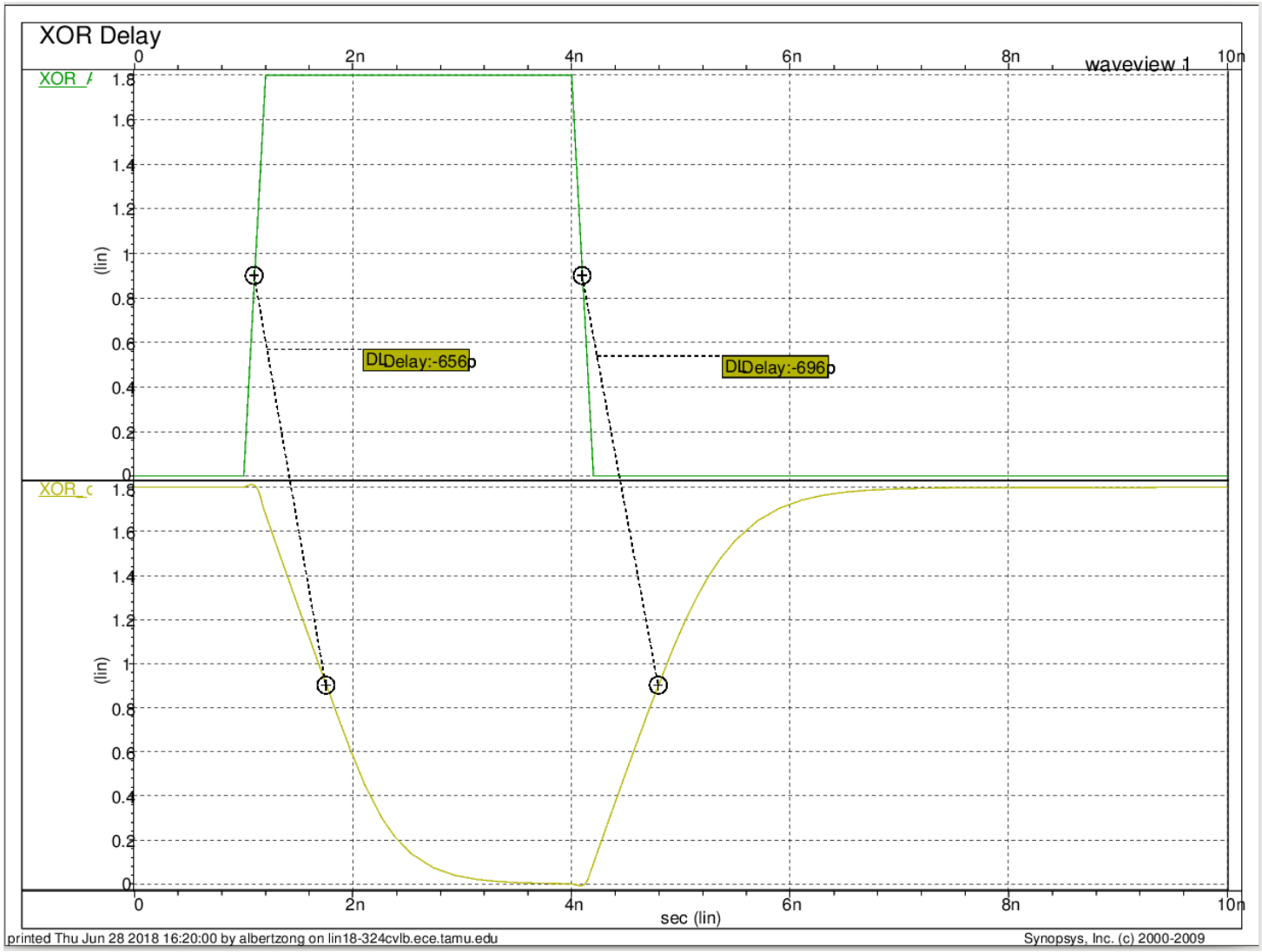


XOR

Rising Delay: 696p
Falling Delay: 656p

XOR (Delay_Table):

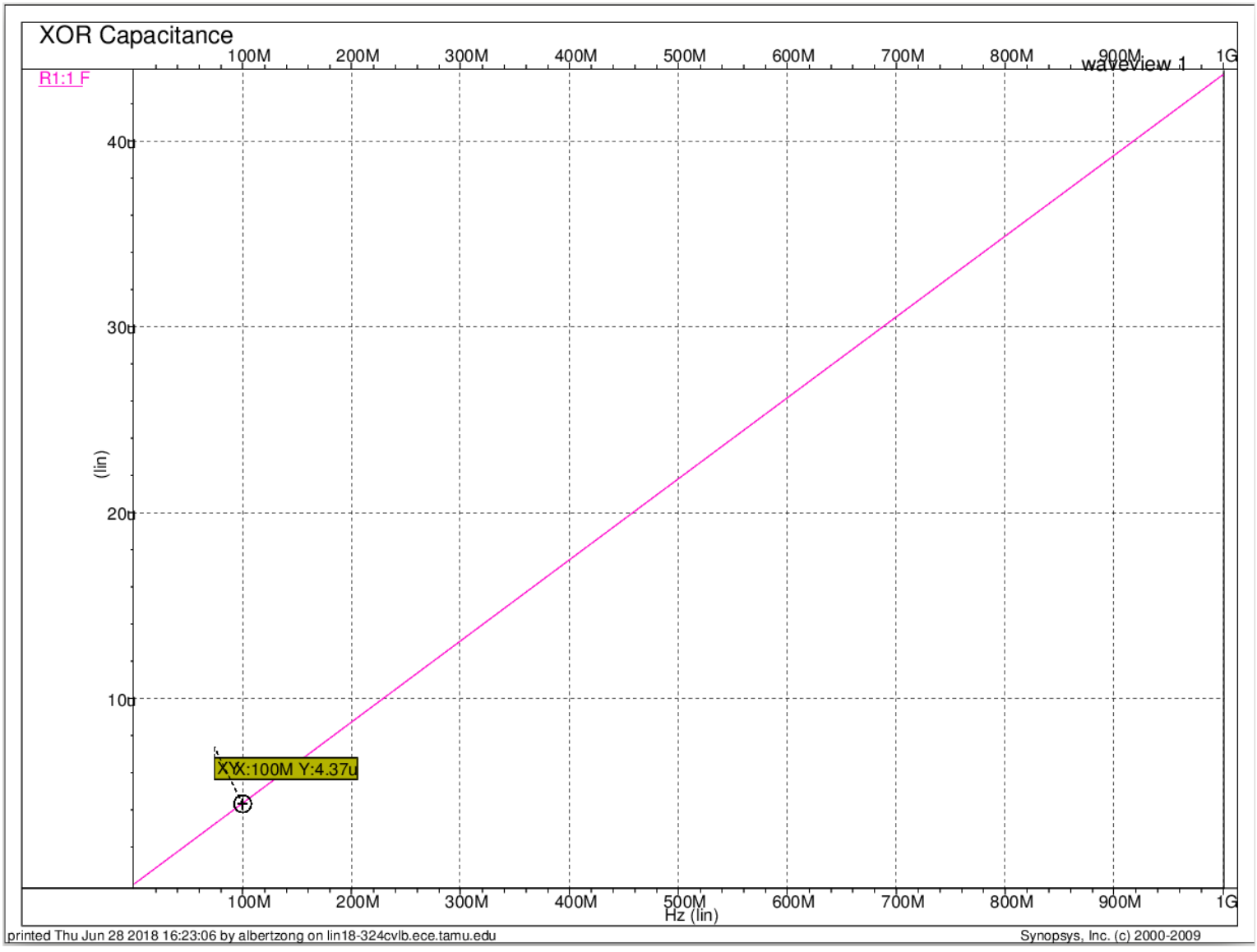
Capacitance	Rising Delay	Falling Delay	% Error
1f	52.9p	39.8p	
10f	116p	103p	
20f	181p	166p	
30f	247p	228p	
40f	310p	290p	
50f	374p	351p	
60f	439p	412p	
70f	506p	474p	
80f	566p	535p	
90f	633p	596p	
100f	696p	656p	6.1 %



XOR (Simcap):

Frequency	Output Current	C = (If)/(2*pi*f)
100 MHz	4.38 uA	6.971 fF
200 MHz	8.74 uA	6.955 fF
300 MHz	13.1 uA	6.950 fF
400 MHz	17.5 uA	6.963 fF
500 MHz	21.8 uA	6.939 fF
600 MHz	26.2 uA	6.950 fF
700 MHz	30.5 uA	6.935 fF
800 MHz	34.9 uA	6.943 fF
900 MHz	39.2 uA	6.932 fF
1 GHz	43.6 uA	6.939 fF

Average Capacitance: 6.9477 fF



Cell18.spi

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV

//Spice netlist for NAND
subckt NAND (A B output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.2u
        M1 output A VDD VDD tsmc18P w=wp l=lp
        M2 output B VDD VDD tsmc18P w=wp l=lp
        M3 output A w1 VSS tsmc18N w=wn l=ln
        M4 w1 B VSS VSS tsmc18N w=wn l=ln
ends NAND

//Spice netlist for an XOR
subckt XOR (A B output VDD VSS)
    parameters wp=1.2u lp=0.2u wn=0.3u ln=0.2u

     inv1(A A_not VDD VSS) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u
     inv2(B B_not VDD VSS) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

     M1 w1 B VDD VDD tsmc18P w=wp l=lp
     M2 output A_not w1 VDD tsmc18P w=wp l=lp
     M3 w2 B_not VDD VDD tsmc18P w=wp l=lp
     M4 output A w2 VDD tsmc18P w=wp l=lp

     M5 w3 A_not output VSS tsmc18N w=wn l=ln
     M6 VSS B_not w3 VSS tsmc18N w=wn l=ln
     M7 w4 A output VSS tsmc18N w=wn l=ln
     M8 VSS B w4 VSS tsmc18N w=wn l=ln
ends XOR
```

inverter.spi & inverter_delaytable.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi"
include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n
0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

inverter_simcap.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi"
include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (IV_in 0) vsource dc=0 mag=1

R1 (IV_in IV_in1) resistor r=0

X1 (IV_in1 IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

NAND.spi & NAND_delaytable.spi

```
;Spice netlist for NAND and a capacitor
simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi"
include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8
vvd (NAND_B 0) vsource dc=1.8

vpwl (NAND_A 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n
0]

X1 (NAND_A NAND_B NAND_OUT vdd gnd) NAND wp=0.6u lp=0.2u wn=0.3u
ln=0.2u

R1 (NAND_OUT 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND_A NAND_B NAND_OUT
```

NAND_simcap.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi"
include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8
vvd (NAND_B 0) vsource dc=1.8

acinput (NAND_A 0) vsource dc=0 mag=1

R1 (NAND_A NAND_A1) resistor r=0

X1 (NAND_A1 NAND_B NAND_out vdd gnd) NAND wp=0.6u lp=0.2u wn=0.3u
ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

XOR.spi & XOR_delaytable.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi"
include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8
vvd (XOR_B 0) vsource dc=1.8

vpwl (XOR_A 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n
0]

X1 (XOR_A XOR_B XOR_out vdd gnd) XOR wp=1.2u lp=0.2u wn=0.3u ln=0.2u

R1 (XOR_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR_A XOR_out
```

XOR_simcap.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi"
include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8
vvd (XOR_B 0) vsource dc=1.8

acinput (XOR_A 0) vsource dc=0 mag=1

R1 (XOR_A XOR_A1) resistor r=0

X1 (XOR_A1 XOR_B XOR_out vdd gnd) XOR wp=1.2u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```