TySOM-M-MPFS250T
Quick Start Guide

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Table of Contents

Table of Figures

1 Powering TySOM-M-MPFS250T

TySOM-M-MPFS250T board should be powered using a power supply equipped with a 6-pin PCIe Power Connector. A 12V and minimum 60W power supply should be used but power consumption depends on what system and peripherals are used and can be up to 200W. A 12V power supply with a 6-pin PCIe connector or an ATX power supply for PCIe cards can be used.

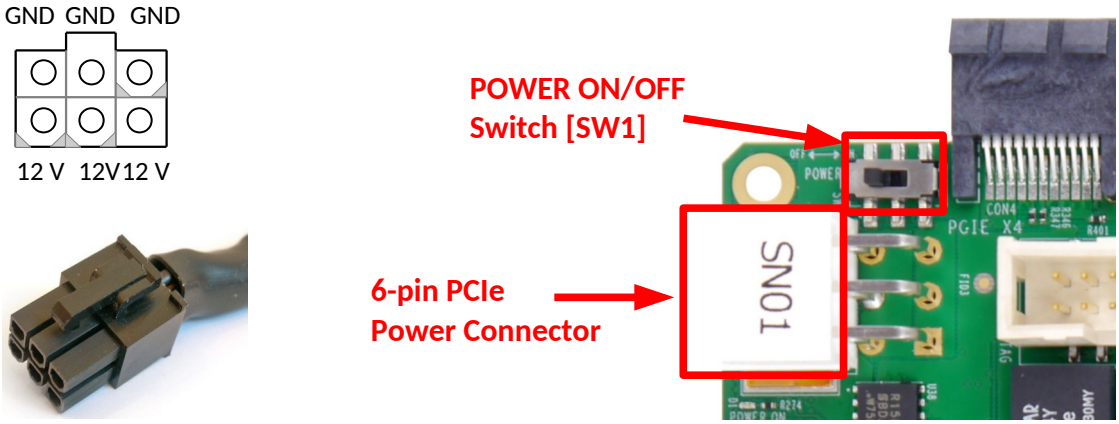

Figure 1: 6-pin PCIe Power Connector Pin Numbering and Power ON/OFF Switch Location

1.1 12V Power Supply with 6-pin PCIe Connector

Please connect the power supply to the TySOM-M-MPFS250T board power connector. Then turn the power on.

Figure 2: 12V Power Supply with 6-pin PCIe Connector

1.2 ATX Power Supply

Please connect the 6-pin connector from the ATX power supplier to the TySOM-M-MPFS250T board power connector. To turn the power on you need to pull down the PS_ON signal on the ATX power supply (short pins 13 and 14 of the main 20-pin connector). Please refer to Figure 3 for more details.

Figure 3: ATX Power Supply

2 How to Prepare TySOM-M-MPFS250T Board to work

1. Set up JTAG configuration DIP switches [S1] and [S2]. Refer to Appendix A or TySOM-M-MPFS250T_Technical_Specification chapter 3.3.4 for more information on the DIP switches configuration.

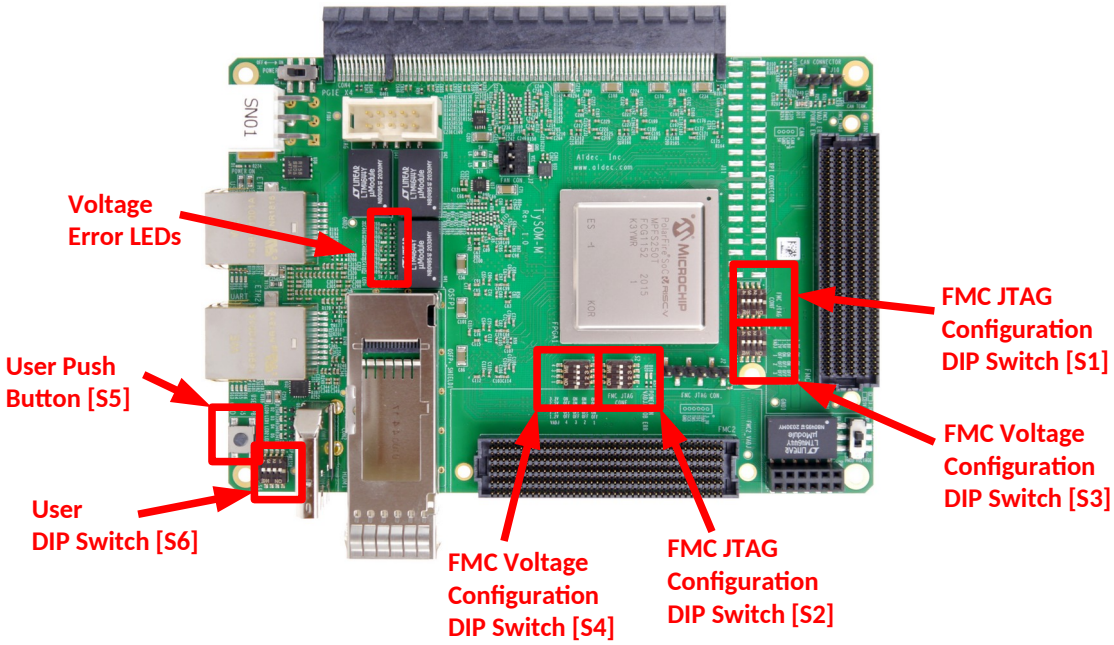

Figure 4: Configuration DIP Switches and Voltage Error LEDs

2. Connect the power supply to the TySOM-M-MPFS250T board. Make sure that the power supply is OFF.
3. Connect all optional peripherals to the TySOM-M-MPFS250T board:
   a) LAN cable to ETH1 or ETH2 connectors.
   b) HDMI cable.
   c) JTAG cable, for debug purpose.
   d) MiniB USB cable to USB UART connector.
   e) MiniB USB cable to USB connector.
   f) Insert µSD card.
   g) QSFP Cable
   h) PMOD Module
   i) Can interface
4. Insert FMC cards into the FMC connectors (optional). If the FMC Connector is used, set value of voltages using the FMC Voltage Configuration DIP Switches ([S3] for FMC1 and [S4] for FMC2). If needed, connect JTAG to the FMC JTAG connector. Refer to Appendix B or TySOM-M-MPFS250T_Technical_Specification for more information on FMC Voltage Configuration. **Note that providing wrong voltage values on the FMC Connector can damage the boards!**

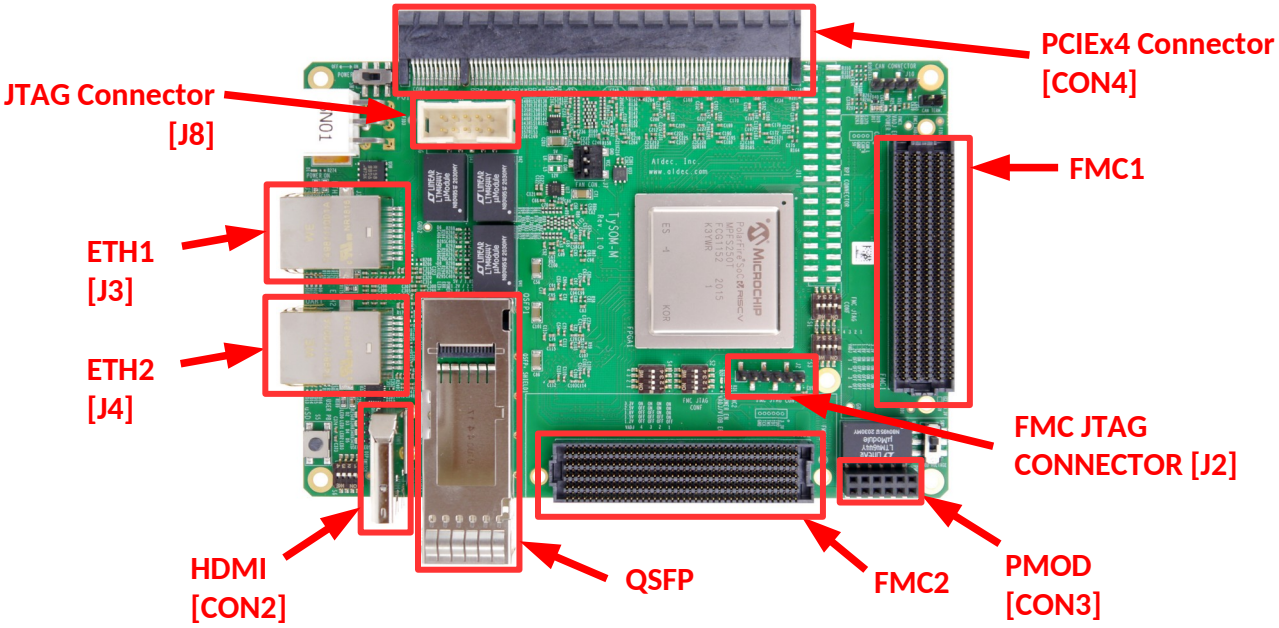

Figure 5: Peripherals Connectors Locations (TOP Side)

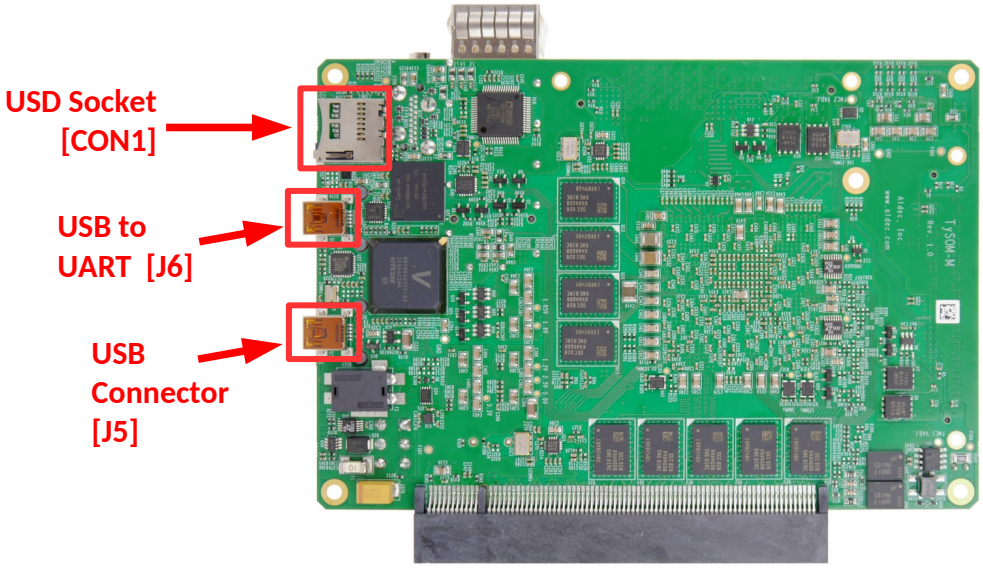

Figure 6: Peripherals Connectors Locations (Bottom Side)

3 TySOM-M-MPFS250T Board Programming – JTAG

Programming the PolarFire FPGA chip on the TySOM-M-MPFS250T board is possible using a standard FlashPro4/5 programmer connected to the JTAG Connector [J8] and the Host PC. The JTAG interface works only when the board is powered.

4 TySOM-M-MPFS250T Running Bare-Metal System

This chapter describes the steps to be taken in order to run a bare-metal application. It allows to verify the correct connection of the TySOM-M-MPFS250T board and communication by the UART console. The project below can be generated using the provided TCL script. The recommended and verified Microchip Libero and SoftConsole version is included in the folder name.

1. Before starting, check that the Aldec PMOD-UART expansion module and the Microchip FlashPro programmer are connected to the board, as shown in the picture below.

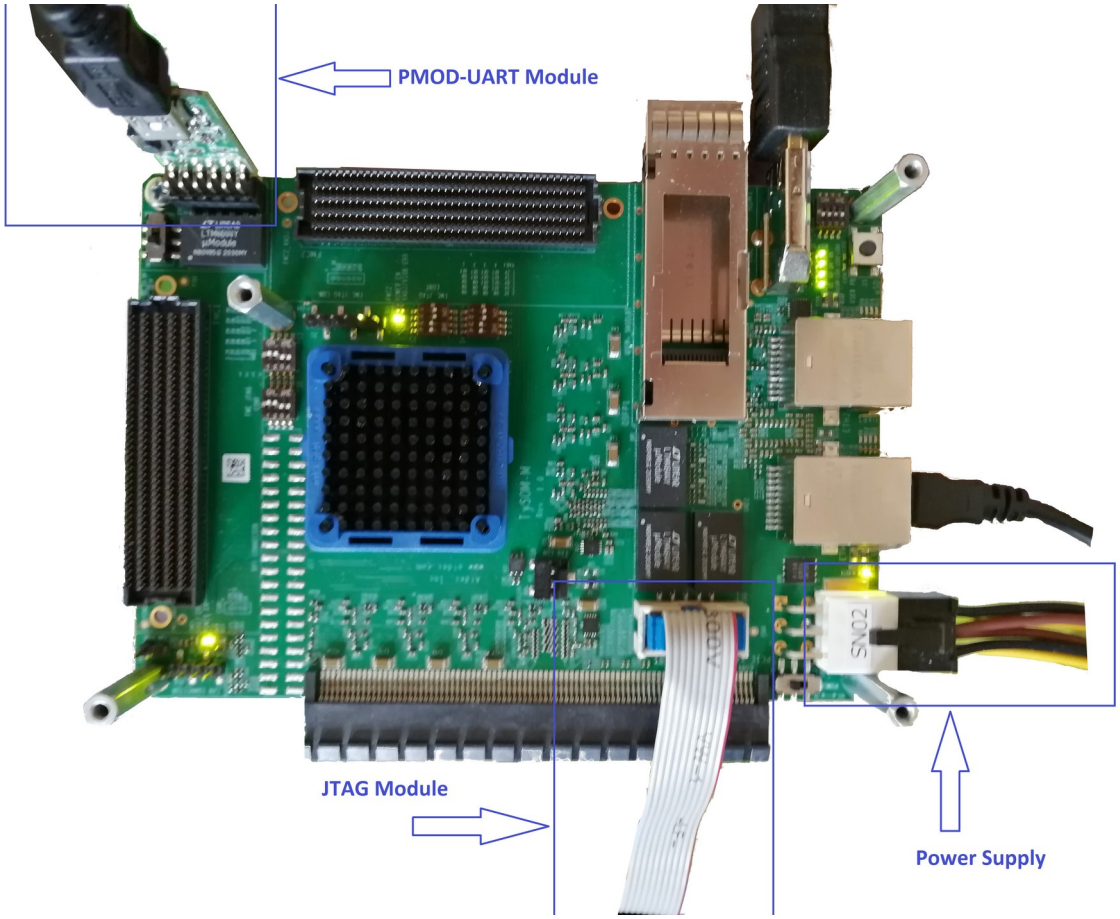

Figure 7: Example of connecting Aldec UART module and FlashPro programmer to the card TySOM-M-MPFS250T board

2. Run Libero and select the dialog box: Execute script

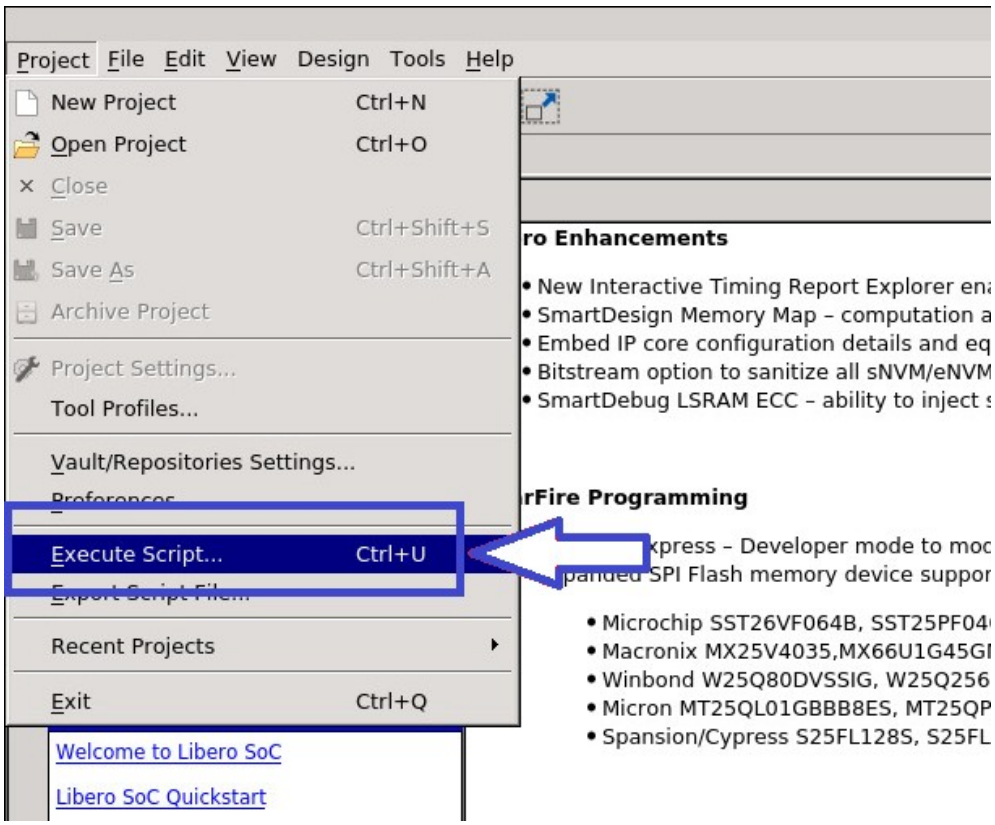

Figure 8: Selection of the Execute script dialog box in Libero

3. Specify the appropriate TCL script to be executed by Libero. Refer to Appendix C for more details about the project structure. The script automatically generates a block design suitable for the TySOM-M-MPFS250T board. In the next step user performs an implementation, inserts the bare-metal application into the eNVM memory and generates a bitstream for programming the board.
4. Navigate to the: TySOM-M-MPFS250T / BSP / designs / <Libero version> / tysom_m_mpfs250t_ref_design / TySOM-M-MPFS250T_eMMC.tcl script and run it. This generates a block design suitable for the TySOM-M-MPFS250T board. Once the process finishes, an appropriate message will be displayed in the Report window.
5. In the Design Flow tab double click the “Generate FPGA Array Data” option and wait for it to finish.
6. Double click the “Configure Design Initialization Data and Memories” option, and select the eNVM tab. Press Add→Add Boot Mode 1 Client and select the TySOM-M-MPFS250T / BSP / baremetal / <SoftConsole version> / mpfs-hal-ddr-demo / mpfs-hal-ddr-demo.hex file. If necessary, this file can be built from the provided sources of the SoftConsole project.

7. Generate the bitstream.
8. To program the board, double-click the “Run PROGRAM Action” option in the “Design Flow” part of Libero. The board is programmed through a FlashPro programmer, verify if one is connected.

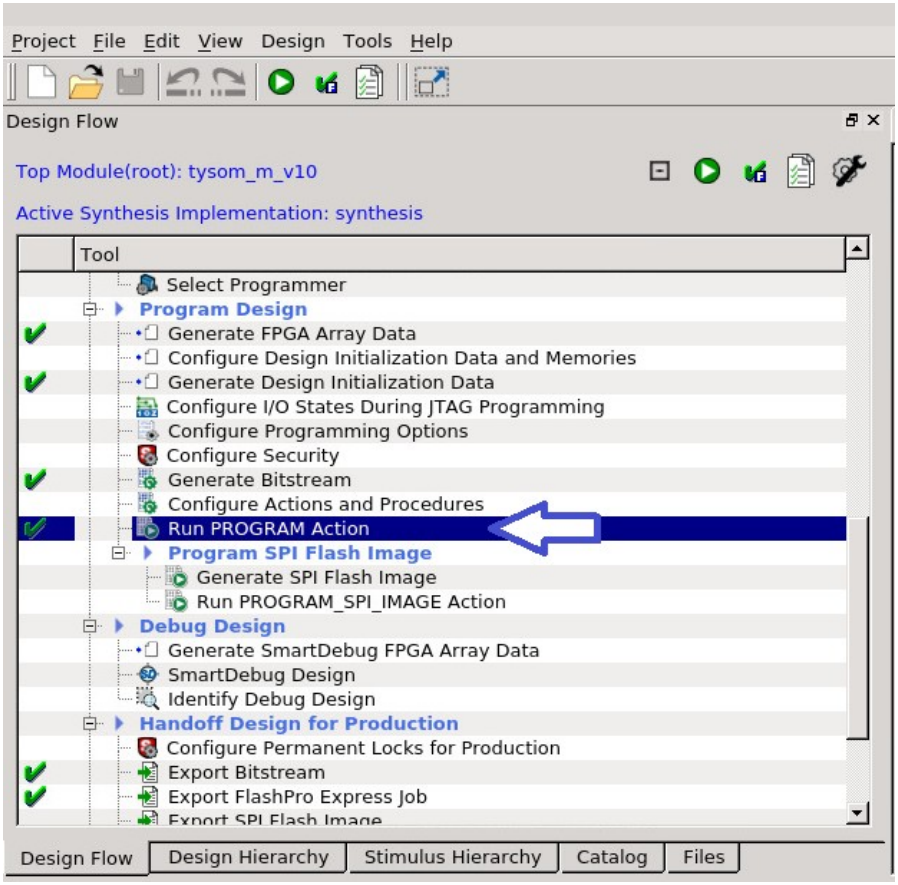

Figure 9: Example of starting the board programming.

9. After programming the board, the UART console should view the log from the application launch. The application enables two-way communication through the serial port terminal. It is possible to run a DDR test, check the correctness of the reset and read the exact parameters of the system. An example of a running application is presented below. Note that the UART terminal is connected to the host (the system default device handle is /dev/ttyACM0, baud rate 115200).

```
*********************************************************

            Accessing 2Gb DDR Non Cached

*********************************************************

        Pattern: 0x00000000wrwr
        Pattern: 0x00000001wrwr
        Pattern: 0x00000002wrwr
        Pattern: 0x00000003wrwr
        Pattern: 0x00000004wrwr
        Pattern: 0x00000005wrwr

*********************************************************

            Finished

*********************************************************


*********************************************************

            Accessing 2Gb DDR Cached

*********************************************************

        Pattern: 0x00000000wrwr
        Pattern: 0x00000001wrwr
        Pattern: 0x00000002wrwr
        Pattern: 0x00000003wrwr
        Pattern: 0x00000004wrwr
        Pattern: 0x00000005wrwr

*********************************************************

            Finished

*********************************************************

This program is run from E51
Type 0  Show this menu
Type 1  Show ddr training values
Type 2  Soft reset the MSS
Type 3  Read/ write memory DDR tests
Type 4  Display clock values
Type 5  Print debug messages from hart0
Type 6  Display MSS PLL registers
```

Figure 10: View from the running application in the UART console

Appendix A

The FMC JTAG can be configured automatically through Bus Switches [U1] and [U3]. It is possible to disconnect the JTAG interface from the FMC Connector through DIP switches [S1] — for FMC1 and [S2] — for FMC2.

Refer to Table 1 for more information on the FMC JTAG DIP Switches settings.

Table 1: FMC JTAG DIP Switches [S1] and [S2] Settings

Switch Number				Setting Description
SW1	SW2	SW3	SW4	
ON	ON	OFF	OFF	Automatic FMC Card detection and JTAG Chain configuration (default)
OFF	OFF	ON	OFF	JTAG is not connected to FMC Connector

Appendix B

There are two DIP Switches for FMC Power Distribution Configuration available on the board. They allow to configure a values of FMC Voltages VIOA and VADJ.
Refer to Table 2 and Table 3 for more details on FMC1-2 Power Distribution Configuration.

Table 2: FMC1 Power Distribution Configuration [S3]

Switch Number	FMC1_VIOA/VADJ Voltage Value				
	1.2V	1.5V	1.8V	2.5V	3.3V
SW1	OFF	ON	ON	ON	ON
SW2	OFF	OFF	ON	ON	ON
SW3	OFF	OFF	OFF	ON	ON
SW4	OFF	OFF	OFF	OFF	ON

Table 3: FMC2 Power Distribution Configuration [S4]

Switch Number	FMC2_VIOA/VADJ Voltage Value				
	1.2V	1.5V	1.8V	2.5V	3.3V
SW1	OFF	ON	ON	ON	ON
SW2	OFF	OFF	ON	ON	ON
SW3	OFF	OFF	OFF	ON	ON
SW4	OFF	OFF	OFF	OFF	ON

Appendix C

1. [Optionally] Changes to be made to solve the DDR training problem that occurs with the default settings in the project. The changes are implemented to the example bare-metal application.

   Change the following settings in the file:
   src/boards/tysom-m/platform_config/mpfs_hal_config/mss_sw_config.h:

   ```
   #define LIBERO_SETTING_TIP_CFG_PARAMS    0x07CFE00FUL
   #define USE_SW_BCLK_SCK_TRAINING    0x00000001UL
   #define SW_TRAING_BCLK_SCLK_OFFSET  0x00000006UL
   #define DEBUG_DDR_INIT
   //#define DEBUG_DDR_RD_RW_FAIL
   //#define DEBUG_DDR_RD_RW_PASS
   //#define DEBUG_DDR_CFG_DDR_SGMII_PHY
   #define DEBUG_DDR_DDRCFG
   ```

   Add a comment in the file: src/platform/mpfs_hal/common/nwc/mss_ddr.c:

   ```
   2005: //config_ddr_io_pull_up_downs_rpc_bits();
   ```

2. Project directory hierarchy:
   - TySOM-M-MPFS250T → Main directory
     - BSP → Board Support Package
       - baremetal → Bare-metal application sources to import in SoftConsole
       - designs → Libero design for the board
       - doc → Documentation
       - hss → Hart Software Services generation
       - mss → Polarfire SOC MSS Configurator
       - yocto → Yocto Project for building Linux OS

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