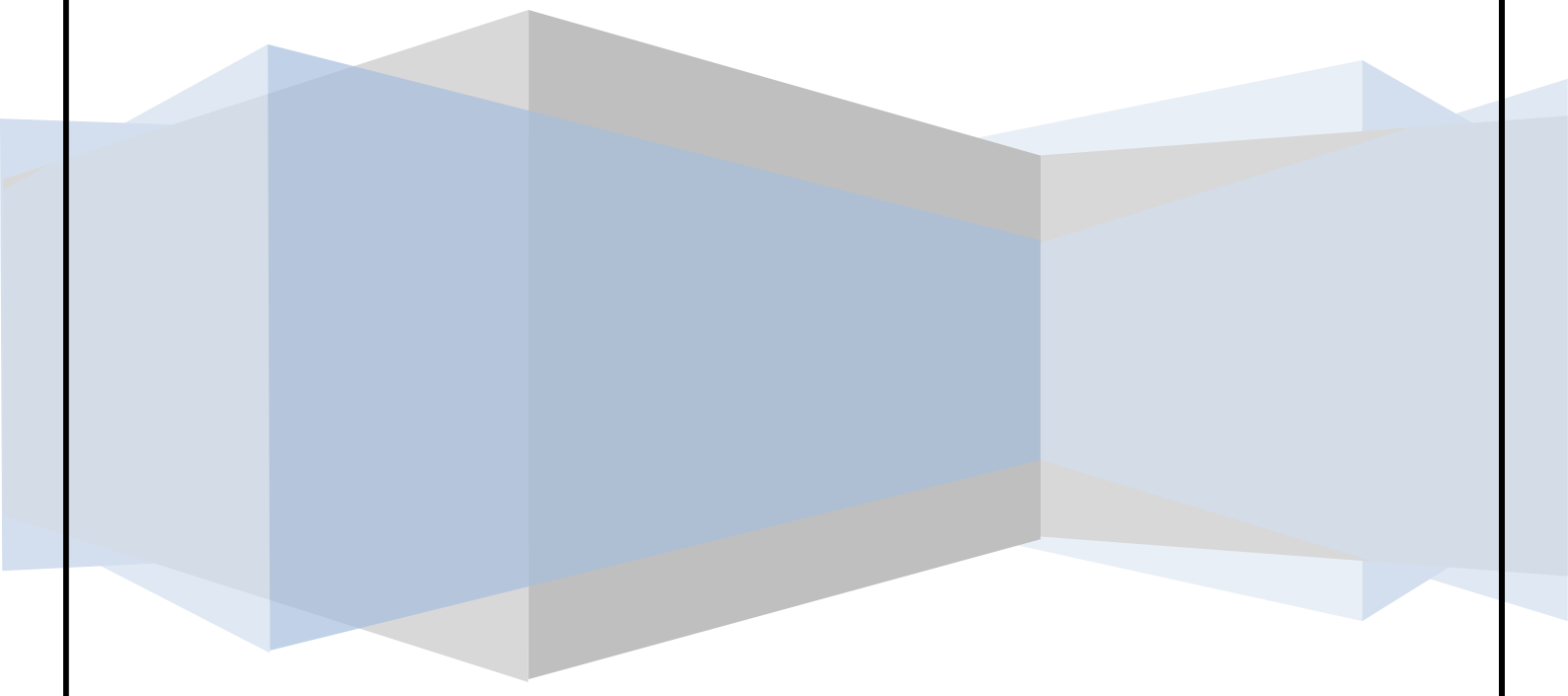
Power Optimization in FPGA Design of BCD Adder using Clock Gating

FPGA Based System Design – 22EC2020

- ALDRIN G (URK22EC1019)



BCD ADDER

Verilog code (*BEHAVIOURAL MODELING****):***

```
module bcd_adder (
   input [3:0] a,
   input [3:0] b,
   output reg [3:0] sum,
   output reg cout
);
   reg [4:0] temp_sum;

   always @(*)
   begin
      temp_sum = a + b;

      if (temp_sum > 4'd9)
      begin
         sum = temp_sum + 4'd6;
         cout = 1;
      end
      else
      begin
         sum = temp_sum[3:0];
         cout = 0;
      end
   end
endmodule
```

Power Optimized Code using Clock Gating Technique:

```
module bcd_adder (
   input [3:0] a,
   input [3:0] b,
   output reg [3:0] sum,
   output reg cout
);
   reg [4:0] temp_sum;
   reg [3:0] prev_a, prev_b;

   always @(*)
   begin
      // Check if there is any change in the inputs
      if (a != prev_a || b != prev_b)
      begin
         // Update temporary sum and store previous inputs
         temp_sum = a + b;
         prev_a = a;
         prev_b = b;

         if (temp_sum > 4'd9)
         begin
            sum = temp_sum + 4'd6;
            cout = 1;
         end
         else
         begin
            sum = temp_sum[3:0];
            cout = 0;
         end
      end
   end
endmodule
```

Key Differences after Design Optimization

Objective: Reduce toggling activity in the BCD adder to save power by updating only when inputs change.

Modifications:

1. **Previous State Registers (`prev_a`, `prev_b`)**: Store the last state of inputs `a` and `b`.
2. **Condition for Computation**: Add a check in the `always` block to update `temp_sum` only when `a` or `b` changes.

Result: This minimizes unnecessary updates, reducing switching activity and saving power by avoiding redundant computations.

Applying Clock Gating for Power Optimization

1. **Purpose of Clock Gating**: Reduces power consumption by activating logic only when necessary.
2. **Clock Gating Mechanism**: Adds a clock enable signal to control when the logic block executes.
3. **Effect on BCD Adder**: Ensures the BCD adder updates only when there's a change in inputs, reducing unnecessary computations.
4. **Simulation in Combinational Logic**:
    - Since the BCD adder is a combinational block (without a clock signal), we simulate clock gating.
    - Implement a condition to perform addition only if `a` or `b` changes.
5. **Power Savings**: Minimizes toggling activity and power consumption by preventing redundant updates to `temp_sum`.

Comparision Table:

Power Parameter	Unoptimized Design	Optimized Design	Power Reduction (W)	Percentage Reduction (%)
Total On-Chip Power	2.88 W	0.228 W	2.652 W	92.08%
Dynamic Power	2.801 W	0.157 W	2.644 W	94.39%
Static Power	0.078 W	0.071 W	0.007 W	8.97%

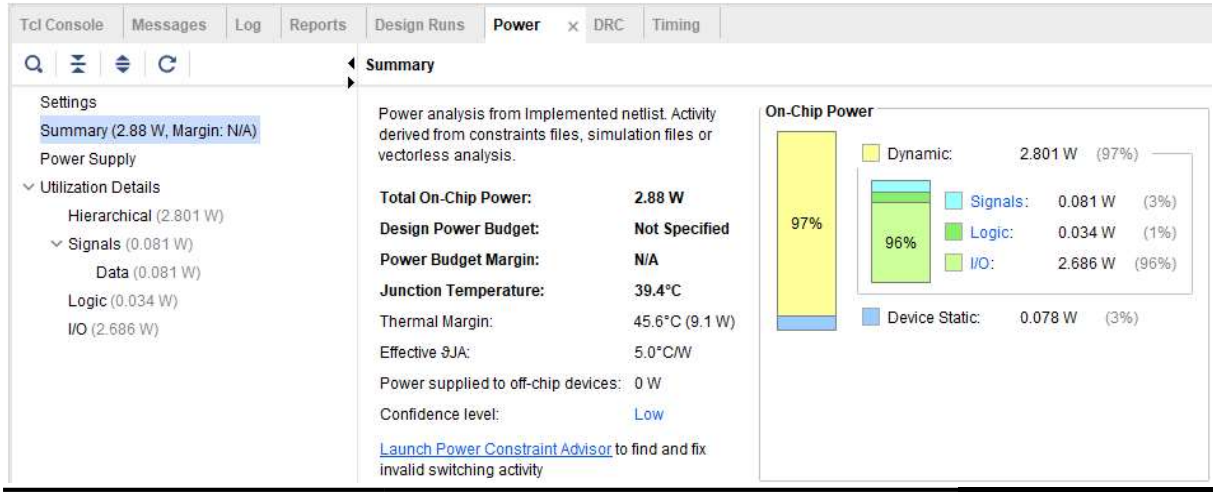
UNOPTIMIZED BCD ADDER

Power Report Summary:

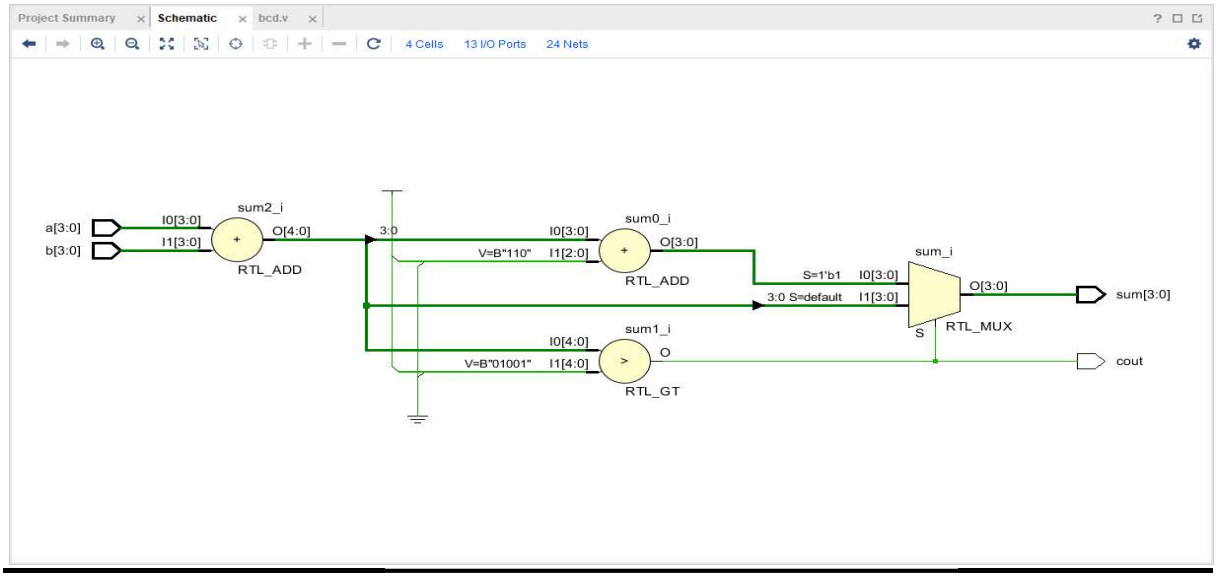
Power — **Summary** | On-Chip

Total On-Chip Power:	**2.88 W**
Junction Temperature:	**39.4 °C**
Thermal Margin:	45.6 °C (9.1 W)
Effective ϑJA:	5.0 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

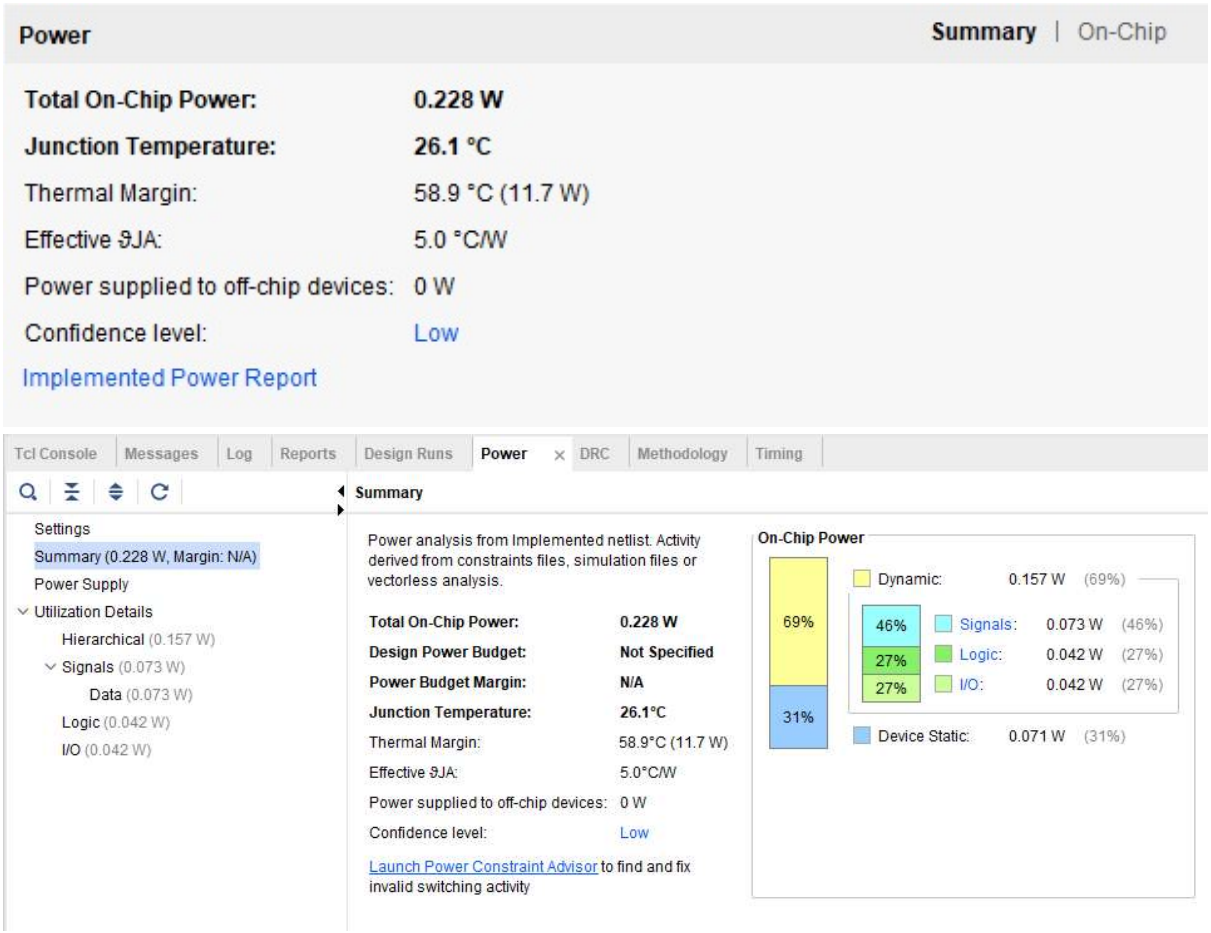


Schematic:



OPTIMIZED BCD ADDER

Power Report Summary:



Schematic: