Andy, Yu-Guang Chen

CS650 Electronic Design Automation
Programming Assignment 4 (Due: 23:59:59, 2021/05/18)

You are asked to implement the slicing floorplan design algorithm which is based on SA and normalized polish expression representation for solving rectangle packing problem. The rectangle packing problem is defined as follows: Given many rectangular modules of arbitrary sizes, place them without overlapping on a layer in the smallest bounding rectangle. It can be used to solve VLSI floorplan/placement problem.

- **Rectangle Packing Problem in this assignment is defined as follows:**

  Input: Given a set of rectangular modules each of which is a soft module with aspect ratio is ranging from **0.5 to 2**

  Output: A legal floorplan/placement result (no overlapping)

  Objective: The area of the packing area is as small as possible

- **Input file format**

The first line gives the number of modules, denoted by *n*. From line 2 through line *n*+1, each line specifies the index and area of a module.

Example:

```
5            //There are 5 modules
0 120        //module 0 with area = 120
1 9300
2 7200
3 1950
4 1200
```

- **Output file format**

For each test case, output the width, height, and area of the best packing found by your program in line 1 with "blank" characters separating them. For each of the next *n* lines (with the **increasing order** of module indices), output the **coordinates** of the lower-left corner (x, y), width, and height of a module. All of the data are separated by a "blank" character. The final line is the normalized polish expression of your floorplan. Every two consecutive elements in the expression are separated by a "blank" character.

Example:

1500 1000 1500000	// width, height, area of the packing
300 200 12 10	// the lower-left corner of module 0 [(300, 200)],
	// and its width and height [(12, 10)].
500 1000 93 100	// module1
…	
400 2000 25 48	// module 4
2 3 V 1 4 H V …	// the normalized polish expression of your floorplan

Algorithm: You are asked to realize the slicing floorplan design algorithm which is based on SA and normalized polish expression representation we discussed in the class.

Requirement: You have to write this program in C or C++. You also need to write a **makefile** which can compile and execute your program directly. I will verify your program on our workstation. You should also write a report in PDF format which should at least include a description of the data structure you used and how to execute your program. The report should also include the results (width, height, and area of the packing area) and runtime for all public testcases. Compress all your source code files to a signal compress file and Name the file as PA4_studID.tar.gz. Upload your code and report to ee-class. Some testcases will be announced on the ee-class soon.

Score: Your assignment will be ranked and scored according to (1) the correctness of your solution, (2) the quality of your solution, (3) the runtime of your program, (4) the readability of your source code, (5) the report you wrote, and (6) the demo session.

If you have any question, please send Email to both me and TA 徐麒惟.