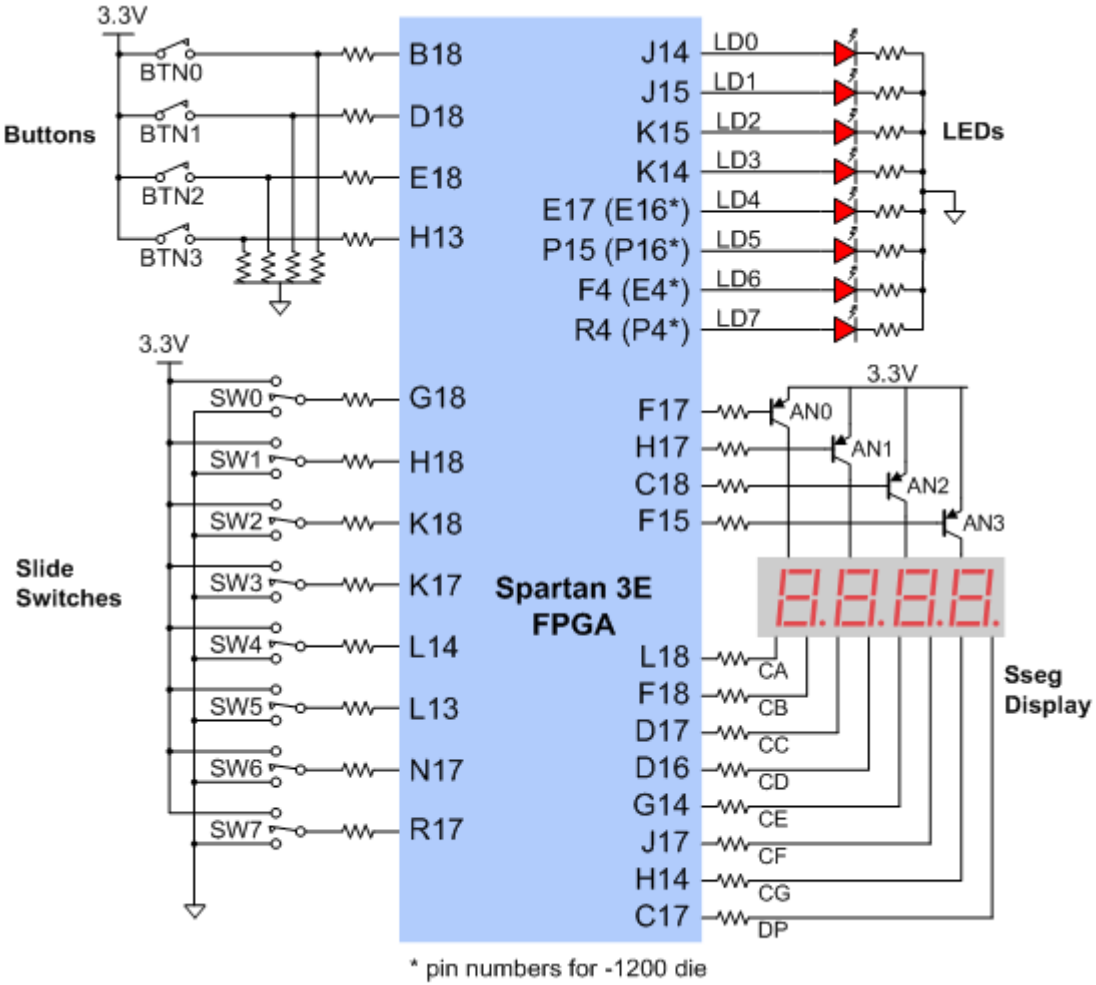
VHDL components:

1. **Instruction Fetch:** This component accesses program memory, retrieves the current instruction, and updates the program counter.
2. **Instruction Decoder:** Responsible for interpreting the instruction and generating various control signals based on the instruction type (R, I, or J).
3. **Execution Unit:** Handles arithmetic and logical operations specified by the decoded instruction.
4. **Control Unit:** Manages the control signals, configuring them based on the instruction type (R, I, or J).
5. **Memory Interface (MEM):** Interfaces with external memory to load and store data.
6. **Write-Back Unit:** Records the computation result in RAM memory.
7. **UART (Universal Asynchronous Receiver-Transmitter):** Facilitates data transmission between the FPGA board and a computer.

Additional resources

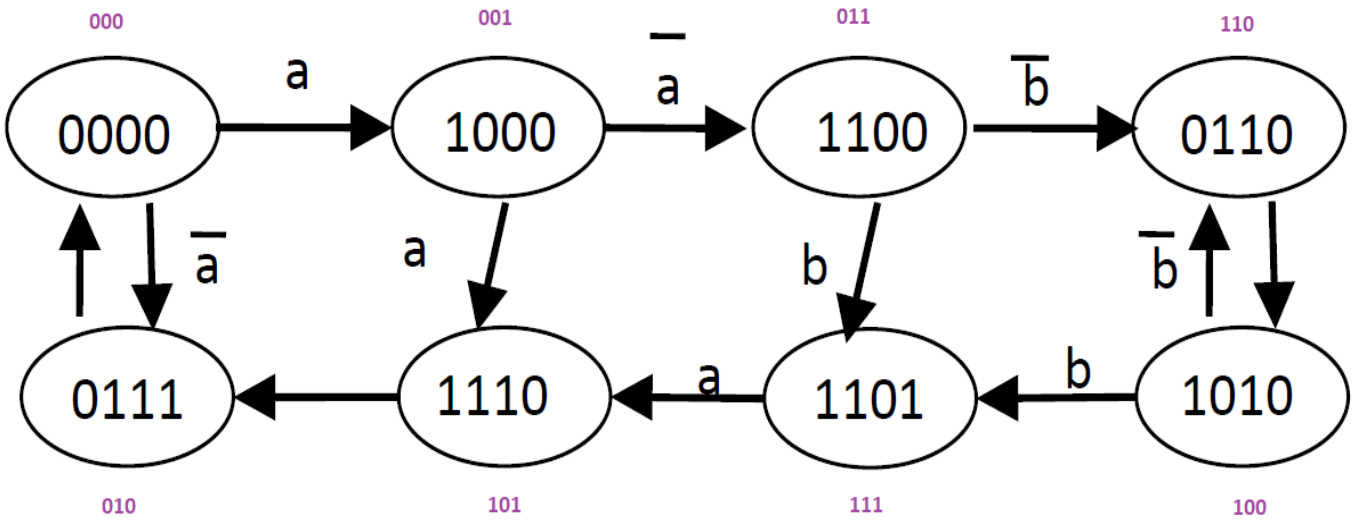
- FPGA board (preferable Spartan3E because of the constraints);
- Cable to connect the FPGA board to the computer;

Project outline



PROJECT CALCULATION

1. STATUS COODING



2. STATE DIAGRAM

STARI ACTUALE			STARI VIITOARE			IESIRI				BISTABIL JK					
Q_2	Q_1	Q_0	Q_2'	Q_1'	Q_0'	Y_3	Y_2	Y_1	Y_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	$\bar{a}$	a	0	0	0	0	0	x	$\bar{a}$	x	a	x
0	0	1	a	$\bar{a}$	1	1	0	0	0	a	x	$\bar{a}$	x	x	0
0	1	0	0	0	0	0	1	1	1	0	x	x	1	0	x
0	1	1	1	1	b	1	1	0	0	1	x	x	0	x	$\bar{b}$
1	0	0	1	$\bar{b}$	b	1	0	1	0	x	0	$\bar{b}$	x	b	x
1	0	1	0	1	0	1	1	1	0	x	1	1	x	x	1
1	1	0	1	0	0	0	1	1	0	x	0	x	1	0	x
1	1	1	1	0	1	1	1	0	1	x	0	x	0	x	0

3. CALCULATION OF BISTABLE FUNCTIONS JK

Q_0 \ Q_2, Q_1	00	01	11	10
0	0	0	x	x
1	a	1	x	x

J_2=a*$\overline{Q_2}$*Q_0+Q_1*Q_0

Q_0 \ Q_2, Q_1	00	01	11	10
0	x	x	0	0
1	x	x	0	1

K_2=$\overline{Q_1}$*Q_0

Q_0 \ Q_2, Q_1	00	01	11	10
0	$\bar{a}$	x	x	$\bar{b}$
1	$\bar{a}$	x	x	1

J_1=$\bar{a}$*$\overline{Q_2}$+$\bar{b}$*Q_2+ Q_2*Q_0

Q_0 \ Q_2, Q_1	00	01	11	10
0	x	1	1	x
1	x	0	0	x

$K_1=\overline{Q_0}$

Q_0 \ Q_2, Q_1	00	01	11	10
0	a	0	0	b
1	x	x	x	x

$J_0=a*\overline{Q_1}*\overline{Q_2}+b*Q_2*\overline{Q_1}$

Q_0 \ Q_2, Q_1	00	01	11	10
0	x	x	x	x
1	0	$\overline{b}$	0	1

$K_0=\overline{b}*Q_1*\overline{Q_2}+\overline{Q_1}*Q_2$

4. OUTPUTS CALCULATION

Q_0 \ Q_2, Q_1	00	01	11	10
0	0	0	0	1
1	1	1	1	1

$Y_3 = Q_2 * \overline{Q_1} + Q_0$

Q_0 \ Q_2, Q_1	00	01	11	10
0	0	1	1	0
1	0	1	1	1

$Y_2 = Q_1 + Q_0 * Q_1$

Q_0 \ Q_2, Q_1	00	01	11	10
0	0	1	1	1
1	0	0	0	1

$Y_1 = \overline{Q_0} * Q_1 + \overline{Q_1} * Q_2 + \overline{Q_0} * Q_2$

Q_0 \ Q_2, Q_1	**00**	**01**	**11**	**10**
0	0	1	0	0
1	0	0	1	0

$$Y_0 = \overline{Q_0} * \overline{Q_2} * Q_1 + Q_1 * Q_2 * Q_0$$