Analytical Optimization for Robust and Efficient Analog IC Design Automation

Alec S. Adair, *Member, IEEE* and Armin Tajalli, *Senior Member, IEEE*
The University of Utah
E-mail: alec.adair@utah.edu

***Abstract*—This article presents a methodology to automatically and optimally design and size analog circuits through an analytically derived objective function and constraints based on given specifications, implement their layout, and produce the corresponding Graphic Data System (GDS) files. To implement this flow, a python implementation of the C/ID methodology is used for technology characterization and lookup tables (LUTs) generation. An open source layout generation platform is used for producing circuit layout from an optimized design in an automatized flow. To adequately implement the flow, a method to analyze complexity of circuit networks, and the concept of "reducibility of problem dimension" is provided. An analytical approach is proposed to formulate a general and technology-agnostic optimization process that is expandable to high degrees of dimensionality for a wide variety of various circuit topologies, accounting for process and temperature variations while maintaining low computational complexity and high accuracy with no simulation iterations required. The methodology and approach affords the ability for clear visualization of design space and and optimums. From this analysis, technology-agnostic topology factors, compute complexity degree, and design scripts will be derived. A case study on a Current Mirror Operational Transconductance Amplifier (CM OTA) illustrates the approach, showing optimal design points for power minimization. The process includes SPICE simulation, layout generation via the ALIGN analog layout generator, and an example using open source Electronic Design Automation (EDA) tools and Skywater's 130 nm design kit, with results compared across analysis, schematic, and post layout netlist simulations. All results, designs, and scripts are publicly available for transparency and easy reproducability.**

***Index Terms*—$\mathrm{C/I_D}$ methodology, circuit design methodology, $\mathrm{gm/I_D}$ tran-conductance efficiency, dimensionality reduction, operational trans-conductance amplifier, convex optimization, computational complexity, field effect transistor, integrated circuit design.**

I. Introduction

Analog Integrated Circuit (IC) design methodologies and automation tools have all lacked behind their respective counter parts in the digital IC design domain [1]. Concepts such as circuit topology independent generalized analyses, technology agnostic simple metrics for Dennard scaling, industry standard technology characterization paradigms, and design automation, are all still considered to be open questions within the field of analog IC design.

From the success of these aspects in the digital IC space, designers have been able to greatly benefit from high degrees of automation in design flows resulting in reduced design risk and large time, effort, and design cost savings when creating, iterating, and migrating circuit designs in a wide variety of technology nodes compared to analog IC designers. Furthermore in the IC design cycle, analog design is often the bottle-neck in both design time and risk when creating mixed signal systems and microchips [2][3]. Addressing these limitations through the development of standardized methods is crucial. By introducing methodologies that enable robust automation and optimization similar to those in digital design, design complexities and power consumption can be reduced to streamline the design process, ultimately improving efficiency and reducing costs in analog IC development. Several methodologies including the Inversion Coefficient [4][5], gm/ID [6][7] [8], and C/ID [9] methodologies have been created to address these challenges. This work proposes a flow as shown in Figure 1 and focuses on the C/ID analog and optimization design methodology, as it offers the possibility to define some fundamental concepts, such as design complexity, problem dimension, and problem reduction to enable electronic design automation tools and algorithms across a wide variety of circuit types. The $\mathrm{C/I_D}$ methodology has shown to be able optimize circuits topologies such as inverter based amplifiers [10], discrete time amplifiers and comparators [11], and a variety of continuous time amplifiers [9] in a technology agnostic and general fashion with $\mathcal{O}(1)$ computational complexity [12].

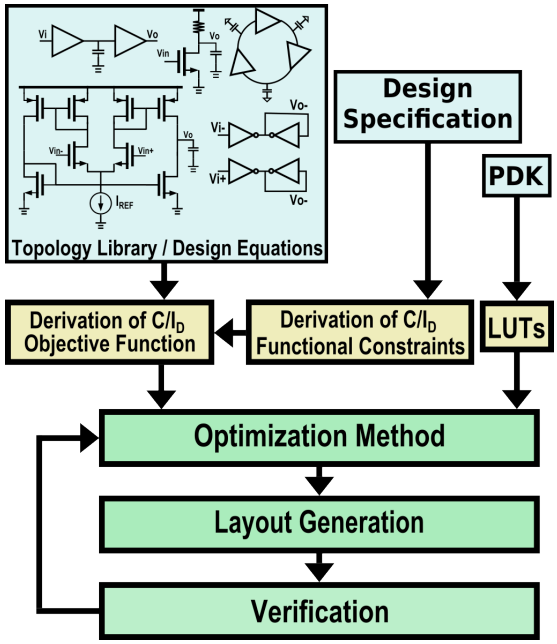

Fig. 1. Automated design flow using $\mathrm{C/I_D}$ coupled with a layout generator.

To set the stage, and properly define the theoretical basis required for automating design of analog circuits, this work will introduce concepts such as circuit problem dimension with design constraint and specification driven reducibility. The formulation of topology factor explored in works [13] and [14] is also revisited and defined further. This work provides a generalized and detailed analysis of how to apply these principles to the optimization of a given analog circuit with comprehensive results and simulations to validate the proposed methodology and flow, showcasing the effectiveness of the approach through a practical example and detailed performance evaluation. The conventional eight transistor current mirror operation transcondutance amplifier (CM OTA) shown in Figure 3 has been used as a test vehicle to demonstrate the proposed flow in Figure 1, including deriving the underlying design equations and optimization problem for a given specification. The resulting netlists from the design flow are provided as input to the ALIGN analog layout generator [18] to create Design Rule Constraint (DRC) and Layout Versus Schematic (LVS) clean layout and GDS files in a completely automated fashion. All results and scripts are published in the open source domain for transparency and accessible reproducibility at [17].

II. Background on C/ID Design Methodology

The $\mathrm{C/I_D}$ design methodology extends the $\mathrm{g_m/I_D}$ methodology by focusing on the ratio of a transistor's self loading capacitance respective to its drain current, as a function of transconductance efficiency $\mathrm{g_m/I_D}$ [6][7][8]. The C/ID methodology provides optimal robust design points across a variety of circuit types and topologies while featuring low computational complexity [12], enabling optimized rapid design convergence with minimal compute resource and technology-agnostic design scripts that can be used with various PDKs across a wide range of minimum feature sizes, including FinFETs and gate-all-around (GAA) FETs. Technology characterization is straightforward without relying on complex or proprietary information and is done with limited number of devices [9]. When coupled with an analog layout generator, it has the high potential to accelerate workflow through the complete analog design cycle with many technologies in parallel while providing power optimization and ultimately lowering design costs.

The main metrics for $\mathrm{C/I_D}$ are the effective self loading capacitance of a transistor normalized to its drain current, called characteristic capacitance denoted as $\mathcal{C}_S$, and device transconductance efficiency denoted as $\mathcal{G}_m$. This definition for characteristic capacitance enables deriving analytical closed form relationships for power versus speed and noise constraints:

$$\mathcal{G}_m = g_m/I_D, \quad \mathcal{C}_S = C_S/I_D \tag{1}$$

$\mathcal{C}_S$ is a monotonically increasing function of $\mathcal{G}_m$ that approaches infinity at maximum $\mathcal{G}_{m,max} = 1/(nU_T)$ as depicted in Fig. 2. Here, n is the subthreshold slope-factor, and U_T is the thermal voltage of a device.

Given a gain-bandwidth product (GBW in Hz denoted and ω_u in radians) specification for single dimension continuous time circuits, such as a common-source amplifier, the C/ID method defines the current consumption as:

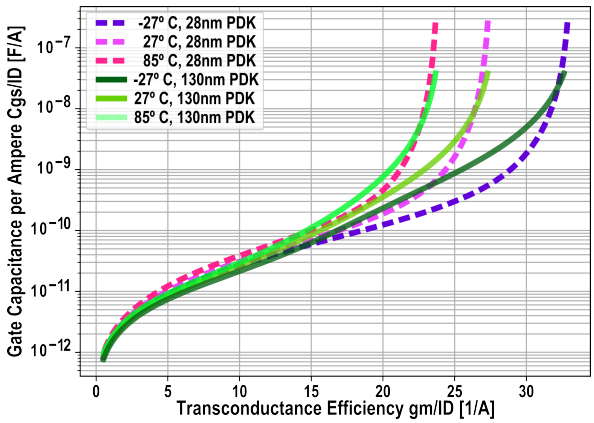

Fig. 2. $\mathcal{C}_{gs}$ vs $\mathcal{G}_m$ for a NFET 1.8V regular-VTH device, characterized at -27°, 27°, and 50°C, in 28 nm and 130 nm technologies with asymptotes at $1/\mathrm{nU_T}$ for the three different temperatures.

$$I_{DS} = I_{DS,0} \times \frac{1}{1-\omega_u/\omega_s}, \qquad I_{DS,0} = \frac{\omega_u C_L}{\mathcal{G}_m}, \quad \omega_s = \frac{\mathcal{G}_m}{\mathcal{C}_S} \tag{2}$$

The first term $I_{DS,0}$ is the current required to meet a GBW (ω_u) specification while neglecting self loading capacitance. The second term is a dimensionless quantity called the self loading excess factor which scales $I_{DS,0}$ to the needed current to compensate for self loading capacitance. In the second term, ω_s is defined as the unity gain bandwidth of the transistor due to self-loading. I_{DS} in equation 2 is a convex function with an analytically derivable global minimum shown in [14] and [15], with decision variable $\mathcal{G}_m$ and an objective function of the form $I_{DS}(\mathcal{G}_m)$.

III. Problem Dimension

The $\mathrm{C/I_D}$ methodology uses $\mathcal{G}_m$ as the only independent variable in circuit design analysis. In simple circuits such as common-source amplifiers, only one single dimensional variable $\mathcal{G}_m$ is required to optimize the design, thus dealing with single dimension unary problems with a degree of one, and single dimension input space. To frame and extend Equation 2 as an N-dimensional convex optimization problem for any given circuit topology, a more generalized analysis with an N-dimensional input space is required. Let $\mathcal{G}_{m_i}$ be the value of $\mathcal{G}_m$ for a given transistor M_i in a design containing N transistors. The set of all of the values of $\mathcal{G}_{m_i}$ for each transistor in a design constitute the input vector and decision variable for the optimization problem:

$$\mathcal{G}_{\mathbf{m}} = \langle \mathcal{G}_{m_1}, \mathcal{G}_{m_2}, \cdots, \mathcal{G}_{m_N} \rangle \tag{3}$$

The number of transistors N, in the design is considered to be the dimensionality of the input space. Each transistor in a design has a fixed number of normalized self loading capacitances and respective topology defined capacitance multipliers. For each transistor $\mathrm{M_i}$ in a design containing N

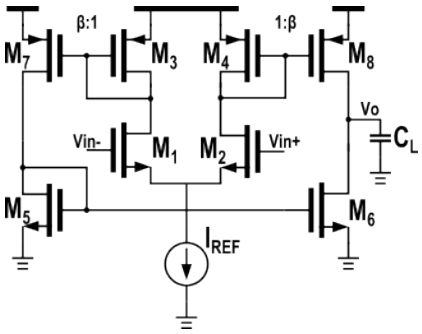

Fig. 3. Conventional 8 transistor current mirror amplifier topology.

FET transistors that each have gate, source, drain, and bulk terminals, there is a set of normalized self loading capacitances that act on transistor $\mathrm{M_i}$. This set for the i-th transistor in a design can be represented as a vector of normalized capacitors $\mathcal{C}_\mathbf{i}$:

$$\mathcal{C}_\mathbf{i} = \langle \mathcal{C}_{gs_i}, \mathcal{C}_{gd_i}, \mathcal{C}_{ds_i}, \mathcal{C}_{gb_i}, \mathcal{C}_{db_i}, \mathcal{C}_{sb_i} \rangle \tag{4}$$

Likewise in the design each transistor M_i has a vector $\mathbf{A_{C_i}}$ of topology defined capacitance multipliers for each capacitive coupling, similar to Miller multiplication factor and for some circuit toplogies maybe the Miller factor itself:

$$\mathbf{A_{C_i}} = \langle A_{gs_i}, A_{gd_i}, A_{ds_i}, A_{gb_i}, A_{db_i}, A_{sb_i} \rangle \tag{5}$$

The total effective normalized capacitance $\mathcal{C}_S$ of each transistor $\mathrm{M_i}$ is the dot product of $\mathbf{A_{C_i}}$ and $\mathcal{C}_\mathbf{i}$ which represents the normalized capacitances multiplied by their topology multipliers all summed together:

$$\mathcal{C}_{S_i} = \mathbf{A_{C_i}} \cdot \mathcal{C}_i \tag{6}$$

IV. CM OTA Design, Analysis, and Optimization

In the following Section IV-A a traditional analysis is done for the CM OTA shown in Fig. 3. The traditional analysis entails deriving the gain, stability criterion, and gain bandwidth for the circuit while total current consumption is not considered. In Section IV-B, the traditional analysis is reformulated in terms of I_D^{-1} using Table I and the steps outlined in Algorithm 1, to derive the C/I_D objective function for optimization.

A. Traditional CM OTA Design Analysis

The total transconductance G_m of the CM OTA is expressed as $G_m = \beta g_{m_{1,2}}$, while the output resistance R_o is given by $R_o = (g_{ds_6} + g_{ds_8})^{-1}$. The DC gain A_v of the OTA is the product of these parameters, calculated as $A_v = G_m R_o$, thus:

$$A_v = \frac{\beta g_{m_{1,2}}}{g_{ds_6} + g_{ds_8}} \tag{7}$$

The unity gain frequency ω_u for the OTA is given by:

$$\omega_u = \frac{G_m}{C_L + C_o} = \frac{\beta g_{m1,2}}{C_L + C_o} \tag{8}$$

where C_o is output capacitance of the OTA itself seen in parallel to C_L:

$$C_o = C_{dg8} + C_{ds8} + C_{db8} + C_{dg6} + C_{ds6} + C_{db6} \tag{9}$$

The output current of the amplifier, flowing through $\mathrm{M_6}$ and $\mathrm{M_8}$, is equal to the input differential pair current scaled by a constant factor β. The current from the differential pair formed by $\mathrm{M_1}$ and $\mathrm{M_2}$ also flows through $\mathrm{M_3}$ and $\mathrm{M_4}$, and is subsequently multiplied by β as it is mirrored through $\mathrm{M_5}$, $\mathrm{M_6}$, $\mathrm{M_7}$, and $\mathrm{M_8}$. That is:

$$I_{D_{5,6,7,8}} = \beta I_{D_{1,2,3,4}} \tag{10}$$

The slew rate (SR) of the OTA is can be approximated as

$$SR \approx \frac{\beta I_{tail}}{C_L} \tag{11}$$

Since the slew rate is not a small signal parameter of the amplifier, the small signal parasitic capacitances of the output transistors are ignored in eq. 11. With these equations β can be written in terms of (a) current ratios, (b) DC gain, (c) unity gain frequency, and (d) slew rate:

$$\begin{aligned} &\text{(a)} \quad \beta = \frac{I_{D6}}{I_{D2}} && \text{(b)} \quad \beta = \frac{A_v}{g_{m_{1,2}}\left(r_{o_6} \parallel r_{o_8}\right)} \\ &\text{(c)} \quad \beta = \frac{\omega_u (C_L + C_o)}{g_{m_{1,2}}} && \text{(d)} \quad \beta = \frac{SR \cdot C_L}{I_{TAIL}} \end{aligned} \tag{12}$$

At the drain of $\mathrm{M_2}$ and gates of $\mathrm{M_4}$ and $\mathrm{M_8}$ a non dominant pole ω_{p2} exists and is defined approximately as:

$$\begin{aligned} \omega_{p2} &\approx \frac{g_{m4}}{C_{gs4} + C_{gs8} + C_{gd8}(1 + |A_V|)} \\ \omega_{p2} &\approx \frac{g_{m4}}{C_{gs4} + C_{gs8} + C_{gd8}(1 + |\beta g_{m_{1,2}}(r_{o_6} // r_{o_8})|)} \end{aligned} \tag{13}$$

To ensure stability of the OTA, a minimum of 60° of phase margin (PM) is required, with phase margin and stability criteria for the circuit defined as:

$$\begin{aligned} PM &= 90^\circ - \tan^{-1}(\omega_u/\omega_{p2}) \geq 60^\circ \\ \omega_{p2} &\geq \alpha \omega_u, \quad \alpha = \frac{1}{\tan(30^\circ)}. \end{aligned} \tag{14}$$

The equations in 12 show that maximizing β enhances the gain, unity gain frequency, and slew rate for a fixed load capacitance and input pair bias current. However, as shown in eq. 13, ω_{p2} and β are inversely proportional, meaning that as β increases, the second pole frequency ω_{p2} decreases, bringing it closer to the unity gain bandwidth and instability. This also suggest that a maximum β threshold exists to satisfy the inequality in Eq. 14. However, determining this threshold value is complex and analytically infeasible, as the other variables in Eq. 13 depend on transistor sizing and biasing.

Algorithm 1 $\mathrm{C/I_D}$ Objective Function Derivation

procedure DeriveObjFunc(Topology, Specifications)
1. $f \leftarrow$ Derive Traditional Design Equations
2. $f(\mathcal{G}_m, I) \leftarrow$ Convert f Into Terms of Inverse Current
3. $f_0 = I_{Total}(\mathcal{G}_m) \leftarrow$ Solve For Current
4. $f_{1,2}(\mathcal{G}_m) = \leftarrow$ Derive Constraints From Specifications
5. $I^*_{TOTAL}, \mathcal{G}^*_m = \leftarrow$ Apply Optimization

end procedure

B. Derivation of I_D^{-1} Variables and Objective Function

The numerator and denominator of Eq. 8 can be divided by the drain current of devices $\mathrm{M}_{1,2}$ then put into terms of $\mathcal{G}_{m1}$ by substituting in Eq. 10 resulting in:

$$\omega_u = \frac{\beta \mathcal{G}_{m_{1,2}}}{\frac{C_L}{I_{D_{1,2}}} + \mathcal{C}_o \beta} \tag{15}$$

with the normalized effective output capacitance equal to:

$$\mathcal{C}_o = \mathcal{C}_{dg_8} + \mathcal{C}_{ds_8} + \mathcal{C}_{db_8} + \mathcal{C}_{dg_6} + \mathcal{C}_{ds_6} + \mathcal{C}_{db_6} \tag{16}$$

A graph for $\mathcal{C}_o$ can be seen in Figure 4(a).

Equation 15 can be re-written in terms of the transistor $M_{1,2}$ drain current $I_{D_{1,2}}$:

$$I_{D_{1,2}} = \frac{\omega_u C_L}{\beta \mathcal{G}_{m_{1,2}}} \times \frac{1}{1 - \omega_u \mathcal{C}_o / \mathcal{G}_{m_{1,2}}} \tag{17}$$

From Eq. 17 the total current consumption of the OTA can be derived since it is a function of β and I_{D_1}:

$$\begin{aligned} I_{\text{TOTAL}} &= I_{D_{1,2}} + \beta I_{D_{1,2}} \\ I_{\text{TOTAL}} &= \frac{\omega_u C_L}{\mathcal{G}_{m_{1,2}}} \cdot \frac{\left(\frac{1}{\beta} + 1\right)}{1 - \frac{\omega_u \mathcal{C}_o}{\mathcal{G}_{m_{1,2}}}}. \end{aligned} \tag{18}$$

This represents the traditional $\mathrm{C}/\mathrm{I}_\mathrm{D}$ optimization in the same form as Eq. 2 for the input differential pair transistors $\mathrm{M}_{1,2}$. However it is different in that $\mathcal{C}_o$ is a function of $\mathcal{G}_{m_{6,8}}$, not $\mathcal{G}_{m_{1,2}}$.

To derive ω_{p2} in terms of $\mathcal{G}_m$ and $\mathcal{C}$, the numerator and denominator of Eq. 13 can be divided by the drain current of device M_1 and be put into terms of $\mathcal{G}_{m4}$

$$\omega_{p2} \approx \frac{\mathcal{G}_{m_4}}{\mathcal{C}_{gs4} + \beta \mathcal{C}_{gs8} + \beta \mathcal{C}_{gd8}(1 + |A_V|)} \tag{19}$$

Now by setting $\omega_{p2} = \alpha \omega_u$, the current mirror factor β can be solved for in terms of the unity gain-bandwidth specification, $\mathcal{G}_{m4}$, $\mathcal{C}_{S_4}$, and $\mathcal{C}_{S_8}$:

$$\begin{aligned} \beta &= \frac{\mathcal{G}_{m_4} - \alpha \omega_u \mathcal{C}_{S_4}}{\alpha \omega_u \mathcal{C}_{S_8}} \\ \mathcal{C}_{S_8} &= \mathcal{C}_{gs8} + (1 + |A_V|)\mathcal{C}_{gd8}, \quad \mathcal{C}_{S_4} = \mathcal{C}_{gs_4} \end{aligned} \tag{20}$$

With the calculation for β, a final form for the total current consumption can be derived by plugging Eq. 20 into Eq. 18:

$$I_{\text{TOTAL}} = \frac{\alpha C_L \omega_u^2 (\mathcal{C}_{S_8} - \mathcal{C}_{S_4}) + \omega_u C_L \mathcal{G}_{m_4}}{(\mathcal{G}_{m_4} - \alpha \omega_u \mathcal{C}_{S_4})(\mathcal{G}_{m_1} - \omega_u \mathcal{C}_o)} \tag{21}$$

Finally the low frequency gain be can be derived for the circuit by dividing both the numerator and denominator in Eq. 7by the drain current of device M_1 and formulated in terms of $\mathcal{G}_m$:

$$A_V = \frac{\mathcal{G}_{m_{1,2}}}{\mathcal{G}_{o_6} + \mathcal{G}_{o_8}} \tag{22}$$

Graphs for Equations 21 and 22 can be seen in Figure 4.

The current mirror OTA leverages current mirrors to achieve current gain β, ensuring equal current density in the NFET and PFET devices respectively. This equal current density aligns the NFET and PFET respective g_m/I_D values, enabling the reduction of the design space down to an independent two-dimensional design space. Figure 4 illustrates the design space meeting the OTA gain-bandwidth requirement and chosen design point discussed in section IV-C. Lower-dimensional visualization, as shown in Figure 4, enhances intuitive understanding and is commonly used in optimization fields.

TABLE I
FET SMALL SIGNAL NORMALIZED PARAMETERS AND DERIVATIONS

Quantity	Traditional Symbol	$\mathbf{I_D^{-1}}$ Symbol	Traditional Symbol Derivation
Transconductance	$\mathbf{g_m}$	$\mathcal{G}_m$	$\mathcal{G}_m \cdot I_D$
Self Loading Cap.	$\mathbf{C}$	$\mathcal{C}$	$\mathcal{C} \cdot I_D$
Output Conductance	$\mathbf{g_o}$	$\mathcal{G}_o$	$\mathcal{G}_o \cdot I_D$
Transition Frequency	$\mathbf{f_t}$	$\mathbf{f_t}$	$\frac{\mathcal{G}_m}{2\pi\mathcal{C}}$
Maximum Gain	$\mathbf{A_v}$	$\mathbf{A_v}$	$\frac{\mathcal{G}_m}{\mathcal{G}_o}$
RMS Thermal Noise	$\sigma_\mathbf{T}^\mathbf{2}$	$\sigma_\mathbf{T}^\mathbf{2}$	$\frac{K_T k T 2\pi f_t}{\mathcal{G}_m \cdot I_D}$
Flicker Noise	$\sigma_\mathbf{f}^\mathbf{2}$	$\sigma_\mathbf{f}^\mathbf{2}$	$\frac{K_F \cdot \ln(f_h/f_l)}{\mathcal{C}_{gg} \cdot I_D}$

Symbols and Constants:
I_D: Drain Current, K_T: Thermal Noise Constant, k: Boltzmann Constant, T: Temperature (Kelvin), K_F: Flicker Noise Constant, f_h: Flicker Noise High frequency Limit, f_l: Flicker Noise Low Frequency Limit, $\mathcal{C}_{gg}$: Normalized Gate Capacitance

C. Applying Constraints and Optimization

To start the optimization process, an objective function to optimize is needed. Equation 21 represents this objective function to be minimized and is entirely in terms of $\mathcal{G}_m$. As it stands Equation 21 has an input dimensionality of 4 since it depends on the $\mathcal{G}_m$ values of $\mathrm{M}_{1,2}, \mathrm{M}_{3,4}, \mathrm{M}_{5,6}$, and $\mathrm{M}_{7,8}$. However as mentioned, due to the nature of the current mirroring within the circuit all NFET and PFET $\mathcal{G}_m$ values are the same respectively. This naturally reduces the problem dimension down to just 2 dimensions. To ensure both circuit functionality and design specifications are met, constraints must be applied to the objective function and design space outlined in section IV-B. The application of constraints can reduce both the solution space and dimensionality of the circuit.

The first constraint constraint to apply is an inequality constraint. This constraint is to ensure that the low frequency gain of the CM OTA does not go below specification. For this example the minimum gain specified is 50 V/V. The inequality constraint can be derived from (22):

$$g_1(\mathcal{G}_m) = A_V - \frac{\mathcal{G}_{m_{1,2}}}{\mathcal{G}_{o_6} + \mathcal{G}_{o_8}} \leq 0 \tag{23}$$

This equality is for circuit functionality and does not reduce the input dimension. The second constraint ensures that β

remains greater than 1. If β has a value less than 1, the current mirror gain is ineffective.

$$g_2\left(\mathcal{G}_m\right) = 1 - \frac{\mathcal{G}_{m_4} - 2\pi\alpha GBW\mathcal{C}_{S_4}}{2\pi\alpha GBW\mathcal{C}_{S_8}} \leq 0 \tag{24}$$

This inequality constraint is for circuit functionality and does not reduce input dimension.

By switching the $\mathcal{G}_{m_i}$ variables to their respective $\mathcal{G}_{m_N}$ and $\mathcal{G}_{m_P}$ counterparts, the constraints and objective function for the optimization problem can be written in standard form:

$$\begin{aligned} \underset{\mathcal{G}_\mathbf{m}}{\text{minimize}} \quad & \frac{\alpha C_L\omega_u^2(\mathcal{C}_{S_8} - \mathcal{C}_{S_4}) + \omega_u C_L\mathcal{G}_{m_P}}{\left(\mathcal{G}_{m_P} - \alpha\omega_u\mathcal{C}_{S_4}\right)\left(\mathcal{G}_{m_N} - \omega_u(\mathcal{C}_{o_N} + \mathcal{C}_{o_P})\right)} \\ \text{subject to} \quad & A_V - \frac{\mathcal{G}_{m_N}}{\mathcal{G}_{o_6} + \mathcal{G}_{o_8}} \leq 0 \\ & 1 - \frac{\mathcal{G}_{m_P} - \alpha\omega_u\mathcal{C}_{S_4}}{\alpha\omega_u\mathcal{C}_{S_8}} \leq 0 \end{aligned} \tag{25}$$

This optimization problem is solvable with an input space of two dimensions and is convex in the $\mathcal{G}_N$ dimension but monotonically increasing in the $\mathcal{G}_P$ dimension. A visualization of the solution space is shown in Figure 4.

V. Design Choice for Variation and Layout

One of the largest benefits of the C/I_D methodology is that design optimization equations and scripts can be formulated without any knowledge of process specific parameters or values. This enables generic and high degrees of automation that are suitable for many PDKs and technologies. Up to this point, the formulation of the optimization problem for the OTA has not required any process-specific parameters or discussions.

The case study example in this paper uses the Skywater 130 nm-A open source process and PDK [16] with characterization done on the 500 nm channel length 1.8V Regular-VTH devices. Figure 4 (d) shows where the temperature variation across the design space is less than 10% for a gain bandwidth product of 100Mhz and a 4pF capacitive load. To ensure functionality across temperature without a wide variation in current, this region should be chosen as the design solution subspace. In this region the minimum current consumption is at $\mathcal{G}_{m_P} \rightarrow 0$. This solution is infeasible for multiple reasons. The first reason begin extremely low $\mathcal{G}_m$ requires extremely high current density [6], which for a fixed current requires smaller devices than what is available in the PDK. Extremely small devices are also susceptible to high mismatch. The second reason is that a very large voltage drop V_{DS} across the drain source terminals of the device is required for very low $\mathcal{G}_m$ [10]. This both limits the available swing of the OTA and can also exceed the limits of the 1.8V device. For these reasons, $\mathcal{G}_{m_P}$ of the device is chosen to be 5.25 as this value represents a balance between power optimization and available headroom. $\mathcal{G}_{m_N}$ is simply chosen to be the maximum value within the 10% temperature variation boundary.

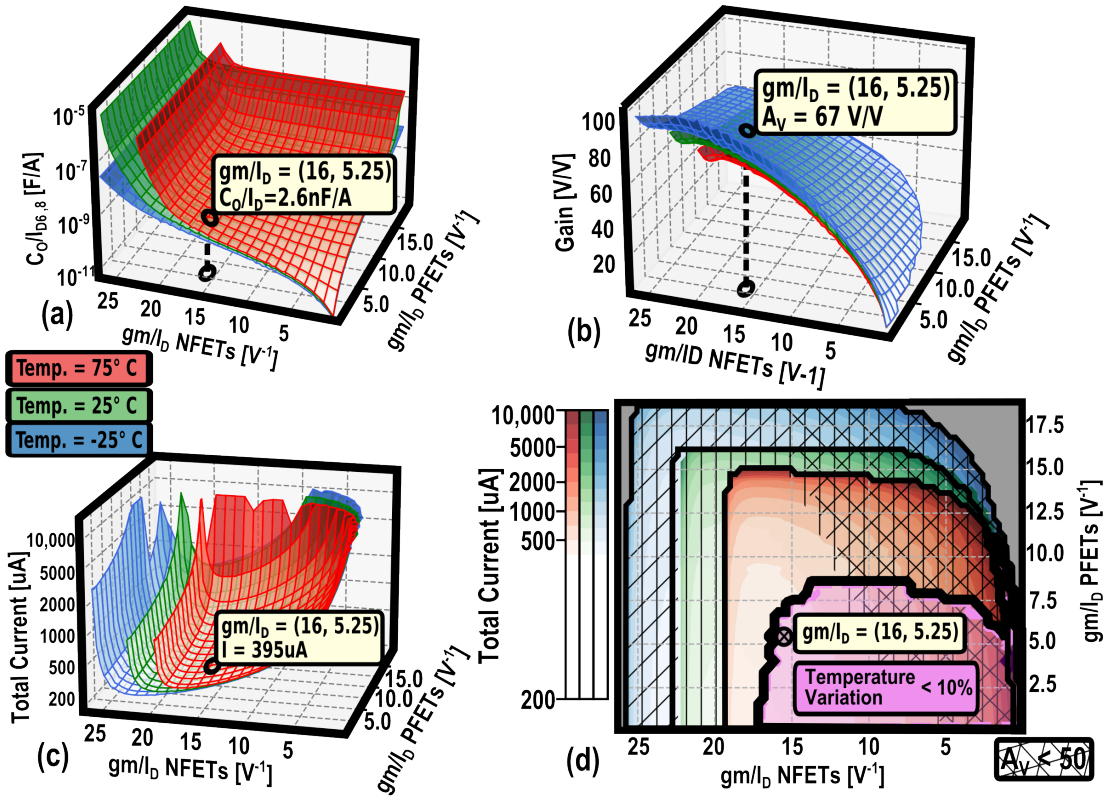

Fig. 4. CM OTA design/solution space for 100Mhz GBW, 34 dB gain, 4 pF capacitive loading with phase margin $\geq 60°$ specifications, characterized at -25°, 25°, and 75°C for 500 nm channel lengths in Skywater 130 nm technology with design points labeled at 25°C characterization: (a) Normalized output capacitance from Equation 16, (b) OTA Gain from Equation 22, (c) Current consumption for OTA from Equation 21, (d) Topological graph of current consumption showing where gain specifications not met in hatches and pink section showing less than 10% variation across temperature.

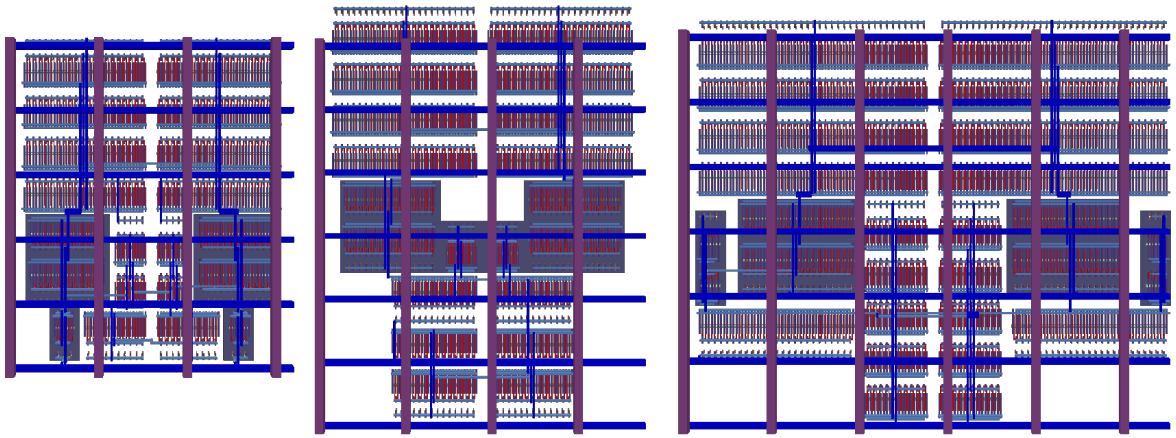

Fig. 5. GDS renderings of 3 layouts generated from ALIGN for -25°, 25°, and 75° C optimization.

To achieve a fixed $\mathcal{G}_m$ value across temperature corners for a fixed bias current, the current density of the device needs to be adjusted accordingly. This is done by adjusting the width of the device. For each corner, a layout has been generated corresponding to the correct current density to achieve the fixed $\mathcal{G}_m$ values and currents in the design. A rise in temperature corresponds to a lower current density required to achieve a given $\mathcal{G}_m$. This lower current density requirement then corresponds to a larger a layout. Layout renderings are shown in Figure 5 to achieve $\mathcal{G}_{m_N} = 16$, $\mathcal{G}_{m_P} = 16$ and 395 uA of total current consumption across three temperatures of -25°, 25°, and 75° C. Software and directions to run the sizing and layout generation scripts are found at [17]. Further work aims to address layout and design convergence.

VI. Simulation and Results

All results use the Skywater 130 nm open-source PDK [16] with 1.8V regular-vth devices at 500 nm length. The Robust Optimal and Analog Reuse (ROAR) python implementation of the C/ID methodology [17] generates SPICE netlists based on design equations from section IV-B, constraints from section IV-C, and lookup tables. The ALIGN tool [18] is used to generate the layout and GDS files, which are extracted for simulation using NGSPICE [19]. Transistor sizing is determined using ROAR's lookup tables for current density and $\mathcal{G}_m$. Characterization, design, lookup table, netlist, and layout generation scripts, are all available at [17] and crafted for ease of use and replication. Specifications, schematic simulation results, and post-layout simulation measurements for the design are shown in Table II. Bode plots for the transfer functions of the current mirror OTA simulations are show in Figure 6.

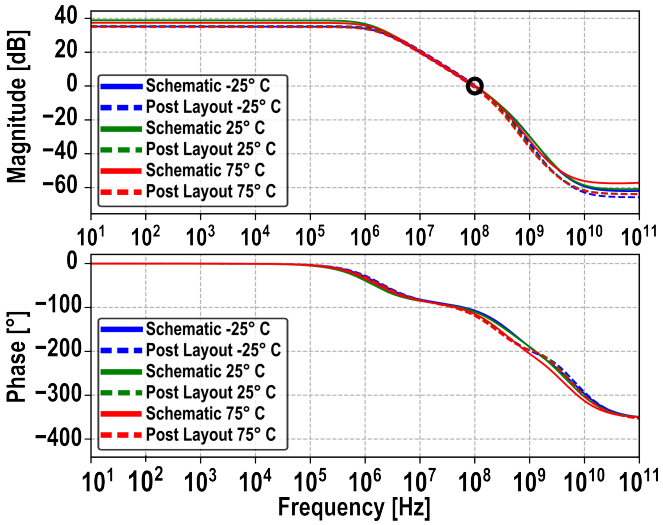

Fig. 6. Bode plots for schematic and post-layout simulations across temperature.

VII. Conclusion

A methodology to analytically optimize and automate the design and generation of a circuit netlist to be used with a layout generator has been proposed. The proposed flow combines design centering with $\mathrm{C/I_D}$ for analysis and device characterization, with ALIGN for layout generation together in an automated fashion. To establish a foundation, definitions for circuit topology complexity and reducibility of problem dimensions have been introduced. A case study involving the design of a current-mirror-based operational transconductance amplifier has been presented. The Skywater 130 nm design kit was used to implement the proposed amplifier. Simulation data has been provided to demonstrate the accuracy of the resulting design based on the post-layout extracted netlist.

TABLE II
Simulation Results Across Temperatures

Parameter	Specification	-25 °C				25 °C				75 °C			
		Schematic		Post Layout		Schematic		Post Layout		Schematic		Post Layout	
		Value	Error (%)	Value	Error (%)	Value	Error (%)	Value	Error (%)	Value	Error (%)	Value	Error (%)
Gain [dB]	$\geq$ 34	35.2	–	35.5	–	38.9	–	35.3	–	37.4	–	34.8	–
Gain Bandwidth Product [MHz]	100	97.2	-2.8	103.7	+3.7	103.7	+3.7	95.8	-4.2	96.3	-3.7	102.1	+2.1
Phase Margin [°]	$\geq$ 60	73.2	–	61.7	–	69.4	–	63.7	–	65	–	60.3	–
Current Consumption [uA]	417 / 420 / 434	425	+1.9	438	+5.0	428	+1.9	435	+3.5	443.0	+2.1	452	+4.15

A capacitive load ($\mathrm{C_L}$) of 4pF is used for all measurements.

REFERENCES

[1] I. E. Sutherland, B. F. Sproull, and D. L. Harris, *Logical Effort: Designing Fast CMOS Circuits*. San Francisco, CA: Morgan Kaufmann Publishers, Inc., 1998.

[2] ISPD '15: Proceedings of the 2015 International Symposium on Physical Design. Association for Computing Machinery, New York, NY, USA, 2015. DOI: 10.1145/2717764.

[3] A. A. Youssef, B. Murmann, and H. Omran, "Analog IC Design Using Precomputed Lookup Tables: Challenges and Solutions," *IEEE Access*, vol. 8, pp. 134640-134652, 2020. DOI: 10.1109/ACCESS.2020.3010875.

[4] C. C. Enz, and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*, Wiley, 2006.

[5] A. Mangla, 'Modeling Nanoscale Quasi-Ballistic MOS transistors: A Circuit Design Persepective," PhD Thesis, Ecole Polytechnique Federale de Lausanne (EPFL), 2017.

[6] P. G. A. Jespers, and B. Murmann, *Systematic Design of Analog CMOS Circuits*, Cambridge University Press, 2017.

[7] C. Enz, H. -C. Han and S. Berner, *Design of Low-power Analog Circuits in Advanced Technology Nodes using the Gm/ID Approach* 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5

[8] Silveira, Flandre, D. Flandre, and P. G. A. Jespers. *A Gm/ID-based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA*, IEEE J. Solid-State Circuits 31.9 (1996): 1314-131

[9] A. Tajalli, 'Power-speed trade-offs in design of scaled FET circuits using C/IDS methodology," *IEEE Trans. on Circ. and Syst. I: Regular Papers*, vol. 68, no. 2, pp. 631-640

[10] B. Jamadi, F. Ordubadi and A. Tajalli, "Design Flow to Develop Wideband Inverter-Based Circuits Using C/ID Methodology," 2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Funchal, Portugal, 2023, pp. 1-4

[11] S. Kalidasan and A. Tajalli, "Extending C/ID Methodology for Optimal Implementation of Single-Stage Discrete-Time Amplifiers," 2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Funchal, Portugal, 2023, pp. 1-4

[12] A. Adair and A. Tajalli, *Computational Efficiency of Circuit Design and Optimization Algorithms: A Comparative Study* 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5

[13] A. Aghighi, *et al.*, 'CMOS amplifier design based on extended $\mathrm{g_m/I_D}$ methodology," in *17th IEEE Int. NEWCAS Conf.*, Munich, Germany, Jun. 23-26, 2019, Paper 8056.

[14] J. Atkinson, *et al.*, 'Multi-stage current steering amplifier design based on extended $\mathrm{g_m/I_D}$ methodology," in *the 62nd Int. Midwest Symp. on Circ. and Syst.*, Dallas, TX, USA, Aug. 4-7, 2019, pp. 129-132.

[15] A. Wahid, J. Atkinson, R. Bindiganavile, F. Jazaeri and A. Tajalli, "Noise-Aware FET Circuit Design Based on C/ID-Invariant," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 7, pp. 2330-2334, July 2023

[16] SkyWater Technology Foundry, 'SkyWater Open Source PDK," *GitHub repository*, 2024. [Online]. Available: https://github.com/google/skywater-pdk.

[17] A. Adair, "DAC2025 Robust Optimal Analog Reuse (ROAR) OTA Design," GitHub repository, 2024. [Online]. Available: https://github.com/alecadair/DAC2025_ROAR

[18] ALIGN Developers, 'ALIGN: Analog Layout, Intelligently Generated from Netlists," *GitHub repository*, 2024. [Online]. Available: : https://github.com/ALIGN-analoglayout/ALIGN-public. [Accessed: Sep. 22, 2024].

[19] The NGSPICE Project, 'NGSPICE: Open Source Spice Simulator," *GitHub repository*, 2024. [Online]. Available: https://github.com/ngspice/ngspice. [Accessed: Sep. 22, 2024].