Gowin SPI Master and Slave IP

User Guide

IPUG510-1.5E,08/11/2021

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. All information in this document should be treated as preliminary. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision

Date	Revision	Description
12/24/2018	1.0E	Initial version published.
03/28/2019	1.1E	Supported devices updated.
05/08/2019	1.2E	Changed AXI interface to SRAM interface.
07/17/2019	1.3E	Interface configuration added.
09/29/2019	1.4E	SPI Master released as an IP; SPI Slave released as an open source reference design.
08/11/2021	1.5E	● IP registers description updated. ● SRAM interface timing added.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

Gowin SPI Master and Slave IP User Guide includes function introduction, working principle, signal definition, interface configuration, etc., which are designed to help you quickly understand the features and usage of Gowin SPI Master IP and Slave reference design.

1.2 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Terminology and Abbreviations

Terminology and abbreviations	Meaning
FPGA	Field Programmable Gate Array
SRAM	Static Random Access Memory
SPI	Serial Peripheral Interface

1.4 Technical Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

URL: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function Introduction

2.1 Overview

SPI (Serial Peripheral Interface) bus is a synchronous high-speed, full-duplex data communication bus. It allows serial communication and data exchange between the MCU and various peripherals. It uses only four signal lines, saving the pins of the chip and space on the layout of the PCB. Because of the ease of use of the SPI bus, this communication protocol is now integrated within more and more chips. Gowin SPI Master IP is a SPI Master controller with a synchronous SRAM interface.

Gowin SPI Slave reference design follows the SPI bus protocol and has the function of receiving and transmitting data that is primarily used to communicate with the SPI Master.

2.2 Features

2.2.1 Gowin SPI Master IP

- Full-duplex synchronous serial data transmission.
- Supports both master and slave modes of operation.
- According to the SPI running status, generate corresponding interrupt signals.
- The serial clock frequency generated by the SPI is configurable.
- Supports configurable clock polarity and phase.
- The data rx register and data tx register can be configured to be 8-32 bit width.
- Can preferentially choose to transmit the lowest or highest bit data.

2.2.2 Gowin SPI Slave

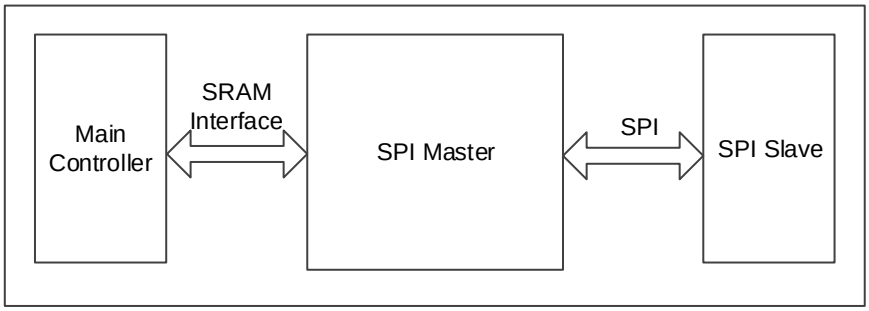
- Full-duplex synchronous serial data transmission.
- Supports configurable clock polarity and phase.
- Can preferentially choose to transmit the lowest or highest bit data.
- The data rx register and data tx register can be configured to be 8-32 bit width.

3 Working Principle

3.1 System Diagram

The main controller transmits the command or data to the SPI Master IP through the synchronous SRAM interface, and then the SPI Master IP transmits the data to the SPI Slave through the SPI; or upload the SPI Slave data to the main controller through the synchronous SRAM interface, as shown in Figure 3-1.

Figure 3-1 System Diagram



3.2 Gowin SPI Master IP Register

Gowin SPI Master IP has 5 registers:

- Rx register
- Tx register
- Status register
- Control register
- Slave select flag register

Table 3-1 Gowin SPI Master IP Register

Register	Address	Bit Width	Type	Description
Rx register	0x00	8	Read only	RX register
Tx register	0x01	8	Write/read	TX register
Status register	0x02	8	Read only	Status register
Control register	0x04	8	Write/read	Control register
Slave select flag	0x10	8	Write/read	Slave select flag

Register	Address	Bit Width	Type	Description
register				register

3.2.1 RX Register

In the data receiving path, the MISO data from the SPI bus is sent to the rx shift register. When the rx shift register is full, the data is sent to the rx register, and the RRDY (receive ready) signal is set to 1. The data in the rx register can be read out through the the synchronous SRAM interface. When the rx register is read, the RRDY signal is set to 0. If the RRDY signal is 1, it indicates that new data is sent to the rx register, and the data in the receiving register is overwritten by the new data. At this time, the ROE (receive overrun error) signal is set to 1.

Table 3-2 RX Register

N-1	reg_rxdata (DN-1 - D0)	0

Table 3-3 RX Register

Bit	Name	Type	Description	Remarks
(N-1) - 0	reg_rxdata (DN-1 - D0)	Read only	N can be 8, 16 or 32.	-

3.2.2 TX Register

In the data transmission path, data from the the synchronous SRAM interface is transferred to the tx register. When writing data to the tx register, the TRDY (transmit ready) bit in the status register is set to 0. If there is no data transmission on the bus at this time, the data in the tx register is transferred to the tx shift register, and trdy is set to 1. If TRDY is 0, indicating that new data is transferred to the tx register, and the TOE (transmit overrun error) is set to 1.

Table 3-4 TX Register

N-1	Reg_txdata (DN-1 - D0)	0

Table 3-5 TX Register

Bit	Name	Type	Description	Remarks
(N-1) - 0	Reg_txdata (DN-1 - D0)	W/R	N can be 8, 16 or 32.	-

3.2.3 Status Register

SPI with synchronous SRAM interface contains status registers and control register, which are used to trigger and clear interrupt signals.

The status register is used to check the working status of the SPI with synchronous SRAM interface. It mainly describes whether the data is received or transmitted overrun, whether the data shift register is empty, and whether the transmission and reception are ready.

Table 3-6 Status Register

31 8	7	6	5	4	3	2	1:0
	E	RRDY	TRDY	TMT	TOE	ROE	Reserved

Table 3-7 Status Register

Bit Name	Bit number	Description	Remarks
Reserved	1:0	Reserved	-
ROE	2	Rx Overrun Error 1: Error, rx data overrun, i.e., data is written during rx register read operation. When ROE occurs, if '1' is written to this bit, an ROE clear and IROE interrupt clear operation can be performed.	-
TOE	3	Tx Overrun Error 1: Error, tx data overrun, i.e., when the data in the tx register is transferred to the tx shift register, new data is transferred to the tx register. When TOE occurs, if '1' is written to this bit, a TOE clear and ITOE interrupt clear operation can be performed.	-
TMT	4	1: Empty. i.e., the tx shift register is empty.	-
TRDY	5	1: Tx register is ready to transmit data	-
RRDY	6	1: Rx register is ready to receive data	-
E	7	1: Error is the logic or operation of ROE and TOE.	-

3.2.4 Control Register

SPI control register with synchronous SRAM interface is used to set the interrupt enable signal, where the interrupt output signal O_SPI_INT in the Gowin SPI Master IP interface is generated by IROE, ITOE, ITRDY, IRRDY after processing.

Table 3-8 Control Register

31 8	7	6	5	4	3	2	1	0
	SSO	Reserved	IE	IRRDY	ITRDY	Reserved	ITOE	IROE

Table 3-9 Control Register

Bit Name	Bit Number	Description	Remarks
IROE	0	Whether to enable ROE interrupt request ● 1: Enable ● 0: Not enable	-
ITOE	1	Whether to enable TOE interrupt request ● 1: Enable ● 0: Not enable	-
Reserved	2	Reserved	-
ITRDY	3	Whether to enable TRDY interrupt request ● 1: Enable ● 0: Not enable The ITRDY interrupt is automatically cleared when the user writes data to the tx register.	-
IRRDY	4	Whether to enable RRDY interrupt request ● 1: Enable ● 0: Not enable The IRRDY interrupt is automatically cleared when the user reads data from the rx register.	-
IE	5	Whether to enable interrupt request (TOE or ROE only)	-
Reserved	6	Reserved	-
SSO	7	In master mode, it is used to select a slave. If set to 1, the data after reg_ssmask is inverted is assigned to SS_N_MASTER to determine the selected slave.	-

3.2.5 Slave Select Flag Register

In master mode, it is used to select slave and perform data transmission. The slave select flag register has a data bit for each SS_N output, and a certain bit 1 in the slave select flag register is set to enable the corresponding SS_N low. For example, if the binary data in the slave select flag register is 00000001, SS_1 is valid, and the master selects the corresponding slave of SS_1 to communicate. In addition, SPI with synchronous SRAM interface allows multiple slave select signals to be asserted simultaneously, but care must be taken to avoid contention on the MISO bus.

In slave mode, SPI with synchronous SRAM interface cannot initiate data transmission by itself, and data transmission is only possible when the SS_N input is low.

Table 3-10 Slave Select Flag Register

31 N	N-1 0
Reserved	Slave Select

Table 3-11 Slave Select Flag Register

Bit Name	Bit number	Description	Remarks
Slave Select	[N-1] - 0	Active-low, N defaults to <=8	-
Reserved	31 - N	Reserved	-

3.2.6 SRAM Interface Timing

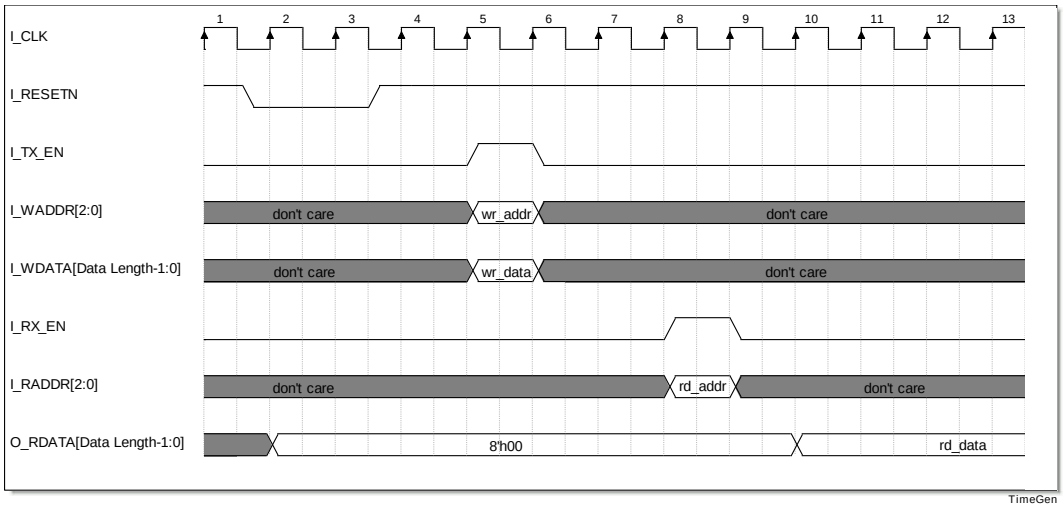
SPI Master IP can receive commands or data from the master controller through the synchronous SRAM interface, and can also return data to the master controller.

If the master controller performs write operation through synchronous SRAM interface, it needs to pull up the I_TX_EN signal for at least one I_CLK clock cycle and input the I_WADDR and I_WDATA signals at the same time.

If the master controller performs read operation through synchronous SRAM interface, it needs to pull up the I_RX_EN signal for at least one I_CLK clock cycle and input the I_RADDR signal at the same time. When the interface detects a read operation request on the rising edge of one I_CLK clock, it will wait for at least one cycle before returning the corresponding data; and read data once from a valid address in one I_CLK.

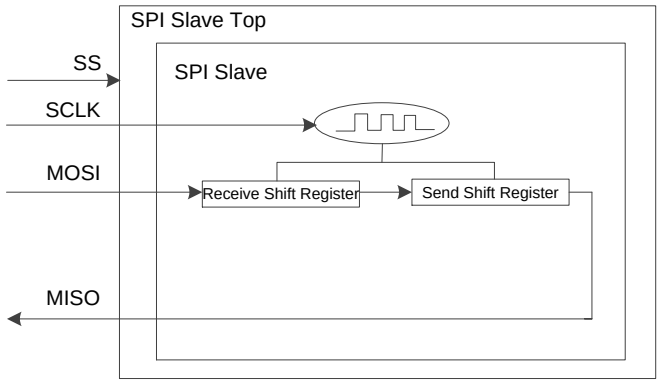
SPI Master IP synchronous SRAM interface write/read operation timing is shown in Figure 3-2.

Figure 3-2 SRAM Interface Timing



3.3 Gowin SPI Slave Implementation

Figure 3-3 SPI Slave Implementation Block Diagram



SPI Slave reference design includes an rx module and tx module.

1. Receive data

The MOSI data is transmitted to the receive shift register bit by bit by the action of the SCLK clock. According to the configured parameter SHIFT_DIRECTION, it is determined whether the data in the shift register is MSB-->LSB or LSB-->MSB; the bit width of the receive shift register is determined by the configured parameter DATA_LENGTH.

2. Send data

The data in the send shift register is transmitted to MISO bit by bit by the action of the SCLK clock. According to the configured parameter SHIFT_DIRECTION, the transmission order is determined to be MSB-->LSB or LSB-->MSB; the bit width of the send shift register is determined by the configured parameter DATA_LENGTH. When the number of tx (rx) bits reaches the configured DATA_LENGTH, the data in the receive shift register is transferred to the send shift register, thereby realizing the data exchange between the Master and the Slave.

4 Signal Definition

4.1 Gowin SPI Master IP

4.1.1 SRAM Interface Signal

Table 4-1 SRAM Interface Signal Definition

No.	Signal name	I/O	Description	Remarks
1	I_CLK	I	Working clock, rising edge sampling	-
2	RESETN	I	Reset signal	-
3	I_TX_EN	I	Write enable signal	SRAM write address channel signal
4	I_WADDR[2:0]	I	Write address signal	
5	I_WDATA[Data Length -1:0]	I	Write data signal	
6	I_RX_EN	I	Read enable signal	SRAM read address channel signal
7	I_RADDR[2:0]	I	Read address signal	
8	O_RDATA[Data Length -1:0]	O	Read data signal	

4.1.2 SPI Signal

Table 4-2 SPI Signal Definition

No.	Signal name	I/O	Description	Remarks
1	SCLK_MASTER	output	Serial clock	Master mode
2	SS_N_MASTER	output	Slave select signal, active-low.	
3	MOSI_MASTER	output	Master output, slave input.	
4	MISO_MASTER	input	Master input, slave output.	
5	SCLK_SLAVE	input	Serial clock	Slave mode
6	SS_N_SLAVE	input	Slave select signal, active-low.	
7	MOSI_SLAVE	input	Master output, slave input.	
8	MISO_SLAVE	output	Master input, slave output.	
9	O_SPI_INT	output	Interrupt signal	

4.2 Gowin SPI Slave

Table 4-3 SPI Slave Signal Definition

No.	Signal name	I/O	Description	Remarks
1	SCLK	input	Clock signal	-
2	SS	input	Slave select signal	-
3	MOSI	input	Master output, slave input.	-
4	MISO	output	Master input, slave output.	-

5 Parameter Definition

5.1 SPI Master Parameter Definition

Table 5-1 SPI Master Parameters

No.	Name	Description	Value
1	Master	Specifies SPI to work in master mode or slave mode ● 0: Slave mode ● 1: Master mode	0/1
2	Slave Number	Specifies the number of slaves that can be supported	1-32
3	Data Length	Specifies the bit width of the serial data	8-32
4	Shift Direction	Specifies the most significant bit (MSB) or least significant bit (LSB) of the priority transmission data ● 0: Priority to transfer MSB ● 1: Priority to transfer LSB	0/1
5	Clock Phase	Specifies the clock phase of the SPI ● 0: Data is valid on the first edge of SCLK ● 1: Data is valid on the second edge of SCLK	0/1
6	Clock Polarity	Specifies the clock polarity of the SPI ● 0: SCLK is active high ● 1: SCLK is active low	0/1
7	Clkcnt Width	Specifies the range of the clock counter, the bit width must be wide enough to meet the data width of SCLK	1-32
8	Clock Sel	Specifies the division factor required to generate SCLK by I_CLK. SCLK can be calculated by the following formula: SCLK= I_CLK/(2*(CLOCK_SEL+1)	0-2clkcnt_width-1
9	Delay Time	Specifies the delay time to wait before the first bit of data is transmitted after the SS_N signal is asserted. The delay time can be calculated by the following formula:Delay=DELAY_TIME*(SCLK	0-63

No.	Name	Description	Value
		period/2)	
10	Interval Length	Specifies the number of SCLK cycles that the SS_N signal waits after the SPI transfers request	0-63

5.2 SPI Slave Parameter Definition

Table 5-2 SPI Slave Parameters

No.	Name	Description	Value	Remarks
1	Shift Direction	Specifies the most significant bit (MSB) or least significant bit (LSB) of the priority transmission data ● 0: Priority to transfer MSB ● 1: Priority to transfer LSB	0/1	-
2	Clock Phase	Specifies the clock phase of the SPI ● 0: Data is valid on the first edge of SCLK ● 1: Data is valid on the second edge of SCLK	0/1	-
3	Clock Polarity	Specifies the clock polarity of the SPI ● 0: SCLK is active high ● 1: SCLK is active low	0/1	-
4	Data Length	Specifies the bit width of the serial data	8-32	-

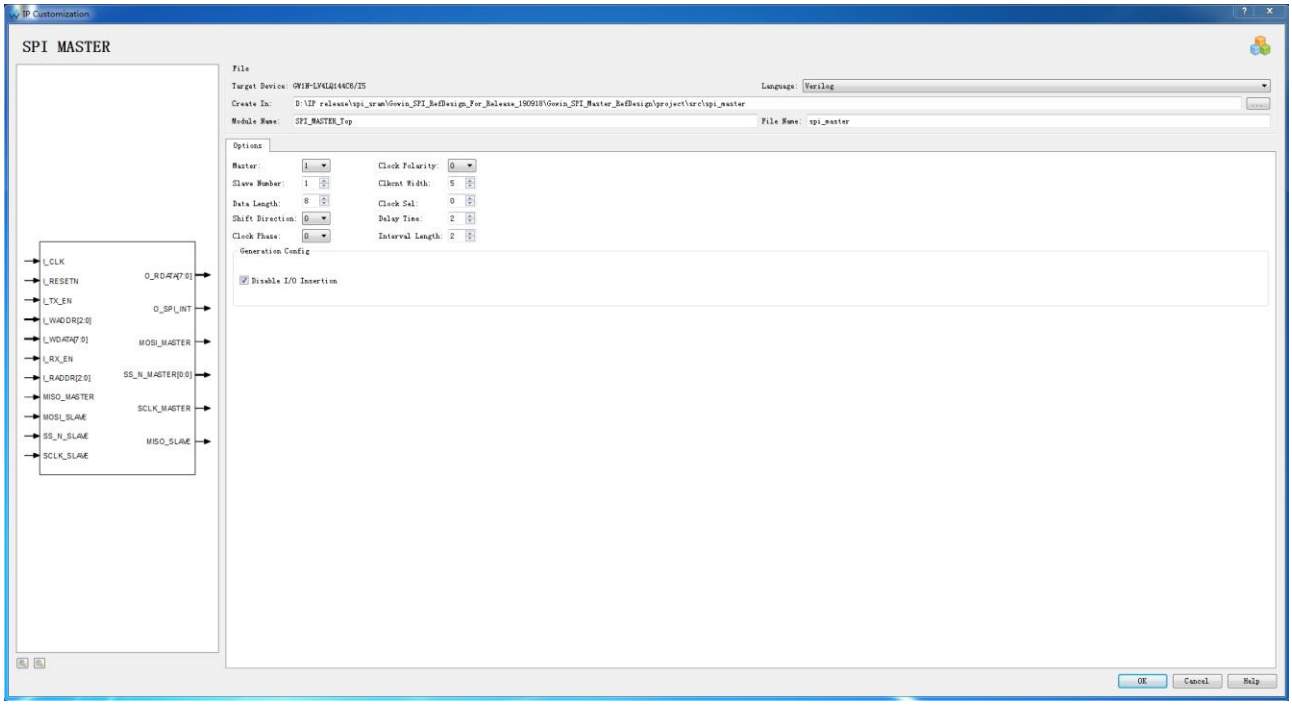
6 Interface Configuration

You can use the IP core generator tool in the IDE to call and configure Gowin SPI Master IP.

6.1 SPI MASTER IP Core Interface

SPI Master configuration interface is shown in Figure 6-1.

Figure 6-1 SPI Master Configuration Interface



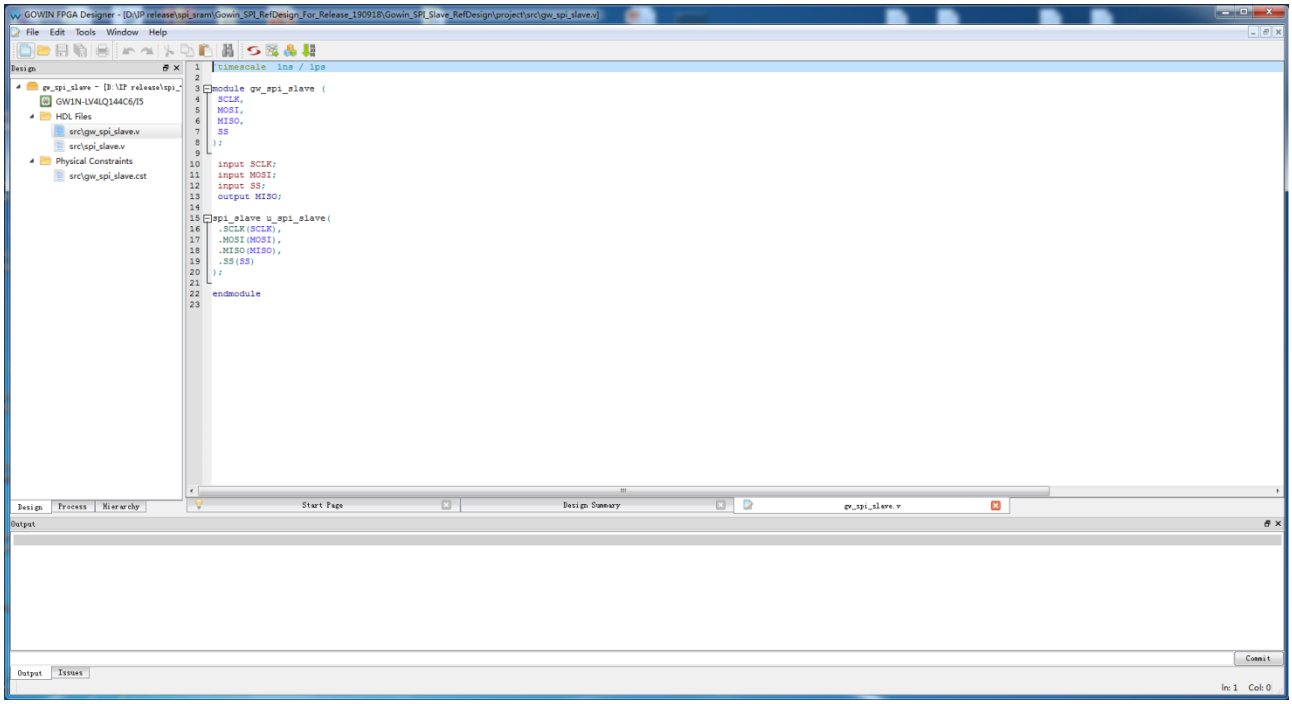
6.2 SPI Slave Reference Design Project

Open Gowin Software, and click "File > Open…" to open the "Open File" dialog box; select the project file (*.gprj), and then open the project, as shown in Figure 6-2.

Note!

There are three menthods to open the project. Please refer to SUG100, Gowin Software User Guide.

Figure 6-2 SPI Slave Configuration Interface



6.3 Bitstream File Generation

After constraints, bitstream file can be generated after synthesis, plancement and routing. Download the bitstream file to the development board or test board via Gowin USB cable. Observe the communication via the test interface.

7 Reference Design

For more details, please refer to the SPI reference design at Gowin official website.


GOWIN
PROGRAMMING FOR THE FUTURE