

For Internal Use Only



GDS Review Tips

Finding Floating pins

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Floating Pin – New Flow

- In GDS review, it is hard to identify floating MIPLAST pins by visual check.
- The following description shows the use of a script for finding floating MIPLAST to MTOP-1 pins.
- The script may not be perfect and official but could flag some critical issues in a GDS.

- **Script location:**

/slowfs/us01dwt2p843/GDSreviews/scripts/icv/exec_missing_pins.tcl

Note: if you just run the script without any inputs , it will give the usage details as shown below:

```
***** Usage: exec_missingPin.tcl -layout <GDS/OAS file> -cell <cellname> -layermap <layermap file>
[-layout_format <GDS|OAS>] [-bot_metal <lowest metal number to include for connectivity>] [-nets
"<net1> <net2> ..."] [-edtext <edtext file>]
```

```
***** [-text_depth <depth, where 0 is top>] [-icv_version <version>] [-grid] [-cores <cores>] [-mem
<memory>]
```

```
***** Contact info: Sergey Chatrchyan (sergeych)
```

Provide the Inputs

- -cell <cellname> *top cell name of your GDS*
- -layermap <layermap file> *layermap file for the technology*
- -layout_format <GDS|OAS>
- -bot_metal <lowest metal number to include for connectivity>
- -nets "<net1> <net2> ..." *You can either provide the choice of your layers or can skip, the script contains a standard list of general power and special pins. Make sure standard list names match the gds pin names. **NOTE: Its not recommended to provide this option for a full gds floating pins check as this will override the default list of MIPLAST pin names. Only use it if you want to check any specific net.***
- -edtext <edtext file>
- -text_depth <depth, where 0 is top> not required
- -icv_version <version> not mandatory [make sure icv is set by checking which icv else use below commands to set icv using module load icv]
- -grid
- -cores <cores>
- -mem <memory>

Flow to Run

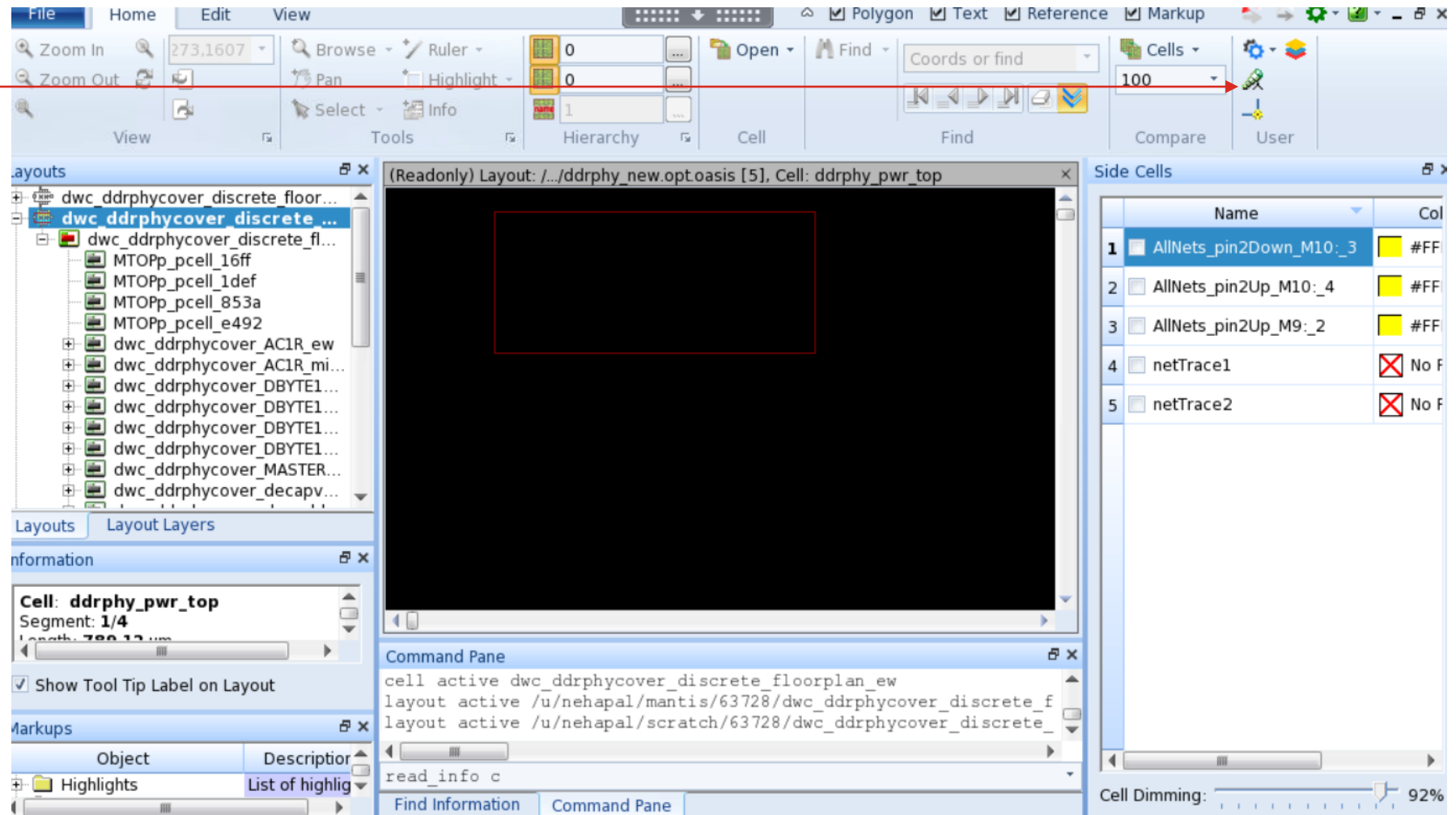
- Steps:
 1. Run the Script on GDS/OAS.
 2. Load the results in Vue.
 3. Check the errors in “DRC Errors” (open the ICV-VUE in ICWB to highlight)
 4. PG openings should be carefully reviewed
 5. PG floating MIPLAST pins might not be at lower level than hard macro top, in another word, these kinds of pins do not exist in LEF, and should not be reported to customer as customer issue, we can point it as internal issue to IP owner.
 6. Check for Special pins (Pending update to add superset of reference nets)
 - VIO_TIE_{HI,LO}_LN*
 - MASTER_ALL_PwrOkDlyd_VIO, MASTER_ALL_VrefOutGlobal
 - PclkC0, PclkC1, PclkDatC0, PclkDatC1
 - BP* (Bump nets)
 - Check connections of must join pins:
Acx4
 - PclkIn, PclkDbyte, VrefGlobal, BP_AC0:3
 - Dbyte
 - PclkIn, VrefGlobal, PwrOkDlyd_VIO, BP_DAT0: 11
 - Master
 - PclkOutC0:1, VrefGlobal, VrefOutGlobal, BP_ALERT_N, BP_MEMRESET_L, BP_VREF, BP_ZN

Example

- `/slowfs/us01dwt2p843/GDSreviews/scripts/icv/exec_missing_pins.tcl -layout
/slowfs/us01dwt2p843/GDSreviews/scripts/icwbev/GDSreview_example/d541_lpddr4xm_top_cut
.gds -cell d541_lpddr4xm_top -layermap
/slowfs/us01dwt2p843/GDSreviews/scripts/icwbev/tsmc/16ff/11M_2Xa1Xd_h_3Xe_vhv_2Y2R/stream.layermap -layout_format GDS -bot_metal 7 -grid -cores 4`

How to open ICV-VUE

- Open ICV-VUE from here.



Load the Results in Vue

VUE: [...382/nehapal/GDSReview_example_16f_3541_lpddr4xm_top/d541_lpddr4xm_top/missing_Pin/d541_lpddr4xm_top.vue]

File View Tools Classification Windows Help

Execution X Load Results X Run Summary X DRC Errors X

Show All Search

Violation Browser

Cell/Violation/Function	Error	Total Errors
▶ AllNets_pin2Down_M9: Metal shape without a VIA connection to below layer.	2	2
▶ AllNets_pin2Down_M8: Metal shape without a VIA connection to below layer.	3,799	3,799
▶ AllNets_pin2Up_M8: Metal shape without a VIA connection to an upper layer.	4,201	4,201
▶ AllNets_pin2Up_M9: Metal shape without a VIA connection to an upper layer.	15,305	15,305
▶ AllNets_pin2Up_M10: Metal shape without a VIA connection to an upper layer.	23	23
▶ AllNets_pin2Down_M10: Metal shape without a VIA connection to below layer.	189	189
▶ VIO*_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.	772	772
▶ PAD*_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.	11	11
▶ Vref*_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.	952	952
▶ PwrOk*_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.	377	377
▶ VSS_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.	137	137

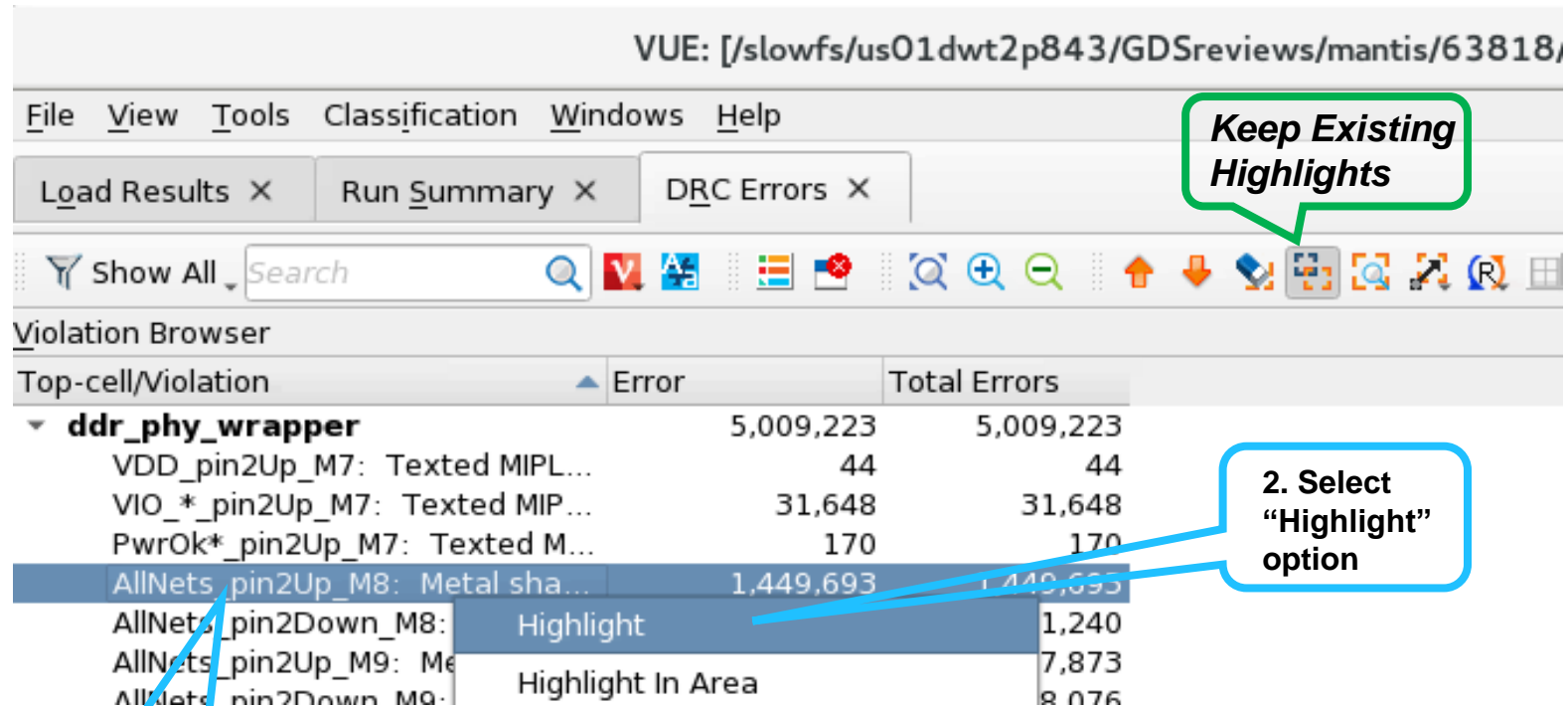
Error List

copy: 144

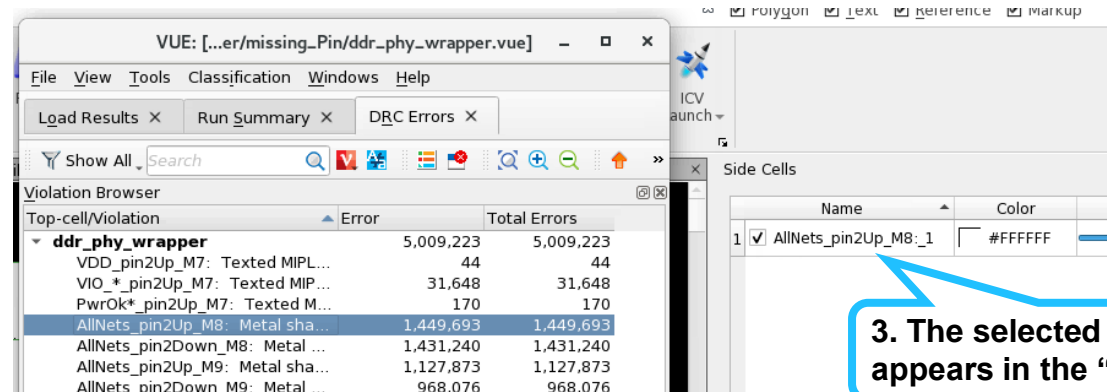
Status	No.	(lower left x, y)	(upper right x, y)	From	User Comment
✖	Error 1	(244.8530, 1228.4640)	(245.3470, 1234.8960)		
✖	Error 2	(3219.1730, 1228.4640)	(3219.6670, 1234.8960)		

Load the Results from Vue to “Side Cells” in ICWBEV

1. Right click by mouse on the desired violation
2. In Drop-down menu select “**Highlight**” option
3. The selected net appears in the “**Side Cells**” pane of ICWBEV.
4. You can add as many as you want violations from VUE. Just be sure that “**Keep Existing Highlights**” is turned **On** in the VUE pane



1. Right click by mouse on the desired violation



Checking the results

Layout Layers

Group ▾ group_conf ▾

Layout Layers

☐ PAD|RDL(74:0)

☐ RDLVIA(85:0)

☐ M11|MTOP(41:...

☐ VIA1011|VIAT...

☐ M10|MTOP-1(4...

☐ VIA910|VIATO...

☒ M9(39:20)

☐ VIA89(58:20)

☐ M8(38:20)

☐ VIA78(57:20)

☐ M7(37:245)

☐ M6(36:240)

☐ VIA67(56:240)

☐ (0:0)

(Readonly) Layout: /.../d541_ipddr4xm_top_cut.gds [4], Cell: d541_ipddr4xm_top

Side Cells

Name

1 ☒ AllNets_pin2Down_M9:_1

2 ☐ AllNets_pin2Up_M9:_0

Violation Groups

Missing pin net violations are separated into 3 groups.

1. **Texted MIPLAST metal without a VIA connection to an upper layer**: detect all textured MIPLAST pins which have no connection to MINTFIRST (no VIA to upper layer)
2. **Metal shape without a VIA connection to below layer**: detect all MINT*, MTOP* shapes which have no connection to below layer
3. **Metal shape without a VIA connection to an upper layer**: detect all MINT* & MTOP-1 shapes which have no connection to upper layer

Note: If the direction of two successive metal shapes (A & B) is the same, then the violations will be repeated, i.e. **AllNets_pin2Up_A** will be equal to **AllNets_pin2Down_B**

Load Results X Run Summary X DRC Errors X

Show All Search

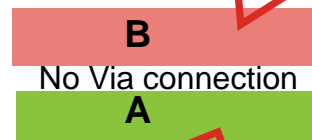
Violation Browser

Top-cell/Violation

ddr_phy_wrapper

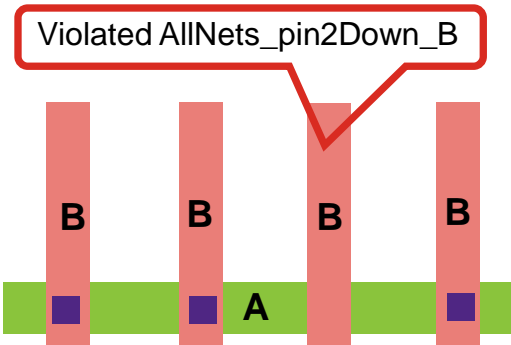
- VDD_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.
- VIO_*_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.
- PwrOk*_pin2Up_M7: Texted MIPLAST metal without a VIA connection to an upper layer.
- AllNets_pin2Up_M8: Metal shape without a VIA connection to an upper layer.
- AllNets_pin2Down_M8: Metal shape without a VIA connection to below layer.
- AllNets_pin2Up_M9: Metal shape without a VIA connection to an upper layer.
- AllNets_pin2Down_M9: Metal shape without a VIA connection to below layer.
- AllNets_pin2Down_M10: MTOP metal shape without a VIA connection to below layer.

Violated AllNets_pin2Down_B



Violated AllNets_pin2Up_A

Note: If the direction of two successive metal shapes (A & B) is opposite, then the violations will be different, i.e. **AllNets_pin2Up_A** != **AllNets_pin2Down_B** (One of them could be ever not violated)



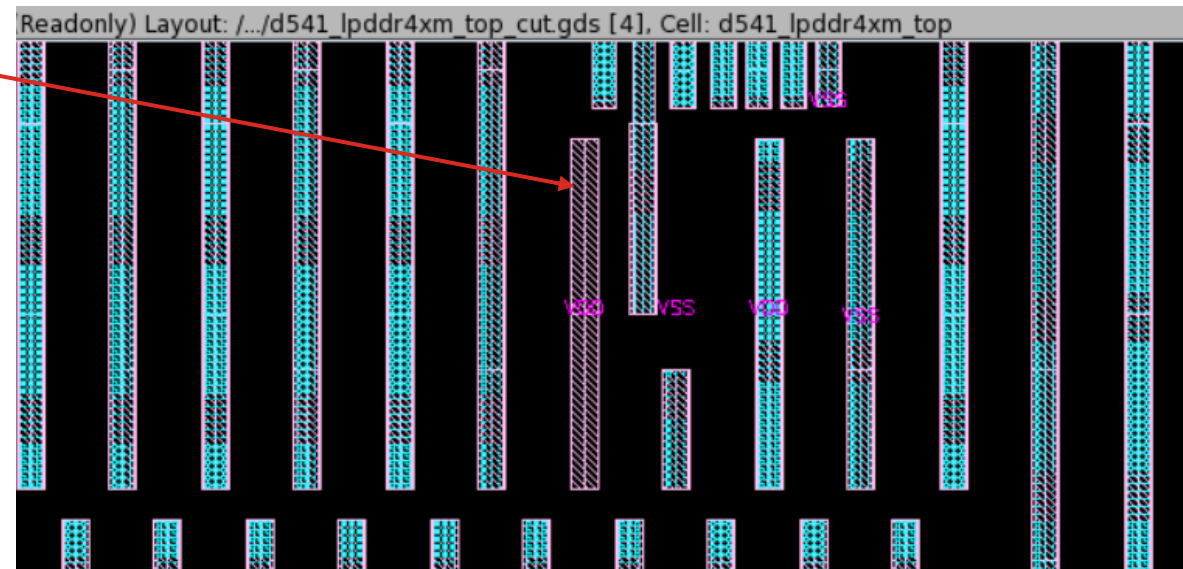
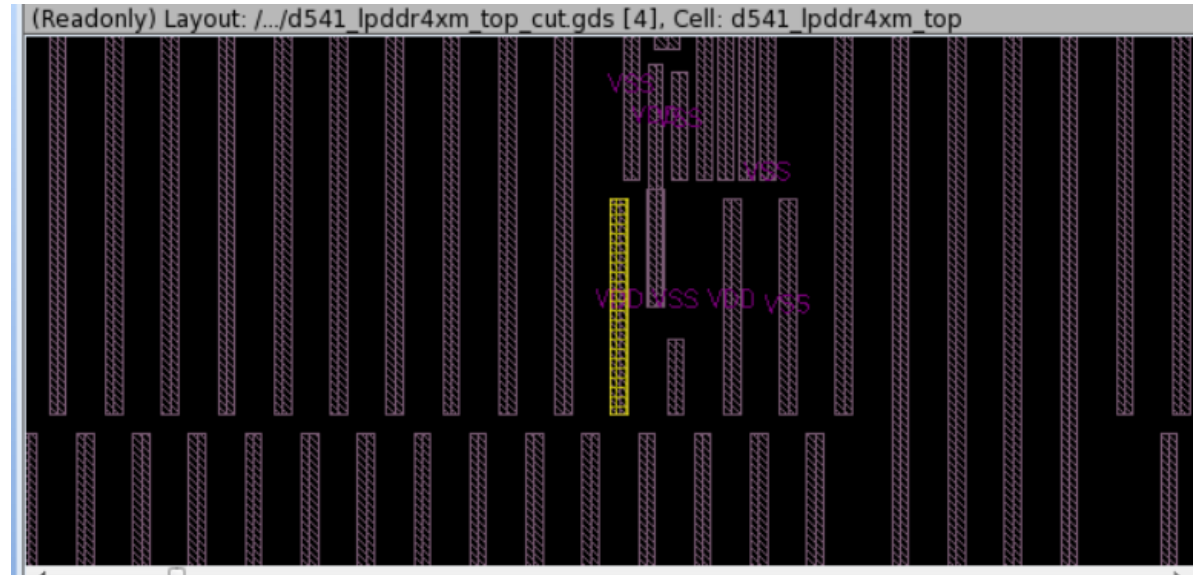
Check Results

- Checking the First error
- Use MIPLAST pin label
- Naming is clear to understand

AllNets_pin2Down_M9: Metal shape without a VIA connection to below layer.

Means VIA89 is missing at this place.

- Pins can be double checked in Lef as well.



Checking the pin level (way 1)

- There can be multiple errors which are below top level. These are not reported to the customer, it should be brought up as an internal issue to IP owner.

- Define hierarchy levels interval in the “**Level**” option in ICWBEV menu pane to show only cells within this interval (typically 0-1 or 0-2).
- Mark checkbox **On** and then **Off** for a violated net in “**Side Cells**” pane
- If no metal shape will be visible after checking **Off** the violated net, then it means the violation is deeper in level of hierarchy and should not be reported. Otherwise the error is real.

Tip: To determine the hierarchy interval just look for level of hierarchy (**k**) for any Hard Macro in the design. The interval will be **0-k**. (Check it in the “**Layouts**” pane of ICWBEV)

1 - Define hierarchy levels interval

2. Check On and check Off a violated net check box

Violation indication

3. No shape observed after switching Off the violated net. Do not report

	Name	Color
1	<input type="checkbox"/> PwrOk*_pin2Up_M7:_5	#8B0000
2	<input checked="" type="checkbox"/> VDD_pin2Up_M7:_1	#DDAA55
3	<input type="checkbox"/> VIO_*.pin2Up_M7:_3	#FF0000

	Name	Color
1	<input type="checkbox"/> PwrOk*_pin2Up_M7:_5	#8B0000
2	<input type="checkbox"/> VDD_pin2Up_M7:_1	#DDAA55
3	<input type="checkbox"/> VIO_*.pin2Up_M7:_3	#FF0000

Checking the pin level (way 2)

1. Turn Off the “**Level**” option in ICWBEV menu pane to show the whole hierarchy
 2. Turn **On** the “**Info**” option in ICWBEV menu pane
 3. Mark checkbox **On** for the considering net in “**Side Cells**” pane. The violated shapes will be indicated in the design
 4. Move cursor to the edge of the indicated shape.
 5. Look for the hierarchy level (and a corresponding cell name) based on “**Info**” floating window.
 6. If the floating shape is found above the hard macro hierarchy (customer owned), it should be addressed with the customer. Otherwise, if the floating shape is found within the hard macro, it can be addressed with the IP owner.
- **We must be very careful not to bring up internal HM questions with the external customers.**

The screenshot displays the ICWBEV tool interface with several annotations explaining the steps for checking the pin level:

- 1. All levels are turned on:** Points to the 'Levels' dropdown menu in the top toolbar, which is set to '5'.
- 2. "Info" is selected:** Points to the 'Info' button in the bottom toolbar.
- 3. Checked net:** Points to the 'Side Cells' pane on the right, where the checkbox for 'VDD_pin2Up_M7:_1' is checked.
- 4. Cursor (mouse) placed on the edge of selected pin:** Points to a yellow rectangular shape on the layout grid.
- 5. Hierarchy level and cell name can be defined from the "info" field:** Points to the 'Info' floating window at the bottom, which displays the path and hierarchy of the selected pin.

The 'Info' window shows the following details:

```

Path: M7(143:0)
Segment: 1/4
Length: 0.975 um
Coords: (503.788,3913.383)-(503.788,3912.408) um
Width: 0.28 um
End Ext: 0.0 um
Hierarchy: /ddr_phy_wrapper/ddr_phy_wrapper_dwc_ddrphybyte_top_ew
/ddr_phy_wrapper_dwc_ddrphybyte_top_ew_dwc_ddrphy_txrxdq_ew
/ddr_phy_wrapper_dwc_ddrphybyte_top_ew_dwc_ddrphy_txrxdq_ew_dwc_ddrphy_txrxdq_ew
/ddr_phy_wrapper_dwc_ddrphybyte_top_ew_dwc_ddrphy_txrxdq_ew_dwc_ddrphy_txrxdq_ew_pwrgrid
/ddr_phy_wrapper_dwc_ddrphybyte_top_ew_dwc_ddrphy_txrxdq_ew_dwc_ddrphy_txrxdq_ew_pwrgrid

```

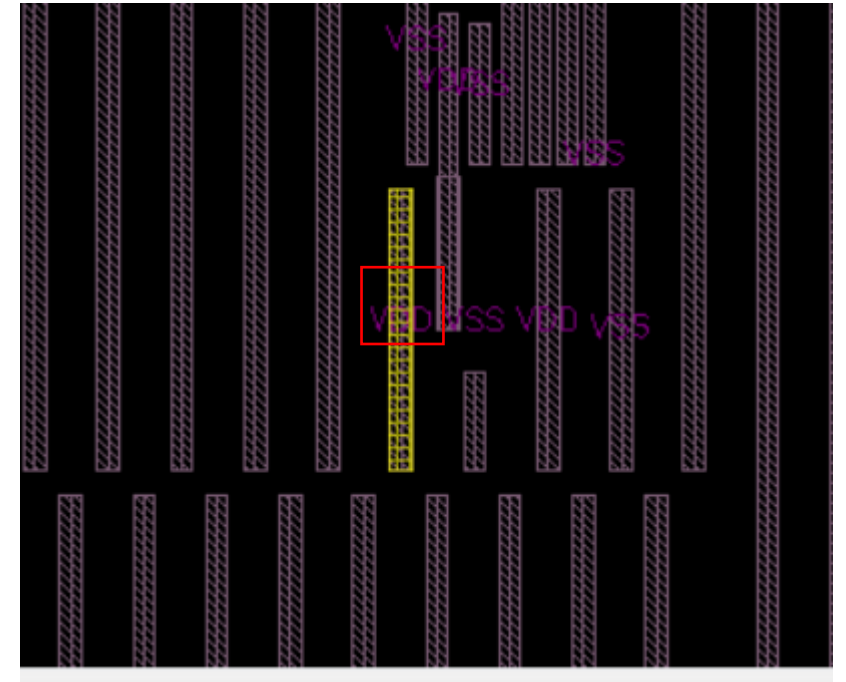
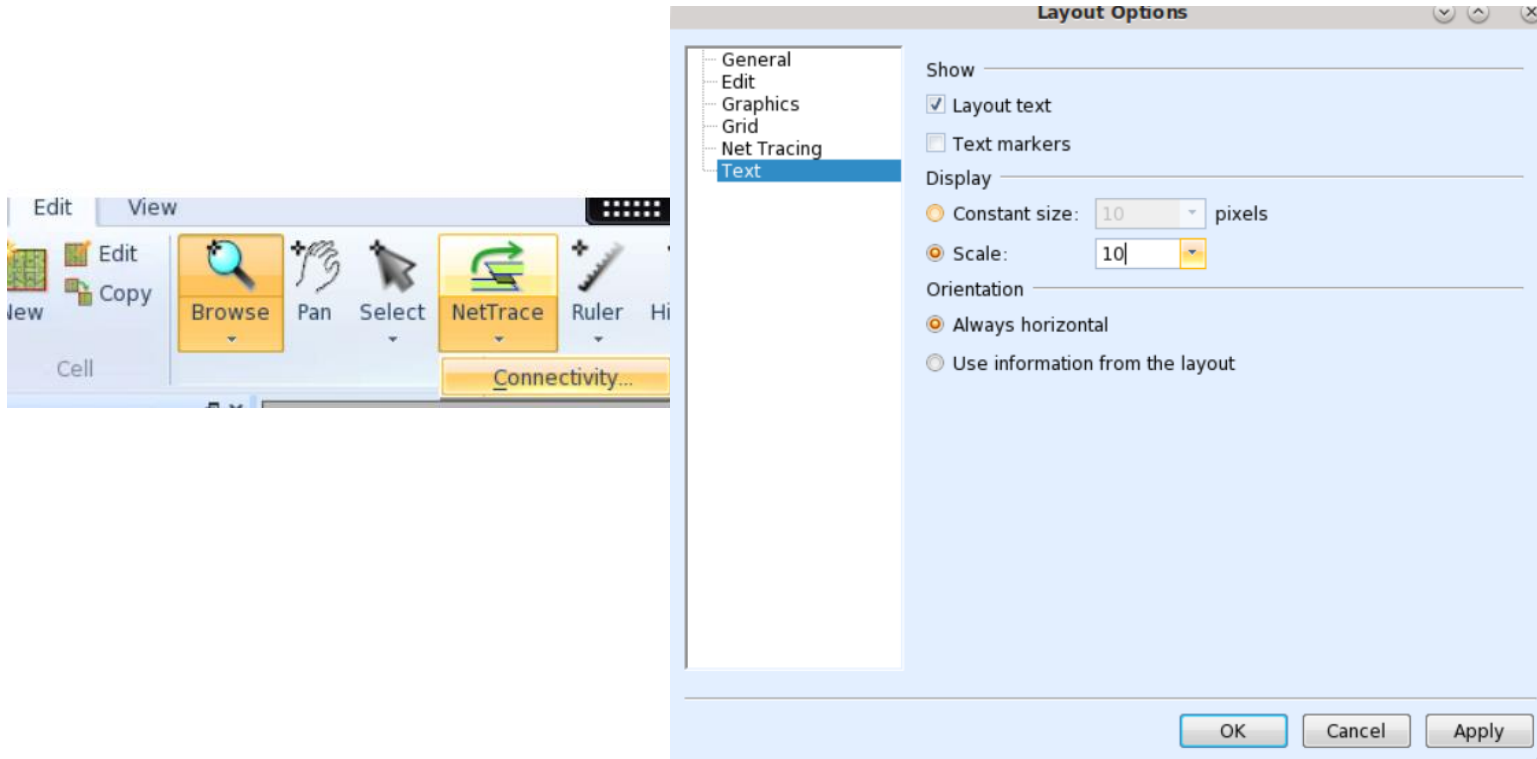
The 'Side Cells' pane shows a table of nets:

Name	Color
<input type="checkbox"/> PwrOk*_pin2Up_M7:_5	#8B0000
<input checked="" type="checkbox"/> VDD_pin2Up_M7:_1	#DDAA55
<input type="checkbox"/> VIO*_pin2Up_M7:_3	#FF0000

The missing pin shape appears in the sixth level of hierarchy in the cell "ddr_phy_wrapper_dwc_ddrphybyte_top_ew_dwc_ddrphy_txrxdq_ew_customPG_rxdq_ew_M5M7_VDD_VDDQ_2". (in this example the shape is within the Hard Macro)

For watching text on pins

Make the scale value more than 5 to see clear texts on pins.

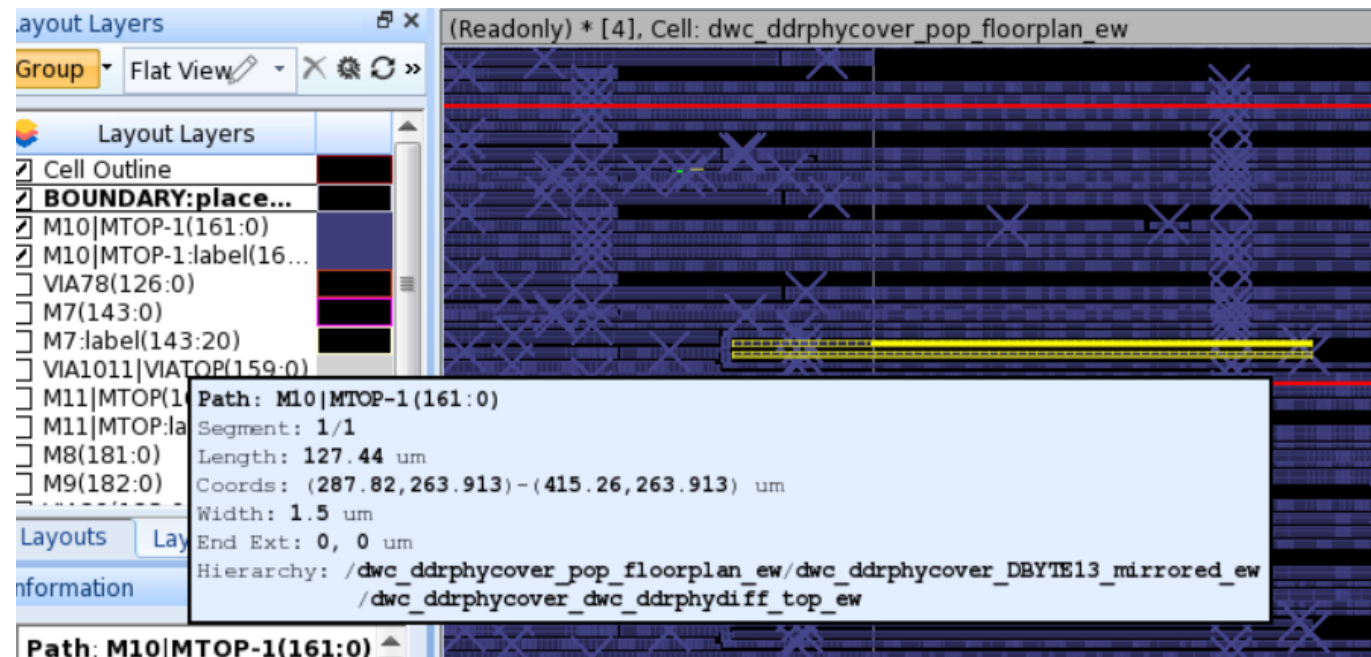
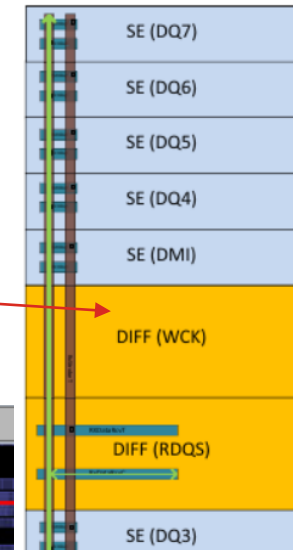


We can use through command line also:
`layout display text_scale 5`

Checking in IG

- For some connections it might not be a requirement to connect at a certain DByte or ACX.
- For such places, we can open the IG and check for reference.
- Sharing an example from another design.
- There is an error for RxStrobeC and RxStrobeTpins as floating.
- While referring to IG , it becomes clear that it is not required to connect in this covercell testbench case.

Figure 11-35 RxStrobeT/C Routing in DBYTE EW Construction – Maximum Length Measurement



Thank You



- One more example:
PClkDbyte pins are not required to be connected in every ACX4.

