SYNOPSYS®
Silicon to Software™

CRD Abutment Verification Script

Version 2022.08-1

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Description

- The script can be used to build then execute physical verification on the following testcase types
  - Abutment and Utility Cell/Block Boundary testcases: testcases as defined in the CRD. For projects without integrated covercells, both macros and covercells can be added to the testcase.
  - Wrapper testcases: macro is instantiated into a wrapper cell, particularly useful for PERC.
  - Abutment Wrapper testcases: macros are abutted prior to being instantiated into a wrapper cell.
  - Standard Cell Boundary testcases: an ~20um standard cell ring is created around the macro.
  - Abutment Standard Cell Boundary testcases: macros are abutted prior to standard cell ring creation.
  - Standard Cell Fill testcases: macros are filled with standard cells.
  - Physical Verification Only testcases: physical verification is run on the macro as is.
  - Utility Cell/Block Abutment testcases: special abutment testcases designed for utility cell/block checking.

Usage

- Location
  - CAD-REP: /remote/cad-rep/projects/alpha/alpha_common/bin/crd_abutment/
  - P4 1999: //wwcad/msip/projects/alpha/alpha_common/bin/crd_abutment/

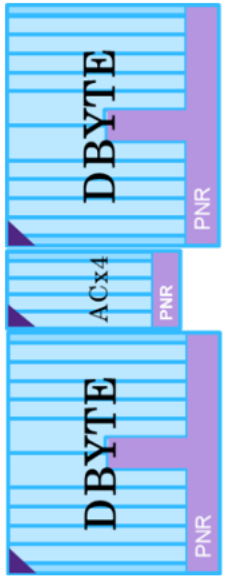
- Instructions
  - Create working directory and change to it
  - Copy crd_abutment_parameters.csv to working directory and modify as per Configuring crd_abutment_parameters.csv. The parameters in the CSV file must be configured prior to running the script for correct operation
  - Execute

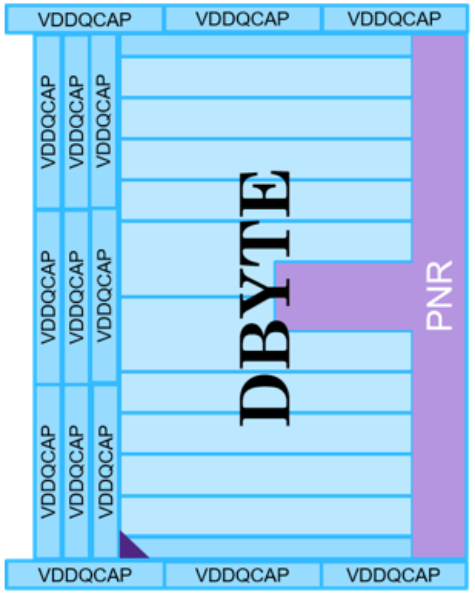
    > /remote/cad-rep/projects/alpha/alpha_common/bin/crd_abutment/crd_abutment.tcl

- Output
  - Script log file called crd_abutment.log
  - Testcase log files called <testcase>.log
  - Subdirectories for each testcase will be created
  - A uniquified_input_CDL subdirectory with the uniquified CDL files, if uniquify_input_cdl parameter is set to 1
  - A uniquified_input_GDS subdirectory with the uniquified GDS files, if uniquify_input_gds parameter is set to 1
  - A results subdirectory containing links to PV and testcase log files
  - PV run directories can be found in <testcase>/pv/ subdirectory, useful for loading results in VUE

Abutment and Utility Cell/Block Boundary testcases

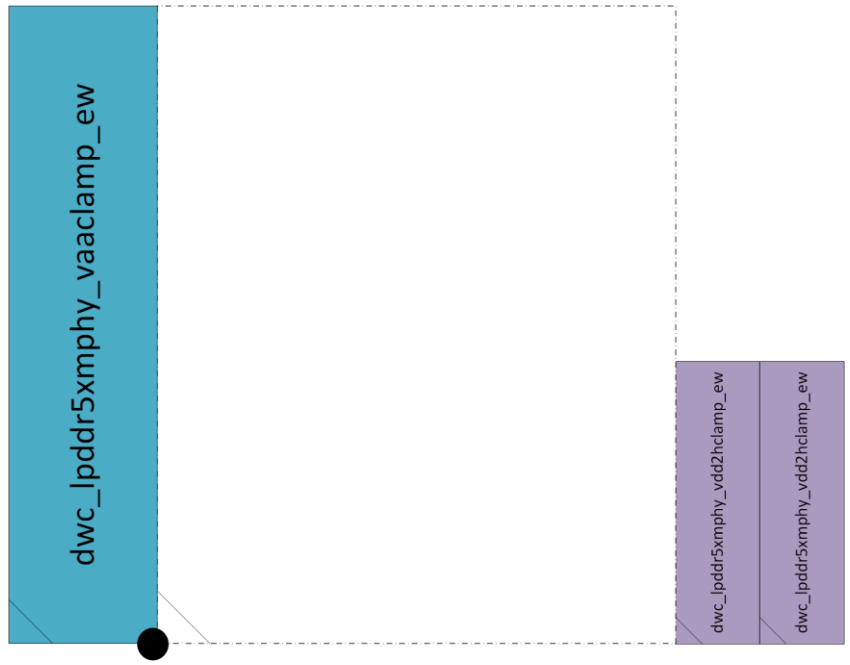
- Generate testcases as per CRD by listing testcase names for testcases_abutment parameter
- Covercells for hard macros can be added by setting test_covercells to 1. Covercells only can be tested by setting test_macros to 0
- Pin texts are propagated to the top level based on the layers specified in the covercell_text_layers and macro_text_layers parameters
- Top level rectangular boundary can be added by setting generate_boundary to 1, and upsized through generated_boundary_upsize_* parameters
- Example: testcases_abutment,abutment_acx4_d0_a0_d0_ew boundary_dbyte_decapvddq_ew





Wrapper testcases

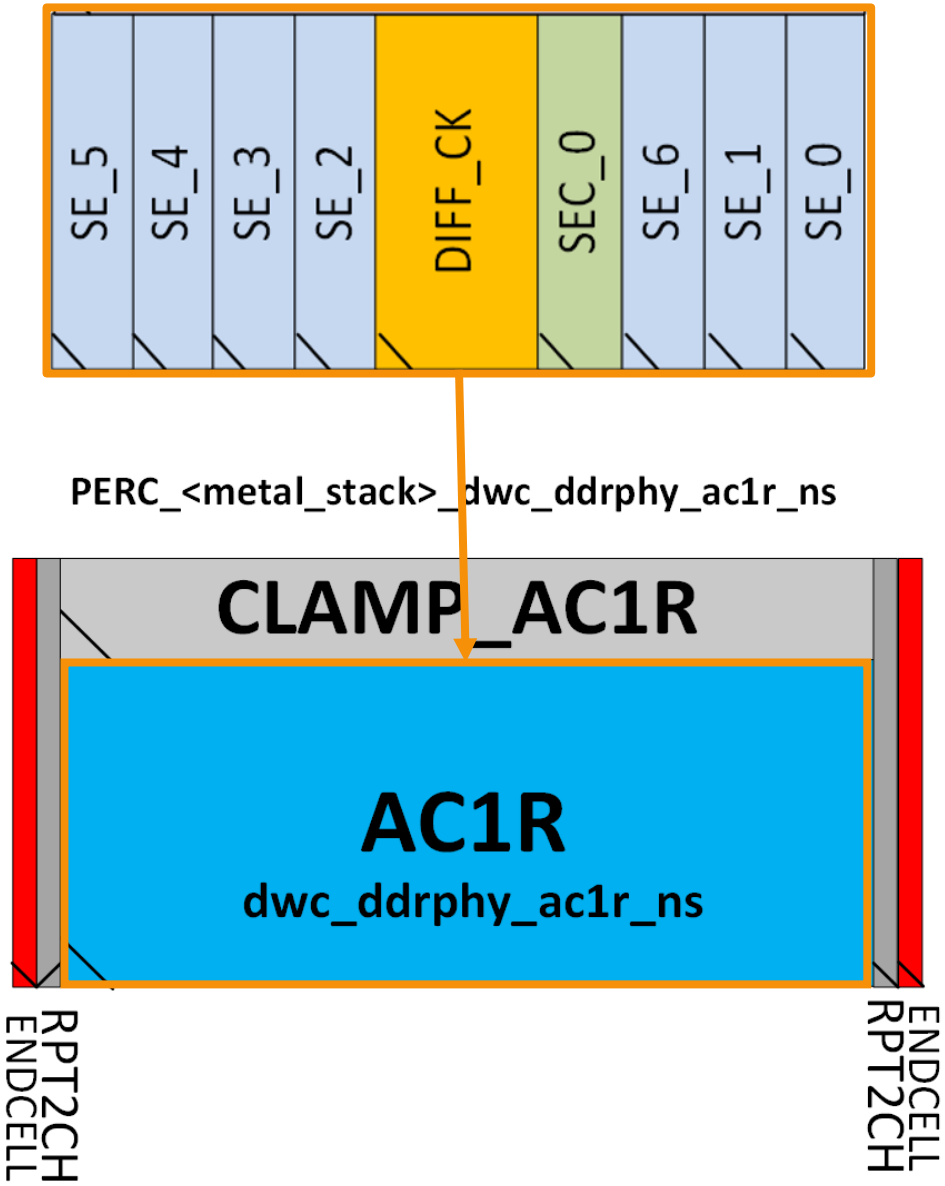
- Wrapper testcases are used to instantiate a macro into a wrapper cell
- The wrapper cell must have a name of the form of *wrapper_<macro>
- The script will add the macro at the origin of the wrapper cell as a subcell
- If the generate_cdl parameter is set to 1, the script will also generate a merged netlist of the wrapper cell with the macro instantiated – useful for LVS and PERCTOPO
- Typical use case is for PERC where the wrapper cell includes clamps, connections and pin labels
- Example: testcases_wrapper, PERC_wrapper_dwc_lpddr5xmphymaster_top_ew



Script will add dwc_lpddr5xmphymaster_top_ew macro into wrapper cell at the origin

Abutment Wrapper testcases

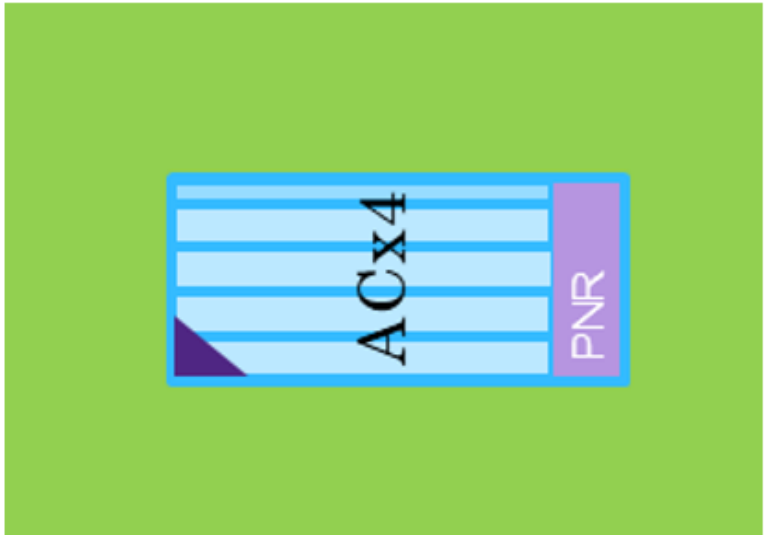
- Similar to Wrapper testcases, but will abut macros as per the specified testcase prior to instantiating into a wrapper cell
- The wrapper cell must have a name of the form of *wrapper_<testcase>
- The script will add the abutted macros at the origin of the wrapper cell as a single subcell
- Typical use case is for LPDDR54 PERC where the wrapper cell includes clamps, connections and pin labels
- Example: testcases_abutment_wrapper,wrapper_PERC_11M_dwc_ddrphy_ac1r_ew



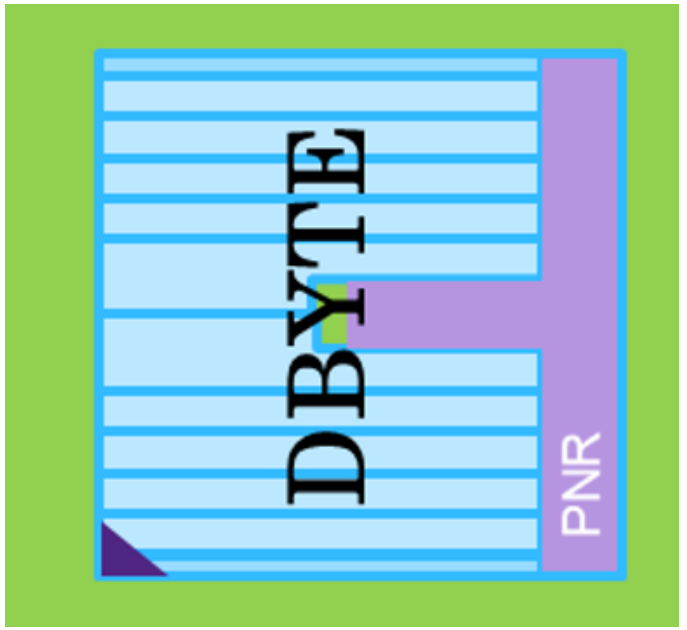
Script will assemble SE, SEC and DIFF macros into AC1R configuration and add other macros as above, prior to insertion into wrapper cell

Standard Cell Boundary testcases

- Testcases named boundary_<macro>_stdcell are generated for each macro listed in the testcases_stdcell parameter
- Stdcell ring of ~20um is added around macro
- Example: testcases_stdcell,dwc_ddrphyacx4_top_ew dwc_ddrphydbyte_top_ew



boundary_dwc_ddrphyacx4_top_ew_stdcell

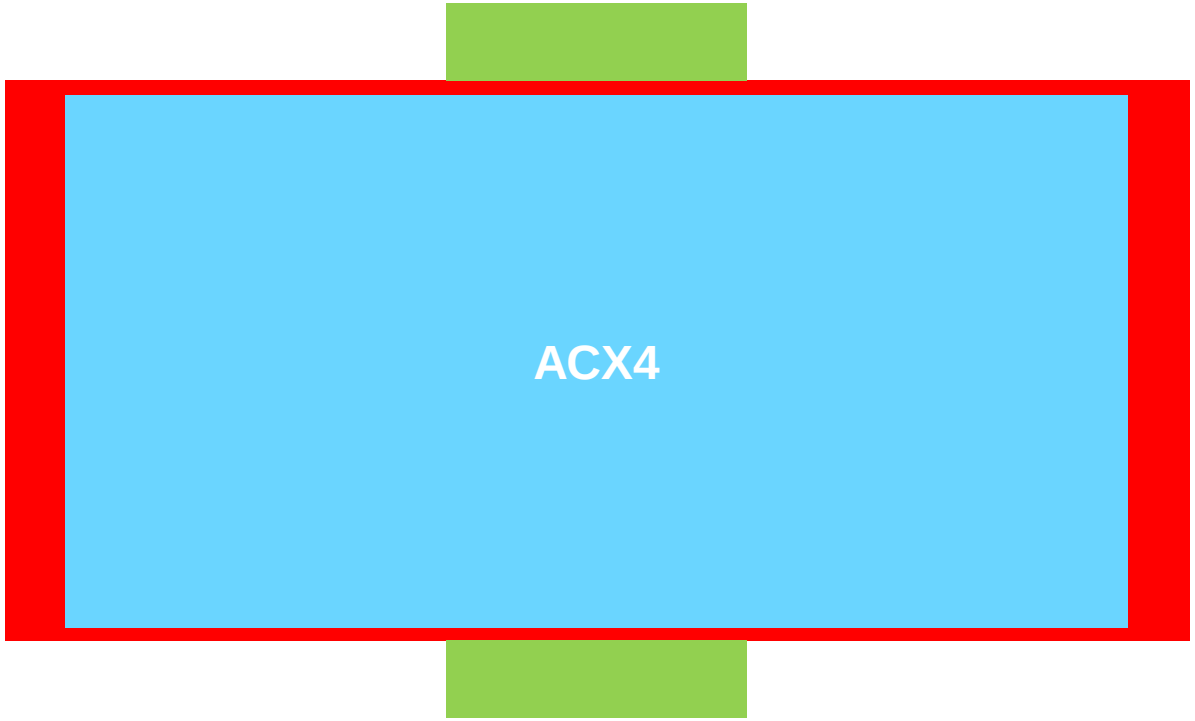


boundary_dwc_ddrphydbyte_top_ew_stdcell

Standard Cell Boundary testcases

Cont'd

- Stdcell keepout regions can be specified using the stdcell_kpt_[b|l|r|t] and stdcell_manual_kpt_<testcase> parameters



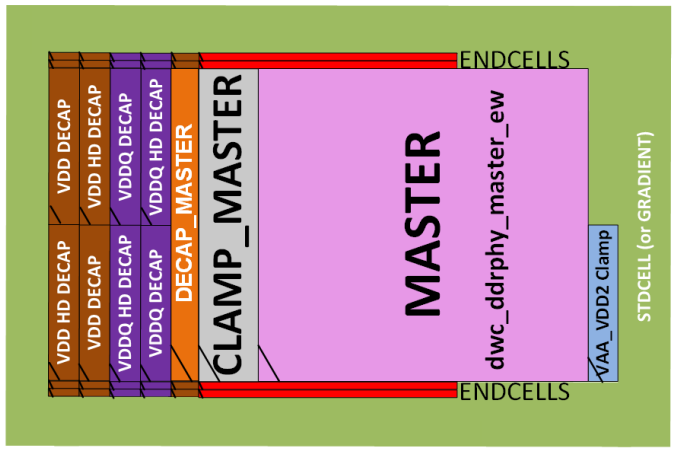
Macro

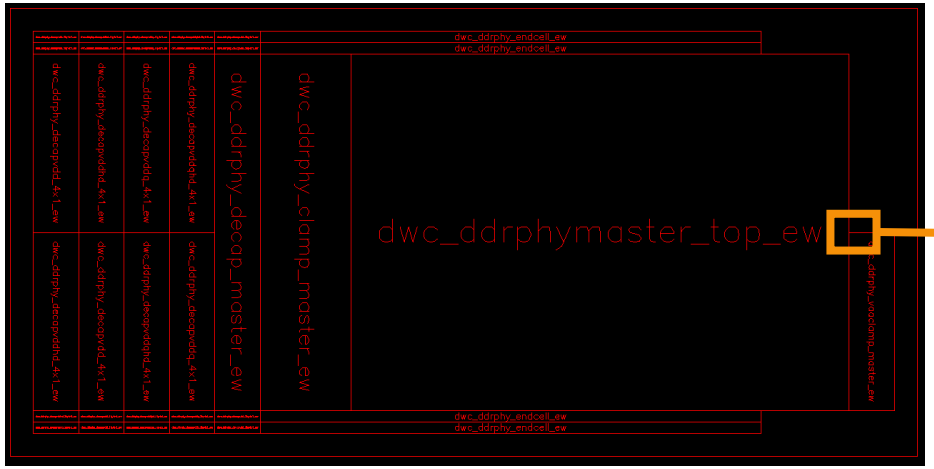
stdcell_kpt_[b|l|r|t]

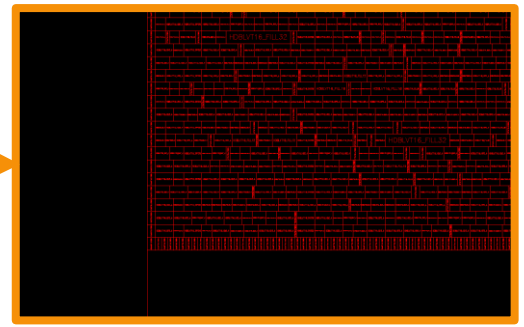
stdcell_manual_kpt_<testcase>

Abutment Standard Cell Boundary testcases

- Similar to Standard Cell Boundary testcases, but will abut macros as per the specified testcase prior to standard cell ring insertion
- Testcases named boundary_<testcase>_stdcell are generated for each <testcase> listed in the testcases_abutment_stdcell parameter
- Stdcell keepout regions can be specified using the stdcell_kpt_* and stdcell_manual_kpt_<macro/testcase> parameters
- Stdcell ring of ~20um is added around testcase
- Typical use case is for LPDDR54
- Example: testcases_abutment_stdcell,boundary_master_decap_stdcell_ew







Standard Cell Fill Testcases

- Fill macro with standard cells and produce GDS
  - Physical Verification can be run on this GDS by enabling the relevant Physical Verification parameters
  - GDS can also be imported into Custom Compiler with reference libraries to have OA view of filled macro
- Inputs
  - List macros to be filled in the testcases_stdcell_fill parameter
  - Provide placement DEF (COMPONENTS section) for macros – example file shown in figure
  - Provide LEF and GDS files for COMPONENTS
  - Provide process and standard cell parameters
- Example for dwc_lpddr5xmphyacx2_top_ew:
  - def_ dwc_lpddr5xmphyacx2_top_ew,<absolute path to DEF>
  - lef_dwc_lpddr5xmphy_lcdl,<absolute path to LEF>
  - <LEF parameters for remaining COMPONENTS>
  - gds_dwc_lpddr5xmphy_lcdl,<absolute path to GDS>
  - <GDS parameters for remaining COMPONENTS>
  - testcases_stdcell_fill,dwc_lpddr5xmphyacx2_top_ew

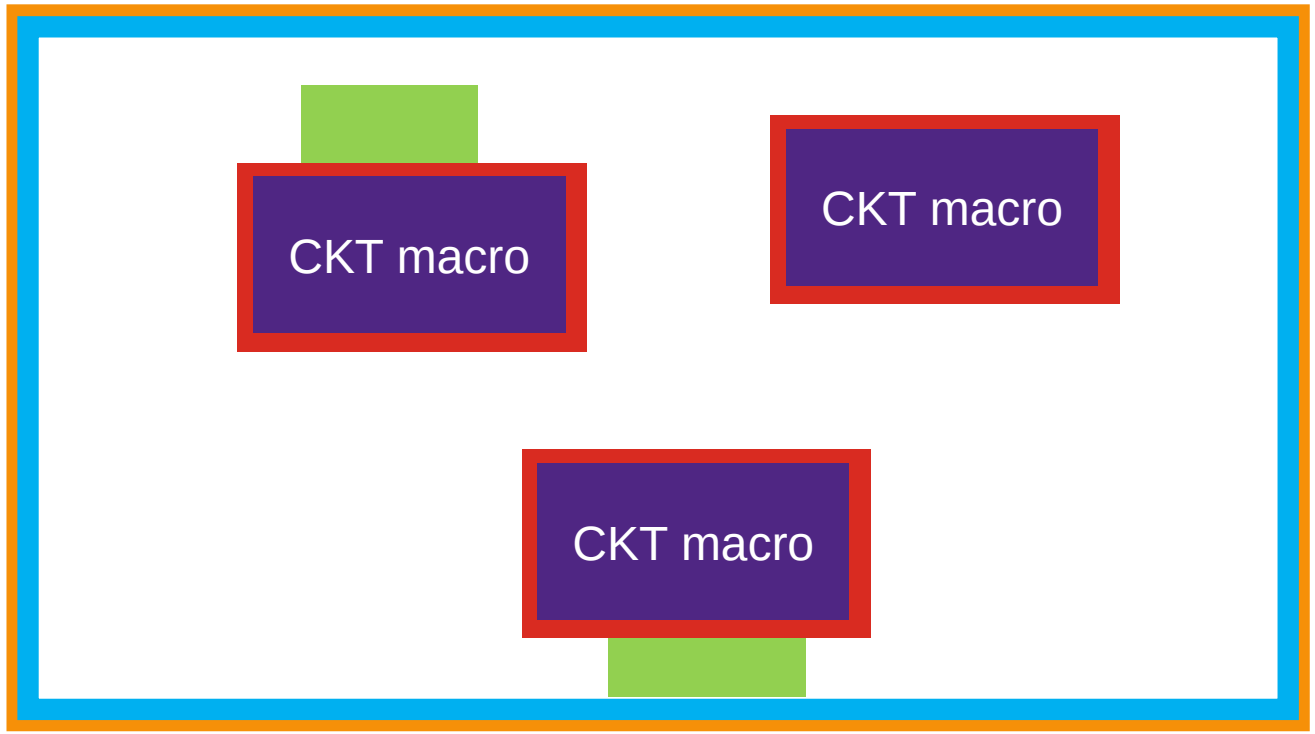
```
VERSION 5.8 ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;

DESIGN dwc_lpddr5xmphyacx2_top_ew ;

UNITS DISTANCE MICRONS 2000 ;
DIEAREA  ( 0 0 )  ( 436458 199920 ) ;

COMPONENTS 9 ;
- lcdl10 dwc_lpddr5xmphy_lcdl + PLACED  ( 31008 176400 ) N
  + SOURCE DIST ;
- pclkrcv1 dwc_lpddr5xmphy_pclk_rxdca + PLACED  ( 75072 36120 ) N
  + SOURCE DIST ;
- lstx_acx2 dwc_lpddr5xmphy_lstx_acx2_ew + PLACED  ( 103428 0 ) FS
  + SOURCE DIST ;
- AX_1 dwc_lpddr5xmphy_txrxac_ew + PLACED  ( 103428 0 ) FS
  + SOURCE DIST ;
- vreg_acx dwc_lpddr5xmphy_vregvsh_ew + PLACED  ( 376380 25200 ) N
  + SOURCE DIST ;
- AX_0 dwc_lpddr5xmphy_txrxac_ew + PLACED  ( 103428 99960 ) N
  + SOURCE DIST ;
- pclkrcv0 dwc_lpddr5xmphy_pclk_rxdca + PLACED  ( 75072 153720 ) FS
  + SOURCE DIST ;
- clamp_acx2 dwc_lpddr5xmphy_vddqclamp_acx2_ew + PLACED  ( 301308 0 ) N
  + SOURCE DIST ;
- lcdl1 dwc_lpddr5xmphy_lcdl + PLACED  ( 31008 0 ) FS
  + SOURCE DIST ;
END COMPONENTS

END DESIGN
```

Sample placement DEF

Standard Cell Fill Testcases

Cont'd

- Stdcell keepout regions can be specified using the stdcell_inner_kpt_[b|l|r|t], stdcell_kpt_[b|l|r|t] and stdcell_manual_kpt_<testcase> parameters



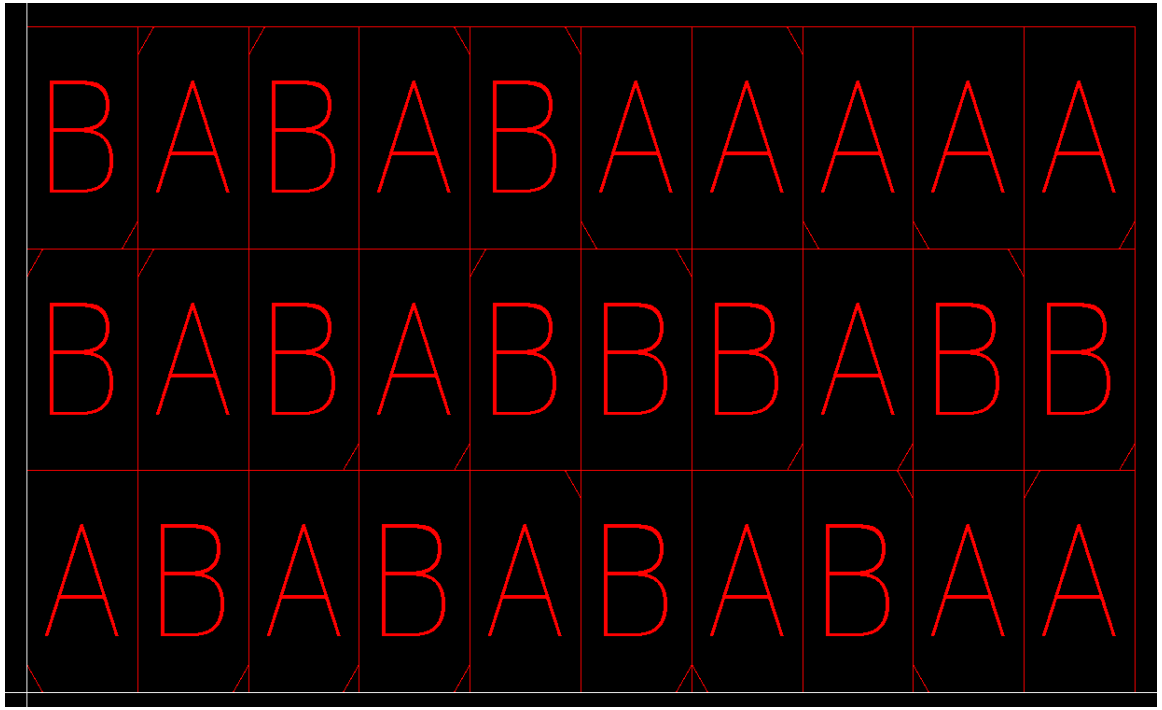
Physical Verification Only testcases

- Run physical verification on macros listed for the testcases_pv_only parameter
- Example: testcases_pv_only,dwc_ddrphyacx4_top_ns dwc_ddrphydbyte_top_ew
- GDS and CDL for macros must be provided
  - gds_<macro>,<path to GDS>
  - cdl_<macro>,<path to CDL>

Utility Cell/Block Abutment testcases

- Testcases are specified as separate parameters with the name testcases_utility_*
- The format for the parameter is <mode>:<cell1> <cell2> <…>:[<cella> <cellb> <…>]

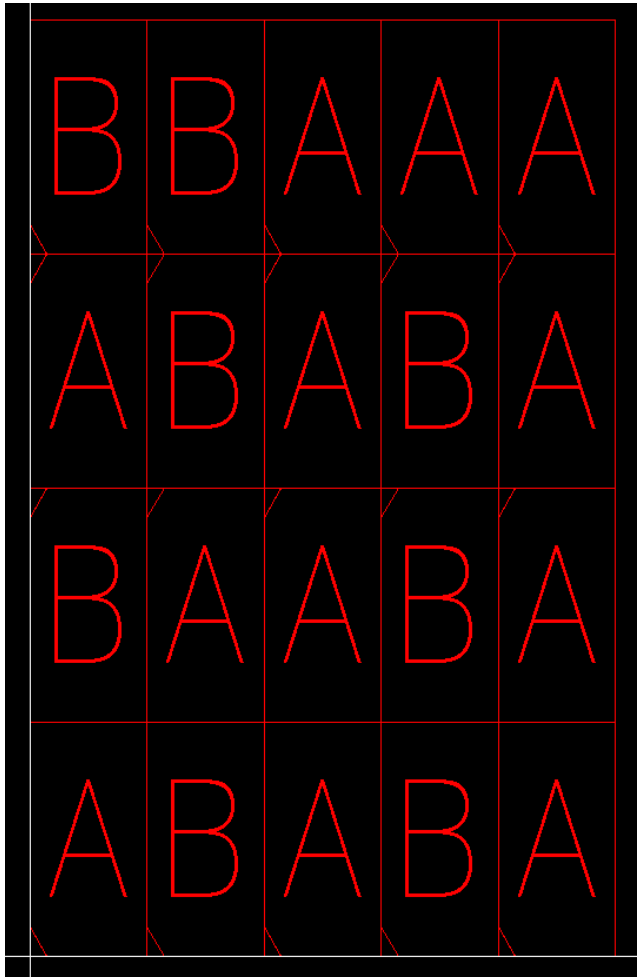
- “full” mode – script builds testcase shown on right for every combination of two cells to check all edge and corner cases
- All cells should be the same size
- Example:
  testcases_utility_full_example,full:dwc_lpddr5xmphy_decapvdd2h_ew dwc_lpddr5xmphy_decapvdd2h_ld_ew dwc_lpddr5xmphy_decapvddq_ew dwc_lpddr5xmphy_decapvddq_ld_ew



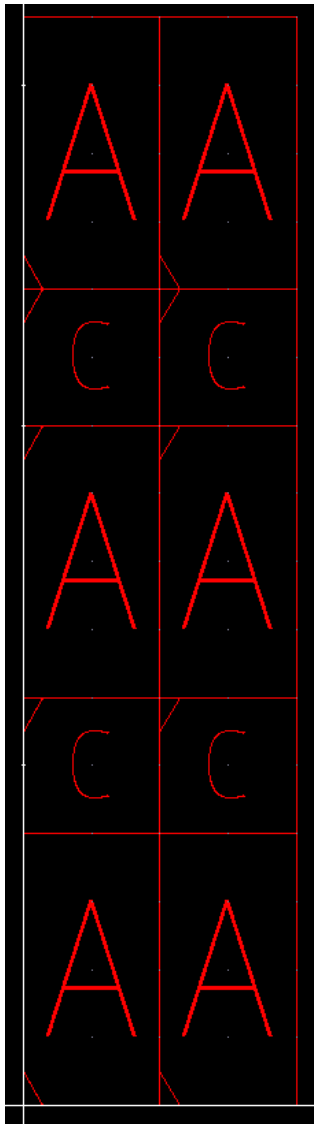
Utility Cell/Block Abutment testcases

Cont'd

- "block_ew" mode
- Script builds testcase (1) for every combination of two utility blocks for the same hard macro
  - Blocks should be the same size
- Script builds testcase (2) for every combination of two utility blocks for different hard macros
  - Blocks should be the same width
- Example: testcases_utility_block_example, block_ew:dwc_lpddr5xmphy_decapvsh_zcal_ew dwc_lpddr5xmphy_decapvsh_ld_zcal_ew dwc_lpddr5xmphy_decapvddq_zcal_ew dwc_lpddr5xmphy_decapvddq_ld_zcal_ew:dwc_lpddr5xmphy_decapvsh_ld_dx5_ew dwc_lpddr5xmphy_decapvsh_dx5_ew dwc_lpddr5xmphy_decapvddq_ld_dx5_ew dwc_lpddr5xmphy_decapvddq_dx5_ew:dwc_lpddr5xmphy_decapvsh_ld_dx4_ew dwc_lpddr5xmphy_decapvsh_dx4_ew dwc_lpddr5xmphy_decapvddq_ld_dx4_ew dwc_lpddr5xmphy_decapvddq_dx4_ew



(1) Same HM



(2) Different HM

Configuring crd_abutment_parameters.csv

- UDE parameters – required for running physical verification through pvbatch

Parameter name	Description
project_type	Project type. Example: ddr54
project_name	Project name. Example:d809-ddr54-tsmc7ff18
release_name	Release name. Example: rel1.00_cktpcs
metal_stack	Metal stack. Example: 15M_1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2Yx2R

Configuring crd_abutment_parameters.csv

Cont'd

- Process parameters – required for testcase GDS generation

Parameter name	Description
boundary_layer	Cell boundary layer. Example: 108:0
dbu	Process DBU in metres. Example: 1e-9
icc2_gds_layer_map	IC Compiler II GDS layer map path. (For Standard Cell Boundary testcases only.) Example: /remote/cad-rep/fab/f101-tsmc/5nm/logic/FF/common/tech_le/icc2/ver1.1_2a/orig/PR_tech/Synopsys/GdsOutMap_ICC2/PRTF_ICC2_N5_gdsout_15M_1X_h_1Xb_v_1Xe_h_1Ya_v_1Yb_h_5Y_vhvhv_2Yy2R_SHDMIM.11_2a.map
icc2_techfile	IC Compiler II techfile path. (For Standard Cell Boundary testcases only.) Example: /remote/cad-rep/fab/f101-tsmc/5nm/logic/FF/common/tech_le/icc2/ver1.1_2a/orig/PR_tech/Synopsys/TechFile/Standard/VHV/PRTF_ICC2_N5_15M_1X1Xb1Xe1Ya1Yb5Y2Yy2R_UTRDL_M1P34_M2P35_M3P42_M4P42_M5P76_M6P76_M7P76_M8P76_M9P76_M10P76_M11P76_H210_SHDMIM.11_2a.tf
tap_distance	Tap distance in microns. As a staggered tap placement is used, this value is typically four times the required device to tap distance. (For Standard Cell Boundary testcases only.) Example: 20

Configuring crd_abutment_parameters.csv

Cont'd

- Abutment parameters – used in testcase GDS generation.

Parameter name	Description
generate_boundary	Set to 1 to generate top level boundary in GDS.
generated_boundary_upsize_*	Specify top level boundary upsizing in microns. There are parameters for left, right, top and bottom.

Configuring crd_abutment_parameters.csv

Cont'd

- Text parameters – required for testcase GDS generation. Specified as layer:datatype. Multiple layers can be specified.

Parameter name	Description
covercell_text_layers	Texts from covercells on specified layers will be promoted to testcase top level. Example: 202:44 202:45
macro_text_layers	Texts from macro cells on specified layers will be promoted to testcase top level. Example: 202:38

Configuring crd_abutment_parameters.csv

Cont'd

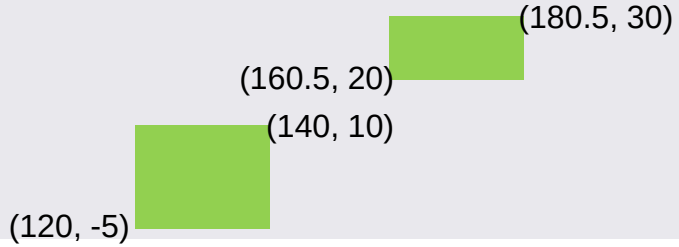
- Macro and covercell collateral – paths to macro and covercell views used for testcase generation.
  - Perforce depot paths, including revision #, can be specified.
  - Example: gds_dwc_lpddr5xphydx4_top_ew,//depot/products/lpddr5x_ddr5_phy/lp5x/project/d930-lpddr5x-tsmc5ff12/di/rel/0.75a/dwc_lpddr5xphydx4_top_ew/views/gds/15M_1X_h_1Xb_v_1Xe_h_1Ya_v_1Yb_h_5Y_vhvhv_2Yy2Z/dwc_lpddr5xphydx4_top_ew.gds.gz#7

Parameter name	Description
cdl_<macro>	Absolute or Perforce path to macro CDL. (For Physical Verification Only testcases. For Wrapper testcases, optionally.)
def_<macro>	Absolute or Perforce path to macro DEF. (For Standard Cell Fill testcases only.)
gds_<macro>	Absolute or Perforce path to macro GDS.
lef_<macro>	Absolute or Perforce path to macro LEF. (For Standard Cell Boundary testcases only.)
gds_dwc_ddrphycover_<macro>	Absolute or Perforce path to covercell GDS. (For Abutment and Utility Cell/Block Boundary testcases only, optionally.)

Configuring crd_abutment_parameters.csv

Cont'd

- Standard cell parameters – paths to standard cell views used for [Abutment] Standard Cell Boundary and Standard Cell Fill testcase generation, along with boundary cell details.

Parameter name	Description
boundary_*	Specify standard cell boundary cell names.
stdcell_drive_strength	Specify version of INV/BUF/ND2/NR2 cells to add. Example: 4
stdcell_gds	Absolute path to standard cell GDS.
stdcell_inner_kpt_[b|l|r|t]	Specify standard cell keepout from top level boundary in microns. There are parameters for left, right, top and bottom. (For Standard Cell Fill testcases only.)
stdcell_kpt_[b|l|r|t]	Specify standard cell keepout from macro in microns. There are parameters for left, right, top and bottom.
stdcell_manual_kpt_<macro/testcase>	Specify manual standard cell keepouts in microns. Values are given as sets of four numbers representing rectangular bbox (llx lly urx ury) of keepout, where ll is lower left and ur is upper right. Example with two keepouts: 160.5 20 180.5 30 120 -5 140 10 

Configuring crd_abutment_parameters.csv

Cont'd

- Standard cell parameters – paths to standard cell views used for [Abutment] Standard Cell Boundary and Standard Cell Fill testcase generation, along with boundary cell details.

Parameter name	Description
stdcell_ndm	Absolute path to standard cell NDM.
stdcell_tap	Specify tap cell name.
stdcell_tap_boundary_wall_cell_*	Specify standard cell tap, boundary and wall cell names.

Configuring crd_abutment_parameters.csv

Cont'd

- Testcase and testing control parameters – control what is being tested and how

Parameter name	Description
testcases_abutment	List of Abutment and Utility Cell/Block Boundary testcases to run. These are as specified in CRD. Example: abutment_acx4_a0_aM_aM_a0_ew abutment_acx4_d0_a0_d0_ew boundary_dbyte_decapvddq_ew
testcases_abutment_stdcell	List of Abutment Standard Cell Boundary testcases to run.
testcases_abutment_wrapper	List of Abutment Wrapper testcases to run.
testcases_pv_only	List of macros for Physical Verification Only testcases.
testcases_stdcell	List of macros for Standard Cell Boundary testcases.
testcases_stdcell_fill	List of macros for Standard Cell Fill testcases.
testcases_utility_*	Parameter to define details of Utility Cell/Block Abutment testcase. See Utility Cell/Block Abutment testcases section for details on how to use. Multiple parameters can be specified.
testcases_wrapper	List of Wrapper testcases to run. Testcases are specified as *wrapper_<macro>.

Configuring crd_abutment_parameters.csv

Cont'd

- Testing parameters – control what is being tested and how

Parameter name	Description
generate_cdl	If set to 1, script will generate CDL for Wrapper testcases instead of using an empty CDL.
generate_lef	If set to 1, script will generate size-only LEF (no pins) for macro for Standard Cell Boundary testcases instead of using user provided LEF.
output_layout_format	Choose between GDS or OASIS for output layout format.
test_covercells	Set to 1 to include hard macro covercells in Abutment and Utility Cell/Block Boundary testcases.
test_macros	Set to 1 to include macros in Abutment and Utility Cell/Block Boundary testcases.
uniquify_input_cdl	Set to 1 to uniquify input CDL files prior to testcase generation. Recommended to avoid cell conflicts if using non-uniquified collateral. (Applies to Physical Verification Only and Wrapper testcases only.)
uniquify_input_cdl_filter_file	Absolute path to CDL uniquification filter file.
uniquify_input_gds	Set to 1 to uniquify input GDS files prior to testcase generation. Recommended to avoid cell conflicts if using non-uniquified collateral.
uniquify_signal_pins	Set to 1 to uniquify signal pin names for each macro in testcase to filter opens. Not recommended as uniquified signal pin names may not match pins listed in PV runset. (Applies to Abutment and Utility Cell/Block Boundary testcases only.)

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
msip_cd_pv_version	Set to override default msip_cd_pv module version. (optional) Example: 2019.07-5
grid	Set to 1 to run ICV on the grid; 0 to run locally.
virtual_connect_icv	Control how virtual connect is handled for ICV. Valid values are ON, OFF and FOUNDRY_DEFAULT. (optional)
virtual_connect_calibre	Control how virtual connect is handled for Calibre. Valid values are ALL and OFF. (optional)

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
DRC parameters	
drc_icv	Set to 1 to run ICV DRC.
drc_calibre	Set to 1 to run Calibre DRC.
drc_icv_grid_processes	Set number of cores for ICV grid job.
drc_icv_options_file	Set to path of ICV options file to override default. (optional)
drc_icv_runset	Set to path of ICV runset file to override default. (optional)
drc_icv_unselect_rule_names	List of ICV DRC rules to not run. (optional) Example: *_DN_*
drc_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
drc_prefix	Specific verification to run. Default is DRC.
drc_feol_fill	Set to 1 to run FEOL fill prior to DRC.
drc_beol_fill	Set to 1 to run BEOL fill prior to DRC.
drc_error_limit	Set to error limit to override CCS/PCS setting. (optional)

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
LVS parameters	
lvs_icv	Set to 1 to run ICV LVS.
lvs_calibre	Set to 1 to run Calibre LVS.
lvs_icv_grid_processes	Set number of cores for ICV grid job.
lvs_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
lvs_prefix	Specific verification to run. Default is LVS.
PERCCNOD parameters	
perccnod_icv	Set to 1 to run ICV PERCCNOD.
perccnod_calibre	Set to 1 to run Calibre PERCCNOD.
perccnod_icv_grid_processes	Set number of cores for ICV grid job.
perccnod_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
perccnod_prefix	Specific verification to run. Default is PERCCNOD.

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
PERCCD parameters	
perccd_icv	Set to 1 to run ICV PERCCD. Note: ICV PERCLDL must be run as well.
perccd_calibre	Set to 1 to run Calibre PERCCD. Note: Calibre PERCLDL must be run as well.
perccd_icv_grid_hosts	Set number of hosts for ICV grid job.
perccd_icv_grid_cores_per_host	Set number of cores per host for ICV grid job.
perccd_icv_grid_h_vmem	Set h_vmem for ICV grid job. Example: 1000G
perccd_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
perccd_prefix	Specific verification to run. Default is PERCCD.

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
PERCLDL parameters	
percldl_icv	Set to 1 to run ICV PERCLDL.
percldl_calibre	Set to 1 to run Calibre PERCLDL.
percldl_icv_grid_processes	Set number of cores for ICV grid job.
percldl_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
percldl_prefix	Specific verification to run. Default is PERCLDL.

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
PERCP2P parameters	
percp2p_icv	Set to 1 to run ICV PERCP2P. Note: ICV PERCLDL must be run as well.
percp2p_calibre	Set to 1 to run Calibre PERCP2P. Note: Calibre PERCLDL must be run as well.
percp2p_icv_grid_hosts	Set number of hosts for ICV grid job.
percp2p_icv_grid_cores_per_host	Set number of cores per host for ICV grid job.
percp2p_icv_grid_h_vmem	Set h_vmem for ICV grid job. Example: 1000G
percp2p_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
percp2p_prefix	Specific verification to run. Default is PERCP2P.

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
PERCTOPO parameters	
perctopo_icv	Set to 1 to run ICV PERCTOPO.
perctopo_calibre	Set to 1 to run Calibre PERCTOPO.
perctopo_icv_grid_processes	Set number of cores for ICV grid job.
perctopo_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
perctopo_prefix	Specific verification to run. Default is PERCTOPO.

Configuring crd_abutment_parameters.csv

Cont'd

- Physical Verification parameters – select PV checks to run

Parameter name	Description
PERCTOPOLA parameters	
perctopola_icv	Set to 1 to run ICV PERCTOPOLA.
perctopola_calibre	Set to 1 to run Calibre PERCTOPOLA.
perctopola_icv_grid_processes	Set number of cores for ICV grid job.
perctopola_calex_extra_arguments	Calex extra arguments for Calibre. (optional) Example: --long
perctopola_prefix	Specific verification to run. Default is PERCTOPOLA.

Appendix A – Sample standard cell boundary configurations

- gf12lpp18 IRL95157 gf12ncpllogl14hdd078f

Process parameters
boundary_layer,62:21
dbu,1e-09
icc2_gds_layer_map,/remote/cad-rep/fab/f123-GF/12nm/LPPLUS/techfiles/icc2/ver1.0_2.0/orig/11M_3Mx_4Cx_2Kx_2Gx_LB/12LPPLUS_11M_3Mx_4Cx_2Kx_2Gx_LB_ndm2gds.layermap
icc2_techfile,/remote/cad-rep/fab/f123-GF/12nm/LPPLUS/techfiles/icc2/ver1.0_2.0/orig/11M_3Mx_4Cx_2Kx_2Gx_LB/12LPPLUS_11M_3Mx_4Cx_2Kx_2Gx_LB_78cpp_ndm.tf
Standard cell parameters
boundary_bottom,HDBLVT14_CAPB3 HDBLVT14_CAPB2
boundary_bottom_left_inside_corner,HDBLVT14_CAPTINC13
boundary_bottom_left_outside_corner,HDBLVT14_CAPBC8
boundary_bottom_right_inside_corner,HDBLVT14_CAPTINC13
boundary_bottom_right_outside_corner,HDBLVT14_CAPBC8
boundary_left,HDBLVT14_CAPLR8
boundary_right,HDBLVT14_CAPLR8
boundary_top,HDBLVT14_CAPT3 HDBLVT14_CAPT2
boundary_top_left_inside_corner,HDBLVT14_CAPBINC13
boundary_top_left_outside_corner,HDBLVT14_CAPTC8
boundary_top_right_inside_corner,HDBLVT14_CAPBINC13
boundary_top_right_outside_corner,HDBLVT14_CAPTC8
stdcell_drive_strength,4
stdcell_gds,<path to>/gf12ncpllogl14hdd078f.gds
stdcell_ndm,<path to>/gf12ncpllogl14hdd078f_frame_only.ndm
stdcell_tap,HDBLVT14_TAPDS

Appendix A – Sample standard cell boundary configurations

Cont’d

- tsmc3eff IRL4259299 ts03nxpllogl03hdd048f

```
# Process parameters
boundary_layer,108:0
dbu,5e-10
icc2_gds_layer_map,/remote/cad-rep/fab/f101-tsmc/3nm/N3E/logic/FF/common/tech_le/fusion_compiler/ver0.9_1a_eval062422/orig/PR_tech/Synopsys/GdsOutMap/PRTF_ICC2_N3E_gdsout_15M_1Xa_h_1Xb_v_1Xc_h_1Xd_v_1Ya_h_1Yb_v_4Y_hvhv_2Yy2Z_SHDMIM.09_1a_eval062422.map
icc2_techfile,/remote/cad-rep/fab/f101-tsmc/3nm/N3E/logic/FF/common/tech_le/fusion_compiler/ver0.9_1a_eval062422/orig/PR_tech/Synopsys/TechFile/Standard/VHV/PRTF_ICC2_N3E_15M_1Xa1Xb1Xc1Xd1Ya1Yb4Y2Yy2Z_UTRDL_M1P48_M2P26_M3P35_M4P35_M5P42_M6P76_M7P76_M8P76_M9P76_M10P76_M11P76_H169_SHDMIM.09_1a_eval062422.tf
tap_distance,16.13
# Standard cell parameters
boundary_bottom,
boundary_bottom_left_inside_corner,
boundary_bottom_left_inside_horizontal_abutment,
boundary_bottom_left_outside_corner,
boundary_bottom_right_inside_corner,
boundary_bottom_right_inside_horizontal_abutment,
boundary_bottom_right_outside_corner,
boundary_left,HDBLVT03_CAPL_9
boundary_right,HDBLVT03_CAPR_9
boundary_top,
boundary_top_left_inside_corner,
boundary_top_left_outside_corner,
boundary_top_right_inside_corner,
boundary_top_right_outside_corner,
stdcell_drive_strength,8
stdcell_gds,/remote/us01sgnfs00502/stdcells/IRL4259299_TSMCN3e_DDR_PHY_H169_Libraries_Release_CQv1p1/ts03nxpllogl03hdd048f/gds/ts03nxpllogl03hdd048f.gds
stdcell_inner_kpt_b,
stdcell_inner_kpt_l,
stdcell_inner_kpt_r,
stdcell_inner_kpt_t,
stdcell_kpt_b,0.338
stdcell_kpt_l,0.144
stdcell_kpt_r,0.144
stdcell_kpt_t,0.338
stdcell_manual_kpt_<macro/testcase>,
stdcell_ndm,/remote/us01sgnfs00502/stdcells/IRL4259299_TSMCN3e_DDR_PHY_H169_Libraries_Release_CQv1p1/ts03nxpllogl03hdd048f/ndm/ts03nxpllogl03hdd048f_frame_only.ndm
stdcell_tap,
stdcell_tap_boundary_wall_cell_n_fill_wall,HDBLVT03_FILL_NWALLY2_15
stdcell_tap_boundary_wall_cell_n_fill_wall_replacement,HDBLVT03_FILL_NWALLCPY2_17
stdcell_tap_boundary_wall_cell_n_inner_corner_boundary,HDBLVT03_CAPNTBINCY2_9
stdcell_tap_boundary_wall_cell_n_left_tap,HDBLVT03_CAPTAPDS_NWLY2_17
stdcell_tap_boundary_wall_cell_n_right_tap,HDBLVT03_CAPTAPDS_NWRY2_17
stdcell_tap_boundary_wall_cell_n_ntap_inner_corner_boundary,HDBLVT03_CAPTAPDS_NWTBINCY3_17
stdcell_tap_boundary_wall_cell_n_ptap_inner_corner_boundary,HDBLVT03_CAPTAPDS_PWTBINCY2_15
stdcell_tap_boundary_wall_cell_n_tap,HDBLVT03_TAPDS_NWY2_10
stdcell_tap_boundary_wall_cell_n_tap_wall,HDBLVT03_TAPDS_NWWALLY2_15
stdcell_tap_boundary_wall_cell_n_tb_boundary,HDBLVT03_CAPNTB_1
stdcell_tap_boundary_wall_cell_n_tb_corner_boundary,HDBLVT03_CAPNTBC_9
stdcell_tap_boundary_wall_cell_n_tb_corner_tap,HDBLVT03_CAPTAPDS_NWTBCY2_19
stdcell_tap_boundary_wall_cell_n_tb_tap,HDBLVT03_CAPTAPDS_NWTBY2_14
stdcell_tap_boundary_wall_cell_n_tb_tap_wall,HDBLVT03_CAPTAPDS_NWWALLTBY2_17
stdcell_tap_boundary_wall_cell_n_tb_wall,HDBLVT03_CAP_NWALLTB_15
stdcell_tap_boundary_wall_cell_p_fill_wall,HDBLVT03_FILL_PWALLY2_15
stdcell_tap_boundary_wall_cell_p_fill_wall_replacement,HDBLVT03_FILL_PWALLCPY2_17
stdcell_tap_boundary_wall_cell_p_inner_corner_boundary,HDBLVT03_CAPPTBINCY2_9
stdcell_tap_boundary_wall_cell_p_left_tap,HDBLVT03_CAPTAPDS_PWLY2_17
stdcell_tap_boundary_wall_cell_p_right_tap,HDBLVT03_CAPTAPDS_PWRY2_17
stdcell_tap_boundary_wall_cell_p_ntap_inner_corner_boundary,HDBLVT03_CAPTAPDS_NWTBINCY2_15
stdcell_tap_boundary_wall_cell_p_ptap_inner_corner_boundary,HDBLVT03_CAPTAPDS_PWTBINCY3_17
stdcell_tap_boundary_wall_cell_p_tap,HDBLVT03_TAPDS_PWY2_10
stdcell_tap_boundary_wall_cell_p_tap_wall,HDBLVT03_TAPDS_PWWALLY2_15
stdcell_tap_boundary_wall_cell_p_tb_boundary,HDBLVT03_CAPPTB_1
stdcell_tap_boundary_wall_cell_p_tb_corner_boundary,HDBLVT03_CAPPTBC_9
stdcell_tap_boundary_wall_cell_p_tb_corner_tap,HDBLVT03_CAPTAPDS_PWTBCY2_21
stdcell_tap_boundary_wall_cell_p_tb_tap,HDBLVT03_CAPTAPDS_PWTBY2_14
stdcell_tap_boundary_wall_cell_p_tb_tap_wall,HDBLVT03_CAPTAPDS_PWWALLTBY2_15
stdcell_tap_boundary_wall_cell_p_tb_wall,HDBLVT03_CAP_PWALLTB_15
```

Appendix A – Sample standard cell boundary configurations

Cont’d

- tsmc5ff12 IRL100162 ts05ncpllogl06hdl051f

Process parameters

boundary_layer,108:0

dbu,5e-10

icc2_gds_layer_map,/remote/cad-rep/fab/f101-tsmc/5nm/logic/FF/common/tech_le/icc2/ver1.2b/orig/PR_tech/Synopsys/GdsOutMap_ICC2/PRTF_ICC2_N5_gdsout_16M_1X_h_1Xb_v_1Xe_h_1Ya_v_1Yb_h_4Y_vhvh_2Yy2Yx2R.12b.map

icc2_techfile,/remote/cad-rep/fab/f101-tsmc/5nm/logic/FF/common/tech_le/icc2/ver1.2b/orig/PR_tech/Synopsys/TechFile/Standard/VHV/PRTF_ICC2_N5_16M_1X1Xb1Xe1Ya1Yb4Y2Yy2Yx2R_UTRDL_M1P34_M2P35_M3P42_M4P42_M5P76_M6P76_M7P76_M8P76_M9P76_M10P76_H210.12b.tf

tap_distance,56

Standard cell parameters

boundary_bottom,HDBLVT06_CAPB1

boundary_bottom_left_inside_corner,HDBLVT06_CAPBLINC14

boundary_bottom_left_inside_horizontal_abutment,HDBLVT06_CAPBLINCGAP3

boundary_bottom_left_outside_corner,HDBLVT06_CAPBLC14

boundary_bottom_right_inside_corner,HDBLVT06_CAPBRINC14

boundary_bottom_right_inside_horizontal_abutment,HDBLVT06_CAPBRINCGAP3

boundary_bottom_right_outside_corner,HDBLVT06_CAPBRC14

boundary_left,HDBLVT06_CAPL14

boundary_right,HDBLVT06_CAPR14

boundary_top,

boundary_top_left_inside_corner,

boundary_top_left_outside_corner,

boundary_top_right_inside_corner,

boundary_top_right_outside_corner,

stdcell_drive_strength,4

stdcell_gds,<path/to>/ts05ncpllogl06hdl051f.gds

stdcell_ndm,<path/to>/ts05ncpllogl06hdl051f_frame_only.ndm

stdcell_tap,HDBLVT06_TAPDS_30

Appendix A – Sample standard cell boundary configurations

Cont’d

- tsmc12ffc18 IRL86969 ts12ncfllogl16hdd090f

```
# Process parameters
boundary_layer,108:0
dbu,1e-09
icc2_gds_layer_map,/remote/cad-rep/fab/f101-tsmc/12nm/logic/FFC/tech_le/icc2/ver1.2a/orig/PR_tech/Synopsys/GdsOutMap/ICC2_N12_gdsout_2Xa1Xd_h_3Xe_vhv_2Y2R.12a.map
icc2_techfile,/remote/cad-rep/fab/f101-tsmc/12nm/logic/FFC/tech_le/icc2/ver1.2a/orig/PR_tech/Synopsys/TechFile/Standard/VHV/PRTF_ICC2_N12_11M_2Xa1Xd3Xe2Y2R_UTRDL_H576_CPODE.12a.tf
# Standard cell parameters
boundary_bottom,HDBLVT16_CAPB3 HDBLVT16_CAPB2
boundary_bottom_left_inside_corner,HDBLVT16_CAPBLIN4
boundary_bottom_left_inside_horizontal_abutment,
boundary_bottom_left_outside_corner,HDBLVT16_CAPBC4
boundary_bottom_right_inside_corner,HDBLVT16_CAPBRIN4
boundary_bottom_right_inside_horizontal_abutment,
boundary_bottom_right_outside_corner,HDBLVT16_CAPBC4
boundary_left,HDBLVT16_CAPL4
boundary_right,HDBLVT16_CAPR4
boundary_top,HDBLVT16_CAPT3 HDBLVT16_CAPT2
boundary_top_left_inside_corner,HDBLVT16_CAPTLIN4
boundary_top_left_outside_corner,HDBLVT16_CAPTC4
boundary_top_right_inside_corner,HDBLVT16_CAPTRIN4
boundary_top_right_outside_corner,HDBLVT16_CAPTC4
stdcell_drive_strength,8
stdcell_gds,<path/to>/ts12ncfllogl16hdd090f.gds
stdcell_ndm,<path/to>/ts12ncfllogl16hdd090f_frame_only.ndm
stdcell_tap,HDBLVT16_TAPDS
```

Appendix A – Sample standard cell boundary configurations

Cont’d

- tsmc16ffc18 IRL95691 ts16ncfllogl16hdd090f

Process parameters
boundary_layer,108:0
dbu,1e-9
icc2_gds_layer_map,/remote/cad-rep/fab/f101-tsmc/16nm/logic/FFC/common/tech_le/icc/ver1.4a/orig/PR_tech/Synopsys/GdsOutMap/ICC_N16_gdsout_2Xa1Xd_h_3Xe_vhv_2Y2R.14a.map
icc2_techfile,/remote/cad-rep/fab/f101-tsmc/16nm/logic/FFC/common/tech_le/icc/ver1.4a/orig/PR_tech/Synopsys/TechFile/Standard/VHV/PRTF_ICC_N16_11M_2Xa1Xd3Xe2Y2R_UTRDL_9T_PODE.14a.tf
Standard cell parameters
boundary_bottom,HDBLVT16_CAPB3 HDBLVT16_CAPB2
boundary_bottom_left_inside_corner,HDBLVT16_CAPBLIN4
boundary_bottom_left_inside_horizontal_abutment,
boundary_bottom_left_outside_corner,HDBLVT16_CAPBC4
boundary_bottom_right_inside_corner,HDBLVT16_CAPBRIN4
boundary_bottom_right_inside_horizontal_abutment,
boundary_bottom_right_outside_corner,HDBLVT16_CAPBC4
boundary_left,HDBLVT16_CAPL4
boundary_right,HDBLVT16_CAPR4
boundary_top,HDBLVT16_CAPT3 HDBLVT16_CAPT2
boundary_top_left_inside_corner,HDBLVT16_CAPTLIN4
boundary_top_left_outside_corner,HDBLVT16_CAPTC4
boundary_top_right_inside_corner,HDBLVT16_CAPTRIN4
boundary_top_right_outside_corner,HDBLVT16_CAPTC4
stdcell_drive_strength,4
stdcell_gds,/remote/us01sgnfs00502/stdcells/IRL95691_TSMC16FFC_DDR_PHY/ts16ncfllogl16hdd090f/gds/ts16ncfllogl16hdd090f.gds
stdcell_ndm,/remote/us01sgnfs00502/stdcells/IRL95691_TSMC16FFC_DDR_PHY/ts16ncfllogl16hdd090f/ndm/ts16ncfllogl16hdd090f_frame_only.ndm
stdcell_tap,HDBLVT16_TAPDS

Revision history

Version	Notes
2019.08	Initial release.
2019.09	Added support for no pin text layers defined.
2019.09-1	Script now determines cell sizes through boundary_layer parameter, eliminating need for size parameters. Added parameters for running DRC, LVS and PERC_LDL (not currently enabled). Parameter added for signal pin uniquification.
2019.10	PERC_LDL now enabled. msip_cd_pv module can be set to a specific version.
2019.10-1	Added support for hard macro specific utility cell testcases. Covercell insertion is now only enabled for hard macros, not utility cells.
2019.11	Floorplan bug fixes.
2019.12	Added LPDDR54 support. Added uu_per_dbu parameter for correct testcase GDS creation.
2020.01	Added support for Calex extra arguments.
2020.01-1	Added support for standard cell boundary testcases. Added support for specifying virtual connect value for LVS.

Revision history

Cont'd

Version	Notes
2020.08	Fixed boundary_master_stdcell_ew/ns testcase macros references. Added support for existing stdcell NDM to bypass stdcell library creation.
2020.08-1	Modified to use techlib from stdcell NDM if given. Added int22ffl18 pin text support.
2021.08	-Updated UDE3/CC log file structure for compatibility with new UDE3. -Stdcell NDM and macro LEFs are now required for stdcell boundary testcases. -Stdcell boundary testcases are now generated with the name "boundary_stdcell_<macro>" for macros listed in the testcases_stdcell parameter. -TSMC5-specific fixes for stdcell boundary testcases. -Added testcases_wrapper parameter for *wrapper_<macro> testcases where script will add <macro> as subcell to *wrapper_<macro>, then run PV. -Added generate_cdl parameter to enable CDL generation for *wrapper_<macro> testcases. -Added testcases_pv_only parameter. Cells listed here will have PV run on them with the provided GDS and CDL. -Added support for testcases_utility_* parameters for utility cell/block abutment checking. See documentation for details on how to use.

Revision history

Cont’d

Version	Notes
2021.08	(cont’d) -Added support for FEOL and BEOL fill during DRC with drc_feol_fill and drc_beol_fill parameters. -PV result files are now copied to the work directory rather than within each testcase directory. -Added "-runnohalt" to ICWB execution to bypass errors that occur when the same GDS is referenced again through "layout reference add". -Added additional power supplies to avoid uniquifying pin names. -Added support for LPDDR5xm testcases with applicable parameters. -Added support for HM+VDD clamp testcases for PERC, with applicable parameters. -ICC2 flows now use scale_factor. -Script now continues to next testcase while PV jobs are executing. PV jobs are run in parallel. -PV parameters modified for specifying ICV or Calibre for DRC/LVS jobs. -Added stdcell_drive_strength parameter to specify version of INV/BUF/ND2/NR2 cells to add.

Revision history

Cont’d

Version	Notes
2021.08	(cont’d) -Added stdcell_tap parameter to specify tap cell to use. Required as some stdcell libraries include several tap options. -Added stdcell_kpt_* parameters to specify stdcell keepout region around macro. -Removed following parameters: • boundary_top* - These boundary cells not required due to even number of stdcell rows and non-flipped first row. • calex_site - only site 3 exists now. • stdcell_lef - no longer used in stdcell boundary testcases. • uu_per_dbu - it is now calculated by the script.
2021.08-1	Links to the physical verification report files are now created in the script's work directory instead of copies of the files.

Revision history

Cont'd

Version	Notes
2021.09	-Renamed testcases parameter to testcases_abutment for clarity. -Added support for abutment standard cell boundary testcases, where macros are first abutted prior to standard cell ring insertion. Specified with testcases_abutment_stdcell parameter. Testcases are generated with the name stdcell_ring_<testcase>. -Added support for rectilinear boundaries in standard cell boundary testcases. Changed generated testcase name to stdcell_ring_<macro>. -Script can now generate LEF for standard cell boundary testcases by setting the generate_lef parameter to 1. Note that size-only LEFs are generated - no pin information is generated. -Re-introduced boundary_top* parameters for rectilinear boundaries where double stdcell row heights are not followed for each boundary segment. -Added support for abutment wrapper testcases where macros are first abutted prior to insertion as a subcell into wrapper. Wrapper cells should be named as *wrapper_<testcase> and supplied to the new testcases_abutment_wrapper parameter. -Updated to use ICVWB instead of ICWBEV. -Added LPDDR54 standard cell boundary and PERC testcases.

Revision history

Cont'd

Version	Notes
2021.11	-Complete set of LPDDR54 CRD abutment and boundary testcases added or updated. -Fix to Generate_Stdcell_Ring proc to use terminal boundary for text origin coordinate instead of bbox as bbox coordinate may not fall within non-rectangular pin shape.
2021.12	-Added CDL uniquification with uniquify_input_cdl and uniquify_input_cdl_filter_file parameters. Only applies to Physical Verification Only and Wrapper testcases.
2021.12-1	-Added support for Standard Cell Fill testcases with the testcases_stdcell_fill parameter.
2022.01	-Added stdcell_inner_kpt_* parameters to specify keepout from top level boundary in Standard Cell Fill testcases.
2022.02	-Added LPDDR5X abutment testcases.
2022.03	-Added abutment parameters to enable generation of boundary with upsizing. -For [Abutment] Standard Cell Boundary testcases, signal pin names for spare cells are now uniquified in order to eliminate LVS opens. -For [Abutment] Standard Cell Boundary testcases, macro is now placed at testbench origin. -For Standard Cell Fill testcases, added pin labels at top level.

Revision history

Cont'd

Version	Notes
2022.03-1	-Addition of stdcell_manual_kpt_<macro/testcase> parameters to add manual standard cell keepouts to [Abutment] Standard Cell Boundary and Standard Cell Fill testcases. -Addition of script log, crd_abutment.log, generation.
2022.03-2	-Fixes to support gf12lpp18 standard cells. -Removed FOUNDRY_DEFAULT value from virtual_connect parameter in parameters file template as some nodes don't report text opens by foundry default.
2022.03-3	-Support for Perforce paths with revision # for CDL, DEF, GDS and LEF collaterals. -Addition of log files for each testcase called <testcase>.log. -Addition of parameter file contents to log files.
2022.03-4	-Fixes to support tsmc12ffc18 standard cells.
2022.04	-Script modified to uniquify all GDS files specified in parameters file if uniquify_input_gds is enabled. -Script modified to not use macros array variable. -Fixes to tsmc5ff12 standard cell support.

Revision history

Cont'd

Version	Notes
2022.04-1	-Fixes to tsmc5ff12 standard cell support. -Setting version of ICC2, ICVWB and msip_cd_pv tools to support result reproducibility. These will get updated with future script versions.
2022.04-2	-Fixes to tsmc12ffc18 standard cell support related to layer map.
2022.05	-Updated LPDDR5X testcases for CRD ver0.7. -Changed ICVWB to now stop on errors.
2022.05-1	-Added DDR5 testcases for CRD ver0.7. -Added CDL to pvbatch call for PERCCNOD_ICV due to new PERCCNOD flow requiring CDL.
2022.05-2	-Adding usage statistics monitor. (wadhawan)

Revision history

Cont'd

Version	Notes
2022.07	-Removed testcase floorplans to a separate crd_abutment_floorplans.tcl file. This file must be in the same directory as the crd_abutment.tcl script file. Note that crd_abutment.tcl no longer needs to be copied to working directory - it can be run from its published location. crd_abutment_parameters is the only file required in working directory. -Updated tool versions: tclsh 8.6.6, ICC2 2022.03-SP2, ICVWB 2022.03-SP1 and msip_cd_pv 2022.05. -Updated output file structure to match CKT P4 release structure. -Added <pv_type>_prefix parameters to support alternate PV types. -Added partial support for layout output in OASIS format. Note that there are still too many issues to recommend using OASIS. -Replaced virtual_connect parameter with virtual_connect_icv and virtual_connect_calibre to support the different settings used by the tools.
2022.07-1	-Addition of LPDDR54 corner clamp floorplans from CRD v1.12.

Revision history

Cont'd

Version	Notes
2022.08	-Standard Cell Boundary and Abutment Standard Cell Boundary testcases are now created as boundary_<macro>_stdcell and boundary_<testcase>_stdcell to match with CRDs. -Added support for tsmc3eff standard cells. -Updated ICC2 version to 2022.03-SP3. -Added support for DRC error limit through drc_error_limit parameter.
2022.08-1	-Fixes for tsmc16ffc18 standard cells for compatibility with newer ICC2 versions.