**LPDDR5X Driver Level Shift Specification**

Cell Name: dwc\_lpddr5xphy\_lstx\_dx4, dwc\_lpddr5xphy\_lstx\_dx5 dwc\_lpddr5xphy\_lstx\_acx2, dwc\_lpddr5xphy\_lstx\_zcal, dwc\_lpddr5xphy\_lstx\_csx2

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1. **Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Date** | **Owner** | **Description** |
| 0 | 3/31/21 | bapna | Copied from Combophy specifications |
| 1 | 4/15/21 | sounakd | Updated logic funcationlity tables, assertion waveforms and pins lists, with reference to D930 changes as compared to D900 |
| 2 | 4/22/21 | sounakd | Added dx4/dx5 related specifications/pin lists |
| 3 | 4/29/21 | sounakd | Removed FuncMode/TxPowerDown<1:0> functionality from the macros, edited the Truth-Tables accordingly. |
| 4 | 5/18/21 | sounakd | Added CSR defaults for unused CSR bits, removed csrreserved<1> (Chip Select) related logic functionality from logic table. |
| 5 | 6/26/21 | sounakd | Added schmitt-trigger functionality to the logic diagram and edited pin list for the same. Added Schmitt trigger simulation plan |
| 6 | 7/8/21 | sounakd | Updated pin lists and logic diagram, Added comment, ‘removed’ for all the unused output pins that are removed from the schematic.  Logic diagram has was updated for csrLSTxSlewPD path. |
| 7 | 7/26/21 | mithunn | Added lstx\_csx2 pin list and description |
| 8 | 7/29/21 | sounakd | Updated pin list for lstx\_acx2/dx4/dx5/zcal with the new VIO\_PwrOK routing. Updated the logic diagram and Index |
| 9 | 9/9/21 | sounakd | Updated pin list for lstx\_acx2 – Removed ForceEn\_VDA |
| 10 | 9/13/21 | mithunn | Removed ForceEn\_VDA, scan\_si and scan\_so pins from lstx\_csx2 as per JIRA [P80001562-173513](https://jira.internal.synopsys.com/browse/P80001562-173513) |
| 11 | 9/22/21 | sounakd | Updated pin list as per the latest hierarchy update – JIRA [P80001562-178185](https://jira.internal.synopsys.com/browse/P80001562-178185)  Added lockup latch and modified output pins to the block diagram, and removed ForceEn\_VDA from the block diagram. |
| 12 | 10/7/2021 | mithunn | Renamed VDDQ\_VDD2H to VDD2H for lstx\_csx2 |
| 13 | 10/8/2021 | sounakd | Added BurnIn pins in the pin list for LSTX\_ACX2/DX4/DX5/ZCAL |
| 14 | 10/24/2021 | sounakd | Added connection details for LSTX\_DX5 csrreserved<4:0> bits |
| 15 | 11/02/2021 | sounakd | Updated top level block diagram for CSR defaults update: <https://jira.internal.synopsys.com/browse/P80001562-126172>  Added table fo slewpd which was missing.  Added HM connection block diagram  Added table for CSR defaults with Resetasync assertion |
| 16 | 12/21/2021 | Bapna | Added Scan/IDDQ mode gating details |
| 17 | 1/28/2021 | mithunn | Added scan\_mode gating on CalUpdate |

**Table** **1****‑1 Revision History**

# Functional outline

## Overview

The main function of a level shifter macro includes

* Centralize the Pctrl, Nctrl blocks for calibration or slew rate control for TXBE. Scanable flops are added to retime calibration codes with Dficlk.
* Buffer csr or non-csr signals to ZCALIO and ACX2, DX4 and DX5
* lstx\_csx2 only buffers the VIO\_PwrOk signal. All other inputs are terminated with load similar to lstx\_acx2. All internal (CKT-CKT interface) unused pins have been removed from the block.

There are few level shifter variants to serve various hard macros that contain different type or number of bitslices or other blocks.

|  |  |  |
| --- | --- | --- |
| Level shifter variants | Hard macro | Hard macro description |
| dwc\_lpddr5xphy\_lstx\_acx2 | dwc\_lpddr5xphy\_acx2 | 2 TXRXAC |
| dwc\_lpddr5xphy\_lstx\_zcal | dwc\_lpddr5xphy\_zcal | 1 ZCALIO, 1 ATO, 1 VREGDAC |
| dwc\_lpddr5xphy\_lstx\_dx4 | dwc\_lpddr5xphy\_dx4 | 4 TXRXDQ, 1 TXRXDQS |
| dwc\_lpddr5xphy\_lstx\_dx5 | dwc\_lpddr5xphy\_dx5 | 5 TXRXDQ, 1 TXRXDQS |
| dwc\_lpddr5xphy\_lstx\_csx2 | dwc\_lpddr5xphy\_csx2 | 2 TXRXCS |

## Floorplan

LSTX is floorplaned as such that DI pins are on DI-CKT beach front and CKT pins abut their load pins in bit slices.

## Architecture

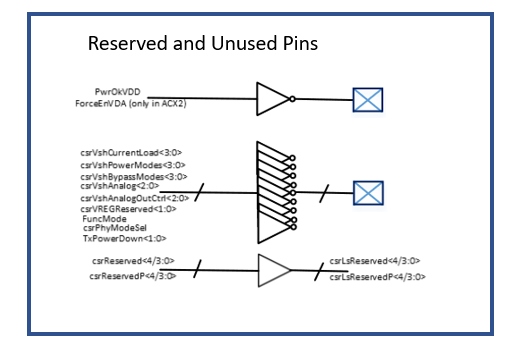
The following block diagram shows the main control logic in dwc\_lpddr5xphy\_lstx\_# macros.

Diagram, schematic

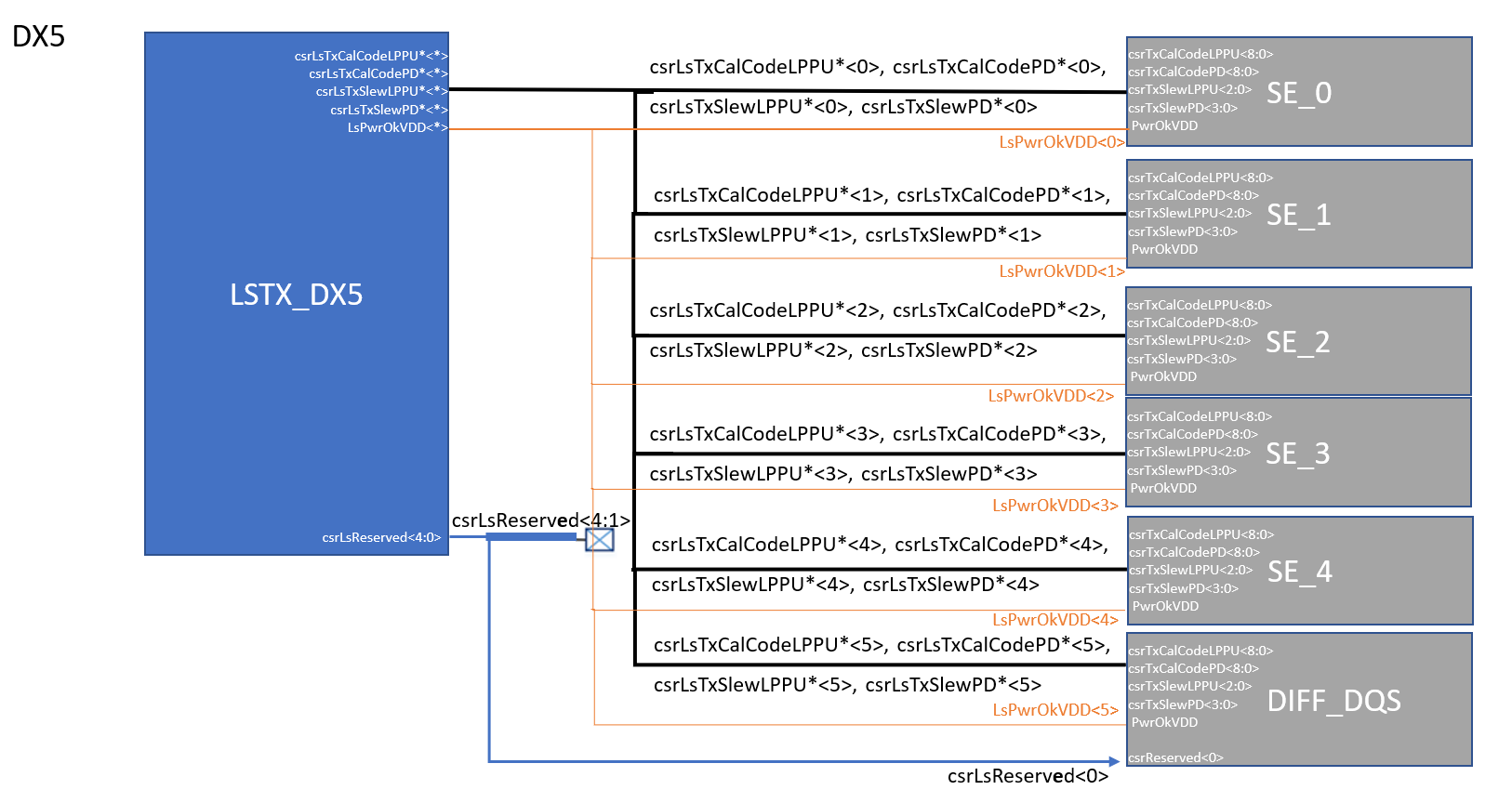
Description automatically generated

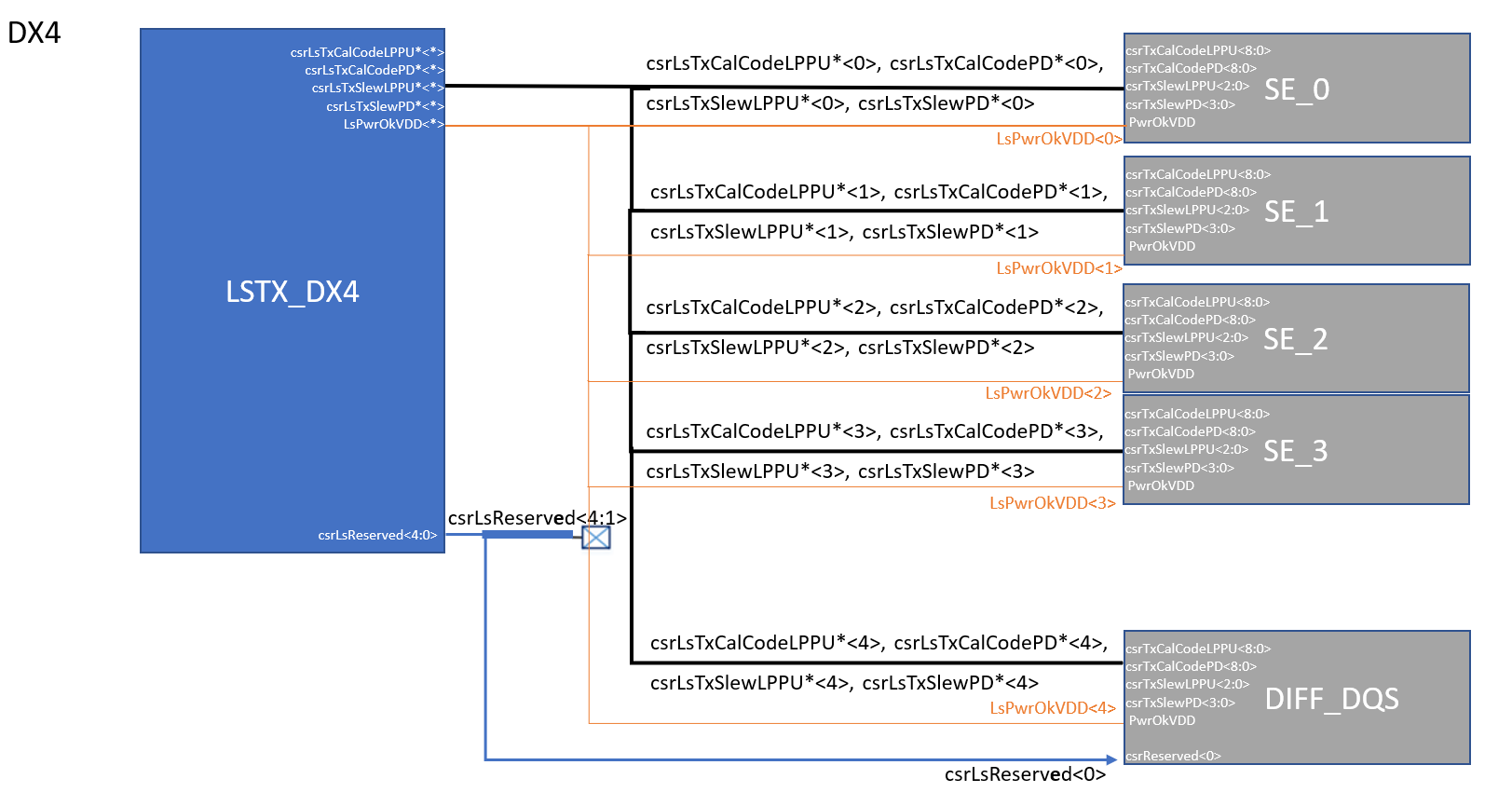
Figure 2‑1 Top Level Functional Diagram

Note: The above diagram includes Scan and iddq mode gating added in //depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_PHY\_CKT\_Input\_Pin\_Specs.xlsx



Note: In csrLsTx\*<x:0>,x stands for the number of slices, that particular outputs is routed to. So in case of DX4 and ACX2, x will be 5 and 2 respectively, and accordingly for the other LSTX macros.







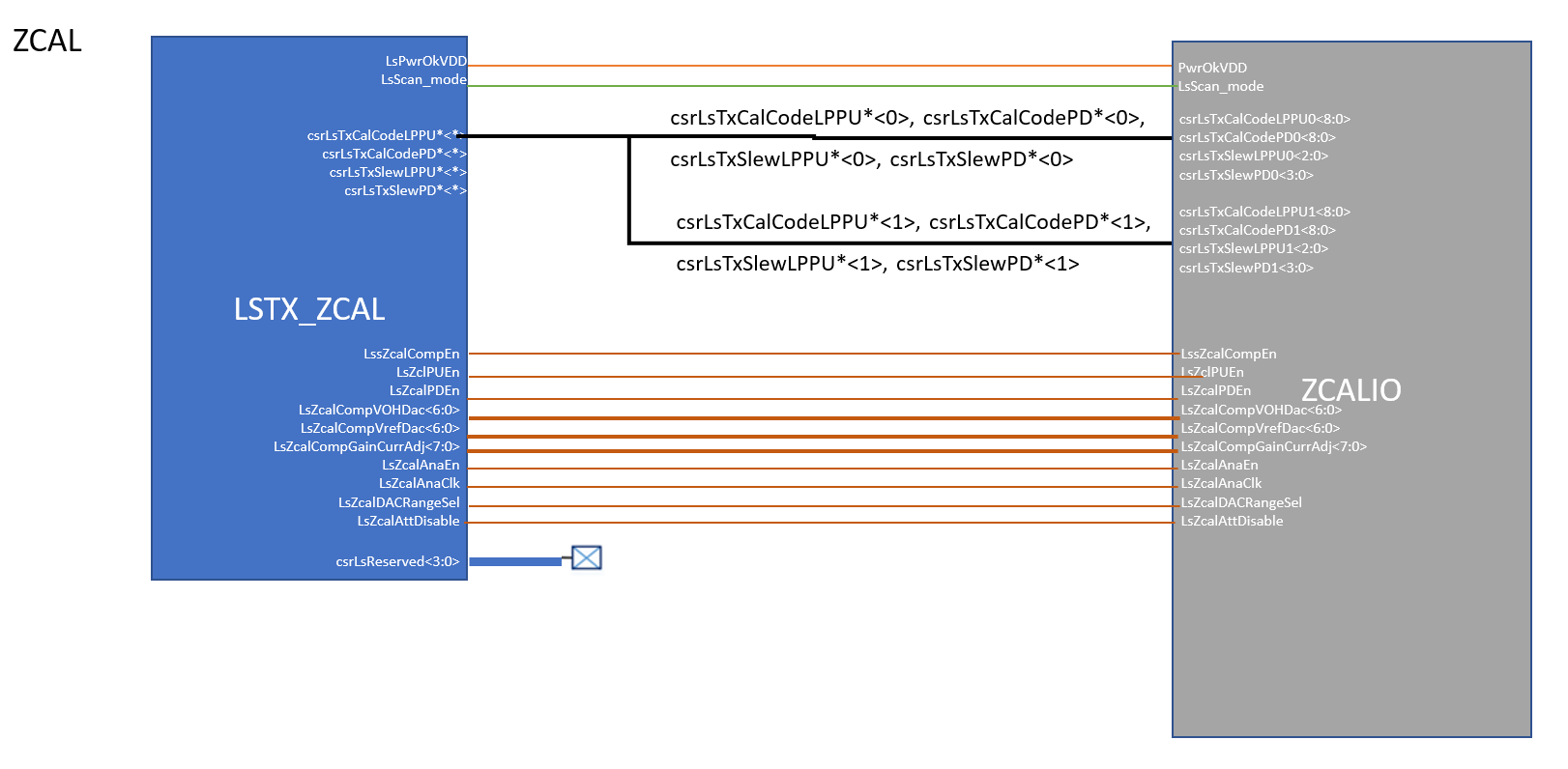


Figure 2‑2 Hard Macro connections for each LSTX Macro

## Assertions

//depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_CKT\_Macro\_Assertions.xlsx

Wave File for wavedrom <http://wavedrom.com/editor.html>

* LP5 Mode

{signal: [

{name: 'scan\_mode' ,wave: 'x0......|...|....'},

{name: 'VDDQ' ,wave: 'x1......|...|....'},

{name: 'VDD' ,wave: 'x1......|..0|1...'},

{name: 'PwrOkVDD' ,wave: '0..1....|..0|...1'},

{name: 'FuncMode' ,wave: 'x0....1.|.0.|....', node: '......c...d.........'},

{name: 'TxPowerDown' ,wave: 'x1...0..|..1|....',node:'.....n....'},

{name: 'csrLsTxCalCodeLPPU' ,wave: 'x3....5.|.3.|....',node:'......f...g.......', data: ["0", "csrTxCalCodePU", "0", "415",],},

{name: 'csrLsTxCalCodePD' ,wave: 'x3...x5.|..3|....',node:'.....hi....j....', data: ["0", "csrTxCalCodePD", "0", ],},

{name: 'CalUpdate' ,wave: 'x0....10|...|....',node:'.....klm.........',}, ],

edge:['a~>c 100ns','d~>b 5ns','a->o','n->h','n->k','k->l','l->i','l<->m','d->g','b->j','n~>c 5ns','c->f']}

## Scan/IDDQ mode gating

Refer: //depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_PHY\_CKT\_Input\_Pin\_Specs.xlsx



CalUpdate scan\_mode and IDDQ\_mode gating



csrReserved / csrReservedP gating with scan\_mode and IDDQ\_mode pins

## Logical functionality

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PwrOkVDD** | **VIO\_PwrOK** | **IDDQ\_mode** | **scan\_mode** | **csrLsTxCalCodeLPPU<8:0>** |
| 0 | 0 | x | x | d’0 |
| 1 | 1 | 1 | x | d’0 |
| 1 | 1 | 0 | 0 | csrTxCalCodePU<8:0> |
| 1 | 1 | 0 | 1 | d’511 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PwrOkVDD** | **VIO\_PwrOK** | **IDDQ\_mode** | **scan\_mode** | **csrLsTxCalCodePD<8:0>** |
| 0 | 0 | x | x | d’0 |
| 1 | 1 | 1 | x | d’0 |
| 1 | 1 | 0 | 0 | csrTxCalCodePD<8:0> |
| 1 | 1 | 0 | 1 | d’511 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PwrOkVDD** | **VIO\_PwrOK** | **IDDQ\_mode** | **scan\_mode** | **csrLsTxSlewLPPU<2:0>** |
| 0 | 0 | x | x | d’0 |
| 1 | 1 | 1 | x | d’0 |
| 1 | 1 | 0 | 0 | csrTxSlewPU<2:0> |
| 1 | 1 | 0 | 1 | d’0 |
| **PwrOkVDD** | **VIO\_PwrOK** | **IDDQ\_mode** | **scan\_mode** | **csrLsTxSlewPD<3:0>** |
| 0 | 0 | x | x | d’0 |
| 1 | 1 | 1 | x | d’0 |
| 1 | 1 | 0 | 0 | csrTxSlewPD<3:0> |
| 1 | 1 | 0 | 1 | d’0 |

Table 2‑2 Control Logic

## Pin list

Table 2‑1 Pin List for dwc\_lpddr5xphy\_lstx\_dx4

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| dwc\_lpddr5xphy\_lstx\_dx4 | | | | | | |
| **Pin name** | **I/O** | **Width** | **Power Domain** | **Description** | **Receiving Clock** | **Changes** |
| IDDQ\_mode | Input | 1 | VDD | when “1”, enable IDDQ test | Async |  |
| scan\_mode | Input | 1 | VDD | refer to Error: Reference source not found | Async |  |
| VDD | Input | 1 | VDD | Core supply voltage | N/A |  |
| VDDQ | Input | 1 | VDDQ | I/O supply voltage | N/A |  |
| VSS | Input | 1 | VSS | Ground | N/A |  |
| VIO\_PwrOk | Input | 1 | ~~VDDQ~~  VDDQ\_VDD2H | PwrOkVDD in VDDQ\_VDD2H domain, refer to Error: Reference source not found | Async |  |
| LsPwrOkVDD | Output | 5 | VDD | Schmitt trigger output (with positive polarity) for ‘VIO\_PwrOk’ input signal for TX BE  LsPwrOkVDD s to the 5 DQ instances | Async |  |
| ResetAsync | Input | 1 | VDD | Asynchronous reset for cal code flops – When asserted, passes CSR Default value 9’b110000000 to csrlstxcalcodelpppu\*<\*>/csrlstxcalcodepd\*<\*> | Async |  |
| csrTxCalCodePU | Input | 9 | VDD | calibration code for PU | Async |  |
| csrTxCalCodePD | Input | 9 | VDD | calibration code for PD | Async |  |
| csrLsTxCalCodeLPPU8 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 8 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU7 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 7 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU6 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 6 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU5 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 5 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU4 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 4 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU3 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 3 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU2 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 2 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU1 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 1 to the 5 DQ instances | Async |  |
| csrLsTxCalCodeLPPU0 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 0 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD8 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 8 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD7 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 7 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD6 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 6 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD5 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 5 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD4 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 4 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD3 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 3 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD2 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 2 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD1 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 1 to the 5 DQ instances | Async |  |
| csrLsTxCalCodePD0 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 0 to the 5 DQ instances | Async |  |
| csrTxSlewPU | Input | 4 | VDD | Slew rate code for PU | Async |  |
| csrTxSlewPD | Input | 4 | VDD | Slew rate code for PD | Async |  |
| csrLsTxSlewLPPU2 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 2 to the 5 DQ instances | Async |  |
| csrLsTxSlewLPPU1 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 1 to the 5 DQ instances | Async |  |
| csrLsTxSlewLPPU0 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 0 to the 5 DQ instances | Async |  |
| csrLsTxSlewPD3 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 3 to the 5 DQ instances | Async |  |
| csrLsTxSlewPD2 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 2 to the 5 DQ instances | Async |  |
| csrLsTxSlewPD1 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 1 to the 5 DQ instances | Async |  |
| csrLsTxSlewPD0 | Output | 5 | VDD | refer to Error: Reference source not found  Bit 0 to the 5 DQ instances | Async |  |
| csrReserved | Input | 5 | VDD | csrReserved<0> to control RXDQS DCC. csrReserved<4:1> are reserved by CKT | Async |  |
| csrReservedP | Input | 5 | VDD | Available in Std-Prod.  For AMD-ComboPHY: these bits are taken by RTL for csrDqVregRsvdP, so don’t use. | Async |  |
| csrLsReserved | Output | 5 | VDD | Buffered csrReserved <4:0> | Async |  |
| csrLsReservedP | Output | 5 | VDD | Buffered csrReservedP<4:0> in Std-Prod or csrDqVregRsvdP<4:0> in AMD-ComboPHY | Async |  |
| Dficlk | Input | 1 | VDD | Half rate clock to retime calibration code | Sync |  |
| CalUpdate | Input | 1 | VDD | Gate Dficlk in mission mode | Async |  |
| scan\_shift\_cg | Input | 1 | VDD | Gate Dficlk in scan mode | Async |  |
| scan\_shift | Input | 1 | VDD | Select scan\_si in flops | Async |  |
| scan\_si | Input | 1 | VDD | Scan input | Sync |  |
| scan\_so | Output | 1 | VDD | Scan output | Sync |  |
| LsIDDQ\_mode | Output | 1 | VDD | Buffered IDDQ\_mode | Async |  |
| LsScan\_mode | Output | 1 | VDD | Buffered scan\_mode | Async |  |
| BurnIn | Input | 1 | VDD | Unused pin with dummy inverter. Single Pin to enter & exit BurnIn. Functionality will be added in future. https://jira.internal.synopsys.com/browse/P80001562-170623 | Async |  |

Table 2‑2 Pin List for dwc\_lpddr5xphy\_lstx\_dx5

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| dwc\_lpddr5xphy\_lstx\_dx5 | | | | | | |
| **Pin name** | **I/O** | **Width** | **Power Domain** | **Description** | **Receiving Clock** | **Changes** |
| IDDQ\_mode | Input | 1 | VDD | when “1”, enable IDDQ test | Async |  |
| scan\_mode | Input | 1 | VDD | refer to Error: Reference source not found | Async |  |
| VDD | Input | 1 | VDD | Core supply voltage | N/A |  |
| VDDQ | Input | 1 | VDDQ | I/O supply voltage | N/A |  |
| VSS | Input | 1 | VSS | Ground | N/A |  |
| VIO\_PwrOk | Input | 1 | ~~VDDQ~~  VDDQ\_VDD2H | PwrOkVDD in VDDQ\_VDD2H domain, refer to Error: Reference source not found | Async |  |
| LsPwrOkVDD | Output | 6 | VDD | Schmitt trigger output (with positive polarity) for ‘VIO\_PwrOk’ input signal for TX BE  LsPwrOkVDD to the 6 DQ instances | Async |  |
| ResetAsync | Input | 1 | VDD | Asynchronous reset for cal code flops – When asserted, passes CSR Default value 9’b110000000 to csrlstxcalcodelpppu\*<\*>/csrlstxcalcodepd\*<\*> | Async |  |
| csrTxCalCodePU | Input | 9 | VDD | calibration code for PU | Async |  |
| csrTxCalCodePD | Input | 9 | VDD | calibration code for PD | Async |  |
| csrLsTxCalCodeLPPU8 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 8 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU7 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 7 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU6 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 6 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU5 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 5 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU4 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 4 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU3 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 3 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU2 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 2 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU1 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 1 to the 6 DQ instances | Async |  |
| csrLsTxCalCodeLPPU0 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 0 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD8 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 8 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD7 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 7 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD6 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 6 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD5 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 5 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD4 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 4 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD3 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 3 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD2 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 2 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD1 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 1 to the 6 DQ instances | Async |  |
| csrLsTxCalCodePD0 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 0 to the 6 DQ instances | Async |  |
| csrTxSlewPU | Input | 4 | VDD | Slew rate code for PU | Async |  |
| csrTxSlewPD | Input | 4 | VDD | Slew rate code for PD | Async |  |
| csrLsTxSlewLPPU2 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 2 to the 6 DQ instances | Async |  |
| csrLsTxSlewLPPU1 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 1 to the 6 DQ instances | Async |  |
| csrLsTxSlewLPPU0 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 0 to the 6 DQ instances | Async |  |
| csrLsTxSlewPD3 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 3 to the 6 DQ instances | Async |  |
| csrLsTxSlewPD2 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 2 to the 6 DQ instances | Async |  |
| csrLsTxSlewPD1 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 1 to the 6 DQ instances | Async |  |
| csrLsTxSlewPD0 | Output | 6 | VDD | refer to Error: Reference source not found  Bit 0 to the 6 DQ instances | Async |  |
| csrReserved | Input | 5 | VDD | csrReserved<0> to control RXDQS DCC. csrReserved<4:1> are reserved by CKT | Async |  |
| csrReservedP | Input | 5 | VDD | Available in Std-Prod.  For AMD-ComboPHY: these bits are taken by RTL for csrDqVregRsvdP, so don’t use. | Async |  |
| csrLsReserved | Output | 5 | VDD | Buffered csrReserved<4:0> | Async |  |
| csrLsReservedP | Output | 5 | VDD | Buffered csrReservedP<4:0> in Std-Prod or csrDqVregRsvdP<4:0> in AMD-ComboPHY | Async |  |
| Dficlk | Input | 1 | VDD | Half rate clock to retime calibration code | Sync |  |
| CalUpdate | Input | 1 | VDD | Gate Dficlk in mission mode | Async |  |
| scan\_shift\_cg | Input | 1 | VDD | Gate Dficlk in scan mode | Async |  |
| scan\_shift | Input | 1 | VDD | Select scan\_si in flops | Async |  |
| scan\_si | Input | 1 | VDD | Scan input | Sync |  |
| scan\_so | Output | 1 | VDD | Scan output | Sync |  |
| LsIDDQ\_mode | Output | 1 | VDD | Buffered IDDQ\_mode | Async |  |
| LsScan\_mode | Output | 1 | VDD | Buffered scan\_mode | Async |  |
| BurnIn | Input | 1 | VDD | Unused pin with dummy inverter. Single Pin to enter & exit BurnIn. Functionality will be added in future. https://jira.internal.synopsys.com/browse/P80001562-170623 | Async |  |

Table 2‑3 Pin List for dwc\_lpddr5xphy\_lstx\_acx2

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| dwc\_lpddr5xphy\_lstx\_acx2 | | | | | | |
| **Pin name** | **I/O** | **Width** | **Power Domain** | **Description** | **Receiving Clock** | **Changes** |
| IDDQ\_mode | Input | 1 | VDD | when “1”, enable IDDQ test | Async |  |
| scan\_mode | Input | 1 | VDD | refer to Error: Reference source not found | Async |  |
| VDD | Input | 1 | VDD | Core supply voltage | N/A |  |
| VDDQ | Input | 1 | VDDQ | I/O supply voltage | N/A |  |
| VSS | Input | 1 | VSS | Ground | N/A |  |
| VIO\_PwrOk | Input | 1 | ~~VDDQ~~  VDDQ\_VDD2H | PwrOkVDD in VDDQ\_VDD2H domain, refer to Error: Reference source not found | Async |  |
| LsPwrOkVDD | Output | 2 | VDD | Schmitt trigger output (with positive polarity) for ‘VIO\_PwrOk’ input signal for TX BE  LsPwrOkVDD to the 2 AC instances | Async |  |
| ResetAsync | Input | 1 | VDD | Asynchronous reset for cal code flops – When asserted, passes CSR Default value 9’b110000000 to csrlstxcalcodelpppu\*<\*>/csrlstxcalcodepd\*<\*> | Async |  |
| csrTxCalCodePU | Input | 9 | VDD | calibration code for PU | Async |  |
| csrTxCalCodePD | Input | 9 | VDD | calibration code for PD | Async |  |
| csrLsTxCalCodeLPPU8 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 8 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU7 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 7 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU6 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 6 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU5 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 5 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU4 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 4 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU3 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 3 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 AC instances | Async |  |
| csrLsTxCalCodeLPPU0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD8 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 8 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD7 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 7 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD6 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 6 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD5 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 5 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD4 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 4 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD3 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 3 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 AC instances | Async |  |
| csrLsTxCalCodePD0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 AC instances | Async |  |
| csrTxSlewPU | Input | 4 | VDD | Slew rate code for PU | Async |  |
| csrTxSlewPD | Input | 4 | VDD | Slew rate code for PD | Async |  |
| csrLsTxSlewLPPU2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 AC instances | Async |  |
| csrLsTxSlewLPPU1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 AC instances | Async |  |
| csrLsTxSlewLPPU0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 AC instances | Async |  |
| csrLsTxSlewPD3 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 3 to the 2 AC instances | Async |  |
| csrLsTxSlewPD2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 AC instances | Async |  |
| csrLsTxSlewPD1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 AC instances | Async |  |
| csrLsTxSlewPD0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 AC instances | Async |  |
| csrReserved | Input | 4 | VDD | Reserved | Async |  |
| csrLsReserved | Output | 4 | VDD | Buffered csrReserved<3:0> | Async |  |
| csrReservedP | Input | 4 | VDD | ReservedP | Async |  |
| csrLsReservedP | Output | 4 | VDD | Buffered csrReservedP<3:0> | Async |  |
| Dficlk | Input | 1 | VDD | Half rate clock to retime calibration code | Sync |  |
| CalUpdate | Input | 1 | VDD | Gate Dficlk in mission mode | Async |  |
| scan\_shift\_cg | Input | 1 | VDD | Gate Dficlk in scan mode | Async |  |
| scan\_shift | Input | 1 | VDD | Select scan\_in in flops | Async |  |
| scan\_si | Input | 1 | VDD | Scan input | Sync |  |
| scan\_so | Output | 1 | VDD | Scan output | Sync |  |
| LsIDDQ\_mode | Output | 1 | VDD | Buffered IDDQ\_mode | Async |  |
| LsScan\_mode | Output | 1 | VDD | Buffered scan\_mode | Async |  |
| BurnIn | Input | 1 | VDD | Unused pin with dummy inverter. Single Pin to enter & exit BurnIn. Functionality will be added in future. https://jira.internal.synopsys.com/browse/P80001562-170623 | Async |  |

**Table** **2****‑4 Pin List for** **dwc\_lpddr5xphy\_lstx\_zcal**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **dwc\_lpddr5xphy\_lstx\_zcal** | | | | | | |
| **Pin name** | **I/O** | **Width** | **Power Domain** | **Description** | **Receiving Clock** | **Changes** |
| IDDQ\_mode | Input | 1 | VDD | when “1”, enable IDDQ test | Async |  |
| scan\_mode | Input | 1 | VDD | refer to Error: Reference source not found | Async |  |
| VDD | Input | 1 | VDD | Core supply voltage | N/A |  |
| VDDQ | Input | 1 | VDDQ | I/O supply voltage | N/A |  |
| VSS | Input | 1 | VSS | Ground | N/A |  |
| VIO\_PwrOk | Input | 1 | ~~VDDQ~~  VDDQ\_VDD2H | PwrOkVDD in VDDQ\_VDD2H domain, refer to Error: Reference source not found | Async |  |
| LsPwrOkVDD | Output | 1 | VDD | Schmitt trigger output (with positive polarity) for ‘VIO\_PwrOk’ input signal for TX BE  LsPwrOkVDD to the 1 ZCALIO instances | Async |  |
| ResetAsync | Input | 1 | VDD | Asynchronous reset for cal code flops – When asserted, passes CSR Default value 9’b110000000 to csrlstxcalcodelpppu\*<\*>/csrlstxcalcodepd\*<\*> | Async |  |
| csrTxCalCodePU | Input | 9 | VDD | calibration code for PU | Async |  |
| csrTxCalCodePD | Input | 9 | VDD | calibration code for PD | Async |  |
| csrLsTxCalCodeLPP8 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 8 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP7 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 7 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP6 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 6 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP5 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 5 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP4 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 4 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP3 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 3 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodeLPP0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD8 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 8 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD7 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 7 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD6 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 6 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD5 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 5 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD4 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 4 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD3 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 3 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 ZCAL instances | Async |  |
| csrLsTxCalCodePD0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 ZCAL instances | Async |  |
| csrTxSlewPU | Input | 4 | VDD | Slew rate code for PU | Async |  |
| csrTxSlewPD | Input | 4 | VDD | Slew rate code for PD | Async |  |
| csrLsTxSlewLPPU2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 ZCAL instances | Async |  |
| csrLsTxSlewLPPU1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 ZCAL instances | Async |  |
| csrLsTxSlewLPPU0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 ZCAL instances | Async |  |
| csrLsTxSlewPD3 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 3 to the 2 ZCAL instances | Async |  |
| csrLsTxSlewPD2 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 2 to the 2 ZCAL instances | Async |  |
| csrLsTxSlewPD1 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 1 to the 2 ZCAL instances | Async |  |
| csrLsTxSlewPD0 | Output | 2 | VDD | refer to Error: Reference source not found  Bit 0 to the 2 ZCAL instances | Async |  |
| Dficlk | Input | 1 | VDD | Half rate clock to retime calibration code | Sync |  |
| CalUpdate | Input | 1 | VDD | Gate Dficlk in mission mode | Async |  |
| scan\_shift\_cg | Input | 1 | VDD | Gate Dficlk in scan mode | Async |  |
| scan\_shift | Input | 1 | VDD | Select scan\_in in flops | Async |  |
| scan\_si | Input | 1 | VDD | Scan input | Sync |  |
| scan\_so | Output | 1 | VDD | Scan output | Sync |  |
| csrReserved | Input | 4 | VDD | Reserved in ZCALIO | Async |  |
| csrLsReserved | Output | 4 | VDD | Buffered csrReserved<3:0> | Async |  |
| csrReservedP | Input | 4 | VDD | ReservedP in ZCALIO | Async |  |
| csrLsReservedP | Output | 4 | VDD | Buffered csrReservedP<3:0> | Async |  |
| LsScan\_mode | Output | 1 | VDD | buffered scan\_mode | Async |  |
| ZCalAnaClk | Input | 1 | VDD | ZCALIO control | Sync |  |
| ZCalAnaEn | Input | 1 | VDD | ZCALIO control | Async |  |
| ZCalCompEn | Input | 1 | VDD | ZCALIO control | Async |  |
| ZCalCompVOHDAC | Input | 7 | VDD | ZCALIO control | Async |  |
| ZCalDACRangeSel | Input | 1 | VDD | ZCALIO control | Async |  |
| ZCalPDEn | Input | 1 | VDD | ZCALIO control | Async |  |
| ZCalPUEn | Input | 1 | VDD | ZCALIO control | Async |  |
| csrZCalCompGainCurrAdj | Input | 8 | VDD | ZCALIO control | Async |  |
| csrZCalCompVrefDAC | Input | 7 | VDD | ZCALIO control | Async |  |
| csrZCalAttDisable | Input | 1 | VDD | ZCALIO control | Async |  |
| LsZCalAnaClk | Output | 1 | VDD | Buffered ZCalAnaClk | Sync |  |
| LsZCalAnaEn | Output | 1 | VDD | Buffered ZCalAnaEn | Async |  |
| LsZCalCompEn | Output | 1 | VDD | Buffered ZCalCompEn | Async |  |
| LsZCalCompVOHDAC | Output | 7 | VDD | Buffered ZCalCompVOHDAC<6:0> | Async |  |
| LsZCalDACRangeSel | Output | 1 | VDD | Buffered ZCalDACRangeSel | Async |  |
| LsZCalPDEn | Output | 1 | VDD | Buffered ZCalPDEn | Async |  |
| LsZCalPUEn | Output | 1 | VDD | Buffered ZCalPUEn | Async |  |
| csrLsZCalCompGainCurrAdj | Output | 8 | VDD | Buffered csrZCalCompGainCurrAdj<7:0> | Async |  |
| csrLsZCalCompVrefDAC | Output | 7 | VDD | Buffered csrZCalCompVrefDAC<6:0> | Async |  |
| csrLsZCalAttDisable | Output | 1 | VDD | Buffered csrZCalAttDisable | Async |  |
| VIO\_AnalogTestBusIn | Input | 1 | VDDQ | Pass through | Async |  |
| VIO\_AnalogTestBusOut | Output | 1 | VDDQ | Pass through | Async |  |
| LsIDDQ\_mode | Output | 1 | VDD | Buffered IDDQ\_mode | Async |  |
| LsResetAsync | Output | 1 | VDD | Buffered ResetAsync | Async |  |
| BurnIn | Input | 1 | VDD | Unused pin with dummy inverter. Single Pin to enter & exit BurnIn. Functionality will be added in future. https://jira.internal.synopsys.com/browse/P80001562-170623 | Async |  |

Table 2‑5 Pin List for dwc\_lpddr5xphy\_lstx\_csx2

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| dwc\_lpddr5xphy\_lstx\_csx2\_ew | | | | | | |
| **Pin name** | **I/O** | **Width** | **Power Domain** | **Description** | **Receiving Clock** | **Changes** |
| IDDQ\_mode | Input | 1 | VDD | when “1”, enable IDDQ test | Async | Unused |
| scan\_mode | Input | 1 | VDD | Enables scan\_mode | Async | Unused |
| BurnIn | Input | 1 | VDD | Unused pin with dummy inverter. Single Pin to enter & exit BurnIn. Functionality will be added in future. https://jira.internal.synopsys.com/browse/P80001562-170623 |  |  |
| VDD | Input | 1 | VDD | Core supply voltage | N/A |  |
| VDD2H | Input | 1 | VDD2H | I/O supply voltage | N/A |  |
| VSS | Input | 1 | VSS | Ground | N/A |  |
| VIO\_PwrOk | Input | 1 | VDD2H | PwrOkVDD in VDDQ\_VDD2H domain | Async |  |
| VIO\_PwrOkTxBE | Output | 2 | VDD2H | Buffered VIO\_PWrOk signal | Async |  |
| csrReserved | Input | 4 | VDD | Reserved | Async | Unused |
| csrReservedP | Input | 4 | VDD | ReservedP | Async | Unused |

## CSR default

//depot/products/lpddr5x\_ddr5\_phy/lp5x/common/csr\_defaults/LP5X\_PHY\_Circuit\_OnReset\_PHYNIT\_Values.xlsx

CSR Defaults for LSTX\_ACX2/DX4/DX5/ZCAL are asserted with Resetasync, as opposed to Calupdate, which was done previously. JIRA: <https://jira.internal.synopsys.com/browse/P80001562-126172>

csrLsTxCalCodeLPPU/PD – 9’b110000000 / d384 for Resetasync assertion.

# Electrical Specification

|  |  |  |  |
| --- | --- | --- | --- |
|  | ~~D5~~ | LP5 | Note |
| max rise/fall time (ps) | ~~200~~ |  | 10%~90% |

**Table 3-1 Electrical Specification**

# Simulation Plan

## Power

### tb\_lstx\_acx2/dx4/dx5/zcal\_power\_post.bbSim

* lstx power in mission mode

### tb\_lstx\_acx2/dx4/dx5/zcal\_power\_s3\_post.bbSim

* lstx power in s3 mode

### tb\_lstx\_acx2/dx4/dx5/zcal\_power\_s3reversepost.bbSim

* lstx power in reverse s3 mode

### tb\_lstx\_power\_sequence\_post.bbSim

* power sequence

## Function

### tb\_lstx\_acx2/dx4/dx5/zcal\_post.bbSim

* edge rate

## Parasitic

### lstx\_acx2/dx4/dx5/zcal\_vddq\_rc\_post.bbSim

* RC on VDDQ

## EMIR

### lstx\_acx2/dx4/dx5/zcal\_emir.bbSim

* EMIR with SHE

## Sub-block

### schmitt\_tran\_post.bbSim

* Schmitt trigger function

### schmitt\_tran\_mc\_post.bbSim

* MC of Schmitt trigger