**LPDDR5X PHY RxAcVref Specification**

Cell Name: dwc\_lpddr5xphy\_rxacvref\_ew

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# Revision History

|  |  |  |
| --- | --- | --- |
| **Date** | **Owner** | **Description** |
| 12/02/2020 | dartur | Copied from DDR54 Vrefglobal specification. |
| 12/23/2020 | dartur | Updated information about black boxed sub cell. |
| 2/09/2021 | dartur | Updated truth table. |
| 3/01/2021 | dartur | Added assertion table. |
| 4/13/2021 | dartur | Added CSR Defaults table. |
| 7/27/2021 | anilsa | Branched from Combo-phy |
| 10/13/2021 | anilsa | Renamed the supply pin from VDDQ\_VDD2H to VDD2H |
| 10/18/2021 | anilsa | Added the scan\_mode functionality |
| 10/26/2021 | anilsa | Added new pin - BurnIn |
| 12/21/2021 | Bapna | Added scan\_mode/iddq\_mode details |
| 01/06/2022 | anilsa | Remove un-used pin - csrPhyModeSel |
| 07/07/2022 | mithunn | Added DVFS vref settings |

# Functional Outline

## Overview

This macro provides a global Vref voltage to all AC and CS byte slices. The Vref voltage is ultimately used as the low/high threshold for the RXAC and RXCS receivers.

## Architecture

The following block diagram shows the architecture of dwc\_lpddr5xphy\_rxacvref\_ew macro. Only vref\_r2r\_dac\_res sub cell needs to be black boxed during equivalency check.

Diagram, schematic

Description automatically generated

Figure 1 : dwc\_lpddr5xphy\_rxacvref block diagram

* **Rxac\_vref\_ctrl** - block consists of digital logic elements.
* **LS –**low to high levelshifter is used for shifting VDD domain to VDD2H.
* **INV -** Additional inverter was used here as LS is an inverted output
* **R2R DAC** - 9bit r2r dac was used with the LSB connected to tie low.

## Logical functionality

Table 1. RxAcVref truth table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **VIO\_PwrOk** | **scan\_mode** | **IDDQ\_mode** | **RxAcVrefDacEn** | **VIO\_RxAcVref** |
| 0 | - | - | - | 0 |
| 1 | 0 | 0 | 1 | VDD2H \* csrRxAcVrefDac [7:0] / 256 |
| 1 | 1 | - | - | 0 |
| 1 | - | 1 | - | 0 |
| 1 | - | - | 0 | 0 |

The RxAcVref DAC supports LPDDR5X, LPDDR4X and LPDDR5X Unterminated mode. The output voltage VIO\_RxAcVref supports full range from VDD2H to VSS. Nominally the output voltage follows:

VIO\_RxAcVref (V) = VDD2H (V) \* csrRxAcVrefDac [7:0] / 256 (1)

The output voltage is connected to a thin gate device in rxac\_ew and rxcs\_ew. Due to overvoltage protection reason, csrRxAcVrefDac[7:0] needs to be limited in rxcs block.

The below table shows the logic behavior of the RxAcVref DAC generator arranged by precedence.

Table 2. Truth table

|  |  |
| --- | --- |
| Condition | Function |
| VIO\_PwrOk=0 | Output are tied to VSS. Minimum current consumed. |
| PwrDown=1 | Output are tied to VSS. Minimum current consumed. |
| All other cases | Mission mode; the ladder is connected between VDD2H and VSS, and the outputs are outputting the voltage associated to the input codes. |

## Illegal conditions

* NONE

## Pin List

Table 3. Pin list

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **PIN NAME** | **DIRECTION** | **SIGNAL WIDTH** | **INTERFACE** | **PURPOSE** | **IS CSR** | **Related Power** | **MODE** | | **DESCRIPTION** |
| **LP5** | **DDR5** |
| VDD2H | Input | 1 | POWER | DRAM\_POWER | N | VDD2H |  |  | VDD2H Power |
| VDD | Input | 1 | POWER | CORE\_POWER | N | VDD |  |  | Core Power |
| VSS | Input | 1 | GROUND | GROUND | N | VSS |  |  | Ground |
| VIO\_PwrOk | Input | 1 | CMOSX2 | logic | N | VDD2H |  | \* | Power On Indicator Signal |
| csrRxAcVrefDac | Input | 8 | DI | logic | Y | VDD |  | \* | RxAcVref DAC code signals |
| scan\_mode | Input | 1 | DI | logic | N | VDD |  | \* | scan\_mode enable |
| IDDQ\_mode | Input | 1 | DI | logic | N | VDD | \* | \* | IDDQ Test Mode Select |
| RxAcVrefDacEn | Input | 1 | DI | logic | N | VDD |  | \* | When asserted VREFAC value is applied to the AC/CS bypass receiver |
| BurnIn | Input | 1 | DI | logic | N | VDD |  |  | *Not Used.* |
| VIO\_RxAcVref | Output | 1 |  | Analog | N | VDD2H |  | \* | Reference Voltage for AC and CS slice bypass mode receivers |

## LEF geometry

* + - 16.353um X 38.219um, (x,y size) with TSMC5

# Electrical parameter

## Operating Condition

Table 4. Operating conditions

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Unit** | **Min** | **Typ** | **Max** | **Notes** |
| Supply Voltage (LP4X) | VDD2H | V | 0.99 | 1.1 | 1.21 | 1 |
| Supply Voltage (LP5X) | VDD2H | V | 0.945 | 1.05 | 1.155 | 1 |
| Supply Voltage | VDD | V | VDD-10% | VDD | VDD+10% | 1 |

Table Notes:

* 1. All voltages are referenced to VSS.

## DC Specification

The accuracy and resolution specifications come from platform margining requirements. Accuracy should be much less than this in order to allow fine resolution comparisons for different phy configurations and settings. Accuracy of +/- 0.05% of VDD2H would be ideal, but +/- 0.5% of VDD2H should provide reasonable resolution for platform debug and qualification.

Table 5. DC spec

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **VIO\_RxAcVref** | **LP4X** | | **LP5** | |
| **MIN** | **MAX** | **MIN** | **MAX** |
| Code | 0 | 203 | 0 | 203 |
| Settling time (us) | - | 1.5 | - | 1.5 |
| Range (%) | 0 | 79 | 0 | 79 |
| Step size (mv) | 3.9 | 4.75 | 3.7 | 4.52 |
| INL (%) | - | 0.04 | - | 0.04 |
| DNL (%) | - | 0.5 | - | 0.5 |

Notes:

* + - * 1. Setpoint accuracy is defined as [VIO\_RxAcVref(actual) – VIO\_RxAcVref (expected)] / VDD2H.
        2. Resolution is defined from the actual measured or simulated VIO\_RxAcVref values from two adjacent steps s and s+1 as [VIO\_RxAcVref (s+1) – VIO\_RxAcVref (s)] / VDD2H

## AC Specification

* + - Not applicable

## DECAP

* None

## Jitter

* + - Not applicable

## Writability

* + - Not applicable

## RTL Assertions and Constraint

//depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_CKT\_Macro\_Assertions.xlsx

## Scan/IDDQ mode Gating

Refer: //depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_PHY\_CKT\_Input\_Pin\_Specs.xlsx

## CSR Defaults - dwc\_lpddr5xphy\_rxacvref\_ew

Refer: //depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_PHY\_CKT\_Input\_Pin\_Specs.xlsx

# Characterization method

* All DC parameters should be characterized with DC simulations. To incorporate leakage, the simulation should include the full circuit. Measurements should always be made on the VIO\_RxAcVref pin.
* Characterization of the accuracy and resolution parameters should be done in several ways.

Raw DC simulations, which will pick up mismatch in the resistor ladder and leakage effects. Extracted simulations should be done including resistor parasitic in order to check for weak wiring.

* Test all functional modes and make sure they operate as described.
  + 1. linearity simulation to measure the Vref stepsize, setpoint accuracy and DNL
    2. output resistance simulations
    3. simulations to confirm functionality according to truth table.
    4. Simulation to measure active, S3 and power down currents.

# Vref Range for RXAC and RXCS

* **For RXAC macro(No-DVFS mode)**, Vref is trained to values using following equation for LP5 and LP4X modes –
  + Rterm = 50 Ohm; Ron = 40Ohm
  + Voh = (vddqval\*(Rterm/(Ron+Rterm))
  + Vref = Voh/2 \* (1 + Voff/100)
  + Voff = -5 , 0 , 5
  + Voff is the Vref noise (+/-5 % of nominal Vref)
  + **For LP5 unterminated mode** –
  + Vref = vddq/2 \* (1 + Voff/100)
  + Voff = -5 , 0 , 5
  + Voff is the Vref noise (+/-5 % of nominal Vref)
* **For RXAC macro (DVFS mode)**:
  + Vref is set to VDD2H/8 (code 64 : 8b’00100000)
* **For RXCS (Chip select) macro:**
  + Vref is set to VDD2H/8 (code 64 : 8b’00100000) for all modes.

# Simulation plan and results

## Testbenches names

Table 6. TB List

|  |  |
| --- | --- |
| TB List | Description |
| tb\_rxacvref\_emba.bbSim | For estimate in advance of current passing through the wires |
| tb\_rxacvref\_step\_lp5.bbSim | Measure DAC linearity (LP5) |
| tb\_rxacvref\_step\_lp4x.bbSim | Measure DAC linearity (LP4X) |
| tb\_rxacvref\_temp\_sensitivity\_lp5.bbSim | Measure DAC temperature sensitivity (LP5) |
| tb\_rxacvref\_temp\_sensitivity\_lp4x.bbSim | Measure DAC temperature sensitivity (LP4X) |
| tb\_rxacvref\_settle\_lp5.bbSim | Measure settling time (LP5) |
| tb\_rxacvref\_settle\_lp4x.bbSim | Measure settling time (LP4X) |
| tb\_rxacvref\_power\_tran\_s3\_lp5.bbSim | Measure power of sleep mode (LP5) |
| tb\_rxacvref\_power\_tran\_s3\_lp4x.bbSim | Measure power of sleep mode (LP4X) |
| tb\_rxacvref\_power\_tran\_pd\_lp5.bbSim | Measure power of power down mode (LP5) |
| tb\_rxacvref\_power\_tran\_pd\_lp4x.bbSim | Measure power of power down mode (LP4X) |
| tb\_rxacvref\_power\_tran\_normal\_lp5.bbSim | Measure power of normal mode (LP5) |
| tb\_rxacvref\_power\_tran\_normal\_lp4x.bbSim | Measure power of normal mode (LP4X) |
| tb\_rxacvref\_power\_dc\_lp5.bbSim | Measure power (LP5) |
| tb\_rxacvref\_power\_dc\_lp4x.bbSim | Measure power (LP4X) |
| tb\_rxacvref\_outputimp\_tran\_lp5.bbSim | Measure output impedance (LP5) |
| tb\_rxacvref\_outputimp\_tran\_lp4x.bbSim | Measure output impedance (LP4X) |
| tb\_ rxacvref\_em\_she\_0\_to\_255.bbSim | For estimate EM, when DAC code changed 0 to 255 |
| tb\_ rxacvref\_em\_she\_127\_to\_128.bbSim | For estimate EM, when DAC code changed 127 to 128 |
| tb\_ rxacvref\_em\_she\_84\_to\_171.bbSim | For estimate EM, when DAC code changed 84 to 171 |
| tb\_ rxacvref\_ir\_she\_0\_to\_255.bbSim | For estimate IR, when DAC code changed 0 to 255 |
| tb\_ rxacvref\_ir\_she\_127\_to\_128.bbSim | For estimate IR, when DAC code changed 127 to 128 |
| tb\_ rxacvref\_ir\_she\_84\_to\_171.bbSim | For estimate IR, when DAC code changed 84 to 171 |
| tb\_rxacvref\_scanmode.bbSim | Monitor Vref during scan\_mode |
| tb\_ rxacvref\_vdd2h\_rc\_post.bbSim | Measure Rdie/Cdie |
| tb\_ rxacvref\_vdd\_rc\_post.bbSim | Measure Rdie/Cdie |