## 

# Pin List

Table 1. dwc\_lpddr5xphy\_ato pins

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **PIN NAME** | **DIRECTION** | **SIGNAL WIDTH** | **INTERFACE** | **PURPOSE** | **IS CSR** | **Related Power** | **DESCRIPTION** | |  |
| **LP5** |  | |
| scan\_mode | input | 1 | DI | logic | N | VDD |  | Test Mode Select | |
| IDDQ\_mode | input | 1 | DI | logic | N | VDD |  | IDDQ Test Mode Select | |
| VIO\_PAD | inout | 1 | IPSOC | Analog | N | VDD | \* | Signal I/O Pad | |
| VDD | input | 1 | POWER | CORE\_POWER | N | VDD | \* | VDD (Core Power Supply) | |
| VDDQ | input | 1 | POWER | DRAM\_POWER | N | VDDQ | \* | VDDQ Power Supply | |
| VSS | input | 1 | GROUND | GROUND | N |  | \* | Ground | |
| csrReserved | input | 4 | DI | logic | Y | VDD | \* | Reserved CSR signals for [3:1]  ~~[1] = VIO\_PwrOkATO control~~( Pin and functionality removed)  [0] = csrPhyModeSelATO control | |
| VIO\_PwrOk | input | 1 | POR | logic | N | VDDQ\_VDD2H |  | VDDQ domain Power OK signal. Indicates VDD power is up | |
| TIEHI | output | 1 | DI | logic | N | VDD | \* | VDD domain connection to VDD for static HI tie offs | |
| TIELO | output | 1 | DI | logic | N | VDD | \* | VDD domain connection to VSS for static LO tie offs | |
| VIO\_TIEHI | output | 1 | DI | logic | N | VDDQ |  | VDDQ domain connection to VDDQ for static HI tie offs | |
| VIO\_TIELO | output | 1 | DI | logic | N | VDDQ |  | VDDQ domain connection to VSS for static LO tie offs | |
| RxPowerDown | input | 1 | DI | logic | N | VDD |  | Receiver Power down Controls (Bias Shutdown) | |
| RxStandBy | input | 1 | DI | logic | N | VDD |  | Receiver Partial Bias Shutdown in StandBy Mode | |
| csrAnalogOutCtrl | input | 8 | DI | logic | Y | VDD |  | Selection control signals for the analog test mux | |
| csrRxDFECtrl | input | 3 | DI | logic | Y | VDD | \* | DFE Mode Control | |
| csrRxCurrAdj | input | 8 | DI | logic | Y | VDD | \* | Receiver Analog Bias Controls. Adjusts Currents depending on Power State, PHY type and speed | |
| csrRxVrefDac | input | 9 | DI | logic | Y | VDD | \* | Reference Voltage DAC Controls. | |
| csrRxModeCtl | input | 4 | DI | logic | Y | VDD | \* | Rx mode control in LP5X | |
| csrRxDFETap1Sel | input | 5 | DI | logic | Y | VDD | \* | DFE Tap 1 Programming Bits | |
| csrRxDFETap2Sel | input | 5 | DI | logic | Y | VDD | \* | DFE Tap 2 Programming Bits | |
| csrRxDFEBiasSel | input | 2 | DI | logic | Y | VDD | \* | DFE Bias Current Control | |
| csrRxOffsetSelEven | input | 5 | DI | logic | Y | VDD | \* | Select Even Bit output Offset calibration | |
| csrRxOffsetSelOdd | input | 5 | DI | logic | Y | VDD | \* | Select Odd Bit output Offset Calibration | |
| csrRxOffsetEn | input | 1 | DI | logic | Y | VDD | \* | Enable offset calibration | |
| csrRxGainCtrl | input | 3 | DI | logic | Y | VDD | \* | RX Front End amplifier Gain Control Bits | |
| PwrOkVDD | input | 1 | por | Logic | N | VDD | \* | 1) VDD PowerOK indicating core VDD power is at sane level 2) Inverse of PwrOkVDD used for gating RxPowerDown signal in ctrl logic 3) One of the control bits to generate output. Refer to ATO functionality table 1.3 | |

# Detailed Functionality

## gm\_bias\_lp5

Refer to rx spec section 4.1.4.

## DFE\_bias

Refer to rx spec section 4.1.5.

## rxdq\_offgen

Refer to rx spec section 4.1.5.  
**Note:** Only single instance of rxdq\_offgen(odd) is needed because we are merely monitoring the signal at VIO\_PAD. Using both even and odd instance is redundant.

## rx\_vrefdac

The receiver contains a R2R internal VREF generator used to provide voltage references. The VREF block receives a 9-bit digital binary-encoded input from the core logic which is converted into an analog signal that is sent to the input receivers. This block is black-boxed for equivalence check.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin Names** | **Type** | **Power Domain** | **Clock Domain** | **Description** |
| VDD | PWR | VDD | N/A | PHY core power |
| VDDQ | PWR | VDDQ | N/A | IO power, needed for the CDM cell. |
| VSS | PWR | N/A | N/A | Shared ground |
| VIO\_PwrOk | Input | VDDQ\_VDD2H | Async | Power Ok signal, connected from top level |
| PwrDown | Input | VDD | Async | Power down signal.  = IDDQ\_mode || scan\_mode || RxPowerDown |
| vref\_code[8:0] | Input | VDD | Async | VREF DAC code, connected from top level csrLsRxVrefDac[8:0] |
| vdac | Output | VDDQ | Async | Output voltage, connected to VREF in rxdq\_afe |

The VREF DAC supports LPDDR5 and DDR5. The output voltage vdac supports full range from VDDQ to VSS. Nominally the output voltage follows:

vdac (V) = VDDQ (V) \* csrLsRxVrefDac[8:0] / 512

Table below shows the logic behavior of the VREF generator arranged by precedence.

|  |  |
| --- | --- |
| Condition | Function |
| VIO\_PwrOk=0 | Output are tied to VSS. Minimum current consumed. |
| PwrDown=1 | Output are tied to VSS. Minimum current consumed. |
| all other cases | mission mode; the ladder is connected between VDDQ and VSS, and the outputs are outputting the voltage associated to the input codes. |

## dfe\_summer

Refer to rx spec section 4.1.2.2.  
One side testing is being done for equivalence checks.  
Connections:  
 1) tap1\_p - TIEHI  
 2) tap1\_n - TIELO  
 3) tap2\_p - TIEHI  
 4) tap2\_n - TIELO

# CONTROL SIGNAL REGISTER DEFAULTS

//depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_PHY\_CKT\_Input\_Pin\_Specs.xlsx

## 5. ASSERTIONS

//depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_CKT\_Macro\_Assertions.xlsx

## 6. SCAN/IDDQ Mode Gating

//depot/products/lpddr5x\_ddr5\_phy/lp5x/common/ckt\_specs/LP5X\_PHY\_CKT\_Input\_Pin\_Specs.xlsx