FUNDAMENTOS Y ESTRUCTURA DE COMPUTADORES
1º Grado en Ingeniería Informática

PRÁCTICA L7: Laboratorio

Circuitos Secuenciales: Contadores

1. Objetivos

- ✓ Estudiar el comportamiento y asimilar el funcionamiento del circuito integrado 74LS163 (contador de 4 bits).
- ✓ Comprender la utilidad y el empleo de la serie de este contador para realizar contadores de módulo arbitrario.

2. Materiales

- ✓ Osciloscopio Textronik 2205 20 MHz.
- ✓ Fuente de alimentación Promax FR–712B.
- ✓ Generador de funciones Promax GF-1000.
- ✓ Placa de laboratorio.
- ✓ Circuitos integrado 4LS163, y puertas NAND 74LS00.
- ✓ Diodos led, resistencias de 1 kΩ y cables de conexiones.

3. Desarrollo de la práctica

En esta práctica se deberá realizar un contador utilizando los circuitos integrados 74LS163 y 74LS00. La cuenta será desde 3 hasta 12, es decir un contador BCD exceso a 3. Se visualizará la cuenta utilizando diodos leds polarizados adecuadamente. El funcionamiento del contador 74LS163 se debe deducir de las hojas características que se adjuntan. La información técnica completa está disponible en el enlace (visitado por última vez el 1-5-2015): http://www.ti.com/lit/ds/symlink/sn54163.pdf

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

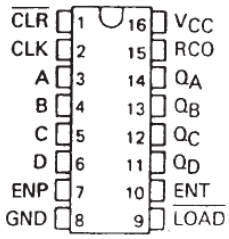
SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

'160,'161,'LS160A,'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162,'163,'LS162A,'LS163A,'S162,'S163 . . . FULLY SYNCHRONOUS COUNTERS

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Load Control Line**
- **Diode-Clamped Inputs**

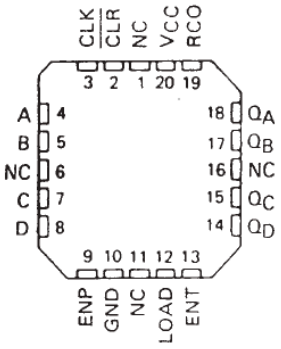
TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

SERIES 54', 54LS' 54S' . . . J OR W PACKAGE
SERIES 74' . . . N PACKAGE
SERIES 74LS', 74S' . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160,'162,'LS160A,'LS162A, and 'S162 are decade counters and the '161,'163,'LS161A,'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161,'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162,'163,'LS162A,'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

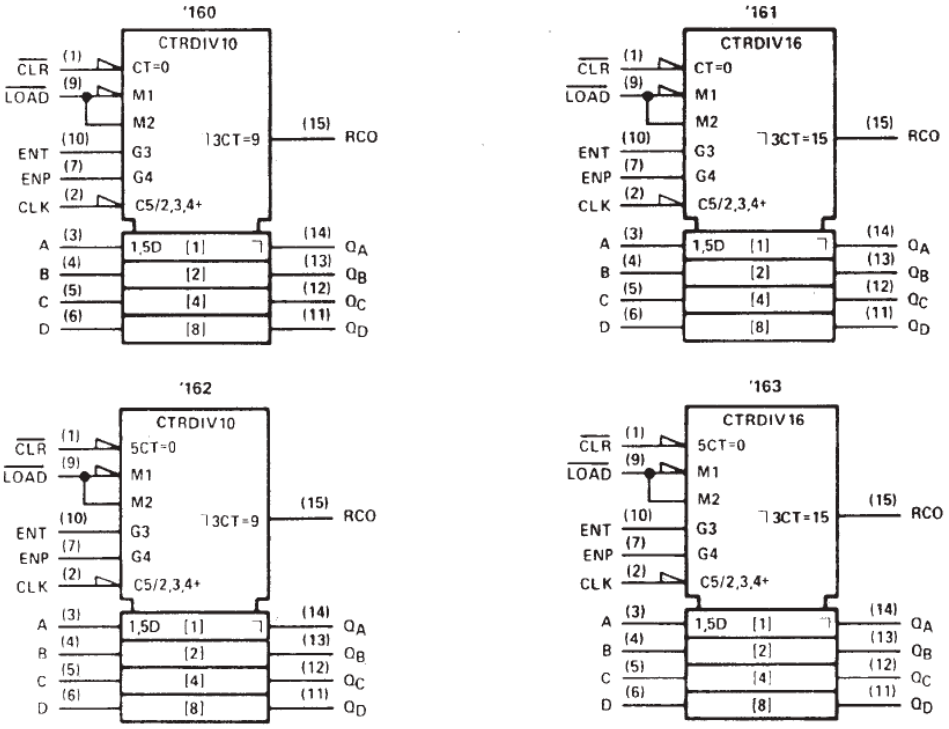
SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols†

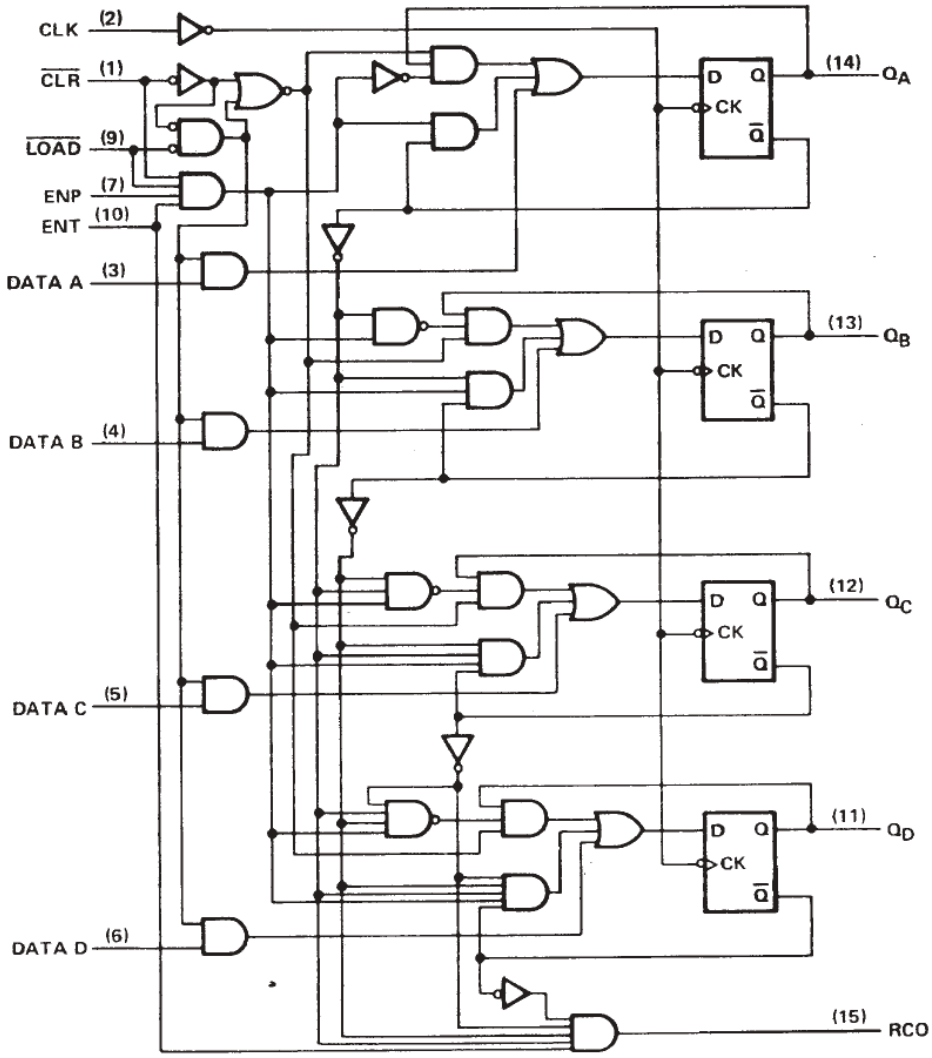


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



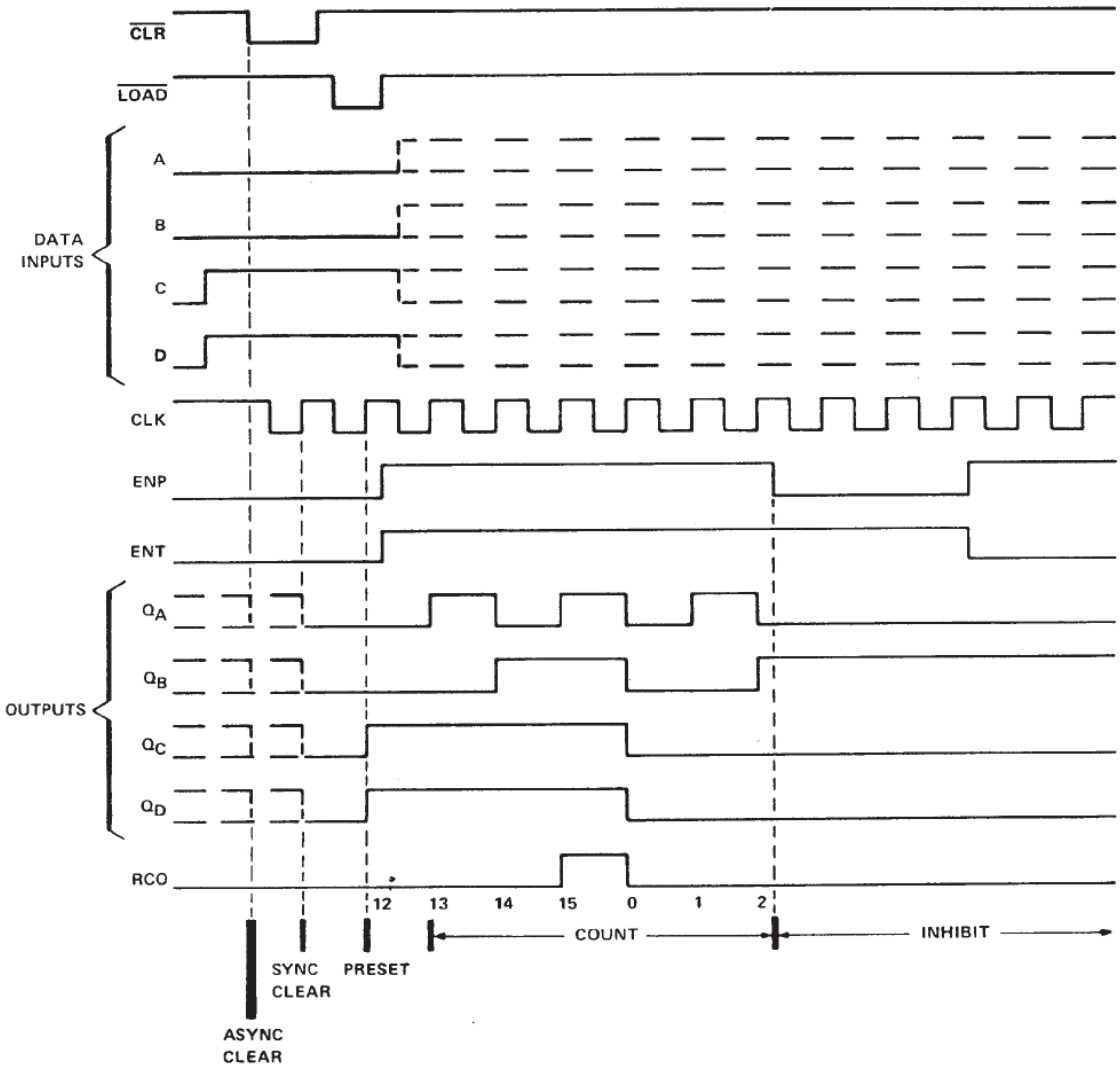
Pin numbers shown are for D, J, N, and W packages.

'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

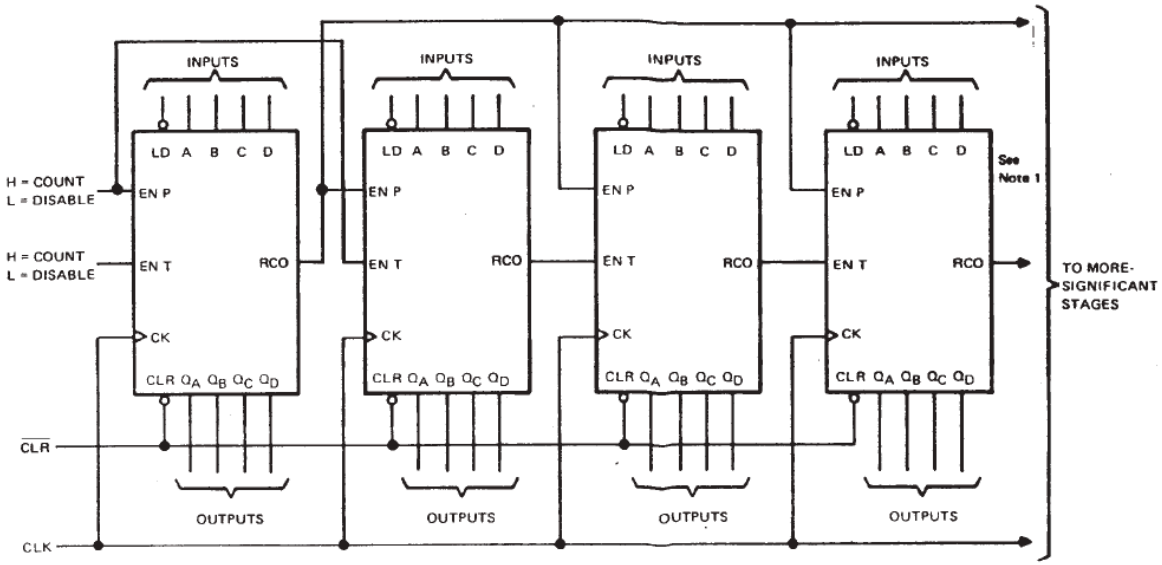
typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



TYPICAL APPLICATION DATA



$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH} + \text{ENP } t_{su})$

FIGURE 2