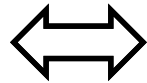


CPU



```
graph LR; CPU[CPU] <--> L1[L1]; L1 <--> L2[L2]; L2 <--> L3[L3]; L3 <--> MEMORY[MEMORY];
```

The diagram illustrates a memory hierarchy. It consists of five rectangular boxes arranged horizontally. From left to right, they are labeled CPU, L1, L2, L3, and MEMORY. Each box is connected to the next one by a bidirectional arrow, indicating data flow in both directions. The CPU box is the tallest, followed by L1, L2, and L3, which are of decreasing height. The MEMORY box is the tallest again, matching the height of the CPU box.



L1



L2



L3



MEMORY