**Assignment 4: edge detect**

**Simulation results:**

Clock cycles: 388800 +

Errors present, might be something to do with making new rows

**Synthesis results:**

Req frequency: 87.7MHz

Total combinational functions 190 of 114480 ( 0%)

Logic element usage by number of inputs

4 input functions 53

3 input functions 9

[=2 input functions 128

Logic elements by mode

normal mode 77

arithmetic mode 113

Total registers 66 of 114480 ( 0%)

I/O pins 38 of 529 ( 7%), total I/O based on largest package of this part.

Number of I/O registers

Input DDRs :0

Output DDRs :0

DSP Blocks: 0 (0 nine-bit DSP elements).

DSP Utilization: 0.00% of available 266 blocks (532 nine-bit).

ShiftTap: 0 (0 registers)

Ena: 7

Sload: 0

Sclr: 0

Total ESB: 10240 bits

Black-boxes: 1

sobel\_720s\_540s : 1

**Timing analysis**

**A close-up of a receipt

AI-generated content may be incorrect.**

**RTL schematic:**

**A diagram of a computer

AI-generated content may be incorrect.**