Quantum supremacy using a programmable superconducting processor

Paper Link Quantum club slides

Abstract

They created *Sycamore*: A programmable superconducting processor to achieve quantum supremacy. They prove it using random circuits and benchmark the fidelity comparing the results from the quantum processor with classical simulations.

They claim to answer two questions:

- Can a quantum system be engineered to perform a computation in a large enough computational (Hilbert) space and with a low enough error rate to provide a quantum speedup?
- Can we formulate a problem that is hard for a classical computer but easy for a quantum computer?

Cross-entropy benchmarking

They design circuits to entangle qubits with single and two-qubit gates. Then they measure the output of the circuit and represent it with a bitstring {0000101, 1011100, …}.

They run the same circuit lots of time to get statistical probability of each bitstring. Then they compare the fidelity of the results with a classical simulation of the same circuit.

They use this formula:

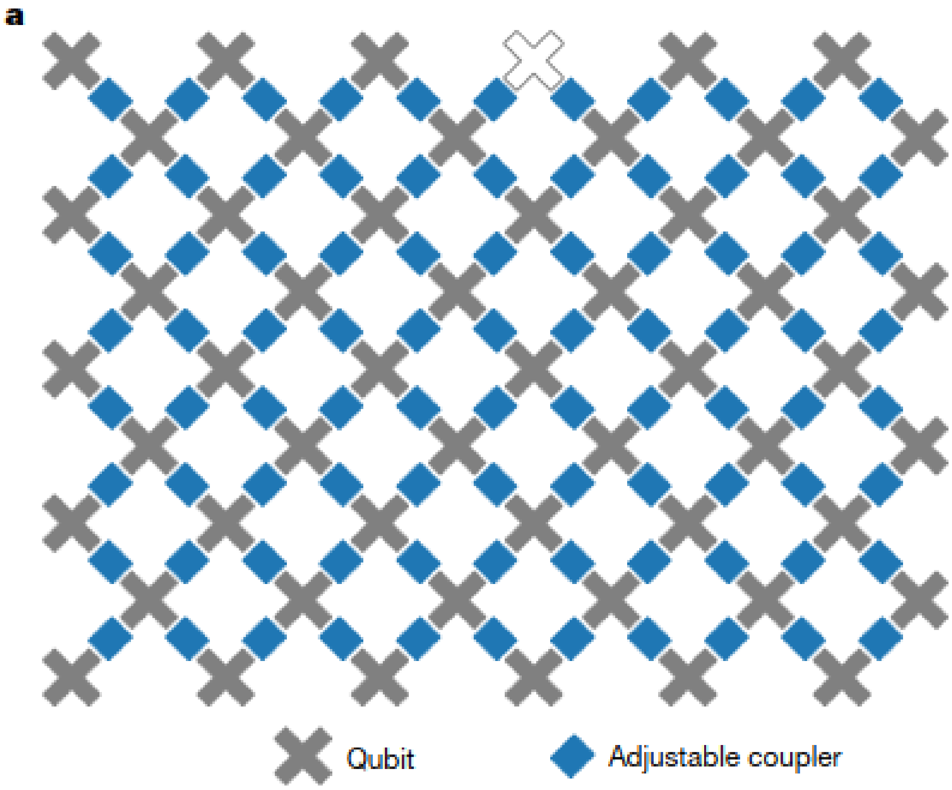
$$F_{xeb} = 2^n \langle P(x)_i \rangle_i - 1$$

Where:

$n = number\ of\ qubits$ | $P(x)_i = Probability\ of\ bitstring\ i$

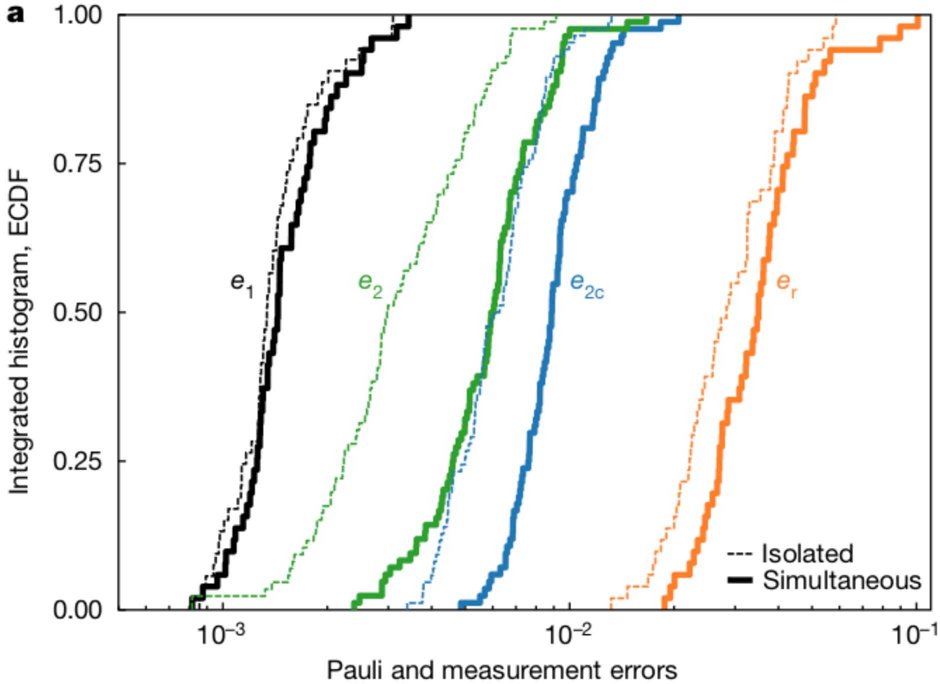
They get the average for all bitstrings. Intuitively, $F_{xeb} = 1$ for an exponential distribution and 0 for a uniform distribution.

Anatomy of a high fidelity processor



Sycamore consists of a two-dimensional array of 54 [transmon] qubits, where each qubit is tunably coupled to four nearest neighbours in a rectangular lattice. The connectivity is forward-compatible with error correction using the [surface code].

Each transmon has two controls: a microwave drive to excite the qubit, and a magnetic flux control to tune the frequency. Each qubit is connected to a linear resonator used to read out the qubit state. The state of all qubits can be read simultaneously by using a frequency-multiplexing technique. In total, they orchestrate 277 digital-to-analog converters (14 bits at 1 GHz) for complete control of the quantum processor.



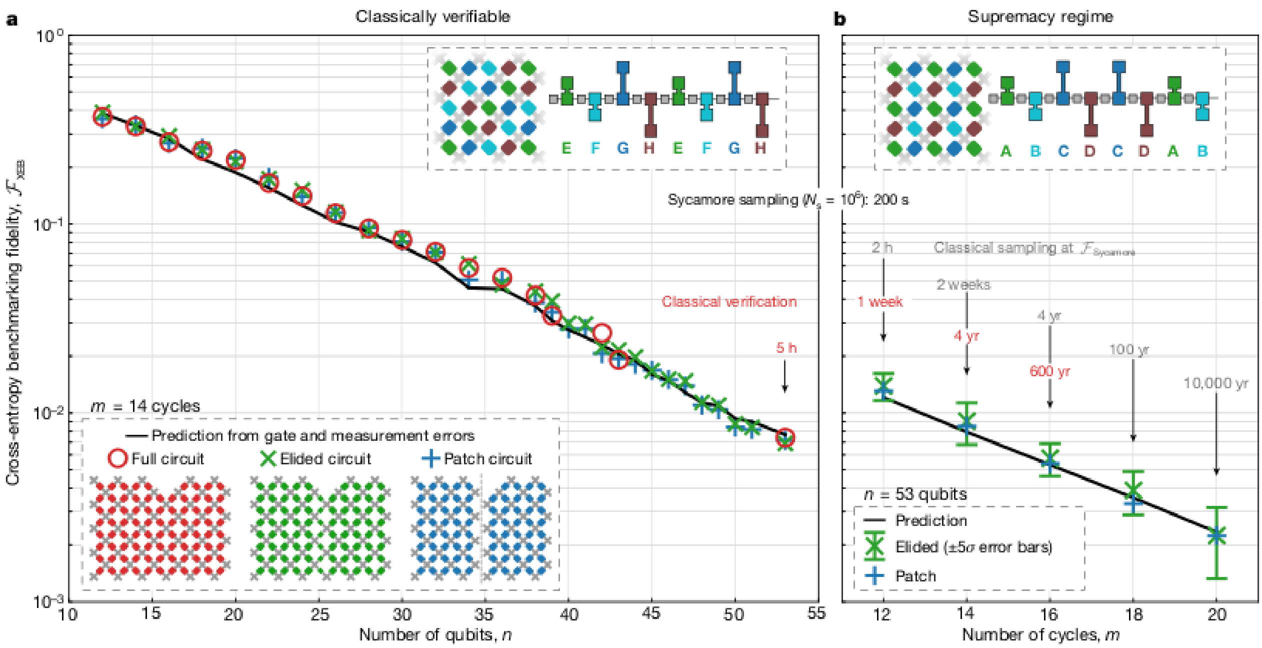
Average error	Isolated	Simultaneous
Single-qubit (e_1)	0.15%	0.16%
Two-qubit (e_2)	0.36%	0.62%
Two-qubit, cycle (e_{2c})	0.65%	0.93%
Readout (e_r)	3.1%	3.8%

They benchmark single-qubit gate performance by using the cross-entropy benchmarking protocol described above, reduced to the single-qubit level (n = 1), to measure the probability of an error occurring during a single-qubit gate.

Same process for two-qubit gate.

They repeat the benchmark with all qubits at the same time to prove and benchmark low crosstalk.

Simulations in the Quantum Supremacy Regime



Since there is not enough computational power to simulate the circuits on the quantum regime, so they use two techniques to estimate the results.

1. They use an Elided circuit, that omits redundant gates for achieving entanglement. In this way they obtain a minimal entangled circuit very similar to the full circuit.
2. They remove gates to divided the circuit into two patches, they calculate the fidelity of both patches and then do the product of both.