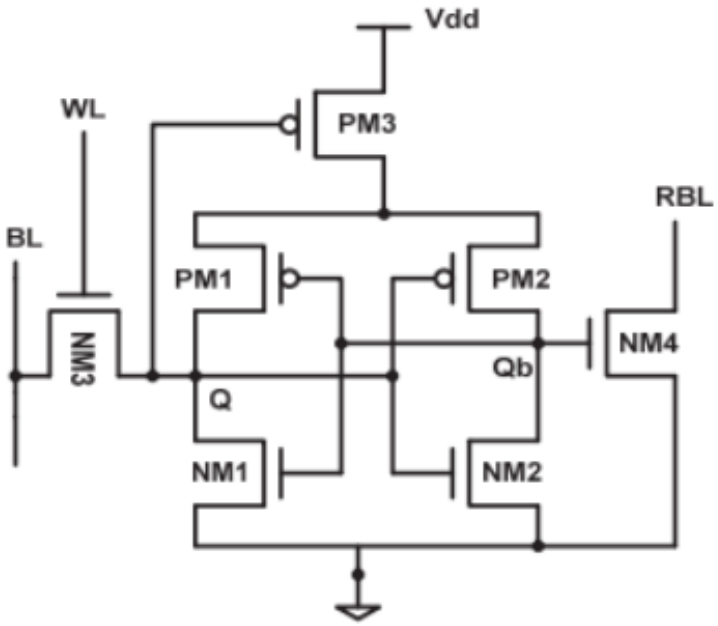
# DESIGN OF 7T SRAM CELL USING SUPPLY FEEDBACK TECHNIQUE

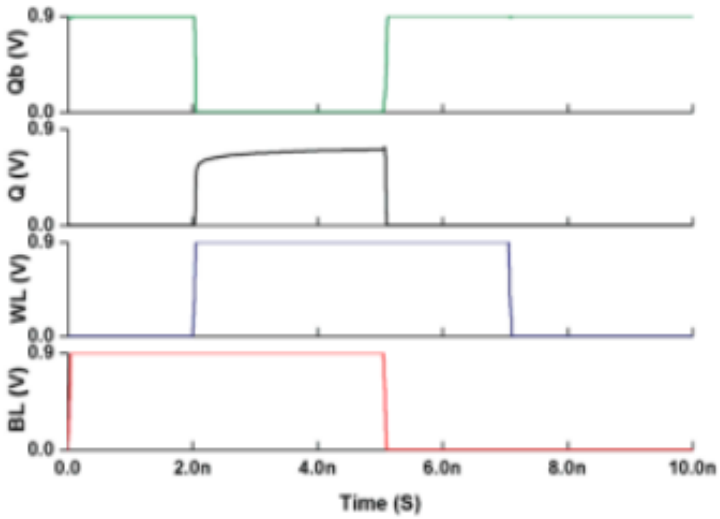

## Abstract

This static random access memory (SRAM) cell design using seven transistors reduces power dissipation using supply feedback transistor using CMOS technology. Stability of SRAM cell is also improved as its structure isolates read path and improves performance of the memory design. All the simulations are performed at 28nm technology node using Synopsys tool to analyze the performance measures of 7T SRAM cell at low supply voltage.


## Reference Circuit diagram



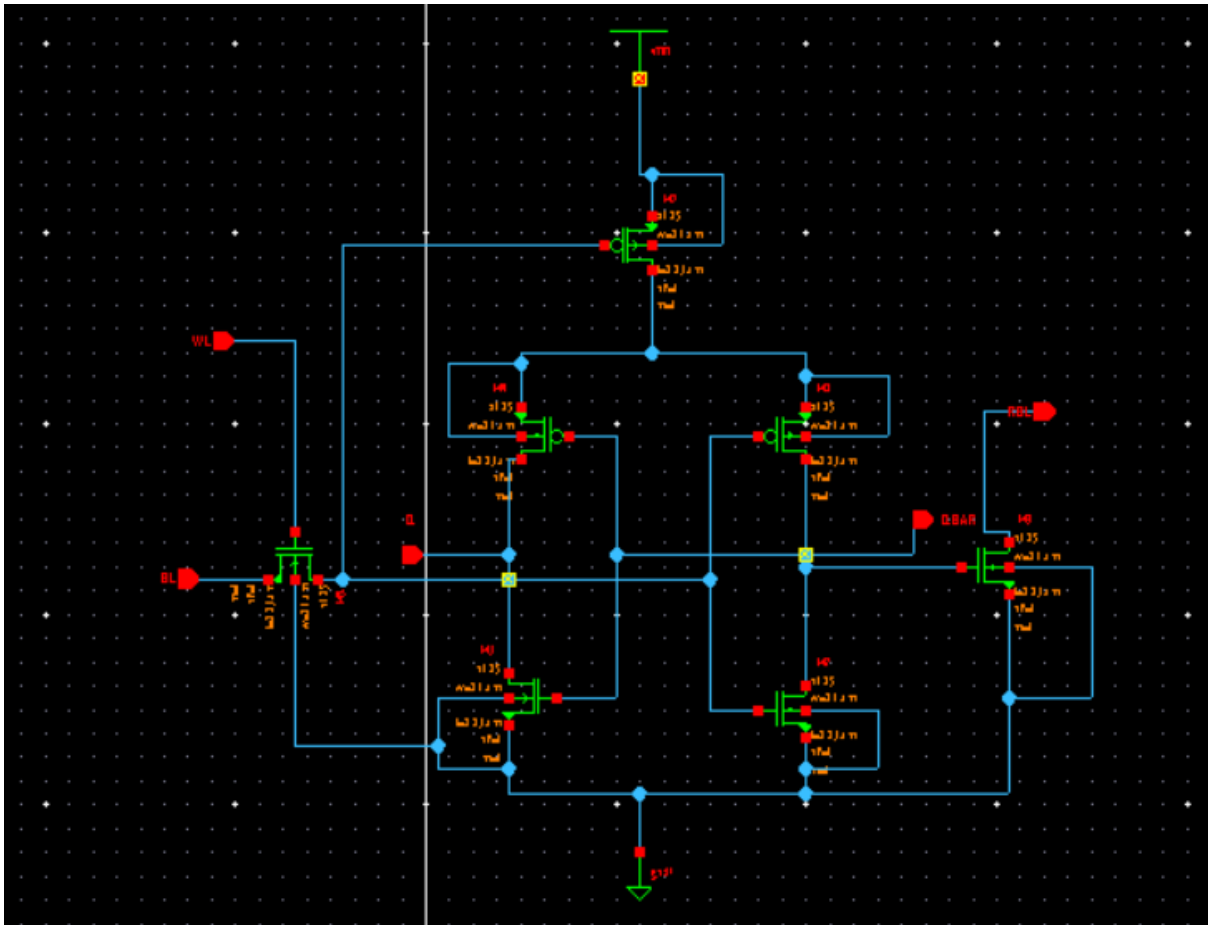

## Reerence waveform



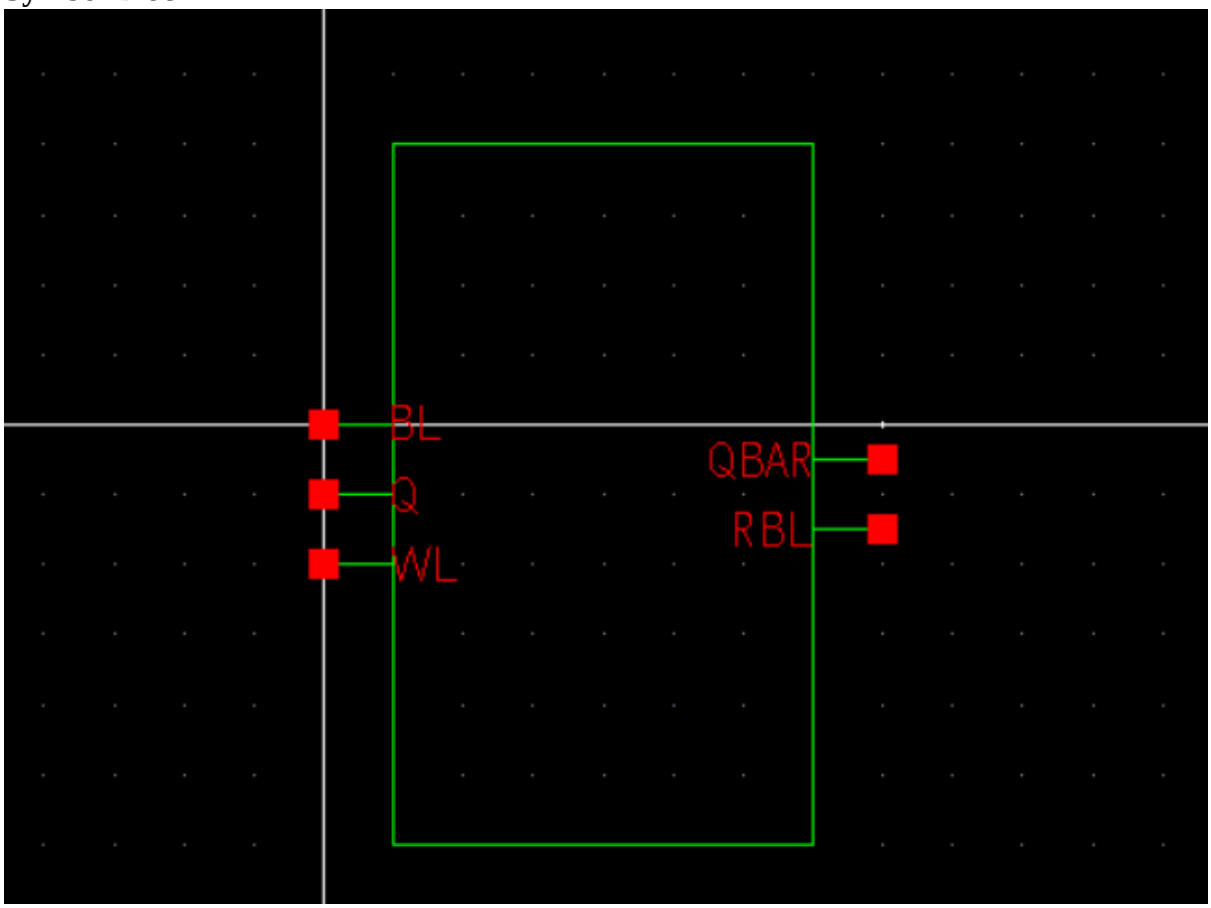
## Circuit Details

The Fig.3 shows 7T SRAM cell consists of of 4 NMOS transistors and three PMOS transistors [5]. Transistor PM1, PM2, NM1, and NM2 forms the latch of SRAM cell where the data has been stored, whereas NM3 acts as an access transistor during the write operation which is activated by word line (WL) signal and NM4 acts as an access transistor during read mode which basically used to separate the RBL from storing nodes Qb and Q of SRAM cell for providing disturb free read operation. The transistor PM3 acts as a feedback transistor which is connected between the power supply and storing node Q. This type of feedback configuration reduces the strength of the pull-up path in write operation which increases the chance of flipping the states of data very fast.

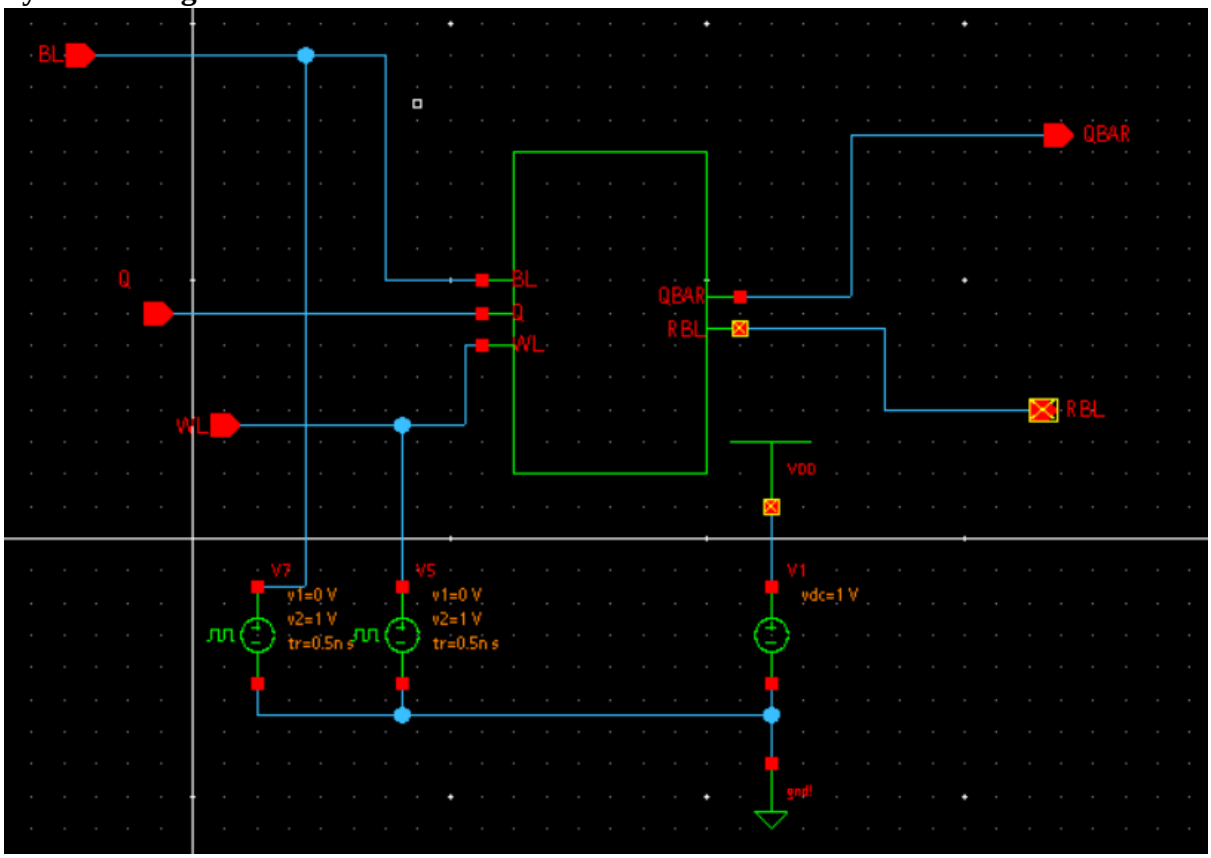
## Schematic block



**Symbol Block**




**Symbolic diagram**



Parameters set of voltage source for input BL

Current Inst V7

| | |
|---|---|
| Name | V7 |
| Origin | (0.25,-0.1875) |
| Orientation | R0 |
| Usage | Normal |
| Physical Only | |
| Placement Status | none |

Parameters

| Prompt | Value |
|---|---|
| DC Voltage | 0 V |
| Voltage1 | 0 V |
| Voltage2 | 1 V |
| Delay Time | 0 s |
| Rise Time | 0.5n s |
| Fall Time | 0.5n s |
| Pulse Width | 5n s |
| Period | 20n s |
| Period Jitter | |

Parameter set of voltage source for input WL

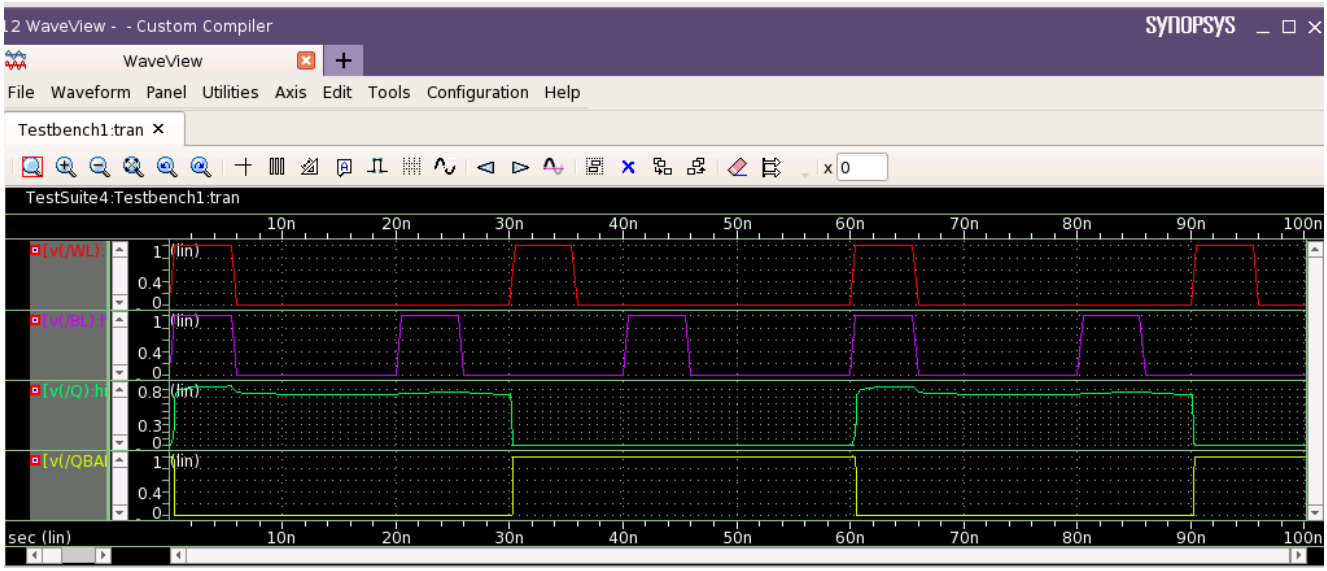
Current Inst V5

| | |
|---|---|
| Name | V5 |
| Origin | (0.8125,-0.1875) |
| Orientation | R0 |
| Usage | Normal |
| Physical Only | |
| Placement Status | none |

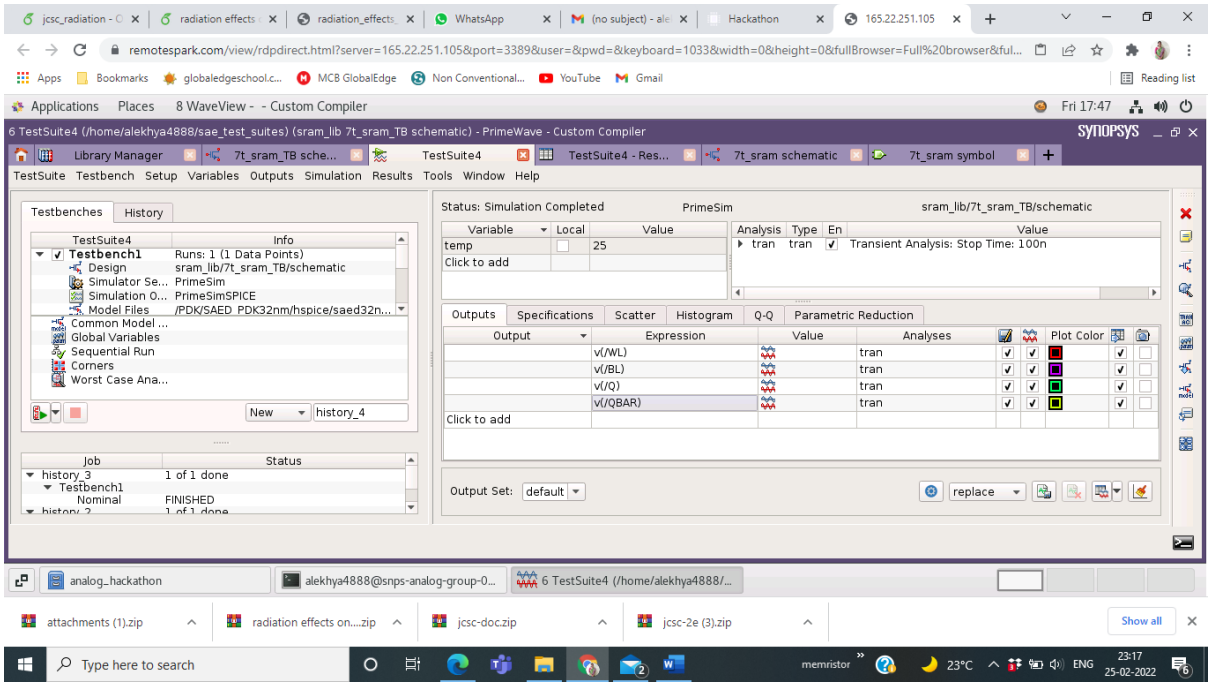
Parameters

| Prompt | Value |
|---|---|
| DC Voltage | 0 V |
| Voltage1 | 0 V |
| Voltage2 | 1 V |
| Delay Time | 0 s |
| Rise Time | 0.5n s |
| Fall Time | 0.5n s |
| Pulse Width | 5n s |
| Period | 30n s |
| Period Jitter | |

**Output waveforms**



## Transient analysis




## NETLIST

* Generated for: PrimeSim

* Design library name: sram_lib

* Design cell name: 7t_sram_TB

* Design view name: schematic

.lib '/PDK/SAED_PDK32nm/hspice/saed32nm.lib' TT

*Custom Compiler Version S-2021.09

*Fri Feb 25 16:34:48 2022

.global vdd gnd!

**********************************************************************

* Library : sram_lib

* Cell : 7t_sram

* View : schematic

* View Search List : hspice hspiceD schematic spice veriloga

* View Stop List : hspice hspiceD

```
********************************************************************************
.subckt _7t_sram bl q qbar rbl wl
xm7 net17 q vdd vdd p105 w=0.1u l=0.03u nf=1 m=1
xm4 q qbar net17 net17 p105 w=0.1u l=0.03u nf=1 m=1
xm0 qbar q net17 net17 p105 w=0.1u l=0.03u nf=1 m=1
xm8 q wl bl gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm9 rbl qbar gnd! gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm3 q qbar gnd! gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm2 qbar q gnd! gnd! n105 w=0.1u l=0.03u nf=1 m=1
.ends _7t_sram

********************************************************************************
* Library         : sram_lib
* Cell            : 7t_sram_TB
* View            : schematic
* View Search List : hspice hspiceD schematic spice veriloga
* View Stop List   : hspice hspiceD
********************************************************************************
xi0 bl q qbar rbl wl _7t_sram
v1 vdd gnd! dc=1
v7 bl gnd! dc=0 pulse ( 0 1 0 0.5n 0.5n 5n 20n )
v5 wl gnd! dc=0 pulse ( 0 1 0 0.5n 0.5n 5n 30n )




.tran '5n' '100n' name=tran
```

```
.option primesim_remove_probe_prefix = 0

.probe v(*) i(*) level=1

.probe tran v(bl) v(q) v(qbar) v(rbl) v(wl)


.temp 25




.option primesim_output=wdf



.option parhier = LOCAL









.end
```


**Acknowledgement**

1. Kunal Ghosh, Co-founder, VSD Corp. Pvt. Ltd. - kunalpghosh@gmail.com
2. Chinmay panda, IIT Hyderabad
3. Sameer Durgoji, NIT Karnataka
4. Synopsys Team/Company
5. https://www.iith.ac.in/events/2022/02/15/Cloud-Based-Analog-IC-Design-Hackathon/


**Conclusion**

The above mentioned circuit is simulated using synopsis tool at 28nm technology node. Power and area estimation of SRAM design is performed

## References

[1] Alekhya Yalla and Umakanta Nanda. Quasi fgmos 6t sram cell de sign: A strategy for low power applications. International Journal of Nanoscience, 2019.

[2] Y Alekhya and J Sudhakar. Design analysis of sram cell with improved noise margin based on aspect ratio adjustments. HELIX, 8(1):2645–2650, 2018.

[3] Y Alekhya and Umakanta Nanda. Investigation of cntfet based energy efficient fast sram cells for edge ai devices. Silicon, pages 1–16, 2022.

[4] Y Alekhya and J Sudhakar. Design of 64 bit sram using lector technique for low leakage power with read and write enable. IOSR Journal of VLSI and Signal Processing (IOSRJVSP), 7:10–19, 2017.

[5] Jitendra Kumar Mishra, Prasanna Kumar Misra, and Manish Goswami. A low power 7t sram cell using supply feedback technique at 28nm cmos technology. In 2020 7th International Conference on Signal Processing and Integrated Networks (SPIN), pages 597–602. IEEE, 2020