DataPath

Projektovanje (Digitalnih) Integrisanih Kola

HDL Projektovanje na bazi standardnih ćelija

Datum preuzimanja: 12. maj 2021.

Datum predaje: 30. avgust 2021.

Student

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Modul

ELK

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```
`timescale 1ns/1ps
module dff(input rst, input clk, input d, output reg q);


    always @(posedge clk or negedge rst)  begin
       if (!rst)
          q <= 1'b0;
       else
          q <= d;
    end
endmodule
```

Slika 1. HDL opis – kod D flip-flopa

```
`timescale 1ns/1ps
module projekat(A, B, C, CLK, RST, Y);

input A;
input B;
input C;
input CLK;
input RST;
output Y;

wire q1;
wire q2;
wire q3;
wire xorr;
wire nott;
wire nandd;
wire orr;



dff dut1(RST, CLK, A, q1);
dff dut2(RST, CLK, B, q2);
dff dut3(RST, CLK, C, q3);
```

```
dff dut1(RST, CLK, A, q1);
dff dut2(RST, CLK, B, q2);
dff dut3(RST, CLK, C, q3);

assign xorr = q1 ^ q2;
assign nott = ~q3;
assign nandd = ~(nott & xorr);
assign orr = q1 | nandd;

dff dut4(RST, CLK, orr, Y);

endmodule
```

Slika 2 i 3 – HDL kod opisanog kola

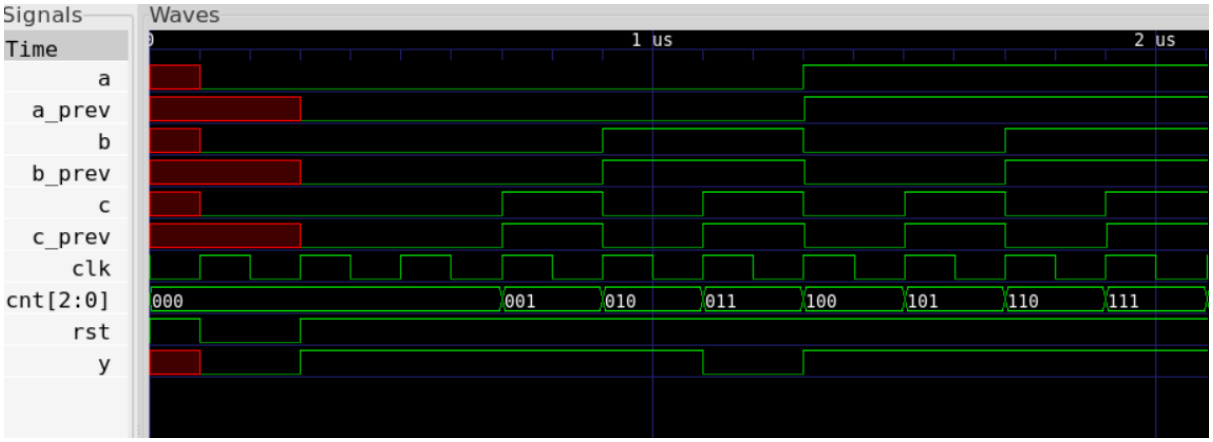
```
`timescale 1ns/1ps
module projekat_tb();

reg clk;
reg rst;
reg a, b, c;
wire y;

projekat projekat_inst(a, b, c, clk, rst, y);
reg[2:0] cnt;
reg a_prev;
reg b_prev;
reg c_prev;

initial begin
  $dumpfile("waves.vcd");
  $dumpvars(0, projekat_tb);
end
initial begin
  cnt = 0;
  clk = 0;
  rst = 1;
  @(posedge  clk);
  a = 0;
  b = 0;
  c = 0;
  rst = 0;
  @(posedge  clk);
  rst = 1;
  repeat (2) begin
```

Line: 21 Col: 11 | INS | LINE | ISO-8859-1 | projekat_tb.v

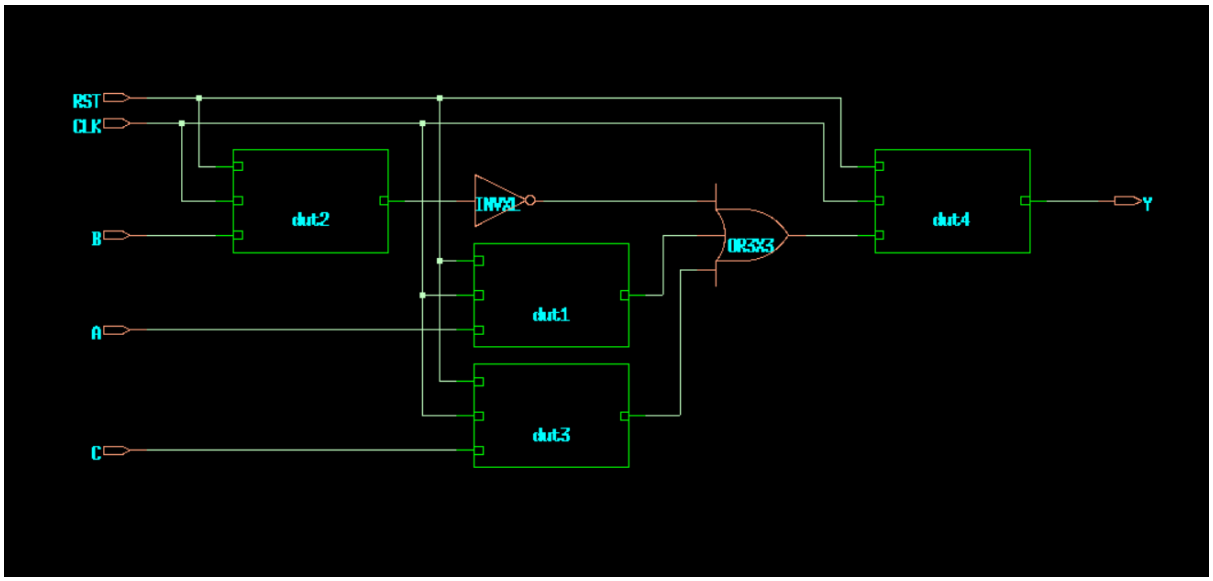
```
  forever begin
    cnt = cnt + 1;
    if (cnt == 0) begin
      $finish();
    end
    else begin
    {a, b, c} = cnt;
    @(posedge  clk);
    end
  end

  ////////
end

initial begin
  @(posedge rst);
  forever begin
    a_prev = a;
    b_prev = b;
    c_prev = c;
    @(posedge clk);
    # 1;
    if (a_prev == 0 && b_prev == 1 && c_prev == 0) begin
      if (y == 0) begin
        $display("Provera uspesna, a = %b, b = %b, c = %b, y = %b, vreme: %f", a_prev, b_prev, c_prev, y, $realtime());
      end
      else begin
        $display("Provera neuspesna, a = %b, b = %b, c = %b, y = %b, vreme: %f !", a_prev, b_prev, c_prev, y, $realtime());
      end
    end
```

```
    @(posedge clk);
    # 1;
    if (a_prev == 0 && b_prev == 1 && c_prev == 0) begin
      if (y == 0) begin
        $display("Provera uspesna, a = %b, b = %b, c = %b, y = %b, vreme: %f", a_prev, b_prev, c_prev, y, $realtime());
      end
      else begin
        $display("Provera neuspesna, a = %b, b = %b, c = %b, y = %b, vreme: %f !", a_prev, b_prev, c_prev, y, $realtime());
      end
    end
    else begin
      if (y == 1) begin
        $display("Provera uspesna, a = %b, b = %b, c = %b, y = %b, vreme: %f", a_prev, b_prev, c_prev, y, $realtime());
      end
      else begin
        $display("Provera neuspesna, a = %b, b = %b, c = %b, y = %b, vreme: %f!", a_prev, b_prev, c_prev, y, $realtime());
      end
    end
  end
end

initial forever begin

  #100;
  clk = ~clk;

end

endmodule
```

Slike 4, 5 i 6 – HDL kod testbenča



Slika 7 - Rezultati simulacije



Slika 8 – RTL Sinteza

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.11-s014_1
  Generated on:           Aug 30 2021  02:31:11 pm
  Module:                 projekat
  Technology library:     c18_CORELIB_WC revision 2.2
  Operating conditions:   worst (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

       Pin                   Type       Fanout  Load  Slew Delay Arrival
                                                (fF)  (ps)  (ps)   (ps)
-------------------------------------------------------------------------
(clock CLK1)             launch                                      0 R
dut4
  q_reg/CP                                                 0          0 R
  q_reg/QN               DFCX1              1   28.6  216  +571     571 F
  g5/A                                                          +0     571
  g5/Q                   INVX24             1 2005.4 1785 +1302    1874 R
dut4/q
Y                   <<<  interconnect                1785   +14    1888 R
                         out port                             +0    1888 R
(const.sdc_line_28)      ext delay                          +100    1988 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock CLK1)             capture                                 20000 R
-------------------------------------------------------------------------
Cost Group   : 'CLK1' (path_group 'CLK1')
Timing slack :   18012ps
Start-point  : dut4/q_reg/CP
End-point    : Y
```

Slika 9 – Kašnjenje

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.11-s014_1
  Generated on:           Aug 30 2021  02:31:11 pm
  Module:                 projekat
  Technology library:     c18_CORELIB_WC revision 2.2
  Operating conditions:   worst (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


 Gate   Instances   Area        Library
-----------------------------------------------
DFCX1           4  259.661    c18_CORELIB_WC
INVX24          1   28.224    c18_CORELIB_WC
INVXL           1    5.645    c18_CORELIB_WC
OR3X3           1   16.934    c18_CORELIB_WC
-----------------------------------------------
total           7  310.464


     Type      Instances   Area  Area %
----------------------------------------
sequential              4 259.661   83.6
inverter                2  33.869   10.9
logic                   1  16.934    5.5
physical_cells          0   0.000    0.0
----------------------------------------
total                   7 310.464  100.0
```

Slika 10 - Zauzeće

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.11-s014_1
  Generated on:           Aug 30 2021  02:31:11 pm
  Module:                 projekat
  Technology library:     c18_CORELIB_WC revision 2.2
  Operating conditions:   worst (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
-----------------------------------------------
projekat     7    92.348 25434.679 25527.026
  dut4       2    44.218 16470.659 16514.876
  dut2       1    13.797  2320.561  2334.358
  dut1       1    13.795  2359.474  2373.269
  dut3       1    13.795  2365.141  2378.936
```

Slika 11 - Potrošnja