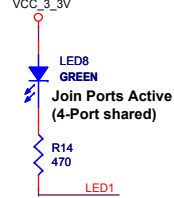
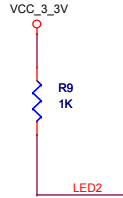
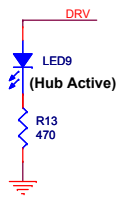
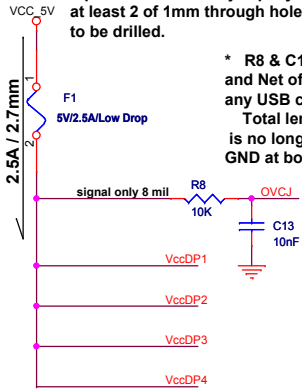


U3, 24LC02, EEPROM, is optional.
*If U3 is used, R14 should not
smaller than 470 ohm.



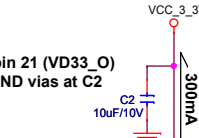
* 2.7mm wide power trace for 2.5A
If power line need to jump layer,
at least 2 of 1mm through holes need
to be drilled.



Trace of VccDP1 to 4 are 1.3mm wide

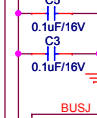
* R8 & C13 close to PIN 26 (OVCJ),
and Net of OVCJ leave far away from
any USB connector.
Total length of OVCJ net and R8 to 5V
is no longer than 400 mil with flood
GND at bottom layer.

* C2 close to pin 21 (VD33_O)
punch more GND vias at C2
GND side.

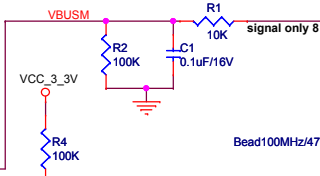


* C3, C5 close to pin 20 (VDD5)

500mA / 1mm



R1, R2, C1 are close to pin 18 (VBUSM).

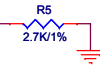


* Punch at least 3 GND
vias near by pin 1 (VSS)

Crystal 12MHZ/16~20pF
30~50ppm/(HC-49S)

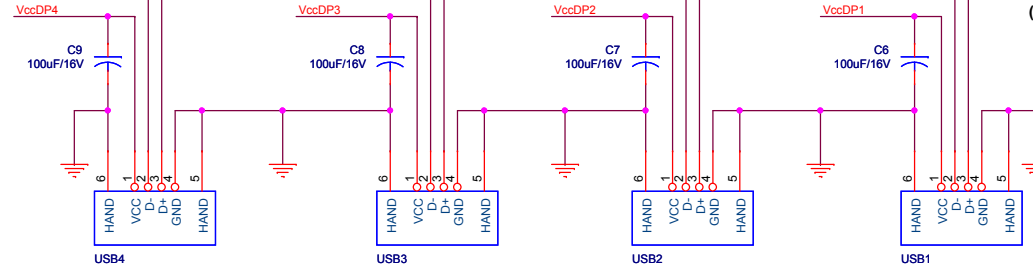


* R5 close to pin 14 (REXT),
punch more GND vias
(at least 3 vias) at R5 GND side.

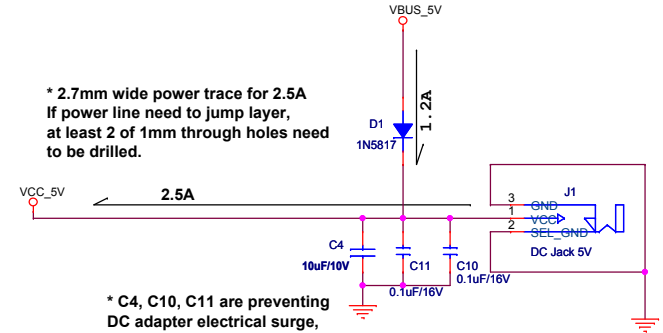


* 5 couples of DP, DM, at least
1500 mil with 15° of 45-degree-angle
(for USB-IF testing only).

* C6, C7, C8, C9 are close to each
USB Down stream port.



* 2.7mm wide power trace for 2.5A
If power line need to jump layer,
at least 2 of 1mm through holes need
to be drilled.



* C4, C10, C11 are preventing
DC adapter electrical surge,
must close to J1.

Title		
Size	Document Number	Rev
A3	FE1_1s_B_SSOP28	V1.3
Date:	Sheet	1 of 1