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ФАКУЛЬТЕТ «Информатика и системы управления»

КАФЕДРА «Программное обеспечение ЭВМ и информационные технологии»(ИУ7)

НАПРАВЛЕНИЕ ПОДГОТОВКИ 09.03.04 «Программная инженерия»

О Т Ч Е Т
по лабораторной работе № 4

Название Разработка ускорителей вычислений на платформе Xilinx Alveo

Дисциплина Архитектура элекронно-вычислительных машин

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Москва — 2021 г.

Цель работы

Изучение архитектуры гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx.

В ходе лабораторной работы предлагается изучить основные сведения о платформе Xilinx Alveo U200, разработать RTL (Register Transfer Language, язык регистровых передач)) описание ускорителя вычислений по индивидуальному варианту, выполнить генерацию ядра ускорителя, выполнить синтез и сборку бинарного модуля ускорителя, разработать и отладить тестирующее программное обеспечение на серверной хост-платформе, провести тесты работы ускорителя вычислений.

1 Работа с исходным проектом

1.1 Копии экранов моделирования исходного проекта VINC

На рисунке 1.1 приведена транзакция чтения данных вектора на шине AXI4 MM из DDR памяти (группы сигналов m00_axi_ar* и m00_axi_r*).

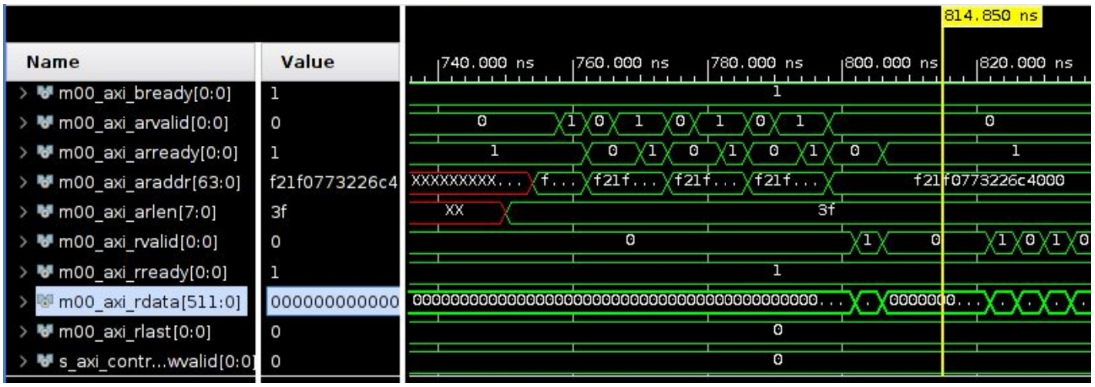

Рисунок 1.1 – Транзакция чтения данных

На рисунке 1.2 приведена транзакция записи результата инкремента данных на шине AXI4 MM (группы сигналов m00_axi_aw*, m00_axi_w* и m00_axi_b*).

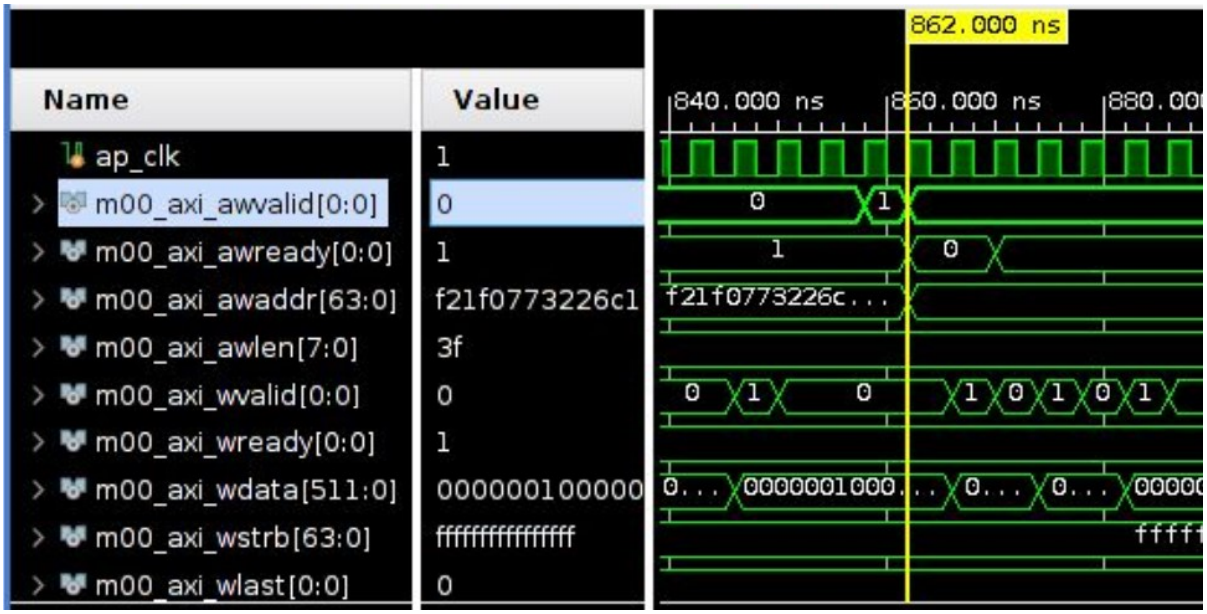

Рисунок 1.2 – Транзакция записи результата инкремента

Инкремент данных в модуле rtl_kernel_wizard_2_example_adder.v приведен на рисунках 1.3 - 1.6.

Рисунок 1.3 – Инкремент данных

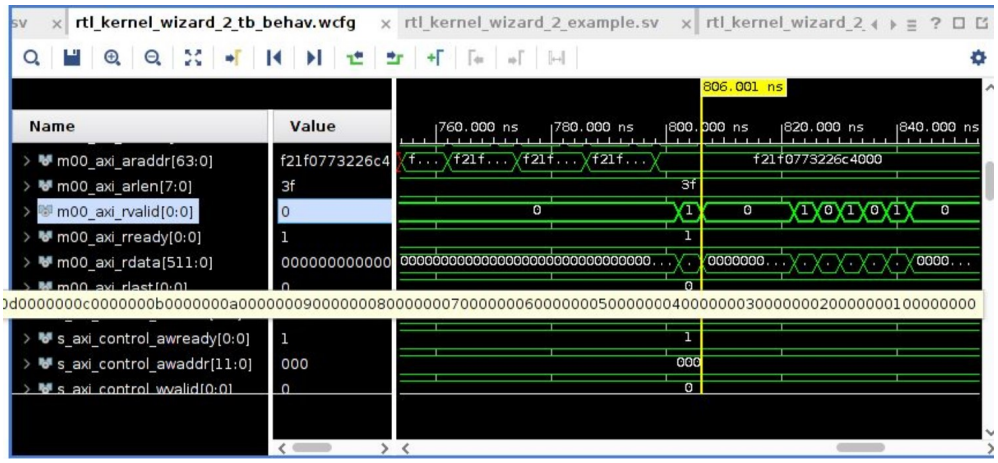

Рисунок 1.4 – Диаграмма инкремента данных (часть 1)

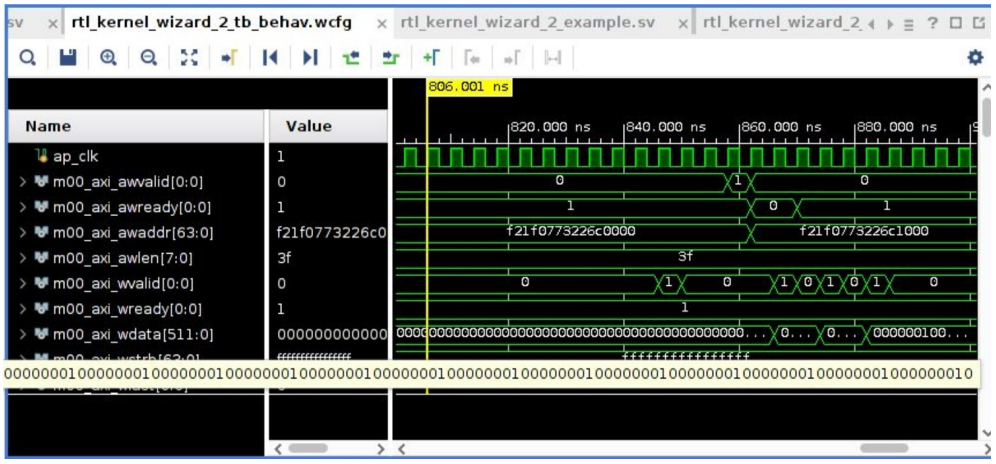

Рисунок 1.5 – Диаграмма инкремента данных (часть 2)

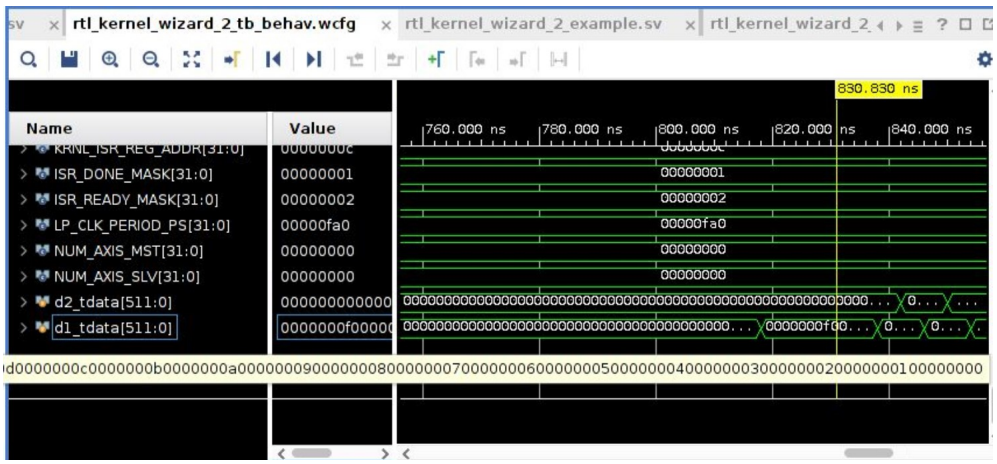

Рисунок 1.6 – Диаграмма инкремента данных (часть 3)

1.2 Линковка

На рисунке 1.7 приведен конфигурационный файл линковки.

```
[connectivity]
nk=rtl_kernel_wizard_2:2:vinc0.vinc1
slr=vinc0:SLR0
sp=vinc0.m00_axi:DDR[0]


[vivado]
# Настройки параметров фазы имплементации
prop=run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
prop=run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
prop=run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
```

Рисунок 1.7 – Конфигурационный файл линковки

В приложении в листинге 2.3 приведено содержимое файла vinc.xclbin.info, а в листинге 2.4 - содержимое файла v++_vinc.log.

2 Работа с измененным проектом

В соответствии с вариантом 6 ускоритель должен выполнять следующую функцию: $R[i] = A[i]\&0xFEDCBA9876543210$.

Измененялся код rtl_kernel_wizard_2_example_adder.v. На рисунке 2.1 приведен момент записи константы 0xFEDCBA9876543210.

```
10
11  module rtl_kernel_wizard_2_example_adder #(
12    parameter integer C_AXIS_TDATA_WIDTH = 512, // Data width of both input and output data
13    parameter integer C_ADDER_BIT_WIDTH  = 32,
14    parameter integer C_NUM_CLOCKS       = 1,
15    parameter integer MY_CONSTANT        = 32'hFEDCBA9876543210
16  )
```

Рисунок 2.1 – Запись константы

Измененный код процедуры сложения привден на рисунке 2.2

```
78    // Adder function
79  always @(posedge s_axis_aclk) begin
80    for (i = 0; i < LP_NUM_LOOPS; i = i + 1) begin
81      d2_tdata[i*C_ADDER_BIT_WIDTH+:C_ADDER_BIT_WIDTH] <= d1_tdata[C_ADDER_BIT_WIDTH*i+:C_ADDER_BIT_WIDTH] & MY_CONSTANT;
82    end
83  end
84
```

Рисунок 2.2 – Измененная процедура сложения

2.1 Копии экранов моделирования измененного проекта VINC

На рисунке 2.3 приведена транзакция чтения данных вектора на шине AXI4 MM из DDR памяти (данные остались теми же).

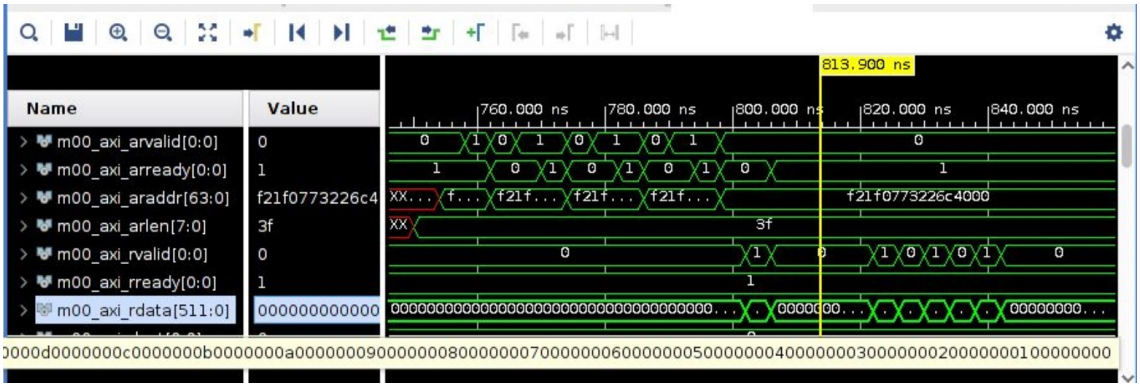

Рисунок 2.3 – Транзакция чтения данных

На рисунке 2.4 приведена транзакция записи результата инкремента данных на шине AXI4 MM (а вот результат инкремента изменился).

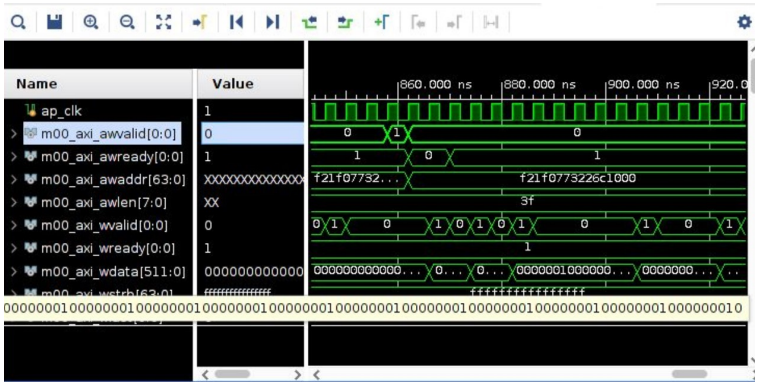

Рисунок 2.4 – Транзакция записи результата

2.2 Линковка

На рисунке 2.5 приведен конфигурационный файл линковки для измененного проекта. В соответсвии с вариантом требовалось использовать регионы SLR1 и DDR[1].

zayts_project2.cfg

```
[connectivity]
nk=rtl_kernel_wizard_2:2:vinc0.vinc1
slr=vinc0:SLR1
sp=vinc0.m00_axi:DDR[1]


[vivado]
# Настройки параметров фазы имплементации
prop=run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
prop=run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
prop=run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
```

Рисунок 2.5 – Конфигурационный файл линковки для измененного проекта

Во приложении в листинге 2.5 приведено содержимое файла vinc.xclbin.info для измененного проекта, а в листинге 2.6 - файла v++_vinc.log для измененного проекта.

2.3 Работа с модулем host_example.cpp

В листинге 2.1 приведен код измененного участка модуля host_example.cpp.

Листинг 2.1 – Код модифицированного модуля host_example.cpp

```
1     for (cl_uint i = 0; i < number_of_words; i++) {
2     if ((h_data[i] & 0xFEDCBA9876543210) != h_axi00_ptr0_output[i]) {
```

```
3           printf("ERROR in rtl_kernel_wizard_2::m00_axi - array index %d
                (host addr 0x%03x) - input=%d (0x%x), output=%d (0x%x)\n",
                i, i*4, h_data[i], h_data[i], h_axi00_ptr0_output[i],
                h_axi00_ptr0_output[i]);
4           check_status = 1;
5       }
6       //printf("i=%d, input=%d, output=%d, expected_output=%d\n", i,
            h_axi00_ptr0_input[i], h_axi00_ptr0_output[i], h_data[i] &
            0xFEDCBA9876543210);
7   }
```

Так как с графическим интерфейсом программы Xilinx Vitis IDE автор отчета ранее не сталкивался, а он оказался довольно непонятным, для тестирования было решено воспользоваться утилитой xgdb. На рисунке 2.6 приведены результаты первого запуска тестирования.

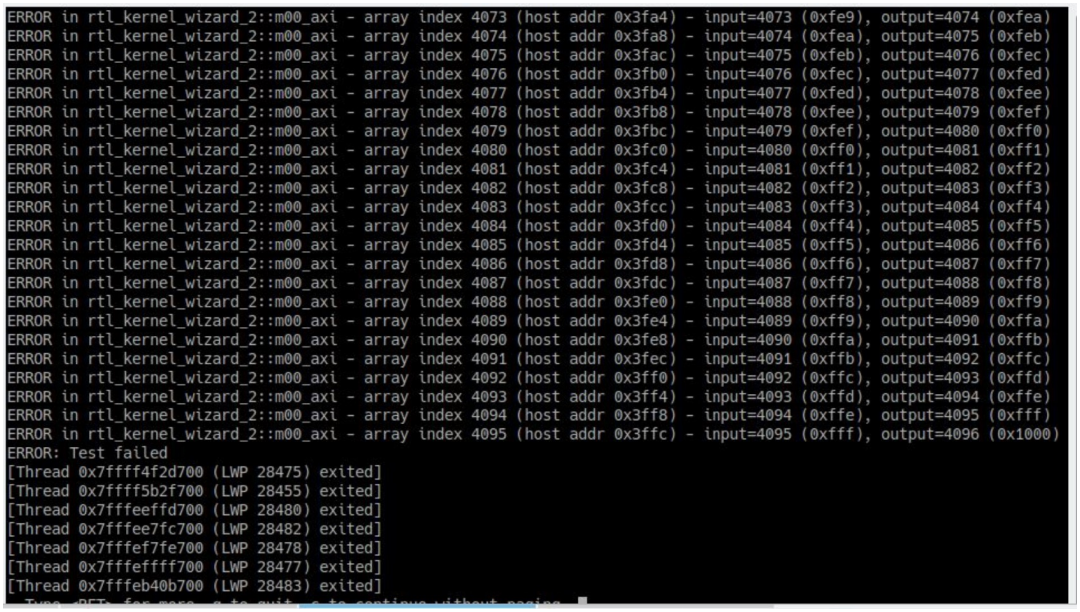

Рисунок 2.6 – Результаты первого запуска тестирования

К сожалению, автор отчета забыл явным образом сохранить измененный файл rtl_kernel_wizard_2_example_adder.v перед повторной линковкой, поэтому функция инкремента осталось той же. Чтобы повторно не выполнять линковку, было решено изменить модуль host_example.cpp, код которого приведен в листинге 2.2.

Листинг 2.2 – Код модифицированного модуля host_example.cpp

```
1           for (cl_uint i = 0; i < number_of_words; i++) {
2           if ((h_data[i] + 1) != h_axi00_ptr0_output[i]) {
3               printf("ERROR in rtl_kernel_wizard_2::m00_axi - array index
                    %d (host addr 0x%03x) - input=%d (0x%x), output=%d
```

```
                (0x%x)\n", i, i*4, h_data[i], h_data[i],
                h_axi00_ptr0_output[i], h_axi00_ptr0_output[i]);
4           check_status = 1;
5       }
6       //printf("i=%d, input=%d, output=%d, expected_output=%d\n", i,
            h_axi00_ptr0_input[i], h_axi00_ptr0_output[i], h_data[i] +
            1);
7   }
```

На рисунке 2.7 приведены результаты второго запуска тестирования. Как видно, все тесты пройдены успешно.

```
(gdb) run
Starting program: /iu_home/iu7036/workspace/zayts/zayts_project_kernels/vivado_rtl_kernel/rtl_kernel_wizard_2_ex/expor
ts/rtl_kernel_wizard_2_host_example.exe /iu_home/iu7036/workspace/zayts/vinc.xclbin
[Thread debugging using libthread_db enabled]
Using host libthread_db library "/lib/x86_64-linux-gnu/libthread_db.so.1".
[New Thread 0x7ffff5b2f700 (LWP 37187)]
INFO: Found 1 platforms
INFO: Selected platform 0 from Xilinx
INFO: Found 1 devices
CL_DEVICE_NAME xilinx_u200_xdma_201830_2
Selected xilinx_u200_xdma_201830_2 as the target device
INFO: loading xclbin /iu_home/iu7036/workspace/zayts/vinc.xclbin
[New Thread 0x7ffff4f2d700 (LWP 37218)]
[New Thread 0x7fffeffff700 (LWP 37219)]
[New Thread 0x7fffef7fe700 (LWP 37220)]
[New Thread 0x7fffeeffd700 (LWP 37221)]
[New Thread 0x7fffee7fc700 (LWP 37222)]
[New Thread 0x7fffeb40b700 (LWP 37223)]
INFO: Test completed successfully.
[Thread 0x7ffff4f2d700 (LWP 37218) exited]
[Thread 0x7ffff5b2f700 (LWP 37187) exited]
[Thread 0x7fffeb40b700 (LWP 37223) exited]
[Thread 0x7fffee7fc700 (LWP 37222) exited]
[Thread 0x7fffeeffd700 (LWP 37221) exited]
[Thread 0x7fffef7fe700 (LWP 37220) exited]
[Thread 0x7fffeffff700 (LWP 37219) exited]
[Inferior 1 (process 37163) exited normally]
(gdb)
```

Рисунок 2.7 – Результаты второго запуска тестирования

Заключение

В результате выполнения лабораторной работы была изучена архитектура гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx.

В ходе работы был проработан теоретический материал, касающийся основных сведений о платформе Xilinx Alveo U200, разработано RTL описание ускорителя вычислений по индивидуальному варианту, выполнена генерация ядра ускорителя, выполнены синтез и сборка бинарного модуля ускорителя, разработано и отлажено тестирующее программное обеспечение на серверной хост-платформе, проведены тесты работы ускорителя вычислений.

Приложение

Листинг 2.3 – Содержимое файла vinc.xclbin.info

```
1  ==========================================================
2  XRT Build Version: 2.8.743 (2020.2)
3  Build Date: 2020-11-16 00:19:11
4  Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
5  ==========================================================
6  xclbin Information
7  ------------------
8  Generated by:            v++ (2020.2) on 2020-11-18-05:13:29
9  Version:                 2.8.743
10 Kernels:                 rtl_kernel_wizard_2
11 Signature:
12 Content:                 Bitstream
13 UUID (xclbin):           8272e136-8d34-4a26-b282-90c6741d22e2
14 Sections:                DEBUG_IP_LAYOUT, BITSTREAM, MEM_TOPOLOGY,
     IP_LAYOUT,
15 CONNECTIVITY, CLOCK_FREQ_TOPOLOGY, BUILD_METADATA,
16 EMBEDDED_METADATA, SYSTEM_METADATA,
17 GROUP_CONNECTIVITY, GROUP_TOPOLOGY
18 ==========================================================
19 Hardware Platform (Shell) Information
20 ------------------------------------
21 Vendor:                  xilinx
22 Board:                   u200
23 Name:                    xdma
24 Version:                 201830.2
25 Generated Version:       Vivado 2018.3 (SW Build: 2568420)
26 Created:                 Tue Jun 25 06:55:20 2019
27 FPGA Device:             xcu200
28 Board Vendor:            xilinx.com
29 Board Name:              xilinx.com:au200:1.0
30 Board Part:              xilinx.com:au200:part0:1.0
31 Platform VBNV:           xilinx_u200_xdma_201830_2
32 Static UUID:             c102e7af-b2b8-4381-992b-9a00cc3863eb
33 Feature ROM TimeStamp:   1561465320
34
35 Clocks
36 ------
37 Name:        DATA_CLK
```

```
    Index:      0
    Type:       DATA
    Frequency:  300 MHz

    Name:       KERNEL_CLK
    Index:      1
    Type:       KERNEL
    Frequency:  500 MHz

    Memory Configuration
    --------------------

    Name:           bank0
    Index:          0
    Type:           MEM_DDR4
    Base Address:   0x4000000000
    Address Size:   0x400000000
    Bank Used:      Yes

    Name:           bank1
    Index:          1
    Type:           MEM_DDR4
    Base Address:   0x5000000000
    Address Size:   0x400000000
    Bank Used:      Yes

    Name:           bank2
    Index:          2
    Type:           MEM_DDR4
    Base Address:   0x6000000000
    Address Size:   0x400000000
    Bank Used:      No

    Name:           bank3
    Index:          3
    Type:           MEM_DDR4
    Base Address:   0x7000000000
    Address Size:   0x400000000
    Bank Used:      No

    Name:           PLRAM[0]
    Index:          4
```

```
    Type:           MEM_DRAM
    Base Address:   0x3000000000
    Address Size:   0x20000
    Bank Used:      No

    Name:           PLRAM[1]
    Index:          5
    Type:           MEM_DRAM
    Base Address:   0x3000200000
    Address Size:   0x20000
    Bank Used:      No

    Name:           PLRAM[2]
    Index:          6
    Type:           MEM_DRAM
    Base Address:   0x3000400000
    Address Size:   0x20000
    Bank Used:      No
    ==========================================================
    Kernel: rtl_kernel_wizard_2

    Definition
    ----------
    Signature: rtl_kernel_wizard_2 (uint scalar00, int* axi00_ptr0)

    Ports
    -----
    Port:           s_axi_control
    Mode:           slave
    Range (bytes):  0x1000
    Data Width:     32 bits
    Port Type:      addressable

    Port:           m00_axi
    Mode:           master
    Range (bytes):  0xFFFFFFFFFFFFFFFF
    Data Width:     512 bits
    Port Type:      addressable

    ---------------------------
    Instance:         vinc0
```

```
120     Base Address: 0x1c00000
121
122     Argument:           scalar00
123     Register Offset:    0x010
124     Port:               s_axi_control
125     Memory:             <not applicable>
126
127     Argument:           axi00_ptr0
128     Register Offset:    0x018
129     Port:               m00_axi
130     Memory:             bank0 (MEM_DDR4)
131
132     ---------------------------
133     Instance:         vinc1
134     Base Address: 0x1800000
135
136     Argument:           scalar00
137     Register Offset:    0x010
138     Port:               s_axi_control
139     Memory:             <not applicable>
140
141     Argument:           axi00_ptr0
142     Register Offset:    0x018
143     Port:               m00_axi
144     Memory:             bank1 (MEM_DDR4)
145     ===========================================================
146     Generated By
147     ------------
148     Command:        v++
149     Version:        2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)
150     Command Line:   v++ --config
        /iu_home/iu7036/workspace/zayts/zayts_project.cfg
        --connectivity.nk rtl_kernel_wizard_2:2:vinc0.vinc1
        --connectivity.slr vinc0:SLR0 --connectivity.sp
        vinc0.m00_axi:DDR[0] --input_files
        /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
        --link --optimize 0 --output
        /iu_home/iu7036/workspace/zayts/vinc.xclbin --platform
        xilinx_u200_xdma_201830_2 --report_level 0 --target hw
        --vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
        --vivado.prop
```

```
    run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
    --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
    --vivado.prop
    run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
    --vivado.prop
    run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
151 Options:        --config
    /iu_home/iu7036/workspace/zayts/zayts_project.cfg
152 --connectivity.nk rtl_kernel_wizard_2:2:vinc0.vinc1
153 --connectivity.slr vinc0:SLR0
154 --connectivity.sp vinc0.m00_axi:DDR[0]
155 --input_files
    /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
156 --link
157 --optimize 0
158 --output /iu_home/iu7036/workspace/zayts/vinc.xclbin
159 --platform xilinx_u200_xdma_201830_2
160 --report_level 0
161 --target hw
162 --vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
163 --vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
164 --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
165 --vivado.prop
    run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
166 --vivado.prop run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
167 ================================================================
168 User Added Key Value Pairs
169 ----------------------------
170 <empty>
171 ================================================================
```

Листинг 2.4 – Содержимое файла v++_vinc.log

```
1 INFO: [v++ 60-1306] Additional information associated with this v++
    link can be found at:
2 Reports: /iu_home/iu7036/_x/reports/link
3 Log files: /iu_home/iu7036/_x/logs/link
4 INFO: [v++ 60-1548] Creating build summary session with primary
    output /iu_home/iu7036/workspace/zayts/vinc.xclbin.link_summary,
    at Sun Nov 21 13:42:16 2021
5 INFO: [v++ 60-1316] Initiating connection to rulecheck server, at
    Sun Nov 21 13:42:17 2021
```

```
6     INFO: [v++ 60-1315] Creating rulecheck session with output
          '/iu_home/iu7036/_x/reports/link/v++_link_vinc_guidance.html',
          at Sun Nov 21 13:42:36 2021
7     INFO: [v++ 60-895]   Target platform:
          /opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_20183
8     INFO: [v++ 60-1578]   This platform contains Device Support Archive
          '/opt/xilinx/platforms/xilinx_u200_xdma_201830_2/hw/xilinx_u200_xdma_2
9     INFO: [v++ 74-74] Compiler Version string: 2020.2
10    INFO: [v++ 60-1302] Platform 'xilinx_u200_xdma_201830_2.xpfm' has
          been explicitly enabled for this release.
11    INFO: [v++ 60-629] Linking for hardware target
12    INFO: [v++ 60-423]   Target device: xilinx_u200_xdma_201830_2
13    INFO: [v++ 60-1332] Run 'run_link' status: Not started
14    INFO: [v++ 60-1443] [13:43:36] Run run_link: Step system_link:
          Started
15    INFO: [v++ 60-1453] Command Line: system_link --xo
          /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
          --config /iu_home/iu7036/_x/link/int/syslinkConfig.ini --xpfm
          /opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_20183
          --target hw --output_dir /iu_home/iu7036/_x/link/int --temp_dir
          /iu_home/iu7036/_x/link/sys_link
16    INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
17    INFO: [SYSTEM_LINK 60-1316] Initiating connection to rulecheck
          server, at Sun Nov 21 13:43:50 2021
18    INFO: [SYSTEM_LINK 82-70] Extracting xo v3 file
          /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
19    INFO: [SYSTEM_LINK 82-53] Creating IP database
          /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
20    INFO: [SYSTEM_LINK 82-38] [13:43:53] build_xd_ip_db started:
          /data/Xilinx/Vitis/2020.2/bin/build_xd_ip_db -ip_search 0
          -sds-pf
          /iu_home/iu7036/_x/link/sys_link/xilinx_u200_xdma_201830_2.hpfm
          -clkid 0 -ip
          /iu_home/iu7036/_x/link/sys_link/iprepo/mycompany_com_kernel_rtl_kernel
          -o /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
21    INFO: [SYSTEM_LINK 82-37] [13:44:26] build_xd_ip_db finished
          successfully
22    Time (s): cpu = 00:00:35 ; elapsed = 00:00:33 . Memory (MB): peak =
          1557.895 ; gain = 0.000 ; free physical = 201364 ; free virtual
          = 230178
23    INFO: [SYSTEM_LINK 82-51] Create system connectivity graph
```

```
24    INFO: [SYSTEM_LINK 82-102] Applying explicit connections to the
         system connectivity graph:
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml
25    INFO: [SYSTEM_LINK 82-38] [13:44:26] cfgen started:
         /data/Xilinx/Vitis/2020.2/bin/cfgen  -nk
         rtl_kernel_wizard_2:2:vinc0.vinc1 -slr vinc0:SLR0 -sp
         vinc0.m00_axi:DDR[0] -dmclkid 0 -r
         /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml -o
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml
26    INFO: [CFGEN 83-0] Kernel Specs:
27    INFO: [CFGEN 83-0]   kernel: rtl_kernel_wizard_2, num: 2  {vinc0
         vinc1}
28    INFO: [CFGEN 83-0] Port Specs:
29    INFO: [CFGEN 83-0]   kernel: vinc0, k_port: m00_axi, sptag: DDR[0]
30    INFO: [CFGEN 83-0] SLR Specs:
31    INFO: [CFGEN 83-0]   instance: vinc0, SLR: SLR0
32    INFO: [CFGEN 83-2228] Creating mapping for argument
         vinc0.axi00_ptr0 to DDR[0] for directive vinc0.m00_axi:DDR[0]
33    INFO: [CFGEN 83-2226] Inferring mapping for argument
         vinc1.axi00_ptr0 to DDR[1]
34    INFO: [SYSTEM_LINK 82-37] [13:44:55] cfgen finished successfully
35    Time (s): cpu = 00:00:28 ; elapsed = 00:00:28 . Memory (MB): peak =
         1557.895 ; gain = 0.000 ; free physical = 201347 ; free virtual
         = 230162
36    INFO: [SYSTEM_LINK 82-52] Create top-level block diagram
37    INFO: [SYSTEM_LINK 82-38] [13:44:55] cf2bd started:
         /data/Xilinx/Vitis/2020.2/bin/cf2bd  --linux --trace_buffer 1024
         --input_file
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml
         --ip_db /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
         --cf_name dr --working_dir
         /iu_home/iu7036/_x/link/sys_link/_sysl/.xsd --temp_dir
         /iu_home/iu7036/_x/link/sys_link --output_dir
         /iu_home/iu7036/_x/link/int --target_bd pfm_dynamic.bd
38    INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer
         1024 -i
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml -r
         /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml -o
         dr.xml
39    INFO: [CF2BD 82-28] cf2xd finished successfully
40    INFO: [CF2BD 82-31] Launching cf_xsd: cf_xsd -disable-address-gen
```

```
    -bd pfm_dynamic.bd -dn dr -dp
    /iu_home/iu7036/_x/link/sys_link/_sysl/.xsd
41  INFO: [CF2BD 82-28] cf_xsd finished successfully
42  INFO: [SYSTEM_LINK 82-37] [13:45:13] cf2bd finished successfully
43  Time (s): cpu = 00:00:16 ; elapsed = 00:00:18 . Memory (MB): peak =
    1557.895 ; gain = 0.000 ; free physical = 201314 ; free virtual
    = 230134
44  INFO: [v++ 60-1441] [13:45:13] Run run_link: Step system_link:
    Completed
45  Time (s): cpu = 00:01:36 ; elapsed = 00:01:37 . Memory (MB): peak =
    1585.129 ; gain = 0.000 ; free physical = 201372 ; free virtual
    = 230187
46  INFO: [v++ 60-1443] [13:45:13] Run run_link: Step cf2sw: Started
47  INFO: [v++ 60-1453] Command Line: cf2sw -sdsl
    /iu_home/iu7036/_x/link/int/sdsl.dat -rtd
    /iu_home/iu7036/_x/link/int/cf2sw.rtd -nofilter
    /iu_home/iu7036/_x/link/int/cf2sw_full.rtd -xclbin
    /iu_home/iu7036/_x/link/int/xclbin_orig.xml -o
    /iu_home/iu7036/_x/link/int/xclbin_orig.1.xml
48  INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
49  INFO: [v++ 60-1441] [13:45:34] Run run_link: Step cf2sw: Completed
50  Time (s): cpu = 00:00:20 ; elapsed = 00:00:21 . Memory (MB): peak =
    1585.129 ; gain = 0.000 ; free physical = 201340 ; free virtual
    = 230157
51  INFO: [v++ 60-1443] [13:45:34] Run run_link: Step
    rtd2_system_diagram: Started
52  INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram
53  INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
54  INFO: [v++ 60-1441] [13:45:45] Run run_link: Step
    rtd2_system_diagram: Completed
55  Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:10 . Memory (MB):
    peak = 1585.129 ; gain = 0.000 ; free physical = 200791 ; free
    virtual = 229608
56  INFO: [v++ 60-1443] [13:45:45] Run run_link: Step vpl: Started
57  INFO: [v++ 60-1453] Command Line: vpl -t hw -f
    xilinx_u200_xdma_201830_2 --remote_ip_cache
    /iu_home/iu7036/.ipcache --output_dir
    /iu_home/iu7036/_x/link/int --log_dir
    /iu_home/iu7036/_x/logs/link --report_dir
    /iu_home/iu7036/_x/reports/link --config
    /iu_home/iu7036/_x/link/int/vplConfig.ini -k
```

```
    /iu_home/iu7036/_x/link/int/kernel_info.dat --webtalk_flag Vitis
    --temp_dir /iu_home/iu7036/_x/link --no-info --iprepo
    /iu_home/iu7036/_x/link/int/xo/ip_repo/mycompany_com_kernel_rtl_kernel_
    --messageDb /iu_home/iu7036/_x/link/run_link/vpl.pb
    /iu_home/iu7036/_x/link/int/dr.bd.tcl
INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link

****** vpl v2020.2 (64-bit)
**** SW Build (by xbuild) on 2020-11-18-05:13:29
** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

INFO: [VPL 60-839] Read in kernel information from file
    '/iu_home/iu7036/_x/link/int/kernel_info.dat'.
INFO: [VPL 74-74] Compiler Version string: 2020.2
INFO: [VPL 60-423]   Target device: xilinx_u200_xdma_201830_2
INFO: [VPL 60-1032] Extracting hardware platform to
    /iu_home/iu7036/_x/link/vivado/vpl/.local/hw_platform
WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not
    exist.
[13:51:54] Run vpl: Step create_project: Started
Creating Vivado project.
[13:52:12] Run vpl: Step create_project: RUNNING...
[13:52:25] Run vpl: Step create_project: Completed
[13:52:25] Run vpl: Step create_bd: Started
[13:54:13] Run vpl: Step create_bd: RUNNING...
[13:55:56] Run vpl: Step create_bd: RUNNING...
[13:57:35] Run vpl: Step create_bd: RUNNING...
[13:59:28] Run vpl: Step create_bd: RUNNING...
[14:01:15] Run vpl: Step create_bd: RUNNING...
[14:03:01] Run vpl: Step create_bd: RUNNING...
[14:03:42] Run vpl: Step create_bd: Completed
[14:03:42] Run vpl: Step update_bd: Started
[14:03:46] Run vpl: Step update_bd: Completed
[14:03:46] Run vpl: Step generate_target: Started
[14:05:38] Run vpl: Step generate_target: RUNNING...
[14:07:18] Run vpl: Step generate_target: RUNNING...
[14:08:50] Run vpl: Step generate_target: RUNNING...
[14:10:30] Run vpl: Step generate_target: RUNNING...
[14:12:05] Run vpl: Step generate_target: RUNNING...
[14:13:52] Run vpl: Step generate_target: RUNNING...
[14:15:27] Run vpl: Step generate_target: RUNNING...
```

```
91    [14:17:22] Run vpl: Step generate_target: RUNNING...
92    [14:18:46] Run vpl: Step generate_target: Completed
93    [14:18:46] Run vpl: Step config_hw_runs: Started
94    [14:20:33] Run vpl: Step config_hw_runs: RUNNING...
95    [14:21:05] Run vpl: Step config_hw_runs: Completed
96    [14:21:05] Run vpl: Step synth: Started
97    [14:24:07] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
98    [14:24:46] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
99    [14:25:26] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
100   [14:26:08] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
101   [14:26:57] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
102   [14:27:39] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
103   [14:28:22] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
104   [14:29:03] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
105   [14:29:44] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
106   [14:30:24] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
107   [14:31:07] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
108   [14:31:49] Block-level synthesis in progress, 0 of 76 jobs
        complete, 8 jobs running.
109   [14:32:35] Block-level synthesis in progress, 7 of 76 jobs
        complete, 1 job running.
110   [14:33:21] Block-level synthesis in progress, 7 of 76 jobs
        complete, 1 job running.
111   [14:34:02] Block-level synthesis in progress, 7 of 76 jobs
        complete, 8 jobs running.
112   [14:34:41] Block-level synthesis in progress, 8 of 76 jobs
        complete, 7 jobs running.
113   [14:35:23] Block-level synthesis in progress, 9 of 76 jobs
        complete, 6 jobs running.
114   [14:36:06] Block-level synthesis in progress, 9 of 76 jobs
```

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        complete, 8 jobs running.
115     [14:36:47] Block-level synthesis in progress, 10 of 76 jobs
        complete, 7 jobs running.
116     [14:37:27] Block-level synthesis in progress, 10 of 76 jobs
        complete, 7 jobs running.
117     [14:38:09] Block-level synthesis in progress, 10 of 76 jobs
        complete, 8 jobs running.
118     [14:38:49] Block-level synthesis in progress, 10 of 76 jobs
        complete, 8 jobs running.
119     [14:39:35] Block-level synthesis in progress, 11 of 76 jobs
        complete, 7 jobs running.
120     [14:40:14] Block-level synthesis in progress, 11 of 76 jobs
        complete, 7 jobs running.
121     [14:40:56] Block-level synthesis in progress, 11 of 76 jobs
        complete, 8 jobs running.
122     [14:41:27] Block-level synthesis in progress, 11 of 76 jobs
        complete, 8 jobs running.
123     [14:42:19] Block-level synthesis in progress, 16 of 76 jobs
        complete, 3 jobs running.
124     [14:42:55] Block-level synthesis in progress, 17 of 76 jobs
        complete, 3 jobs running.
125     [14:43:39] Block-level synthesis in progress, 17 of 76 jobs
        complete, 7 jobs running.
126     [14:44:16] Block-level synthesis in progress, 17 of 76 jobs
        complete, 8 jobs running.
127     [14:45:00] Block-level synthesis in progress, 18 of 76 jobs
        complete, 7 jobs running.
128     [14:45:38] Block-level synthesis in progress, 20 of 76 jobs
        complete, 5 jobs running.
129     [14:46:24] Block-level synthesis in progress, 20 of 76 jobs
        complete, 7 jobs running.
130     [14:47:00] Block-level synthesis in progress, 20 of 76 jobs
        complete, 8 jobs running.
131     [14:47:47] Block-level synthesis in progress, 21 of 76 jobs
        complete, 7 jobs running.
132     [14:48:24] Block-level synthesis in progress, 21 of 76 jobs
        complete, 7 jobs running.
133     [14:49:09] Block-level synthesis in progress, 21 of 76 jobs
        complete, 8 jobs running.
134     [14:49:45] Block-level synthesis in progress, 21 of 76 jobs
        complete, 8 jobs running.
```

```
135     [14:50:28] Block-level synthesis in progress, 22 of 76 jobs
          complete, 7 jobs running.
136     [14:51:07] Block-level synthesis in progress, 22 of 76 jobs
          complete, 7 jobs running.
137     [14:51:51] Block-level synthesis in progress, 26 of 76 jobs
          complete, 4 jobs running.
138     [14:52:29] Block-level synthesis in progress, 26 of 76 jobs
          complete, 4 jobs running.
139     [14:53:11] Block-level synthesis in progress, 26 of 76 jobs
          complete, 8 jobs running.
140     [14:53:48] Block-level synthesis in progress, 28 of 76 jobs
          complete, 6 jobs running.
141     [14:54:33] Block-level synthesis in progress, 28 of 76 jobs
          complete, 6 jobs running.
142     [14:55:10] Block-level synthesis in progress, 29 of 76 jobs
          complete, 7 jobs running.
143     [14:55:56] Block-level synthesis in progress, 31 of 76 jobs
          complete, 5 jobs running.
144     [14:56:34] Block-level synthesis in progress, 31 of 76 jobs
          complete, 6 jobs running.
145     [14:57:19] Block-level synthesis in progress, 31 of 76 jobs
          complete, 8 jobs running.
146     [14:57:55] Block-level synthesis in progress, 32 of 76 jobs
          complete, 7 jobs running.
147     [14:58:42] Block-level synthesis in progress, 32 of 76 jobs
          complete, 7 jobs running.
148     [14:59:22] Block-level synthesis in progress, 32 of 76 jobs
          complete, 8 jobs running.
149     [15:00:07] Block-level synthesis in progress, 34 of 76 jobs
          complete, 6 jobs running.
150     [15:00:47] Block-level synthesis in progress, 34 of 76 jobs
          complete, 6 jobs running.
151     [15:01:32] Block-level synthesis in progress, 35 of 76 jobs
          complete, 7 jobs running.
152     [15:02:10] Block-level synthesis in progress, 35 of 76 jobs
          complete, 7 jobs running.
153     [15:02:55] Block-level synthesis in progress, 35 of 76 jobs
          complete, 8 jobs running.
154     [15:03:32] Block-level synthesis in progress, 35 of 76 jobs
          complete, 8 jobs running.
155     [15:04:23] Block-level synthesis in progress, 37 of 76 jobs
```

```
        complete, 6 jobs running.
156     [15:05:00] Block-level synthesis in progress, 37 of 76 jobs
        complete, 6 jobs running.
157     [15:05:47] Block-level synthesis in progress, 39 of 76 jobs
        complete, 6 jobs running.
158     [15:06:23] Block-level synthesis in progress, 39 of 76 jobs
        complete, 7 jobs running.
159     [15:07:07] Block-level synthesis in progress, 39 of 76 jobs
        complete, 8 jobs running.
160     [15:07:43] Block-level synthesis in progress, 40 of 76 jobs
        complete, 7 jobs running.
161     [15:08:28] Block-level synthesis in progress, 40 of 76 jobs
        complete, 7 jobs running.
162     [15:09:09] Block-level synthesis in progress, 40 of 76 jobs
        complete, 8 jobs running.
163     [15:09:53] Block-level synthesis in progress, 42 of 76 jobs
        complete, 6 jobs running.
164     [15:10:33] Block-level synthesis in progress, 42 of 76 jobs
        complete, 6 jobs running.
165     [15:11:17] Block-level synthesis in progress, 42 of 76 jobs
        complete, 8 jobs running.
166     [15:12:00] Block-level synthesis in progress, 43 of 76 jobs
        complete, 7 jobs running.
167     [15:12:48] Block-level synthesis in progress, 43 of 76 jobs
        complete, 7 jobs running.
168     [15:13:30] Block-level synthesis in progress, 44 of 76 jobs
        complete, 7 jobs running.
169     [15:14:29] Block-level synthesis in progress, 45 of 76 jobs
        complete, 6 jobs running.
170     [15:15:09] Block-level synthesis in progress, 45 of 76 jobs
        complete, 7 jobs running.
171     [15:15:54] Block-level synthesis in progress, 45 of 76 jobs
        complete, 8 jobs running.
172     [15:16:32] Block-level synthesis in progress, 45 of 76 jobs
        complete, 8 jobs running.
173     [15:17:20] Block-level synthesis in progress, 46 of 76 jobs
        complete, 7 jobs running.
174     [15:17:58] Block-level synthesis in progress, 47 of 76 jobs
        complete, 6 jobs running.
175     [15:18:46] Block-level synthesis in progress, 47 of 76 jobs
        complete, 7 jobs running.
```

```
[15:19:24] Block-level synthesis in progress, 48 of 76 jobs complete, 7 jobs running.
[15:20:08] Block-level synthesis in progress, 48 of 76 jobs complete, 7 jobs running.
[15:20:47] Block-level synthesis in progress, 48 of 76 jobs complete, 8 jobs running.
[15:21:32] Block-level synthesis in progress, 49 of 76 jobs complete, 7 jobs running.
[15:22:10] Block-level synthesis in progress, 50 of 76 jobs complete, 6 jobs running.
[15:22:56] Block-level synthesis in progress, 50 of 76 jobs complete, 7 jobs running.
[15:23:34] Block-level synthesis in progress, 51 of 76 jobs complete, 7 jobs running.
[15:24:23] Block-level synthesis in progress, 51 of 76 jobs complete, 7 jobs running.
[15:25:02] Block-level synthesis in progress, 52 of 76 jobs complete, 7 jobs running.
[15:25:46] Block-level synthesis in progress, 52 of 76 jobs complete, 7 jobs running.
[15:26:25] Block-level synthesis in progress, 52 of 76 jobs complete, 8 jobs running.
[15:27:11] Block-level synthesis in progress, 52 of 76 jobs complete, 8 jobs running.
[15:27:52] Block-level synthesis in progress, 53 of 76 jobs complete, 7 jobs running.
[15:28:36] Block-level synthesis in progress, 53 of 76 jobs complete, 7 jobs running.
[15:29:15] Block-level synthesis in progress, 53 of 76 jobs complete, 8 jobs running.
[15:29:59] Block-level synthesis in progress, 53 of 76 jobs complete, 8 jobs running.
[15:30:38] Block-level synthesis in progress, 54 of 76 jobs complete, 7 jobs running.
[15:31:23] Block-level synthesis in progress, 55 of 76 jobs complete, 6 jobs running.
[15:32:01] Block-level synthesis in progress, 56 of 76 jobs complete, 6 jobs running.
[15:32:44] Block-level synthesis in progress, 56 of 76 jobs complete, 7 jobs running.
[15:33:25] Block-level synthesis in progress, 57 of 76 jobs
```

```
        complete, 7 jobs running.
197     [15:34:10] Block-level synthesis in progress, 58 of 76 jobs
        complete, 6 jobs running.
198     [15:34:48] Block-level synthesis in progress, 58 of 76 jobs
        complete, 6 jobs running.
199     [15:35:31] Block-level synthesis in progress, 58 of 76 jobs
        complete, 8 jobs running.
200     [15:36:10] Block-level synthesis in progress, 59 of 76 jobs
        complete, 7 jobs running.
201     [15:36:54] Block-level synthesis in progress, 60 of 76 jobs
        complete, 6 jobs running.
202     [15:37:34] Block-level synthesis in progress, 61 of 76 jobs
        complete, 6 jobs running.
203     [15:38:19] Block-level synthesis in progress, 62 of 76 jobs
        complete, 6 jobs running.
204     [15:38:58] Block-level synthesis in progress, 62 of 76 jobs
        complete, 7 jobs running.
205     [15:39:41] Block-level synthesis in progress, 63 of 76 jobs
        complete, 7 jobs running.
206     [15:40:20] Block-level synthesis in progress, 63 of 76 jobs
        complete, 7 jobs running.
207     [15:41:05] Block-level synthesis in progress, 65 of 76 jobs
        complete, 6 jobs running.
208     [15:41:45] Block-level synthesis in progress, 67 of 76 jobs
        complete, 4 jobs running.
209     [15:42:29] Block-level synthesis in progress, 67 of 76 jobs
        complete, 6 jobs running.
210     [15:43:07] Block-level synthesis in progress, 68 of 76 jobs
        complete, 5 jobs running.
211     [15:43:54] Block-level synthesis in progress, 69 of 76 jobs
        complete, 4 jobs running.
212     [15:44:33] Block-level synthesis in progress, 69 of 76 jobs
        complete, 4 jobs running.
213     [15:45:20] Block-level synthesis in progress, 69 of 76 jobs
        complete, 5 jobs running.
214     [15:45:58] Block-level synthesis in progress, 70 of 76 jobs
        complete, 4 jobs running.
215     [15:46:45] Block-level synthesis in progress, 72 of 76 jobs
        complete, 2 jobs running.
216     [15:47:25] Block-level synthesis in progress, 72 of 76 jobs
        complete, 3 jobs running.
```

```
217     [15:48:11] Block-level synthesis in progress, 73 of 76 jobs
          complete, 2 jobs running.
218     [15:48:50] Block-level synthesis in progress, 73 of 76 jobs
          complete, 2 jobs running.
219     [15:49:38] Block-level synthesis in progress, 73 of 76 jobs
          complete, 2 jobs running.
220     [15:50:17] Block-level synthesis in progress, 73 of 76 jobs
          complete, 2 jobs running.
221     [15:51:05] Block-level synthesis in progress, 74 of 76 jobs
          complete, 1 job running.
222     [15:51:44] Block-level synthesis in progress, 74 of 76 jobs
          complete, 1 job running.
223     [15:52:30] Block-level synthesis in progress, 74 of 76 jobs
          complete, 2 jobs running.
224     [15:53:09] Block-level synthesis in progress, 74 of 76 jobs
          complete, 2 jobs running.
225     [15:53:56] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
226     [15:54:36] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
227     [15:55:23] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
228     [15:56:03] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
229     [15:56:50] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
230     [15:57:30] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
231     [15:58:17] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
232     [15:58:57] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
233     [15:59:44] Block-level synthesis in progress, 75 of 76 jobs
          complete, 1 job running.
234     [16:00:25] Block-level synthesis in progress, 76 of 76 jobs
          complete, 0 jobs running.
235     [16:01:12] Block-level synthesis in progress, 76 of 76 jobs
          complete, 0 jobs running.
236     [16:01:51] Top-level synthesis in progress.
237     [16:02:37] Top-level synthesis in progress.
238     [16:03:17] Top-level synthesis in progress.
```

```
239     [16:04:05] Top-level synthesis in progress.
240     [16:04:45] Top-level synthesis in progress.
241     [16:05:32] Top-level synthesis in progress.
242     [16:06:12] Top-level synthesis in progress.
243     [16:06:59] Top-level synthesis in progress.
244     [16:07:39] Top-level synthesis in progress.
245     [16:08:25] Top-level synthesis in progress.
246     [16:09:05] Top-level synthesis in progress.
247     [16:09:53] Top-level synthesis in progress.
248     [16:10:33] Top-level synthesis in progress.
249     [16:11:19] Top-level synthesis in progress.
250     [16:12:00] Top-level synthesis in progress.
251     [16:12:47] Top-level synthesis in progress.
252     [16:13:28] Top-level synthesis in progress.
253     [16:14:14] Top-level synthesis in progress.
254     [16:14:55] Run vpl: Step synth: Completed
255     [16:14:55] Run vpl: Step impl: Started
256     [17:21:17] Finished 2nd of 6 tasks (FPGA linking synthesized
          kernels to platform). Elapsed time: 03h 35m 19s
257
258     [17:21:17] Starting logic optimization..
259     [17:28:46] Phase 1 Generate And Synthesize MIG Cores
260     [18:06:40] Phase 2 Generate And Synthesize Debug Cores
261     [18:39:02] Phase 3 Retarget
262     [18:42:09] Phase 4 Constant propagation
263     [18:43:40] Phase 5 Sweep
264     [18:48:13] Phase 6 BUFG optimization
265     [18:50:31] Phase 7 Shift Register Optimization
266     [18:51:23] Phase 8 Post Processing Netlist
267     [19:05:36] Finished 3rd of 6 tasks (FPGA logic optimization).
          Elapsed time: 01h 44m 19s
268
269     [19:05:36] Starting logic placement..
270     [19:13:05] Phase 1 Placer Initialization
271     [19:13:05] Phase 1.1 Placer Initialization Netlist Sorting
272     [19:24:00] Phase 1.2 IO Placement/ Clock Placement/ Build Placer
          Device
273     [19:33:45] Phase 1.3 Build Placer Netlist Model
274     [19:48:26] Phase 1.4 Constrain Clocks/Macros
275     [19:49:37] Phase 2 Global Placement
276     [19:49:37] Phase 2.1 Floorplanning
```

```
277     [19:52:57] Phase 2.1.1 Partition Driven Placement
278     [19:54:10] Phase 2.1.1.1 PBP: Partition Driven Placement
279     [19:56:29] Phase 2.1.1.2 PBP: Clock Region Placement
280     [20:02:10] Phase 2.1.1.3 PBP: Compute Congestion
281     [20:03:00] Phase 2.1.1.4 PBP: UpdateTiming
282     [20:04:57] Phase 2.1.1.5 PBP: Add part constraints
283     [20:06:31] Phase 2.2 Update Timing before SLR Path Opt
284     [20:07:16] Phase 2.3 Global Placement Core
285     [20:37:16] Phase 2.3.1 Physical Synthesis In Placer
286     [20:53:43] Phase 3 Detail Placement
287     [20:53:43] Phase 3.1 Commit Multi Column Macros
288     [20:54:25] Phase 3.2 Commit Most Macros & LUTRAMs
289     [21:01:25] Phase 3.3 Small Shape DP
290     [21:01:25] Phase 3.3.1 Small Shape Clustering
291     [21:04:30] Phase 3.3.2 Flow Legalize Slice Clusters
292     [21:04:30] Phase 3.3.3 Slice Area Swap
293     [21:11:21] Phase 3.4 Place Remaining
294     [21:12:11] Phase 3.5 Re-assign LUT pins
295     [21:14:31] Phase 3.6 Pipeline Register Optimization
296     [21:14:31] Phase 3.7 Fast Optimization
297     [21:19:53] Phase 4 Post Placement Optimization and Clean-Up
298     [21:19:53] Phase 4.1 Post Commit Optimization
299     [21:31:42] Phase 4.1.1 Post Placement Optimization
300     [21:32:36] Phase 4.1.1.1 BUFG Insertion
301     [21:32:36] Phase 1 Physical Synthesis Initialization
302     [21:35:44] Phase 4.1.1.2 BUFG Replication
303     [21:37:58] Phase 4.1.1.3 Replication
304     [21:45:40] Phase 4.2 Post Placement Cleanup
305     [21:46:34] Phase 4.3 Placer Reporting
306     [21:46:34] Phase 4.3.1 Print Estimated Congestion
307     [21:48:06] Phase 4.4 Final Placement Cleanup
308     [23:11:30] Finished 4th of 6 tasks (FPGA logic placement). Elapsed
          time: 04h 05m 54s
309
310     [23:11:30] Starting logic routing..
311     [23:17:48] Phase 1 Build RT Design
312     [23:29:35] Phase 2 Router Initialization
313     [23:30:20] Phase 2.1 Fix Topology Constraints
314     [23:30:20] Phase 2.2 Pre Route Cleanup
315     [23:31:12] Phase 2.3 Global Clock Net Routing
316     [23:34:27] Phase 2.4 Update Timing
```

```
317     [23:50:21] Phase 2.5 Update Timing for Bus Skew
318     [23:50:21] Phase 2.5.1 Update Timing
319     [23:55:51] Phase 3 Initial Routing
320     [23:55:51] Phase 3.1 Global Routing
321     [00:01:38] Phase 4 Rip-up And Reroute
322     [00:01:38] Phase 4.1 Global Iteration 0
323     [00:26:30] Phase 4.2 Global Iteration 1
324     [00:42:54] Phase 4.3 Global Iteration 2
325     [00:49:50] Phase 5 Delay and Skew Optimization
326     [00:49:50] Phase 5.1 Delay CleanUp
327     [00:49:50] Phase 5.1.1 Update Timing
328     [00:57:25] Phase 5.2 Clock Skew Optimization
329     [00:58:06] Phase 6 Post Hold Fix
330     [00:58:06] Phase 6.1 Hold Fix Iter
331     [00:58:06] Phase 6.1.1 Update Timing
332     [01:05:00] Phase 7 Route finalize
333     [01:05:00] Phase 8 Verifying routed nets
334     [01:06:36] Phase 9 Depositing Routes
335     [01:11:24] Phase 10 Route finalize
336     [01:11:24] Phase 11 Post Router Timing
337     [01:19:46] Finished 5th of 6 tasks (FPGA routing). Elapsed time:
          02h 08m 16s
338
339     [01:19:46] Starting bitstream generation..
340     [03:21:47] Creating bitmap...
341     [04:13:14] Writing bitstream
          ./pfm_top_i_dynamic_region_my_rm_partial.bit...
342     [04:13:14] Finished 6th of 6 tasks (FPGA bitstream generation).
          Elapsed time: 02h 53m 27s
343     [04:18:56] Run vpl: Step impl: Completed
344     [04:19:10] Run vpl: FINISHED. Run Status: impl Complete!
345     INFO: [v++ 60-1441] [04:19:53] Run run_link: Step vpl: Completed
346     Time (s): cpu = 00:59:51 ; elapsed = 14:34:08 . Memory (MB): peak =
          1585.129 ; gain = 0.000 ; free physical = 137289 ; free virtual
          = 172885
347     INFO: [v++ 60-1443] [04:19:53] Run run_link: Step rtdgen: Started
348     INFO: [v++ 60-1453] Command Line: rtdgen
349     INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
350     INFO: [v++ 60-991] clock name 'clkwiz_kernel_clk_out1' (clock ID
          '0') is being mapped to clock name 'DATA_CLK' in the xclbin
351     INFO: [v++ 60-991] clock name 'clkwiz_kernel2_clk_out1' (clock ID
```

```
    '1') is being mapped to clock name 'KERNEL_CLK' in the xclbin
352 INFO: [v++ 60-1230] The compiler selected the following frequencies
    for the runtime controllable kernel clock(s) and scalable system
    clock(s): Kernel (DATA) clock: clkwiz_kernel_clk_out1 = 300,
    Kernel (KERNEL) clock: clkwiz_kernel2_clk_out1 = 500
353 INFO: [v++ 60-1453] Command Line: cf2sw -a
    /iu_home/iu7036/_x/link/int/address_map.xml -sdsl
    /iu_home/iu7036/_x/link/int/sdsl.dat -xclbin
    /iu_home/iu7036/_x/link/int/xclbin_orig.xml -rtd
    /iu_home/iu7036/_x/link/int/vinc.rtd -o
    /iu_home/iu7036/_x/link/int/vinc.xml
354 INFO: [v++ 60-1652] Cf2sw returned exit code: 0
355 INFO: [v++ 60-2311]
    HPISystemDiagram::writeSystemDiagramAfterRunningVivado,
    rtdInputFilePath: /iu_home/iu7036/_x/link/int/vinc.rtd
356 INFO: [v++ 60-2312]
    HPISystemDiagram::writeSystemDiagramAfterRunningVivado,
    systemDiagramOutputFilePath:
    /iu_home/iu7036/_x/link/int/systemDiagramModelSlrBaseAddress.json
357 INFO: [v++ 60-1618] Launching
358 INFO: [v++ 60-1441] [04:20:13] Run run_link: Step rtdgen: Completed
359 Time (s): cpu = 00:00:18 ; elapsed = 00:00:20 . Memory (MB): peak =
    1585.129 ; gain = 0.000 ; free physical = 137288 ; free virtual
    = 172885
360 INFO: [v++ 60-1443] [04:20:13] Run run_link: Step xclbinutil:
    Started
361 INFO: [v++ 60-1453] Command Line: xclbinutil --add-section
    DEBUG_IP_LAYOUT:JSON:/iu_home/iu7036/_x/link/int/debug_ip_layout.rtd
    --add-section
    BITSTREAM:RAW:/iu_home/iu7036/_x/link/int/partial.bit --force
    --target hw --key-value SYS:dfx_enable:true --add-section
    :JSON:/iu_home/iu7036/_x/link/int/vinc.rtd --append-section
    :JSON:/iu_home/iu7036/_x/link/int/appendSection.rtd
    --add-section
    CLOCK_FREQ_TOPOLOGY:JSON:/iu_home/iu7036/_x/link/int/vinc_xml.rtd
    --add-section
    BUILD_METADATA:JSON:/iu_home/iu7036/_x/link/int/vinc_build.rtd
    --add-section
    EMBEDDED_METADATA:RAW:/iu_home/iu7036/_x/link/int/vinc.xml
    --add-section
    SYSTEM_METADATA:RAW:/iu_home/iu7036/_x/link/int/systemDiagramModelSlrE
```

```
    --output /iu_home/iu7036/workspace/zayts/vinc.xclbin
INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
XRT Build Version: 2.8.743 (2020.2)
Build Date: 2020-11-16 00:19:11
Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
Creating a default 'in-memory' xclbin image.

Section: 'DEBUG_IP_LAYOUT'(9) was successfully added.
Size   : 440 bytes
Format : JSON
File   : '/iu_home/iu7036/_x/link/int/debug_ip_layout.rtd'

Section: 'BITSTREAM'(0) was successfully added.
Size   : 44676646 bytes
Format : RAW
File   : '/iu_home/iu7036/_x/link/int/partial.bit'

Section: 'MEM_TOPOLOGY'(6) was successfully added.
Format : JSON
File   : 'mem_topology'

Section: 'IP_LAYOUT'(8) was successfully added.
Format : JSON
File   : 'ip_layout'

Section: 'CONNECTIVITY'(7) was successfully added.
Format : JSON
File   : 'connectivity'

Section: 'CLOCK_FREQ_TOPOLOGY'(11) was successfully added.
Size   : 274 bytes
Format : JSON
File   : '/iu_home/iu7036/_x/link/int/vinc_xml.rtd'

Section: 'BUILD_METADATA'(14) was successfully added.
Size   : 3100 bytes
Format : JSON
File   : '/iu_home/iu7036/_x/link/int/vinc_build.rtd'

Section: 'EMBEDDED_METADATA'(2) was successfully added.
Size   : 3182 bytes
```

```
402     Format : RAW
403     File   : '/iu_home/iu7036/_x/link/int/vinc.xml'
404
405     Section: 'SYSTEM_METADATA'(22) was successfully added.
406     Size   : 6310 bytes
407     Format : RAW
408     File   :
           '/iu_home/iu7036/_x/link/int/systemDiagramModelSlrBaseAddress.json'
409
410     Section: 'IP_LAYOUT'(8) was successfully appended to.
411     Format : JSON
412     File   : 'ip_layout'
413     Successfully wrote (44700519 bytes) to the output file:
           /iu_home/iu7036/workspace/zayts/vinc.xclbin
414     Leaving xclbinutil.
415     INFO: [v++ 60-1441] [04:20:15] Run run_link: Step xclbinutil:
           Completed
416     Time (s): cpu = 00:00:00.76 ; elapsed = 00:00:03 . Memory (MB):
           peak = 1585.129 ; gain = 0.000 ; free physical = 137174 ; free
           virtual = 172856
417     INFO: [v++ 60-1443] [04:20:15] Run run_link: Step xclbinutilinfo:
           Started
418     INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info
           /iu_home/iu7036/workspace/zayts/vinc.xclbin.info --input
           /iu_home/iu7036/workspace/zayts/vinc.xclbin
419     INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
420     INFO: [v++ 60-1441] [04:20:20] Run run_link: Step xclbinutilinfo:
           Completed
421     Time (s): cpu = 00:00:04 ; elapsed = 00:00:05 . Memory (MB): peak =
           1585.129 ; gain = 0.000 ; free physical = 137197 ; free virtual
           = 172879
422     INFO: [v++ 60-1443] [04:20:20] Run run_link: Step
           generate_sc_driver: Started
423     INFO: [v++ 60-1453] Command Line:
424     INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
425     INFO: [v++ 60-1441] [04:20:20] Run run_link: Step
           generate_sc_driver: Completed
426     Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.07 . Memory (MB):
           peak = 1585.129 ; gain = 0.000 ; free physical = 137196 ; free
           virtual = 172878
427     INFO: [v++ 60-244] Generating system estimate report...
```

```
428     INFO: [v++ 60-1092] Generated system estimate report:
          /iu_home/iu7036/_x/reports/link/system_estimate_vinc.xtxt
429     INFO: [v++ 60-586] Created /iu_home/iu7036/workspace/zayts/vinc.ltx
430     INFO: [v++ 60-586] Created
          /iu_home/iu7036/workspace/zayts/vinc.xclbin
431     INFO: [v++ 60-1307] Run completed. Additional information can be
          found in:
432     Guidance:
          /iu_home/iu7036/_x/reports/link/v++_link_vinc_guidance.html
433     Timing Report:
          /iu_home/iu7036/_x/reports/link/imp/impl_1_xilinx_u200_xdma_201830_2_
434     Vivado Log: /iu_home/iu7036/_x/logs/link/vivado.log
435     Steps Log File: /iu_home/iu7036/_x/logs/link/link.steps.log
436
437     INFO: [v++ 60-2343] Use the vitis_analyzer tool to visualize and
          navigate the relevant reports. Run the following command.
438     vitis_analyzer
          /iu_home/iu7036/workspace/zayts/vinc.xclbin.link_summary
439     INFO: [v++ 60-791] Total elapsed time: 14h 38m 41s
440     INFO: [v++ 60-1653] Closing dispatch client.
```

Листинг 2.5 – Содержимое файла vinc.xclbin.info для измененного проекта

```
1
2       ==========================================================
3       XRT Build Version: 2.8.743 (2020.2)
4       Build Date: 2020-11-16 00:19:11
5       Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
6       ==========================================================
7       xclbin Information
8       ------------------
9       Generated by:           v++ (2020.2) on 2020-11-18-05:13:29
10      Version:                2.8.743
11      Kernels:                rtl_kernel_wizard_2
12      Signature:
13      Content:                Bitstream
14      UUID (xclbin):          7169bb39-e284-40f9-8b54-7d7eefa39744
15      Sections:               DEBUG_IP_LAYOUT, BITSTREAM, MEM_TOPOLOGY,
          IP_LAYOUT,
16      CONNECTIVITY, CLOCK_FREQ_TOPOLOGY, BUILD_METADATA,
17      EMBEDDED_METADATA, SYSTEM_METADATA,
18      GROUP_CONNECTIVITY, GROUP_TOPOLOGY
```

```
==========
Hardware Platform (Shell) Information
--------------------------------------------------
Vendor:                   xilinx
Board:                    u200
Name:                     xdma
Version:                  201830.2
Generated Version:        Vivado 2018.3 (SW Build: 2568420)
Created:                  Tue Jun 25 06:55:20 2019
FPGA Device:              xcu200
Board Vendor:             xilinx.com
Board Name:               xilinx.com:au200:1.0
Board Part:               xilinx.com:au200:part0:1.0
Platform VBNV:            xilinx_u200_xdma_201830_2
Static UUID:              c102e7af-b2b8-4381-992b-9a00cc3863eb
Feature ROM TimeStamp:    1561465320

Clocks
------
Name:       DATA_CLK
Index:      0
Type:       DATA
Frequency:  300 MHz

Name:       KERNEL_CLK
Index:      1
Type:       KERNEL
Frequency:  500 MHz

Memory Configuration
--------------------
Name:           bank0
Index:          0
Type:           MEM_DDR4
Base Address:   0x4000000000
Address Size:   0x400000000
Bank Used:      No

Name:           bank1
Index:          1
Type:           MEM_DDR4
```

```
    Base Address: 0x5000000000
    Address Size: 0x400000000
    Bank Used:    Yes

    Name:         bank2
    Index:        2
    Type:         MEM_DDR4
    Base Address: 0x6000000000
    Address Size: 0x400000000
    Bank Used:    No

    Name:         bank3
    Index:        3
    Type:         MEM_DDR4
    Base Address: 0x7000000000
    Address Size: 0x400000000
    Bank Used:    No

    Name:         PLRAM[0]
    Index:        4
    Type:         MEM_DRAM
    Base Address: 0x3000000000
    Address Size: 0x20000
    Bank Used:    No

    Name:         PLRAM[1]
    Index:        5
    Type:         MEM_DRAM
    Base Address: 0x3000200000
    Address Size: 0x20000
    Bank Used:    No

    Name:         PLRAM[2]
    Index:        6
    Type:         MEM_DRAM
    Base Address: 0x3000400000
    Address Size: 0x20000
    Bank Used:    No
    ================================================================================
    Kernel: rtl_kernel_wizard_2

```

```
Definition
----------
Signature: rtl_kernel_wizard_2 (uint scalar00, int* axi00_ptr0)

Ports
-----
Port:           s_axi_control
Mode:           slave
Range (bytes): 0x1000
Data Width:     32 bits
Port Type:      addressable

Port:           m00_axi
Mode:           master
Range (bytes): 0xFFFFFFFFFFFFFFFF
Data Width:     512 bits
Port Type:      addressable

---------------------------
Instance:         vinc0
Base Address: 0x1800000

Argument:           scalar00
Register Offset:    0x010
Port:               s_axi_control
Memory:             <not applicable>

Argument:           axi00_ptr0
Register Offset:    0x018
Port:               m00_axi
Memory:             bank1 (MEM_DDR4)

---------------------------
Instance:         vinc1
Base Address: 0x1810000

Argument:           scalar00
Register Offset:    0x010
Port:               s_axi_control
Memory:             <not applicable>
```

```
142 Argument:          axi00_ptr0
143 Register Offset:   0x018
144 Port:              m00_axi
145 Memory:            bank1 (MEM_DDR4)
146 ================================================================
147 Generated By
148 ------------
149 Command:       v++
150 Version:       2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)
151 Command Line:  v++ --config
    /iu_home/iu7036/workspace/zayts/zayts_project2.cfg
    --connectivity.nk rtl_kernel_wizard_2:2:vinc0.vinc1
    --connectivity.slr vinc0:SLR1 --connectivity.sp
    vinc0.m00_axi:DDR[1] --input_files
    /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
    --link --optimize 0 --output
    /iu_home/iu7036/workspace/zayts/vinc.xclbin --platform
    xilinx_u200_xdma_201830_2 --report_level 0 --target hw
    --vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
    --vivado.prop
    run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
    --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
    --vivado.prop
    run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
    --vivado.prop
    run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
152 Options:       --config
    /iu_home/iu7036/workspace/zayts/zayts_project2.cfg
153 --connectivity.nk rtl_kernel_wizard_2:2:vinc0.vinc1
154 --connectivity.slr vinc0:SLR1
155 --connectivity.sp vinc0.m00_axi:DDR[1]
156 --input_files
    /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
157 --link
158 --optimize 0
159 --output /iu_home/iu7036/workspace/zayts/vinc.xclbin
160 --platform xilinx_u200_xdma_201830_2
161 --report_level 0
162 --target hw
163 --vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
164 --vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
```

```
165     --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
166     --vivado.prop
            run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
167     --vivado.prop run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
168     ================================================================================
169     User Added Key Value Pairs
170     ------------------------------
171     <empty>
172     ================================================================================
```

Листинг 2.6 – Содержимое файла v++_vinc.log для измененного проекта

```
1     INFO: [v++ 60-1306] Additional information associated with this v++
          link can be found at:
2     Reports: /iu_home/iu7036/_x/reports/link
3     Log files: /iu_home/iu7036/_x/logs/link
4     INFO: [v++ 60-1548] Creating build summary session with primary
          output /iu_home/iu7036/workspace/zayts/vinc.xclbin.link_summary,
          at Mon Nov 22 21:12:49 2021
5     INFO: [v++ 60-1316] Initiating connection to rulecheck server, at
          Mon Nov 22 21:12:50 2021
6     INFO: [v++ 60-1315] Creating rulecheck session with output
          '/iu_home/iu7036/_x/reports/link/v++_link_vinc_guidance.html',
          at Mon Nov 22 21:13:08 2021
7     INFO: [v++ 60-895]   Target platform:
          /opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_20183
8     INFO: [v++ 60-1578]   This platform contains Device Support Archive
          '/opt/xilinx/platforms/xilinx_u200_xdma_201830_2/hw/xilinx_u200_xdma_2
9     INFO: [v++ 74-74] Compiler Version string: 2020.2
10    INFO: [v++ 60-1302] Platform 'xilinx_u200_xdma_201830_2.xpfm' has
          been explicitly enabled for this release.
11    INFO: [v++ 60-629] Linking for hardware target
12    INFO: [v++ 60-423]   Target device: xilinx_u200_xdma_201830_2
13    INFO: [v++ 60-1332] Run 'run_link' status: Not started
14    INFO: [v++ 60-1443] [21:14:14] Run run_link: Step system_link:
          Started
15    INFO: [v++ 60-1453] Command Line: system_link --xo
          /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
          --config /iu_home/iu7036/_x/link/int/syslinkConfig.ini --xpfm
          /opt/xilinx/platforms/xilinx_u200_xdma_201830_2/xilinx_u200_xdma_20183
          --target hw --output_dir /iu_home/iu7036/_x/link/int --temp_dir
          /iu_home/iu7036/_x/link/sys_link
```

```
16    INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
17    INFO: [SYSTEM_LINK 60-1316] Initiating connection to rulecheck
         server, at Mon Nov 22 21:14:30 2021
18    INFO: [SYSTEM_LINK 82-70] Extracting xo v3 file
         /iu_home/iu7036/workspace/zayts/zayts_project_kernels/src/vitis_rtl_ke
19    INFO: [SYSTEM_LINK 82-53] Creating IP database
         /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
20    INFO: [SYSTEM_LINK 82-38] [21:14:33] build_xd_ip_db started:
         /data/Xilinx/Vitis/2020.2/bin/build_xd_ip_db -ip_search 0
         -sds-pf
         /iu_home/iu7036/_x/link/sys_link/xilinx_u200_xdma_201830_2.hpfm
         -clkid 0 -ip
         /iu_home/iu7036/_x/link/sys_link/iprepo/mycompany_com_kernel_rtl_kernel
         -o /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
21    INFO: [SYSTEM_LINK 82-37] [21:15:09] build_xd_ip_db finished
         successfully
22    Time (s): cpu = 00:00:37 ; elapsed = 00:00:36 . Memory (MB): peak =
         1557.895 ; gain = 0.000 ; free physical = 122364 ; free virtual
         = 156431
23    INFO: [SYSTEM_LINK 82-51] Create system connectivity graph
24    INFO: [SYSTEM_LINK 82-102] Applying explicit connections to the
         system connectivity graph:
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml
25    INFO: [SYSTEM_LINK 82-38] [21:15:10] cfgen started:
         /data/Xilinx/Vitis/2020.2/bin/cfgen  -nk
         rtl_kernel_wizard_2:2:vinc0.vinc1 -slr vinc0:SLR1 -sp
         vinc0.m00_axi:DDR[1] -dmclkid 0 -r
         /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml -o
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml
26    INFO: [CFGEN 83-0] Kernel Specs:
27    INFO: [CFGEN 83-0]   kernel: rtl_kernel_wizard_2, num: 2  {vinc0
         vinc1}
28    INFO: [CFGEN 83-0] Port Specs:
29    INFO: [CFGEN 83-0]   kernel: vinc0, k_port: m00_axi, sptag: DDR[1]
30    INFO: [CFGEN 83-0] SLR Specs:
31    INFO: [CFGEN 83-0]   instance: vinc0, SLR: SLR1
32    INFO: [CFGEN 83-2228] Creating mapping for argument
         vinc0.axi00_ptr0 to DDR[1] for directive vinc0.m00_axi:DDR[1]
33    INFO: [CFGEN 83-2226] Inferring mapping for argument
         vinc1.axi00_ptr0 to DDR[1]
34    INFO: [SYSTEM_LINK 82-37] [21:15:43] cfgen finished successfully
```

```
35    Time (s): cpu = 00:00:32 ; elapsed = 00:00:33 . Memory (MB): peak =
         1557.895 ; gain = 0.000 ; free physical = 122290 ; free virtual
         = 156373
36    INFO: [SYSTEM_LINK 82-52] Create top-level block diagram
37    INFO: [SYSTEM_LINK 82-38] [21:15:43] cf2bd started:
         /data/Xilinx/Vitis/2020.2/bin/cf2bd --linux --trace_buffer 1024
         --input_file
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml
         --ip_db /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
         --cf_name dr --working_dir
         /iu_home/iu7036/_x/link/sys_link/_sysl/.xsd --temp_dir
         /iu_home/iu7036/_x/link/sys_link --output_dir
         /iu_home/iu7036/_x/link/int --target_bd pfm_dynamic.bd
38    INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer
         1024 -i
         /iu_home/iu7036/_x/link/sys_link/cfgraph/cfgen_cfgraph.xml -r
         /iu_home/iu7036/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml -o
         dr.xml
39    INFO: [CF2BD 82-28] cf2xd finished successfully
40    INFO: [CF2BD 82-31] Launching cf_xsd: cf_xsd -disable-address-gen
         -bd pfm_dynamic.bd -dn dr -dp
         /iu_home/iu7036/_x/link/sys_link/_sysl/.xsd
41    INFO: [CF2BD 82-28] cf_xsd finished successfully
42    INFO: [SYSTEM_LINK 82-37] [21:16:02] cf2bd finished successfully
43    Time (s): cpu = 00:00:17 ; elapsed = 00:00:19 . Memory (MB): peak =
         1557.895 ; gain = 0.000 ; free physical = 122278 ; free virtual
         = 156350
44    INFO: [v++ 60-1441] [21:16:02] Run run_link: Step system_link:
         Completed
45    Time (s): cpu = 00:01:46 ; elapsed = 00:01:48 . Memory (MB): peak =
         1585.129 ; gain = 0.000 ; free physical = 122333 ; free virtual
         = 156400
46    INFO: [v++ 60-1443] [21:16:02] Run run_link: Step cf2sw: Started
47    INFO: [v++ 60-1453] Command Line: cf2sw -sdsl
         /iu_home/iu7036/_x/link/int/sdsl.dat -rtd
         /iu_home/iu7036/_x/link/int/cf2sw.rtd -nofilter
         /iu_home/iu7036/_x/link/int/cf2sw_full.rtd -xclbin
         /iu_home/iu7036/_x/link/int/xclbin_orig.xml -o
         /iu_home/iu7036/_x/link/int/xclbin_orig.1.xml
48    INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
49    INFO: [v++ 60-1441] [21:16:24] Run run_link: Step cf2sw: Completed
```

```
50    Time (s): cpu = 00:00:21 ; elapsed = 00:00:22 . Memory (MB): peak =
         1585.129 ; gain = 0.000 ; free physical = 122352 ; free virtual
         = 156421
51    INFO: [v++ 60-1443] [21:16:24] Run run_link: Step
         rtd2_system_diagram: Started
52    INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram
53    INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
54    INFO: [v++ 60-1441] [21:16:36] Run run_link: Step
         rtd2_system_diagram: Completed
55    Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:11 . Memory (MB):
         peak = 1585.129 ; gain = 0.000 ; free physical = 121721 ; free
         virtual = 155789
56    INFO: [v++ 60-1443] [21:16:36] Run run_link: Step vpl: Started
57    INFO: [v++ 60-1453] Command Line: vpl -t hw -f
         xilinx_u200_xdma_201830_2 --remote_ip_cache
         /iu_home/iu7036/.ipcache --output_dir
         /iu_home/iu7036/_x/link/int --log_dir
         /iu_home/iu7036/_x/logs/link --report_dir
         /iu_home/iu7036/_x/reports/link --config
         /iu_home/iu7036/_x/link/int/vplConfig.ini -k
         /iu_home/iu7036/_x/link/int/kernel_info.dat --webtalk_flag Vitis
         --temp_dir /iu_home/iu7036/_x/link --no-info --iprepo
         /iu_home/iu7036/_x/link/int/xo/ip_repo/mycompany_com_kernel_rtl_kernel_
         --messageDb /iu_home/iu7036/_x/link/run_link/vpl.pb
         /iu_home/iu7036/_x/link/int/dr.bd.tcl
58    INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
59
60    ****** vpl v2020.2 (64-bit)
61    **** SW Build (by xbuild) on 2020-11-18-05:13:29
62    ** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.
63
64    INFO: [VPL 60-839] Read in kernel information from file
         '/iu_home/iu7036/_x/link/int/kernel_info.dat'.
65    INFO: [VPL 74-74] Compiler Version string: 2020.2
66    INFO: [VPL 60-423]   Target device: xilinx_u200_xdma_201830_2
67    INFO: [VPL 60-1032] Extracting hardware platform to
         /iu_home/iu7036/_x/link/vivado/vpl/.local/hw_platform
68    WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not
         exist.
69    [21:24:01] Run vpl: Step create_project: RUNNING...
70    [21:23:47] Run vpl: Step create_project: Started
```

```
71      Creating Vivado project.
72      [21:24:23] Run vpl: Step create_project: Completed
73      [21:24:23] Run vpl: Step create_bd: Started
74      [21:26:22] Run vpl: Step create_bd: RUNNING...
75      [21:28:28] Run vpl: Step create_bd: RUNNING...
76      [21:30:04] Run vpl: Step create_bd: RUNNING...
77      [21:32:15] Run vpl: Step create_bd: RUNNING...
78      [21:34:04] Run vpl: Step create_bd: RUNNING...
79      [21:35:48] Run vpl: Step create_bd: RUNNING...
80      [21:37:03] Run vpl: Step create_bd: Completed
81      [21:37:03] Run vpl: Step update_bd: Started
82      [21:37:07] Run vpl: Step update_bd: Completed
83      [21:37:07] Run vpl: Step generate_target: Started
84      [21:38:48] Run vpl: Step generate_target: RUNNING...
85      [21:40:39] Run vpl: Step generate_target: RUNNING...
86      [21:42:13] Run vpl: Step generate_target: RUNNING...
87      [21:43:57] Run vpl: Step generate_target: RUNNING...
88      [21:45:32] Run vpl: Step generate_target: RUNNING...
89      [21:45:38] Run vpl: Step generate_target: Completed
90      [21:45:38] Run vpl: Step config_hw_runs: Started
91      [21:46:09] Run vpl: Step config_hw_runs: Completed
92      [21:46:09] Run vpl: Step synth: Started
93      [21:48:19] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
94      [21:48:56] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
95      [21:49:39] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
96      [21:50:18] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
97      [21:50:59] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
98      [21:51:44] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
99      [21:52:25] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
100     [21:53:04] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
101     [21:53:43] Block-level synthesis in progress, 0 of 4 jobs complete,
          3 jobs running.
102     [21:54:22] Block-level synthesis in progress, 0 of 4 jobs complete,
```

```
      3 jobs running.
103   [21:55:07] Block-level synthesis in progress, 0 of 4 jobs complete,
      3 jobs running.
104   [21:55:48] Block-level synthesis in progress, 0 of 4 jobs complete,
      3 jobs running.
105   [21:56:26] Block-level synthesis in progress, 0 of 4 jobs complete,
      3 jobs running.
106   [21:57:05] Block-level synthesis in progress, 0 of 4 jobs complete,
      3 jobs running.
107   [21:57:45] Block-level synthesis in progress, 0 of 4 jobs complete,
      3 jobs running.
108   [21:58:27] Block-level synthesis in progress, 1 of 4 jobs complete,
      2 jobs running.
109   [21:59:08] Block-level synthesis in progress, 1 of 4 jobs complete,
      2 jobs running.
110   [21:59:48] Block-level synthesis in progress, 1 of 4 jobs complete,
      2 jobs running.
111   [22:00:29] Block-level synthesis in progress, 1 of 4 jobs complete,
      2 jobs running.
112   [22:01:07] Block-level synthesis in progress, 1 of 4 jobs complete,
      2 jobs running.
113   [22:01:49] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
114   [22:02:31] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
115   [22:03:13] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
116   [22:03:52] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
117   [22:04:31] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
118   [22:05:09] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
119   [22:05:50] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
120   [22:06:29] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
121   [22:07:09] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
122   [22:07:47] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
```

```
123     [22:08:25] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
124     [22:09:04] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
125     [22:09:43] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
126     [22:10:22] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
127     [22:11:00] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
128     [22:11:37] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
129     [22:12:16] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
130     [22:12:54] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
131     [22:13:31] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
132     [22:14:08] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
133     [22:14:46] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
134     [22:15:24] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
135     [22:16:02] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
136     [22:16:41] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
137     [22:17:21] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
138     [22:18:01] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
139     [22:18:39] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
140     [22:19:19] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
141     [22:20:00] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
142     [22:20:39] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
143     [22:21:19] Block-level synthesis in progress, 2 of 4 jobs complete,
```

```
      1 job running.
144   [22:21:57] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
145   [22:22:38] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
146   [22:24:16] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
147   [22:25:06] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
148   [22:25:50] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
149   [22:29:00] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
150   [22:29:45] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
151   [22:30:23] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
152   [22:31:11] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
153   [22:31:50] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
154   [22:32:36] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
155   [22:33:17] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
156   [22:34:06] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
157   [22:34:46] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
158   [22:35:31] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
159   [22:36:11] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
160   [22:36:57] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
161   [22:37:39] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
162   [22:38:23] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
163   [22:39:03] Block-level synthesis in progress, 2 of 4 jobs complete,
      1 job running.
```

```
164     [22:39:48] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
165     [22:40:28] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
166     [22:41:14] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
167     [22:41:55] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
168     [22:42:43] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
169     [22:43:22] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
170     [22:44:08] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
171     [22:44:49] Block-level synthesis in progress, 2 of 4 jobs complete,
          1 job running.
172     [22:45:35] Block-level synthesis in progress, 3 of 4 jobs complete,
          0 jobs running.
173     [22:46:14] Block-level synthesis in progress, 3 of 4 jobs complete,
          0 jobs running.
174     [22:46:59] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
175     [22:47:37] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
176     [22:48:20] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
177     [22:49:00] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
178     [22:49:42] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
179     [22:50:25] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
180     [22:51:08] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
181     [22:51:49] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
182     [22:52:34] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
183     [22:53:14] Block-level synthesis in progress, 3 of 4 jobs complete,
          1 job running.
184     [22:53:57] Block-level synthesis in progress, 3 of 4 jobs complete,
```

```
    1 job running.
[22:54:36] Block-level synthesis in progress, 3 of 4 jobs complete,
    1 job running.
[22:55:19] Block-level synthesis in progress, 3 of 4 jobs complete,
    1 job running.
[22:55:59] Block-level synthesis in progress, 3 of 4 jobs complete,
    1 job running.
[22:56:43] Block-level synthesis in progress, 3 of 4 jobs complete,
    1 job running.
[22:57:24] Block-level synthesis in progress, 3 of 4 jobs complete,
    1 job running.
[22:58:08] Block-level synthesis in progress, 3 of 4 jobs complete,
    1 job running.
[22:58:49] Block-level synthesis in progress, 3 of 4 jobs complete,
    1 job running.
[22:59:33] Block-level synthesis in progress, 4 of 4 jobs complete,
    0 jobs running.
[23:00:14] Block-level synthesis in progress, 4 of 4 jobs complete,
    0 jobs running.
[23:01:00] Block-level synthesis in progress, 4 of 4 jobs complete,
    0 jobs running.
[23:01:40] Top-level synthesis in progress.
[23:02:25] Top-level synthesis in progress.
[23:03:06] Top-level synthesis in progress.
[23:03:50] Top-level synthesis in progress.
[23:04:32] Top-level synthesis in progress.
[23:05:13] Top-level synthesis in progress.
[23:05:53] Top-level synthesis in progress.
[23:06:34] Top-level synthesis in progress.
[23:07:21] Top-level synthesis in progress.
[23:08:06] Top-level synthesis in progress.
[23:08:49] Top-level synthesis in progress.
[23:09:37] Top-level synthesis in progress.
[23:10:29] Top-level synthesis in progress.
[23:11:09] Top-level synthesis in progress.
[23:11:51] Top-level synthesis in progress.
[23:12:32] Top-level synthesis in progress.
[23:13:27] Run vpl: Step synth: Completed
[23:13:27] Run vpl: Step impl: Started
[00:15:59] Finished 2nd of 6 tasks (FPGA linking synthesized
    kernels to platform). Elapsed time: 02h 59m 09s
```

```
214
215     [00:15:59] Starting logic optimization..
216     [00:24:49] Phase 1 Retarget
217     [00:27:36] Phase 2 Constant propagation
218     [00:28:58] Phase 3 Sweep
219     [00:34:20] Phase 4 BUFG optimization
220     [00:36:19] Phase 5 Shift Register Optimization
221     [00:37:00] Phase 6 Post Processing Netlist
222     [00:53:29] Finished 3rd of 6 tasks (FPGA logic optimization).
          Elapsed time: 00h 37m 30s
223
224     [00:53:29] Starting logic placement..
225     [00:58:25] Phase 1 Placer Initialization
226     [00:58:25] Phase 1.1 Placer Initialization Netlist Sorting
227     [01:14:04] Phase 1.2 IO Placement/ Clock Placement/ Build Placer
          Device
228     [01:23:01] Phase 1.3 Build Placer Netlist Model
229     [01:36:41] Phase 1.4 Constrain Clocks/Macros
230     [01:38:02] Phase 2 Global Placement
231     [01:38:02] Phase 2.1 Floorplanning
232     [01:41:25] Phase 2.1.1 Partition Driven Placement
233     [01:41:25] Phase 2.1.1.1 PBP: Partition Driven Placement
234     [01:42:48] Phase 2.1.1.2 PBP: Clock Region Placement
235     [01:46:58] Phase 2.1.1.3 PBP: Compute Congestion
236     [01:47:40] Phase 2.1.1.4 PBP: UpdateTiming
237     [01:50:21] Phase 2.1.1.5 PBP: Add part constraints
238     [01:51:00] Phase 2.2 Update Timing before SLR Path Opt
239     [01:51:40] Phase 2.3 Global Placement Core
240     [02:13:46] Phase 2.3.1 Physical Synthesis In Placer
241     [02:25:54] Phase 3 Detail Placement
242     [02:25:54] Phase 3.1 Commit Multi Column Macros
243     [02:26:36] Phase 3.2 Commit Most Macros & LUTRAMs
244     [02:32:36] Phase 3.3 Small Shape DP
245     [02:32:36] Phase 3.3.1 Small Shape Clustering
246     [02:33:57] Phase 3.3.2 Flow Legalize Slice Clusters
247     [02:34:38] Phase 3.3.3 Slice Area Swap
248     [02:38:38] Phase 3.4 Place Remaining
249     [02:39:18] Phase 3.5 Re-assign LUT pins
250     [02:40:40] Phase 3.6 Pipeline Register Optimization
251     [02:41:22] Phase 3.7 Fast Optimization
252     [02:46:06] Phase 4 Post Placement Optimization and Clean-Up
```

```
253     [02:46:06] Phase 4.1 Post Commit Optimization
254     [02:56:08] Phase 4.1.1 Post Placement Optimization
255     [02:56:48] Phase 4.1.1.1 BUFG Insertion
256     [02:56:48] Phase 1 Physical Synthesis Initialization
257     [02:59:35] Phase 4.1.1.2 BUFG Replication
258     [03:01:39] Phase 4.1.1.3 Replication
259     [03:08:22] Phase 4.2 Post Placement Cleanup
260     [03:09:46] Phase 4.3 Placer Reporting
261     [03:09:46] Phase 4.3.1 Print Estimated Congestion
262     [03:11:50] Phase 4.4 Final Placement Cleanup
263     [04:29:09] Finished 4th of 6 tasks (FPGA logic placement). Elapsed
            time: 03h 35m 39s
264
265     [04:29:09] Starting logic routing..
266     [04:35:16] Phase 1 Build RT Design
267     [04:46:48] Phase 2 Router Initialization
268     [04:46:48] Phase 2.1 Fix Topology Constraints
269     [04:47:27] Phase 2.2 Pre Route Cleanup
270     [04:48:06] Phase 2.3 Global Clock Net Routing
271     [04:50:47] Phase 2.4 Update Timing
272     [05:04:35] Phase 2.5 Update Timing for Bus Skew
273     [05:04:35] Phase 2.5.1 Update Timing
274     [05:09:59] Phase 3 Initial Routing
275     [05:09:59] Phase 3.1 Global Routing
276     [05:15:20] Phase 4 Rip-up And Reroute
277     [05:15:20] Phase 4.1 Global Iteration 0
278     [05:32:56] Phase 4.2 Global Iteration 1
279     [05:38:53] Phase 4.3 Global Iteration 2
280     [05:43:31] Phase 5 Delay and Skew Optimization
281     [05:43:31] Phase 5.1 Delay CleanUp
282     [05:43:31] Phase 5.1.1 Update Timing
283     [05:50:55] Phase 5.2 Clock Skew Optimization
284     [05:51:34] Phase 6 Post Hold Fix
285     [05:51:34] Phase 6.1 Hold Fix Iter
286     [05:51:34] Phase 6.1.1 Update Timing
287     [05:56:54] Phase 7 Route finalize
288     [05:57:35] Phase 8 Verifying routed nets
289     [05:58:56] Phase 9 Depositing Routes
290     [06:02:52] Phase 10 Route finalize
291     [06:03:31] Phase 11 Post Router Timing
292     [06:10:44] Finished 5th of 6 tasks (FPGA routing). Elapsed time:
```

```
    01h 41m 35s
293
294 [06:10:44] Starting bitstream generation..
295 [08:16:30] Creating bitmap...
296 [09:09:36] Writing bitstream
    ./pfm_top_i_dynamic_region_my_rm_partial.bit...
297 [09:10:17] Finished 6th of 6 tasks (FPGA bitstream generation).
    Elapsed time: 02h 59m 32s
298 [09:14:00] Run vpl: Step impl: Completed
299 [09:14:06] Run vpl: FINISHED. Run Status: impl Complete!
300 INFO: [v++ 60-1441] [09:14:41] Run run_link: Step vpl: Completed
301 Time (s): cpu = 00:25:39 ; elapsed = 11:58:05 . Memory (MB): peak =
    1585.129 ; gain = 0.000 ; free physical = 40554 ; free virtual =
    87405
302 INFO: [v++ 60-1443] [09:14:41] Run run_link: Step rtdgen: Started
303 INFO: [v++ 60-1453] Command Line: rtdgen
304 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
305 INFO: [v++ 60-991] clock name 'clkwiz_kernel_clk_out1' (clock ID
    '0') is being mapped to clock name 'DATA_CLK' in the xclbin
306 INFO: [v++ 60-991] clock name 'clkwiz_kernel2_clk_out1' (clock ID
    '1') is being mapped to clock name 'KERNEL_CLK' in the xclbin
307 INFO: [v++ 60-1230] The compiler selected the following frequencies
    for the runtime controllable kernel clock(s) and scalable system
    clock(s): Kernel (DATA) clock: clkwiz_kernel_clk_out1 = 300,
    Kernel (KERNEL) clock: clkwiz_kernel2_clk_out1 = 500
308 INFO: [v++ 60-1453] Command Line: cf2sw -a
    /iu_home/iu7036/_x/link/int/address_map.xml -sdsl
    /iu_home/iu7036/_x/link/int/sdsl.dat -xclbin
    /iu_home/iu7036/_x/link/int/xclbin_orig.xml -rtd
    /iu_home/iu7036/_x/link/int/vinc.rtd -o
    /iu_home/iu7036/_x/link/int/vinc.xml
309 INFO: [v++ 60-1652] Cf2sw returned exit code: 0
310 INFO: [v++ 60-2311]
    HPISystemDiagram::writeSystemDiagramAfterRunningVivado,
    rtdInputFilePath: /iu_home/iu7036/_x/link/int/vinc.rtd
311 INFO: [v++ 60-2312]
    HPISystemDiagram::writeSystemDiagramAfterRunningVivado,
    systemDiagramOutputFilePath:
    /iu_home/iu7036/_x/link/int/systemDiagramModelSlrBaseAddress.json
312 INFO: [v++ 60-1618] Launching
313 INFO: [v++ 60-1441] [09:14:59] Run run_link: Step rtdgen: Completed
```

```
314     Time (s): cpu = 00:00:17 ; elapsed = 00:00:19 . Memory (MB): peak =
           1585.129 ; gain = 0.000 ; free physical = 40756 ; free virtual =
           87608
315     INFO: [v++ 60-1443] [09:14:59] Run run_link: Step xclbinutil:
           Started
316     INFO: [v++ 60-1453] Command Line: xclbinutil --add-section
           DEBUG_IP_LAYOUT:JSON:/iu_home/iu7036/_x/link/int/debug_ip_layout.rtd
           --add-section
           BITSTREAM:RAW:/iu_home/iu7036/_x/link/int/partial.bit --force
           --target hw --key-value SYS:dfx_enable:true --add-section
           :JSON:/iu_home/iu7036/_x/link/int/vinc.rtd --append-section
           :JSON:/iu_home/iu7036/_x/link/int/appendSection.rtd
           --add-section
           CLOCK_FREQ_TOPOLOGY:JSON:/iu_home/iu7036/_x/link/int/vinc_xml.rtd
           --add-section
           BUILD_METADATA:JSON:/iu_home/iu7036/_x/link/int/vinc_build.rtd
           --add-section
           EMBEDDED_METADATA:RAW:/iu_home/iu7036/_x/link/int/vinc.xml
           --add-section
           SYSTEM_METADATA:RAW:/iu_home/iu7036/_x/link/int/systemDiagramModelSlrE
           --output /iu_home/iu7036/workspace/zayts/vinc.xclbin
317     INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
318     XRT Build Version: 2.8.743 (2020.2)
319     Build Date: 2020-11-16 00:19:11
320     Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
321     Creating a default 'in-memory' xclbin image.
322
323     Section: 'DEBUG_IP_LAYOUT'(9) was successfully added.
324     Size   : 440 bytes
325     Format : JSON
326     File   : '/iu_home/iu7036/_x/link/int/debug_ip_layout.rtd'
327
328     Section: 'BITSTREAM'(0) was successfully added.
329     Size   : 39794726 bytes
330     Format : RAW
331     File   : '/iu_home/iu7036/_x/link/int/partial.bit'
332
333     Section: 'MEM_TOPOLOGY'(6) was successfully added.
334     Format : JSON
335     File   : 'mem_topology'
336
```

```
337     Section: 'IP_LAYOUT'(8) was successfully added.
338     Format : JSON
339     File   : 'ip_layout'
340
341     Section: 'CONNECTIVITY'(7) was successfully added.
342     Format : JSON
343     File   : 'connectivity'
344
345     Section: 'CLOCK_FREQ_TOPOLOGY'(11) was successfully added.
346     Size   : 274 bytes
347     Format : JSON
348     File   : '/iu_home/iu7036/_x/link/int/vinc_xml.rtd'
349
350     Section: 'BUILD_METADATA'(14) was successfully added.
351     Size   : 3101 bytes
352     Format : JSON
353     File   : '/iu_home/iu7036/_x/link/int/vinc_build.rtd'
354
355     Section: 'EMBEDDED_METADATA'(2) was successfully added.
356     Size   : 3182 bytes
357     Format : RAW
358     File   : '/iu_home/iu7036/_x/link/int/vinc.xml'
359
360     Section: 'SYSTEM_METADATA'(22) was successfully added.
361     Size   : 6310 bytes
362     Format : RAW
363     File   :
          '/iu_home/iu7036/_x/link/int/systemDiagramModelSlrBaseAddress.json'
364
365     Section: 'IP_LAYOUT'(8) was successfully appended to.
366     Format : JSON
367     File   : 'ip_layout'
368     Successfully wrote (39818600 bytes) to the output file:
          /iu_home/iu7036/workspace/zayts/vinc.xclbin
369     Leaving xclbinutil.
370     INFO: [v++ 60-1441] [09:15:02] Run run_link: Step xclbinutil:
          Completed
371     Time (s): cpu = 00:00:00.64 ; elapsed = 00:00:03 . Memory (MB):
          peak = 1585.129 ; gain = 0.000 ; free physical = 40743 ; free
          virtual = 87628
372     INFO: [v++ 60-1443] [09:15:02] Run run_link: Step xclbinutilinfo:
```

```
    Started
373 INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info
    /iu_home/iu7036/workspace/zayts/vinc.xclbin.info --input
    /iu_home/iu7036/workspace/zayts/vinc.xclbin
374 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
375 INFO: [v++ 60-1441] [09:15:06] Run run_link: Step xclbinutilinfo:
    Completed
376 Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak =
    1585.129 ; gain = 0.000 ; free physical = 40724 ; free virtual =
    87609
377 INFO: [v++ 60-1443] [09:15:06] Run run_link: Step
    generate_sc_driver: Started
378 INFO: [v++ 60-1453] Command Line:
379 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7036/_x/link/run_link
380 INFO: [v++ 60-1441] [09:15:06] Run run_link: Step
    generate_sc_driver: Completed
381 Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.06 . Memory (MB):
    peak = 1585.129 ; gain = 0.000 ; free physical = 40724 ; free
    virtual = 87609
382 INFO: [v++ 60-244] Generating system estimate report...
383 INFO: [v++ 60-1092] Generated system estimate report:
    /iu_home/iu7036/_x/reports/link/system_estimate_vinc.xtxt
384 INFO: [v++ 60-586] Created /iu_home/iu7036/workspace/zayts/vinc.ltx
385 INFO: [v++ 60-586] Created
    /iu_home/iu7036/workspace/zayts/vinc.xclbin
386 INFO: [v++ 60-1307] Run completed. Additional information can be
    found in:
387 Guidance:
    /iu_home/iu7036/_x/reports/link/v++_link_vinc_guidance.html
388 Timing Report:
    /iu_home/iu7036/_x/reports/link/imp/impl_1_xilinx_u200_xdma_201830_2_
389 Vivado Log: /iu_home/iu7036/_x/logs/link/vivado.log
390 Steps Log File: /iu_home/iu7036/_x/logs/link/link.steps.log
391
392 INFO: [v++ 60-2343] Use the vitis_analyzer tool to visualize and
    navigate the relevant reports. Run the following command.
393 vitis_analyzer
    /iu_home/iu7036/workspace/zayts/vinc.xclbin.link_summary
394 INFO: [v++ 60-791] Total elapsed time: 12h 2m 42s
395 INFO: [v++ 60-1653] Closing dispatch client.
```