

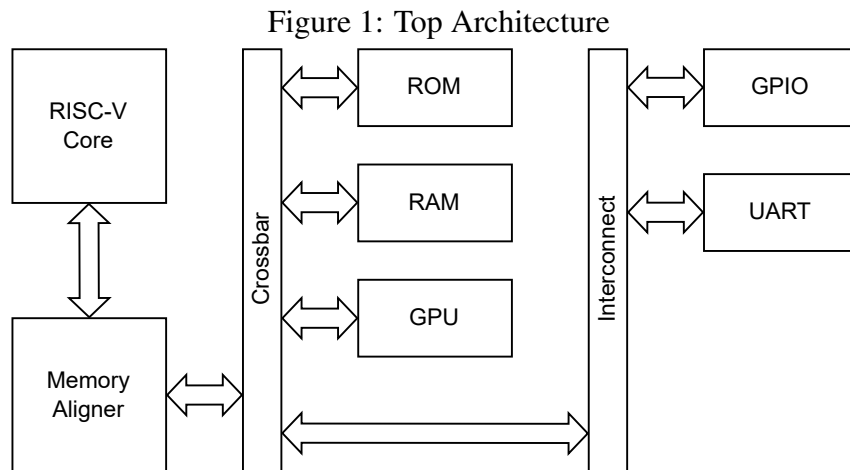
## Project Details

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- Subject: Embedded Systems - Pascal Benoit
- University: Polytech Montpellier
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## Features

- **RISC-V Core:**
  - DIY implementation of the RV32I instruction set architecture (ISA), providing a flexible and customizable processing core.
  - Uses the AXI4-Lite memory interface enabling a seamless interface with different memory devices.
  - Has support for interrupts allowing the implementation of event-driven functionalities.
- **Graphics:**
  - The sprite architecture presented in class, has been enhanced to enable dynamic changes to sprite contents, multiple texture scales, and memory sharing between sprites.
- Fully parametric, has support 80 sprites arranged in 5 clusters in the default configuration.
- **Memory:**
  - 4 kilobytes of ROM: Storing a small bootloader that also performs a quick test of the ISA implementation.
  - 64 kilobytes of RAM: More than sufficient memory capacity to handle game, texture, and world data.
  - 20.48 kilopixels of texture memory: arranged in 5 clusters of sprites.
- **Peripherals:**
  - General Purpose Input/Output (GPIO) that allows the interface of the software with the buttons and switches.
  - Universal asynchronous receiver-transmitter (UART) that provides a communication channel.
- **Build Tools:**
  - The build and flashing process is efficiently automated by a well designed Makefile, simplifying the compilation, texture packaging, world generation, and linking tasks.
  - Support for bulding and flashing via a single command, saving valuable development time and effort.

# Hardware



The top architecture is composed of a RISC-V core, a memory aligner, a crossbar, read-only memory (ROM), random-access memory (RAM) and simple 2D graphics accelerator. Furthermore, the GPIO and UART are classified as peripherals and communicate with the CPU via a simpler interconnect.

Everything is interconnected with the help of AXI4-Lite interfaces. The crossbar and interconnect are imported from the `verilog-axi` library. Everything else, including the RISC-V core, was completely developed in-house. Both of them are overkill for this context, but this architecture was conceived with the use of multiple cores in mind where the use of crossbars and interconnects would be fundamental.

The RISC-V core implements the `rv32i` Base Integer Instruction Set. The `Zicsr` Control and Status Register (CSR) Instructions were also implemented because they are essential for the implementation of interrupts. Interrupts were implemented, but are not currently used for anything useful. The core is multicycle but not pipelined. A simple ISA test is performed by the bootloader in order to maintain one's mental well-being during the process of software development.

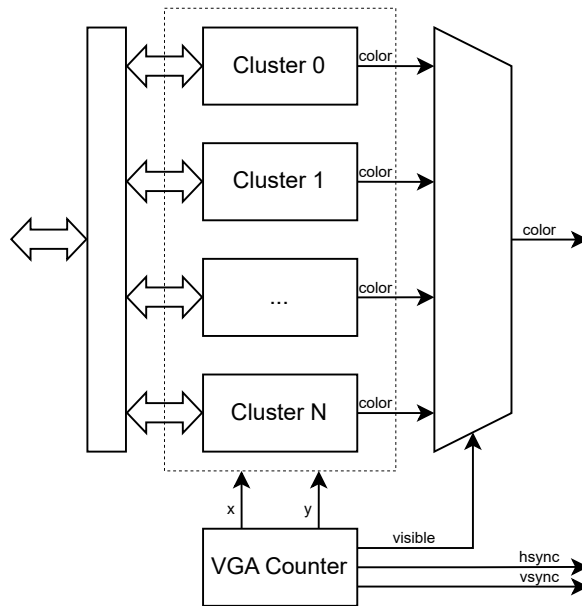
The read-only memory (ROM) is 4 kilobytes long and is used by the bootloader. The use of a bootloader was developed to avoid having to rebuild the FPGA bitstream every software iteration.

The random-access memory (RAM) is 64 kilobytes long and is used for the C code, texture data and world data. The texture data is initially located in RAM, but is moved to the video memory before the start of the game. This allows for changes in the textures without having to rebuild the bitstream. In fact, one could implement a completely different game without rebuilding the hardware implementation.

The General Purpose Input/Output (GPIO) implementation is very basic consisting of simple registers. Therefore, there is no hardware support for changing the GPIO state with a mask.

The Universal Asynchronous Receiver Transmitter (UART) operates at 115200 bauds with 8 data bits, 1 stop bit and no parity bits. This interface is fundamental for the bootloader and is very helpful during software development since it provides some kind of debugging support through the use of the `printf` function.

Figure 2: GPU Architecture

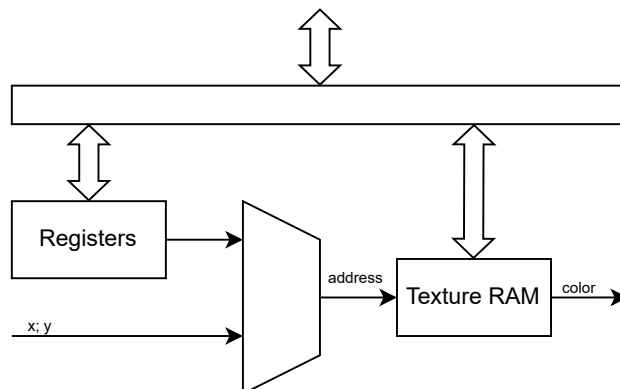


The graphics accelerator developed in class was greatly overhauled into the architecture described in the schema above. The renewed architecture is fully parametric and is capable of displaying 80 sprites with transparency support in the current configuration. These sprites are divided in 5 clusters. A cluster is a group of sprites that uses the same texture RAM. This division was introduced to mitigate the hardware size. A perk of this architecture is that transparency does not work between overlapping sprites in the same cluster. Furthermore, a sprite is not obliged to use the whole texture. A sub-region can be configured for each sprite through register access in software.

The GPU has AXI4-Lite interface that allows for cluster register access. This interface is not propagated to the clusters because its features are not needed and using a simpler interface reduces hardware complexity. Therefore, a converter is present in the GPU top architecture. The converter is not present in the schema.

The VGA Counter provides the VGA synchrony signals and the current position of the electron beam in the screen. This position is used by each cluster to compute the pixel color value. Finally, combinatory logic decides the final value of the VGA color signals based upon the color value of each cluster, the visibility signal of the VGA Counter and the cluster priority order. Transparency is implemented resignifying the value 0xFF to mean transparency. The sky color is hardcoded in this logic.

Figure 3: Cluster Architecture



Each cluster is composed of registers that store the position and texture coordinates of each sprite. With the position value, combinatory logic computes the address that stores the current color value. Then, this value is retrieved in the texture RAM. A very simple interconnect provides a write-only interface for the registers and RAM.

## **Software**