

## EDUCATION

### National University of Singapore, Singapore

- Doctor of Philosophy (*Ph.D.*) in Computer Science *Jan 2019 – Dec 2024*
  - Thesis: Accelerating the Evaluation of Large Workloads on Post-Dennard Systems with Sampling
  - Advisor: Dr. Trevor E. Carlson
  - Areas: CPU Microarchitecture, Workload Characterization, Dynamic Program Analysis, Performance Modeling and Measurements, Simulation Infrastructure, Heterogeneous Systems

### Birla Institute of Technology & Science, Pilani, Rajasthan, India

- Master of Engineering (*M.E.*) in Computer Science *Aug 2014 – May 2016*
  - Thesis: Performance Improvement of Multicore Scheduler in Real-Time Mixed Criticality Systems
  - Advisor: Dr. Biju K. Raveendran
  - Selected coursework: Advanced Computer Architecture, Advanced Algorithms and Complexity, Advanced Operating Systems, Cloud Computing, Data Mining, Real-time Systems.

### University of Kerala, Thiruvananthapuram, Kerala, India

- Bachelor of Technology (*B.Tech.*) in Computer Science and Engineering *Aug 2009 – Dec 2013*
  - FYP: Online Object Recognition from Images using Kohonen Neural Networks

## WORK EXPERIENCE

### Arm Holdings, Cambridge, UK

- Staff Performance Engineer *Feb 2025 – Till date*
  - Design and develop methodologies for the sample selection of multi-core ARM workloads

### Intel Corporation, Massachusetts, USA

- Research Intern *Jul 2022 – Dec 2022*
  - Host: Dr. Harish Patil
  - Sample validation using performance counters, performance analysis of heterogeneous workloads

### NetApp, Bengaluru, India

- Member Technical Staff II *Jul 2016 – Nov 2018*
  - Performance modeling of data storage devices, empirical analysis of storage protocols and workloads

## PUBLICATIONS

### WORKS IN PROGRESS

- [1] [Alen Sabu](#), Harish Patil, Changxi Liu, Wim Heirman, and Trevor E. Carlson, “Simulator-Agnostic Sample Selection Methodology for Heterogeneous CPU-GPU Applications” (Submitted)
- [2] [Alen Sabu](#), Zhantong Qiu, Harish Patil, Wim Heirman, Jason Lowe-Power, and Trevor E. Carlson, “Accelerated Simulation of Parallel Workloads using Loop-Bounded Checkpoints” (Submitted)

### CONFERENCES & JOURNALS

- [1] Changxi Liu\*, [Alen Sabu](#)\*, Akanksha Chaudhari, Qingxuan Kang, and Trevor E. Carlson, “Pac-Sim: Simulation of Multi-threaded Workloads using Intelligent, Live Sampling.” in *ACM Transactions on Architecture and Code Optimization (TACO)*, Jun 2024
- [2] [Alen Sabu](#)\*, Changxi Liu\*, and Trevor E. Carlson, “Viper: Utilizing Hierarchical Program Structure to Accelerate Multi-core Simulation.” in *IEEE Access*, Jan 2024
- [3] [Alen Sabu](#), Harish Patil, Wim Heirman, and Trevor E. Carlson, “LoopPoint: Checkpoint-driven Sampled Simulation for Multi-threaded Applications,” in *The 28<sup>th</sup> IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Apr 2022
- [4] Harish Patil, Alexander Isaev, Wim Heirman, [Alen Sabu](#), Ali Hajiabadi, and Trevor E. Carlson, “ELFies: Executable Region Checkpoints for Performance Analysis and Simulation,” in *The 19<sup>th</sup> International Symposium on Code Generation and Optimization (CGO)*, Mar 2021
- [5] [Alen Sabu](#), Biju Raveendran, and Rituparna Ghosh, “SMILEY: A Mixed-Criticality Real-Time Task Scheduler for Multicore Systems,” in *The 22<sup>nd</sup> International Symposium on Distributed Simulation and Real Time Applications (DS-RT)*, Oct 2018 (*Nominated best paper*)

\* *Joint first authors*

## WORKSHOPS & POSTERS

- [1] Alen Sabu, Harish Patil, Wim Heirman, and Trevor E. Carlson, “ROIperf: A Framework to Rapidly Validate Workload Sampling Methodologies,” in *The 1<sup>st</sup> Workshop on Computer Architecture Modeling and Simulation (CAMS)*, Oct 2023
- [2] Alen Sabu, Harish Patil, Wim Heirman, Alexander Isaev, and Trevor E. Carlson, “Approaching a High-Performance, General-Purpose Multi-Threaded Sampling Methodology,” in *The 2<sup>nd</sup> Young Architect Workshop (YArch)*, Mar 2020

## TUTORIALS & TALKS

- [1] “Release of Sniper v8.1 and Guide on Common Simulation Practices”
  - The 2<sup>nd</sup> Workshop on Computer Architecture Modeling and Simulation (CAMS) Nov 2024
- [2] “The gem5 Tutorial: Public Release of SPEC CPU2017 ELFies for Simulation on gem5”
  - The 51<sup>st</sup> International Symposium on Computer Architecture (ISCA) Jun 2024
- [3] “LoopPoint Tools: Sampled Simulation of Complex Multi-threaded Workloads using Sniper and gem5”
  - The 29<sup>th</sup> International Symposium on High-Performance Computer Architecture (HPCA) Feb 2023
- [4] “Studies in Selection and Validation of Regions of Interest in Heterogeneous CPU-GPU Workloads”
  - VSSAD Seminar, Intel Corporation, MA, USA Dec 2022
- [5] “LoopPoint and ELFies: Tools and Techniques to Accelerate Architecture Simulations of Complex Multi-threaded Applications using Checkpointing”
  - The 49<sup>th</sup> International Symposium on Computer Architecture (ISCA) Jun 2022
  - International Symposium on Performance Analysis of Systems & Software (ISPASS) May 2022
- [6] “LoopPoint: Checkpoint-Driven Sampled Simulation for Multi-threaded Applications”
  - VSSAD Seminar, Intel Corporation, MA, USA Mar 2022

## OPEN-SOURCE PROJECTS

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|---|---|---|
| ▪ LoopPoint Methodology   | ▪ Sniper Simulator  | ▪ ELFie Checkpointing   |
| 📄 Main developer  | 📄 Maintainer  | 📄 Contributor   |
| 🔗 <a href="https://github.com/nus-comparch/looppoint">github.com/nus-comparch/looppoint</a> | 🔗 <a href="https://github.com/snipersim/snipersim">github.com/snipersim/snipersim</a> | 🔗 <a href="https://github.com/intel/pinball2elf">github.com/intel/pinball2elf</a> |

## SKILLS

C, C++, Python, Bash, L<sup>A</sup>T<sub>E</sub>X, Git, Docker, GDB, Intel Pin, Intel GTPin, NVIDIA NVBit, Sniper, gem5

## AWARDS

- Travel grant for the 56<sup>th</sup> International Symposium on Microarchitecture (MICRO’23), Canada
- Research Achievement Award 2021/2022 from the School of Computing, National University of Singapore
- Travel grant for the 49<sup>th</sup> International Symposium on Computer Architecture (ISCA’22), USA
- Travel grant for the 2<sup>nd</sup> Young Architect Workshop at ASPLOS’20, Switzerland
- NUS Graduate Research Scholarship, National University of Singapore Jan 2019 – Till date
- BITS Higher Degree Scholarship, Birla Institute of Technology & Science, Pilani Aug 2014 – May 2016

## PROFESSIONAL SERVICE

- Member of Artifact Evaluation Committee for IEEE/ACM MICRO 2023
- Member of Program Committee on posters/short-papers for IEEE IISWC 2023
- Member of Artifact Evaluation Committee for IEEE/ACM CGO 2023
- Reviewing member for Master of Computing admissions in School of Computing, NUS 2021

## TEACHING AND MENTORING

- Research Mentor for Jikun Zhang at NUS on integrating ML models in Sniper Fall 2024
- Research Mentor for Qingxuan Kang at NUS on improving sampled simulation techniques Summer 2021
- Teaching Assistant for CS2030 Programming Methodology II at NUS Spring 2021
- Teaching Assistant for CS2106 Introduction to Operating Systems at NUS Fall 2020
- Teaching Assistant for CS1010E Programming Methodology at NUS Spring 2020
- Teaching Assistant for CSF111 Computer Programming at BITS-Pilani Spring 2016, Spring 2015
- Teaching Assistant for CSF342 Computer Architecture at BITS Pilani Fall 2015

## REFERENCES

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| ▪ <b>Dr. Trevor E. Carlson</b><br>Associate Professor<br>National University of Singapore<br>Singapore<br>✉ <a href="mailto:tcarlson@comp.nus.edu.sg">tcarlson@comp.nus.edu.sg</a> | ▪ <b>Dr. Harish Patil</b><br>Principal Engineer<br>Intel Corporation<br>USA<br>✉ <a href="mailto:harish.patil@intel.com">harish.patil@intel.com</a> | ▪ <b>Dr. Wim Heirman</b><br>Principal Engineer<br>Intel Corporation<br>Belgium<br>✉ <a href="mailto:wim.heirman@intel.com">wim.heirman@intel.com</a> |
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