ALEN SABU *he/him*
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EDUCATION

National University of Singapore, Singapore

- Doctor of Philosophy (*Ph.D.*) in Computer Science *Jan 2019 – Jul 2024* (Expected)
  - Thesis: Accelerating the Evaluation of Large Workloads on Post-Dennard Systems using Sampling
  - Advisor: Dr. Trevor E. Carlson
  - Areas: Processor architecture, workload characterization, dynamic program analysis, performance modeling and measurements, simulation infrastructure

Birla Institute of Technology & Science, Pilani, Rajasthan, India

- Master of Engineering (*M.E.*) in Computer Science *Aug 2014 – May 2016*
  - Thesis: Performance Improvement of Multicore Scheduler in Real-Time Mixed Criticality Systems
  - Advisor: Dr. Biju K. Raveendran
  - Selected coursework: Advanced Computer Architecture, Advanced Algorithms and Complexity, Advanced Operating Systems, Cloud Computing, Data Mining, Real-time Systems.

University of Kerala, Thiruvananthapuram, Kerala, India

- Bachelor of Technology (*B.Tech.*) in Computer Science and Engineering *Aug 2009 – Dec 2013*
  - Thesis: Online Object Recognition from Images using Kohonen Neural Networks

PUBLICATIONS

CONFERENCES & JOURNALS

[1] Changxi Liu*, Alen Sabu*, Akanksha Chaudhari, Qingxuan Kang, and Trevor E. Carlson, "Pac-Sim: Simulation of Multi-threaded Workloads using Intelligent, Live Sampling," in *ArXiv, Oct 2023*
* Joint first authors

[2] Alen Sabu, Harish Patil, Wim Heirman, and Trevor E. Carlson, "LoopPoint: Checkpoint-driven Sampled Simulation for Multi-threaded Applications," in *The 28th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Apr 2022*

[3] Harish Patil, Alexander Isaev, Wim Heirman, Alen Sabu, Ali Hajiabadi, and Trevor E. Carlson, "ELFies: Executable Region Checkpoints for Performance Analysis and Simulation," in *The 19th International Symposium on Code Generation and Optimization (CGO), Mar 2021*

[4] Alen Sabu, Biju Raveendran, and Rituparna Ghosh, "SMILEY: A Mixed-Criticality Real-Time Task Scheduler for Multicore Systems," in *The 22nd International Symposium on Distributed Simulation and Real Time Applications (DS-RT), Oct 2018* (*Nominated best paper*)

WORKSHOPS & POSTERS

[1] Alen Sabu, Harish Patil, Wim Heirman, and Trevor E. Carlson, "ROIperf: A Framework to Rapidly Validate Workload Sampling Methodologies," in *The 1st Workshop on Computer Architecture Modeling and Simulation (CAMS), Oct 2023*

[2] Alen Sabu, Harish Patil, Wim Heirman, Alexander Isaev, and Trevor E. Carlson, "Approaching a High-Performance, General-Purpose Multi-Threaded Sampling Methodology," in *The 2nd Young Architect Workshop (YArch), Mar 2020*

TUTORIALS & TALKS

[1] "LoopPoint Tools: Sampled Simulation of Complex Multi-threaded Workloads using Sniper and gem5"
- The 29th International Symposium on High-Performance Computer Architecture (HPCA) *Feb 2023*

[2] "Studies in Selection and Validation of Regions of Interest in Heterogeneous CPU-GPU Workloads"
- VSSAD Seminar, Intel Corporation, MA, USA *Dec 2022*

[3] "LoopPoint and ELFies: Tools and Techniques to Accelerate Architecture Simulations of Complex Multi-threaded Applications using Checkpointing"
- The 49th International Symposium on Computer Architecture (ISCA) *Jun 2022*
- International Symposium on Performance Analysis of Systems & Software (ISPASS), *May 2022*

[4] "LoopPoint: Checkpoint-Driven Sampled Simulation for Multi-threaded Applications"
- VSSAD Seminar, Intel Corporation, MA, USA *Mar 2022*

SKILLS

C, C++, Python, Bash, LaTeX, Git, Docker, GDB, Intel Pin, Intel GTPin, NVIDIA NVBit, Sniper x86 simulator

EXPERIENCE

Intel Corporation, Massachusetts, USA

- Research Intern *Jul 2022 – Dec 2022*
  - Host: Dr. Harish Patil
  - Performance analysis, sampling, and simulation of heterogeneous CPU-GPU workloads

National University of Singapore, Singapore

- Research Intern *Nov 2018 – Jan 2019*
  - Host: Dr. Trevor E. Carlson

NetApp, Bengaluru, India

- Member Technical Staff II *Jul 2016 – Nov 2018*
  - Performance modeling of data storage devices, empirical analysis of storage protocols and workloads

AWARDS

- Travel grant for the 56th International Symposium on Microarchitecture (MICRO'23), Canada
- Research Achievement Award 2021/2022 from the School of Computing, National University of Singapore
- Travel grant for the 49th International Symposium on Computer Architecture (ISCA'22), USA
- Travel grant for the 2nd Young Architect Workshop at ASPLOS'20, Switzerland
- NUS Graduate Research Scholarship, National University of Singapore *Jan 2019 – Till date*
- BITS Higher Degree Scholarship, Birla Institute of Technology & Science, Pilani *Aug 2014 – May 2016*

PROFESSIONAL SERVICE

- Served in the Artifact Evaluation Committee of IEEE/ACM International Symposium on Microarchitecture (MICRO), 2023
- Served in the Program Committee of posters/short-papers at IEEE International Symposium on Workload Characterization (IISWC), 2023
- Served in the Artifact Evaluation Committee of IEEE/ACM International Symposium on Code Generation and Optimization (CGO), 2023
- Served as a reviewing member for Master of Computing admissions in the School of Computing, National University of Singapore, 2021

TEACHING EXPERIENCE

- Teaching Assistant for CS2030 Programming Methodology II at NUS *Spring 2021*
- Teaching Assistant for CS2106 Introduction to Operating Systems at NUS *Fall 2020*
- Teaching Assistant for CS1010E Programming Methodology at NUS *Spring 2020*
- Teaching Assistant for CSF111 Computer Programming at BITS-Pilani *Spring 2016, Spring 2015*
- Teaching Assistant for CSF342 Computer Architecture at BITS Pilani *Fall 2015*

REFERENCES

- **Dr. Trevor E. Carlson**
  Assistant Professor
  School of Computing
  National University of Singapore, Singapore
  tcarlson@nus.edu.sg
- **Dr. Harish Patil**
  Principal Engineer
  Technology Path-finding and Innovation Group
  Intel Corporation, USA
  harish.patil@intel.com