

1. VFAT2 I2C

This module handles I2C transactions with a single VFAT2 hybrid.

Addressing

OptoHybrid Wishbone address: 0b 0000 0000 0000 000X XXXX YYYY YYYYY

Y register	Mode	Function
VFAT2 registers		
0 - 150	Read / write	Read or write the register on VFAT2 n°X (5 bit chip identifier)

2. VFAT2 I2C Extended

This module broadcasts I2C requests to all the VFAT2s that are not masked by the *mask* register.

Addressing

OptoHybrid Wishbone address: 0b 0001 0000 0000 0000 000Y YYYY YYYYY

Y register	Mode	Function
VFAT2 registers		
0 - 150	Read / write	Access the Y (8 bit address) on all VFAT2s not masked by the <i>mask</i> register
151 - 255	Reserved	
256	Read / write	<i>mask</i> - 24 bits Asserting a bit in this register will remove the corresponding VFAT2 from the broadcast list
257	Read only	FIFO holding the results of a request. This register will return the response of each individual request made to the VFAT2s: 8 MSbits are constant 0s 8 next MSbits are the VFAT2 id (0 to 23) 8 next MSBits hold the success/error code of the transaction 8 LSBits hold response from the VFAT2 If no data is present, an error is returned.
258	Write only	Local reset of the module

3. Threshold & Latency Scans

This module performs a threshold or latency scan on VFAT2 *vfat2* by varying its threshold/latency from a minimum value *min* to a maximum value *max* by steps of *step* and by counting the number of events where the SBits/strips are fired in a set of *N* events.

Addressing

OptoHybrid Wishbone address: 0b 0010 0000 0000 0000 0000 000Y YYYY

Y register	Mode	Function
Control		
0	Write only	Start the scan. This will also empty the FIFO holding the data of the previous scan. The written value is ignored.
1	Read / write	<i>mode</i> - 2 bits - {0, 1, 2} 0 = threshold scan 1 = threshold scan by channel 2 = latency scan
Parameters		
2	Read / write	<i>vfat2</i> - 5 bits - [0, 23]
3	Read / write	<i>channel</i> - 8 bits - [0x0, 0xFF] Only used for a threshold scan by channel
4	Read / write	<i>min</i> - 8 bits - [0x0, <i>max</i> [
5	Read / write	<i>max</i> - 8 bits -] <i>min</i> , 0xFF]
6	Read / write	<i>step</i> - 8 bits - [0x0, 0xFF]
7	Read / write	<i>N</i> - 24 bits -]0x0, 0xFFFFFFFF]
Results		
8	Read only	FIFO holding the results of the scan. This register will return the data points collected by the scan using the following data format: 8 MSBits hold the threshold/latency value of the point 24 LSBits hold the number of events that have fired If no data is present, an error is returned.
9	Read only	<i>Status</i> - 2 bits - {0, 1, 2} 1 = threshold scan running 2 = threshold scan by channel running 3 = latency scan running
Reset		
10	Write only	Local reset of the module

Description

The module will store the value of the register before the scan and reapply the later after the end of the operation.

Errors

Two types of errors can be returned by the module when running the scan: global errors and local errors.

A global error occurs if the VFAT2 is not present or running at the start of the scan. In that case, a single 32 bits word of value 0xFF000000 is stored in the FIFO. No other read operations of the FIFO should occur afterwards.

A local error occurs if one of the I2C operations used to change the value did not succeed. In that case, the value of the 24 LSBits of that particular point is 0xFFFFFF. Other data points will still be saved and be present in the FIFO.

4. T1 Controller

This module sends T1 commands to the VFAT2s according to different operation modes defined by *mode*.

Addressing

OptoHybrid Wishbone address: 0b 0011 0000 0000 0000 0000 0000 0YYYY

Y register	Mode	Function
Control		
0	Read / write	Enable (1) / disable (0) the module.
1	Read / write	<i>mode</i> - 2 bits - {0, 1, 2}
Mode 0 & 1 parameters		
2	Read / write	<i>type</i> - 2 bits - {0, 1, 2, 3} 0 = LV1A - 1 = Calpulse - 2 = Resync - 3 = BC0
3	Read / write	<i>N</i> - 32 bits - [0, 0xFFFFFFFF] 0 = infinite
4	Read / write	<i>interval</i> - 32 bits - [4, 0xFFFFFFFF]
5	Read / write	<i>delay</i> - 32 bits - [<i>interval</i> + 4, 0xFFFFFFFF]
Mode 2 parameters		
7 & 6	Read / write	<i>lv1a_sequence</i> - 64 bits
9 & 8	Read / write	<i>calpulse_sequence</i> - 64 bits
11 & 10	Read / write	<i>resync_sequence</i> - 64 bits
13 & 12	Read / write	<i>bc0_sequence</i> - 64 bits
Reset		
14	Write only	Local reset of the module

Operation modes

Mode 0

Send N T1 commands of type *type* with an interval of *interval* BXs. Note that *interval* cannot be smaller than 4 BXs which is the time needed to encode a T1 command on the wire. Example with an *interval* of 4 BXs:

[illegible]

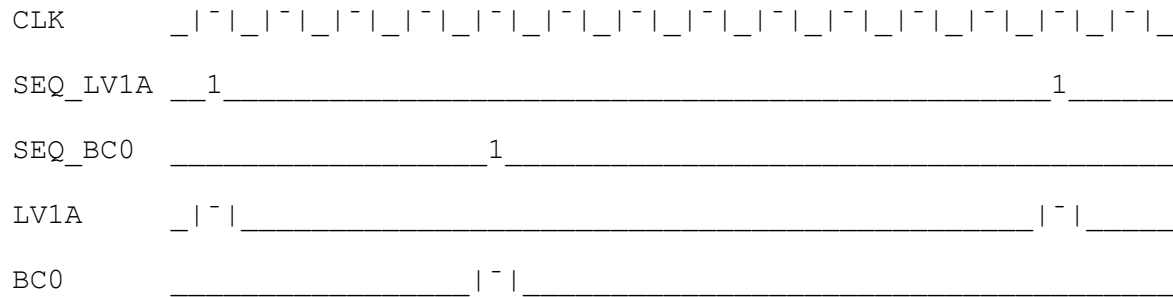
Mode 1

Send N packets composed of a Calpulse followed by an LV1A separated by *interval* BXs. The packets are spaced by *delay* BXs. Note that *interval* cannot be smaller than 4 BXs which is the time needed to encode a T1 command on the wire and that *delay* must be greater or equal to (*interval* + 4) BXs. Example with an *interval* of 4 BXs and a *delay* of 10 BXs:

Timing diagram showing the relationship between CLK, LV1A, and CAL signals. CLK is a periodic square wave. LV1A is a single pulse occurring during the high phase of CLK. CAL is a single pulse occurring during the low phase of CLK.

Mode 2

Send T1 commands according to a pattern defined by the sequence registers: *lv1a_sequence*, *calpulse_sequence*, *resync_sequence*, and *bc0_sequence*. Every 4 BXs, the module reads a bit in each of the registers and sets/resets the T1 line according to the asserted bits. This operation mode allows the user to create custom patterns of T1 commands. The module will loop over the registers indefinitely. Example of a generated pattern using the *lv1a_sequence* and *calpulse_sequence* registers.



Notes

In mode 0 and 1 the module needs to be turned off and on again using the enable/disable register in order to send another burst of packets.