

# OptoHybrid Modules & Functionalities

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This document describes how to interact with the OptoHybrid (OH) modules and how to parameterize and use the various functionalities integrated in the firmware.

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# VFAT2 I2C

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This module handles I2C transactions with a single VFAT2 hybrid.

## Addressing

Module ID      0  
Address        0x4000XXYY  
                 0b 0100 0000 0000 0000 000X XXXX YYYY YYYYY

Y register	Mode	Function
<a href="#">VFAT2 registers</a>		
0 - 150	Read / write	Read or write the register on VFAT2 n°X (5 bit chip identifier)

## Errors

The module returns an error if the parameters are not in spec or if the VFAT2 is not accessible.

## Errors to avoid

- The VFAT2 number must be in the range 0 to 23.
- The register ID must be in the range 0 to 150.

# VFAT2 I2C Extended

This module broadcasts I2C requests to all the VFAT2s that are not masked by the *mask* register.

## Addressing

Module ID      1  
Address        0x41000YYY  
                 0b 0100 0001 0000 0000 0000 000Y YYYY YYYYY

Y register	Mode	Function
VFAT2 registers		
0 - 150	Read / write	Read or write the register on all VFAT2s not masked by the <i>mask</i> register
Parameters		
256	Read / write	<i>mask</i> - 24 bits Asserting a bit in this register will remove the corresponding VFAT2 from the broadcast list
Results		
257	Read only	FIFO holding the results of a request. This register will return the response of each individual request made to the VFAT2s: 8 MSBits are constant 0s 8 next bits are the VFAT2 id (0 to 23) 8 next bits hold the status of the transaction 8 LSBits hold response from the VFAT2 If no data is present, an error is returned.
Reset		
258	Write only	Local reset of the module

## Errors

The module returns an error if the parameters are not in spec. The errors related to individual VFAT2s are stored in the FIFO.

## Errors to avoid

- The register ID must be in the range 0 to 150 or 256 to 258.

# Threshold & Latency Scans

This module performs a threshold or latency scan on VFAT2 *vfat2* by varying its threshold/latency from a minimum value *min* to a maximum value *max* by steps of *step* and by counting the number of events where the SBits/strips are fired in a set of *N* events.

## Addressing

Module ID      2  
Address        0x4200000Y  
                 0b 0100 0010 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
Control		
0	Write only	Start the scan. This will also empty the FIFO holding the data of the previous scan.
Parameters		
1	Read / write	<i>mode</i> - 2 bits   - [0, 2] 0 = threshold scan 1 = threshold scan by channel 2 = latency scan
2	Read / write	<i>vfat2</i> - 5 bits   - [0, 23]
3	Read / write	<i>channel</i> - 8 bits   - [0x0, 0xFF] Only used for a threshold scan by channel
4	Read / write	<i>min</i> - 8 bits   - [0x0, <i>max</i> ]
5	Read / write	<i>max</i> - 8 bits   - [ <i>min</i> , 0xFF] Default: 0 = 0xFF
6	Read / write	<i>step</i> - 8 bits   - [0x0, 0xFF] Default: 0 = 0x1
7	Read / write	<i>N</i> - 24 bits - ]0x0, 0xFFFFFFFF] Default: 0 = 0xFFFFFFFF
Results		
8	Read only	FIFO holding the results of the scan. This register will return the data points collected by the scan using the following data format: 8 MSBits hold the threshold/latency value of the point 24 LSBits hold the number of events that have fired If no data is present, an error is returned.
Monitoring		
9	Read only	<i>Status</i> - 2 bits   - {0, 1, 2, 3} 0 = nothing running 1 = threshold scan running 2 = threshold scan by channel running 3 = latency scan running
Reset		
10	Write only	Local reset of the module

## Description

The module will store the value of the register before the scan and reapply the later after the end of the operation.

## Errors

When starting the scan, the returned status of the write operation informs the user about the validity of the parameters. Invalid parameters will return an error and prevent the scan from starting. Other errors related to the VFAT2s are stored in the FIFO.

Two types of errors are stored in the FIFO when running the scan: global errors and local errors.

A global error occurs if the VFAT2 is not present or running at the start of the scan. In that case, a single 32 bits word of value 0xFF000000 is stored in the FIFO. No other read operations of the FIFO should occur afterwards.

A local error occurs if one of the I2C operations used to change the value did not succeed. In that case, the value of the 24 LSBits of that particular point is 0xFFFFFF. Other data points will still be saved and be present in the FIFO.

### **Errors to avoid**

- The VFAT2 number must be in the range 0 to 23.
- The maximum value of the register to scan must be higher than the minimum value.
- The register ID must be in the range 0 to 10.

# T1 Controller

This module sends T1 commands to the VFAT2s according to different operation modes defined by *mode*.

## Addressing

Module ID      3  
Address        0x4300000Y  
                 0b 0100 0011 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
<b>Control</b>		
0	Write only	Toggle the module on and off.
1	Read / write	<i>mode</i> - 2 bits - [0, 2]
<b>Mode 0 &amp; 1 parameters</b>		
2	Read / write	<i>type</i> - 2 bits - [0, 3] 0 = LV1A 1 = Calpulse 2 = Resync 3 = BC0
3	Read / write	<i>N</i> - 32 bits - [0, 0xFFFFFFFF] Default: 0 = infinite
4	Read / write	<i>interval</i> - 32 bits - [3, 0xFFFFFFFF]
5	Read / write	<i>delay</i> - 32 bits - [3, interval - 3]
<b>Mode 2 parameters</b>		
7 & 6	Read / write	<i>lv1a_sequence</i> - 64 bits
9 & 8	Read / write	<i>calpulse_sequence</i> - 64 bits
11 & 10	Read / write	<i>resync_sequence</i> - 64 bits
13 & 12	Read / write	<i>bc0_sequence</i> - 64 bits
<b>Monitoring</b>		
14	Read only	<i>Status</i> - 2 bits - [0, 3] 0 = nothing running 1 = MODE 0 running 2 = MODE 1 running 3 = MODE 2 running
<b>Reset</b>		
15	Write only	Local reset of the module

## Errors

When starting the module, the returned status of the write operation informs the user about the validity of the parameters. Invalid parameters will return an error and prevent the module from starting.

## Operation modes

### Mode 0

Send *N* T1 commands of type *type* with an interval of *interval* BXs. Note that *interval* cannot be smaller than 3 BXs which is the time needed to encode a T1 command on the wire. Example with an *interval* of 4 BXs:



# DAC Scans

This module performs a scan of a DAC register *dac* on a single VFAT2 *vfat2* by varying its value from a minimum value *min* to a maximum value *max* by steps of *step* and by averaging the value on  $2^N$  readouts.

## Addressing

Module ID      4  
 Address        0x4400000Y  
                  0b 0100 0100 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
<b>Control</b>		
<b>0</b>	Write only	Start the scan. This will also empty the FIFO holding the data of the previous scan. The written value is ignored.
<b>Parameters</b>		
<b>1</b>	Read / write	<i>dac</i> - 4 bits - [0, 9] 0 = IPreampIn 1 = IPreampFeed 2 = IPreampOut 3 = IShaper 4 = IShaperFeed 5 = IComp 6 = VThreshold1 7 = VThreshold2 8 = VCal 9 = CalOut
<b>2</b>	Read / write	<i>vfat2</i> - 5 bits - [0, 23]
<b>3</b>	Read / write	<i>min</i> - 8 bits - [0x0, <i>max</i> ]
<b>4</b>	Read / write	<i>max</i> - 8 bits - [ <i>min</i> , 0xFF] Note: 0 = 0xFF
<b>5</b>	Read / write	<i>step</i> - 8 bits - [0x0, 0xFF] Note: 0 = 0x1
<b>6</b>	Read / write	<i>N</i> - 4 bits - [0, 15] Events = $2^N$
<b>Results</b>		
<b>7</b>	Read only	FIFO holding the results of the scan. This register will return the data points collected by the scan using the following data format: 8 MSBits hold the DAC value of the point 24 LSBits hold the mean of the ADC values If no data is present, an error is returned.
<b>Monitoring</b>		
<b>8</b>	Read only	<i>Status</i> - 1 bits - {0, 1} 0 = nothing running 1 = DAC scan running
<b>Reset</b>		
<b>9</b>	Write only	Local reset of the module

## Description



The module will store the value of the register before the scan and reapply the later after the end of the operation. It will also set the “Control Register 1” of all the VFAT2s to 0 in order to avoid conflicting scans.

## **Errors**

When starting the scan, the returned status of the write operation informs the user about the validity of the parameters. Invalid parameters will return an error and prevent the scan from starting. Other errors related to the VFAT2s are stored in the FIFO.

Two types of errors are stored in the FIFO when running the scan: global errors and local errors.

A global error occurs if the VFAT2 is not present or running at the start of the scan. In that case, a single 32 bits word of value 0xFF000000 is stored in the FIFO. No other read operations of the FIFO should occur afterwards.

A local error occurs if one of the I2C operations used to change the value did not succeed. In that case, the value of the 24 LSBits of that particular point is 0xFFFFFF. Other data points will still be saved and be present in the FIFO.

## **Errors to avoid**

- The DAC number must be in the range 0 to 9.
- The VFAT2 number must be in the range 0 to 23.
- The maximum value of the register to scan must be higher than the minimum value.
- The register ID must be in the range 0 to 9.

# ADC (in development)

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This module handles the read out of the ADC.

## Addressing

Module ID      8  
Address        0x4800000Y  
                 0b 0100 1000 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
<a href="#">ADC registers</a>		
0 - 15	Read only	Returns the conversion value of a given channel

## Errors

The module returns an error if the parameters are not in spec.

## Errors to avoid

- The register ID must be in the range 0 to 15.

# Clocking

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Registers that control and monitor various clocking parameters

## Addressing

Module ID      9  
Address        0x4900000Y  
                 0b 0100 1001 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
<a href="#">VFAT2 readout clock</a>		
<b>0 - 2</b>	Read / write	<i>phase shift</i> - 8 bits - [0, 255] Controls the phase shift between the VFAT2 clock and the data readout clocks (for each column) on the FPGA in order to minimize data corruption

# Counters

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List of counters

## Addressing

Module ID      10  
Address        0x4A0000YY  
                 0b 0100 1010 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
<a href="#">VFAT2 readout clock</a>		
<b>0 - 2</b>	Read / write	<i>phase shift</i> - 8 bits - [0, 255] Controls the phase shift between the VFAT2 clock and the data readout clocks (for each column) on the FPGA in order to minimize data corruption