OptoHybrid Modules & Functionalities

Thomas Lenzi (thomas.lenzi@cern.ch)

This document describes how to interact with the OptoHybrid (OH) modules and how to parameterize and use the various functionalities integrated in the firmware.

Contents

VFAT2 I2C

This module handles I2C transactions with a single VFAT2 hybrid.

Addressing

Module ID 0
Address 0x4000XXYY
0b 0100 0000 0000 0000 000X XXXX YYYY YYYY

Y register	Mode	Function
VFAT2 registers		
0 - 150	Read / write	Read or write the register on VFAT2 n°X (5 bit chip identifier) 5 MSBits are constant 0s 1 next bit is set when an error occurred 1 next bit is set when the transaction is valid 1 next bit is the read/not write bit of the transaction 8 next bits hold the id of the addressed VFAT2 8 next bits hold the id of the addressed register 8 LSBits hold the response from the VFAT2

Errors

The module returns an error if the parameters are not in spec or if the VFAT2 is not accessible.

Errors to avoid

- The VFAT2 number must be in the range 0 to 23.
- The register ID must be in the range 0 to 150.

VFAT2 I2C Extended

This module broadcasts I2C requests to all the VFAT2s that are not masked by the *mask* register.

Addressing

Module ID 1
Address 0x41000YYY
0b 0100 0001 0000 0000 0000 000Y YYYY YYYYY

Y register	Mode	Function
VFAT2 registers		
0 - 150	Read / write	Read or write the register on all VFAT2s not masked by the *mask* register
Parameters		
256	Read / write	*mask* - 24 bits Asserting a bit in this register will remove the corresponding VFAT2 from the broadcast list
Results		
257	Read only	FIFO holding the results of a request. This register will return the response of each individual request made to the VFAT2s: 8 MSBits are constant 0s 8 next bits hold the status of the transaction 8 next bits are the VFAT2 id (0 to 23) 8 LSBits hold response from the VFAT2 If no data is present, an error is returned.
Reset		
258	Write only	Local reset of the module

Errors

The module returns an error if the parameters are not in spec. The errors related to individual VFAT2s are stored in the FIFO.

Errors to avoid

- The register ID must be in the range 0 to 150 or 256 to 258.

Threshold, Latency, and S-Curve Scans

This module performs a threshold, threshold by channel, latency, or s-curve scan on (channel *channel* of) VFAT2 *vfat2* by varying its threshold/latency/calibration pulse from a minimum value *min* to a maximum value *max* by steps of *step* and by counting the number of events where the SBits/strips are fired in a set of *N* events.

Addressing

Module ID 2
Address 0x4200000Y
0b 0100 0010 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
Control		
0	Write only	Start the scan. This will also empty the FIFO holding the data of the previous scan.
Parameters		
1	Read / write	*mode* - 2 bits - [0, 2] 0 = threshold scan 1 = threshold scan by channel 2 = latency scan 3 = s-curve
2	Read / write	*VFAT2* - 5 bits - [0, 23]
3	Read / write	*channel* - 8 bits - [0x0, 0xFF] Only used for a threshold scan by channel
4	Read / write	*min* - 8 bits - [0x0, *max*]
5	Read / write	*max* - 8 bits - [*min*, 0xFF] Default: 0 = 0xFF
6	Read / write	*step* - 8 bits - [0x0, 0xFF] Default: 0 = 0x1
7	Read / write	*N* - 24 bits -]0x0, 0xFFFFFF] Default: 0 = 0xFFFFFF
Results		
8	Read only	FIFO holding the results of the scan. This register will return the data points collected by the scan using the following data format: 8 MSBits hold the threshold/latency value of the point 24 LSBits hold the number of events that have fired If no data is present, an error is returned.
Monitoring		
9	Read only	*Status* - 3 bits - [0, 4] 0 = nothing running 1 = threshold scan running 2 = threshold scan by channel running 3 = latency scan running 4 = s-curve scan running
Reset		
10	Write only	Local reset of the module

Description

The module will store the value of the register before the scan and reapply the later after the end of the operation.

Errors

When starting the scan, the returned status of the write operation informs the user about the validity of the parameters. Invalid parameters will return an error and prevent the scan from starting. Other errors related to the VFAT2s are stored in the FIFO.

Two types of errors are stored in the FIFO when running the scan: global errors and local errors.

A global error occurs if the VFAT2 is not present or running at the start of the scan. In that case, a single 32 bits word is stored in the FIFO. No other read operations of the FIFO should occur afterwards:

- 0xF0000000 means that the VFAT2 is not running ;
- 0xFF000000 means that the current value of the register could not be saved.

A local error occurs if one of the I2C operations used to change the value did not succeed. In that case, the value of the 24 LSBits of that particular point is 0xFFFFFF. Other data points will still be saved and be present in the FIFO.

Errors to avoid

- The VFAT2 number must be in the range 0 to 23.
- The maximum value of the register to scan must be higher than the minimum value.
- The register ID must be in the range 0 to 10.

Note

When performing a threshold scan by channel or an s-curve scan, the user should provide a source of triggers in order to generate tracking data.

T1 Controller

This module sends T1 commands to the VFAT2s according to different operation modes defined by *mode*.

Addressing

Module ID 3
Address 0x4300000Y
0b 0100 0011 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
Control		
0	Write only	Toggle the module on and off.
1	Read / write	*mode* - 2 bits - [0, 2]
Mode 0 & 1 parameters		
2	Read / write	*type* - 2 bits - [0, 3] 0 = LV1A 1 = Calpulse 2 = Resync 3 = BC0
3	Read / write	*N* - 32 bits - [0, 0xFFFFFFFF] Default: 0 = infinite
4	Read / write	*interval* - 32 bits - [3, 0xFFFFFFFF]
5	Read / write	*delay* - 32 bits - [*3*, interval - 3]
Mode 2 parameters		
7 & 6	Read / write	*lv1a_sequence* - 64 bits
9 & 8	Read / write	*calpulse_sequence* - 64 bits
11 & 10	Read / write	*resync_sequence* - 64 bits
13 & 12	Read / write	*bc0_sequence* - 64 bits
Monitoring		
14	Read only	*Status* - 2 bits - [0, 3] 0 = nothing running 1 = MODE 0 running 2 = MODE 1 running 3 = MODE 2 running
Reset		
15	Write only	Local reset of the module

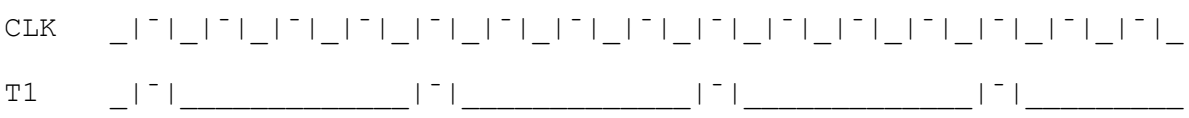
Errors

When starting the module, the returned status of the write operation informs the user about the validity of the parameters. Invalid parameters will return an error and prevent the module from starting.

Operation modes

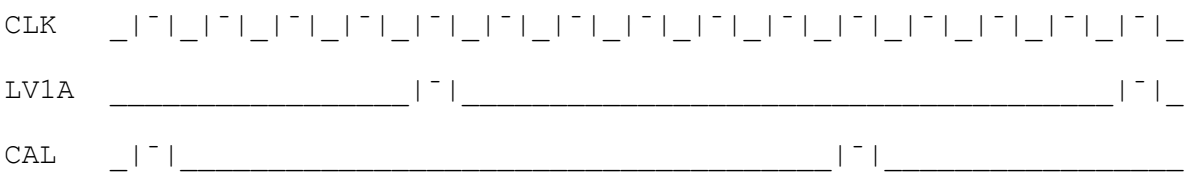
Mode 0

Send *N* T1 commands of type *type* with an interval of *interval* BXs. Note that *interval* cannot be smaller than 3 BXs which is the time needed to encode a T1 command on the wire. Example with an *interval* of 4 BXs:



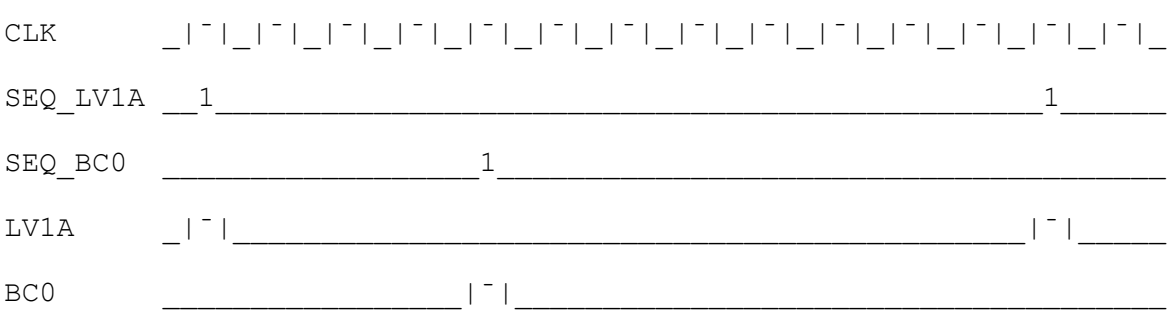
Mode 1

Send *N* packets composed of a Calpulse followed by an LV1A separated by *delay* BXs. The packets are spaced by *interval* BXs. Note that *interval* cannot be smaller than 3 BXs which is the time needed to encode a T1 command on the wire and that *delay* must be in the range [3, *interval* – 3] BXs. Example with a *delay* of 4 BXs and an *interval* of 10 BXs:



Mode 2

Send T1 commands according to a pattern defined by the sequence registers: *lv1a_sequence*, *calpulse_sequence*, *resync_sequence*, and *bc0_sequence*. Every 4 BXs, the module reads a bit in each of the registers and sets/resets the T1 line according to the asserted bits. This operation mode allows the user to create custom patterns of T1 commands. The module will loop over the registers *N* times. Example of a generated pattern using the *lv1a_sequence* and *calpulse_sequence* registers.



Notes

The module will stop automatically once all the signals are sent.

Errors to avoid

- The interval must have a value higher than 3 (not checked when sending only 1 command).
- The delay must have a value higher than interval + 3.
- The register ID must be in the range 0 to 15.

DAC Scans (in development)

This module performs a scan of a DAC register *dac* on a single VFAT2 *vfat2* by varying its value from a minimum value *min* to a maximum value *max* by steps of *step* and by averaging the value on 2^*N* readouts.

Addressing

Module ID 4
Address 0x4400000Y
0b 0100 0100 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
Control		
0	Write only	Start the scan. This will also empty the FIFO holding the data of the previous scan. The written value is ignored.
Parameters		
1	Read / write	*dac* - 4 bits - [0, 9] 0 = IPreampIn 1 = IPreampFeed 2 = IPreampOut 3 = IShaper 4 = IShaperFeed 5 = IComp 6 = VThreshold1 7 = VThreshold2 8 = VCal 9 = CalOut
2	Read / write	*VFAT2* - 5 bits - [0, 23]
3	Read / write	*min* - 8 bits - [0x0, *max*]
4	Read / write	*max* - 8 bits - [*min*, 0xFF] Note: 0 = 0xFF
5	Read / write	*step* - 8 bits - [0x0, 0xFF] Note: 0 = 0x1
6	Read / write	*N* - 4 bits - [0, 15] Events = 2^N
Results		
7	Read only	FIFO holding the results of the scan. This register will return the data points collected by the scan using the following data format: 8 MSBits hold the DAC value of the point 24 LSBits hold the mean of the ADC values If no data is present, an error is returned.
Monitoring		
8	Read only	*Status* - 1 bits - {0, 1} 0 = nothing running 1 = DAC scan running
Reset		
9	Write only	Local reset of the module

Description

The module will store the value of the register before the scan and reapply the later after the end of the operation. It will also set the “Control Register 1” of all the VFAT2s to 0 in order to avoid conflicting scans.

Errors

When starting the scan, the returned status of the write operation informs the user about the validity of the parameters. Invalid parameters will return an error and prevent the scan from starting. Other errors related to the VFAT2s are stored in the FIFO.

Two types of errors are stored in the FIFO when running the scan: global errors and local errors.

A global error occurs if the VFAT2 is not present or running at the start of the scan. In that case, a single 32 bits word of value 0xFF000000 is stored in the FIFO. No other read operations of the FIFO should occur afterwards.

A local error occurs if one of the I2C operations used to change the value did not succeed. In that case, the value of the 24 LSBits of that particular point is 0xFFFFFF. Other data points will still be saved and be present in the FIFO.

Errors to avoid

- The DAC number must be in the range 0 to 9.
- The VFAT2 number must be in the range 0 to 23.
- The maximum value of the register to scan must be higher than the minimum value.
- The register ID must be in the range 0 to 9.

ADC (in development)

This module handles the read out of the ADC.

Addressing

Module ID 8
Address 0x4800000Y
0b 0100 1000 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
ADC registers		
0 - 15	Read only	Returns the conversion value of a given channel

Errors

The module returns an error if the parameters are not in spec.

Errors to avoid

- The register ID must be in the range 0 to 15.

Clocking (not available for test beam, use system registers to control clocking options)

Registers that control and monitor various clocking parameters

Addressing

Module ID 9
Address 0x4900000Y
0b 0100 1001 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
VFAT2 readout clock		
0 - 2	Read / write	*phase shift* - 8 bits - [0, 255] Controls the phase shift between the VFAT2 clock and the data readout clocks (for each column) on the FPGA in order to minimize data corruption

Counters

This module holds all the counters of the OptoHybrid. Writing to a given register will reset its value.

Addressing

Module ID 10
Address 0x4A0000YY
0b 0100 1010 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
Wishbone		
0 - 3	Read	*Wishbone masters strobe* Order: GTX, Extended I2C, Scan, DAC
4 - 7	Read	*Wishbone masters acknowledgments*
8 - 21	Read	*Wishbone slaves strobe* Order: I2C 0, I2C 1, I2C 2, I2C 3, I2C 4, I2C 5, Extended I2C, Scan, T1, DAC, ADC, Clocking, Counters, System
22 - 35	Read	*Wishbone slaves acknowledgments*
VFAT2		
36 - 59	Read	*VFAT2 tracking data valid CRC* For each VFAT2 counts the number of data packets that come with a valid CRC
60 - 83	Read	*VFAT2 tracking data incorrect CRC* For each VFAT2 counts the number of data packets that come with an incorrect CRC
T1 commands		
84 - 87	Read	*T1 from AMC13* Order: LV1A, Calpulse, Resync, BC0
88 - 91	Read	*T1 from firmware*
92 - 95	Read	*T1 from external source*
96 - 99	Read	*T1 from loopback*
100 - 103	Read	*T1 sent to the VFAT2*
GTX		
104	Read	*Tracking link error*
105	Read	*Trigger link error*
106	Read	*Data packets sent*

System Registers

List of system registers

Addressing

Module ID 11
Address 0x4B0000YY
0b 0100 1011 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
VFAT2		
0	Read / write	*VFAT2 tracking data mask* - 24 bits Allows to mask individual VFAT2s for tracking data readout over the optical link
1	Read / write	*VFAT2 T1 source select* - 3 bits 0 : T1 from AMC13 1 : T1 from OptoHybrid 2 : T1 from external source 3 : Internal loopback on SBits 4 : Logical OR of all sources
2	Read / write	*T1 loopback SBit select* - 5 bits
3	Write only	*VFAT2 reset* - 1 bit This register automatically returns to a 0 state
Clocking		
4	Read / write	*Reference clock source* - 2 bits 0 : allow clock switch to GTX recovered clock 1 : GTX recovered clock 2 : external clock 3 : on board oscillator
Misc		
5	Read / write	*TDC SBits selects* - 30 bits
6	Read / write	*Trigger throttling* - 32 bits

Status Registers

List of status registers

Addressing

Module ID 12
Address 0x4C0000YY
0b 0100 1011 0000 0000 0000 0000 0000 YYYY

Y register	Mode	Function
Global		
0	Read only	*OH firmware version*
Clocking		
1	Read only	*FPGA clock PLL locked*
2	Read only	*External clock PLL locked*
3	Read only	*CDCE locked*
4	Read only	*Recovered clock locked*
5	Read only	*Clock switch operated*