1. Description

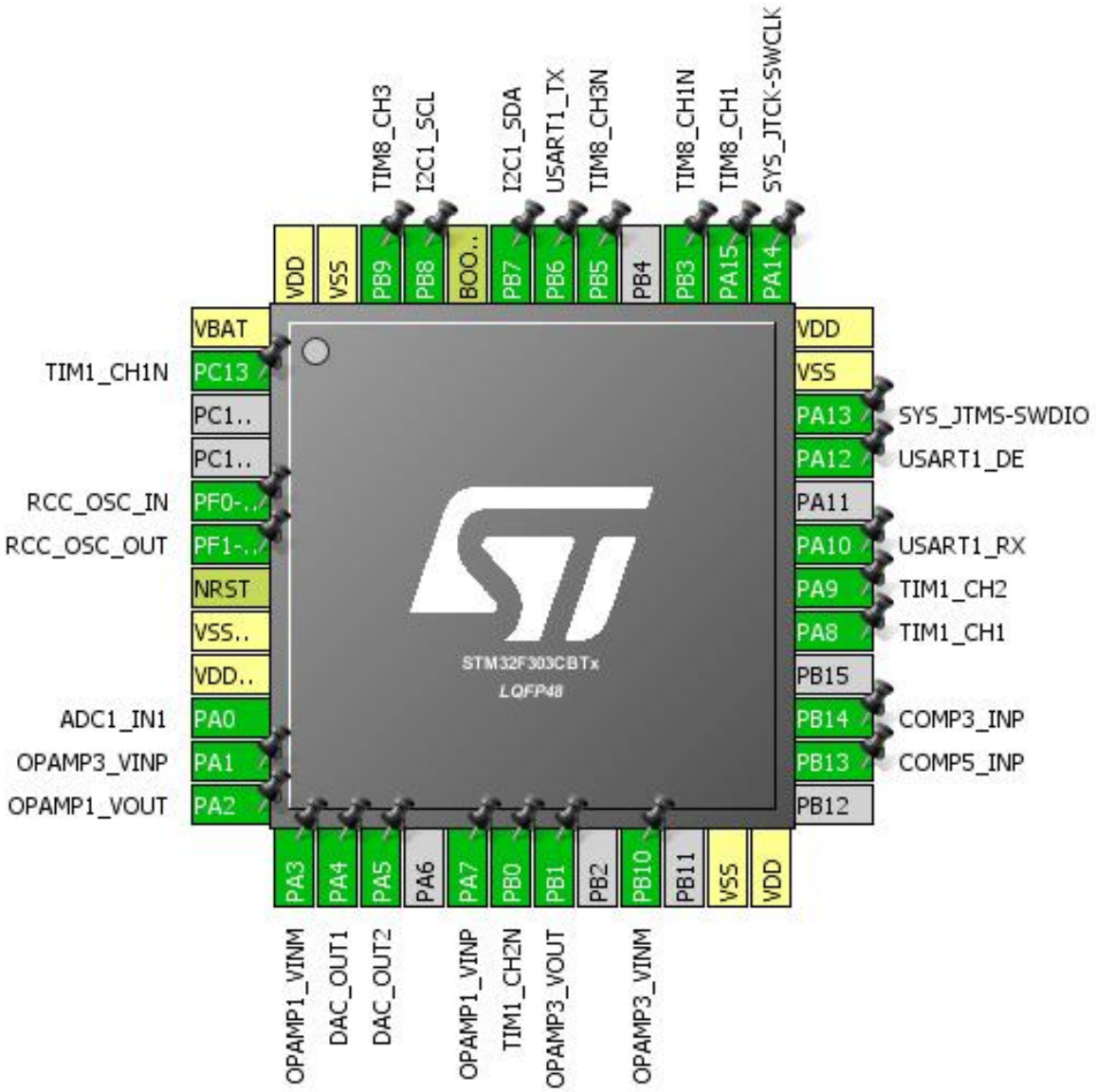
1.1. Project

Project Name	Cube_F303
Board Name	Cube_F303
Generated with:	STM32CubeMX 4.22.0
Date	07/19/2017

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303CBTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration

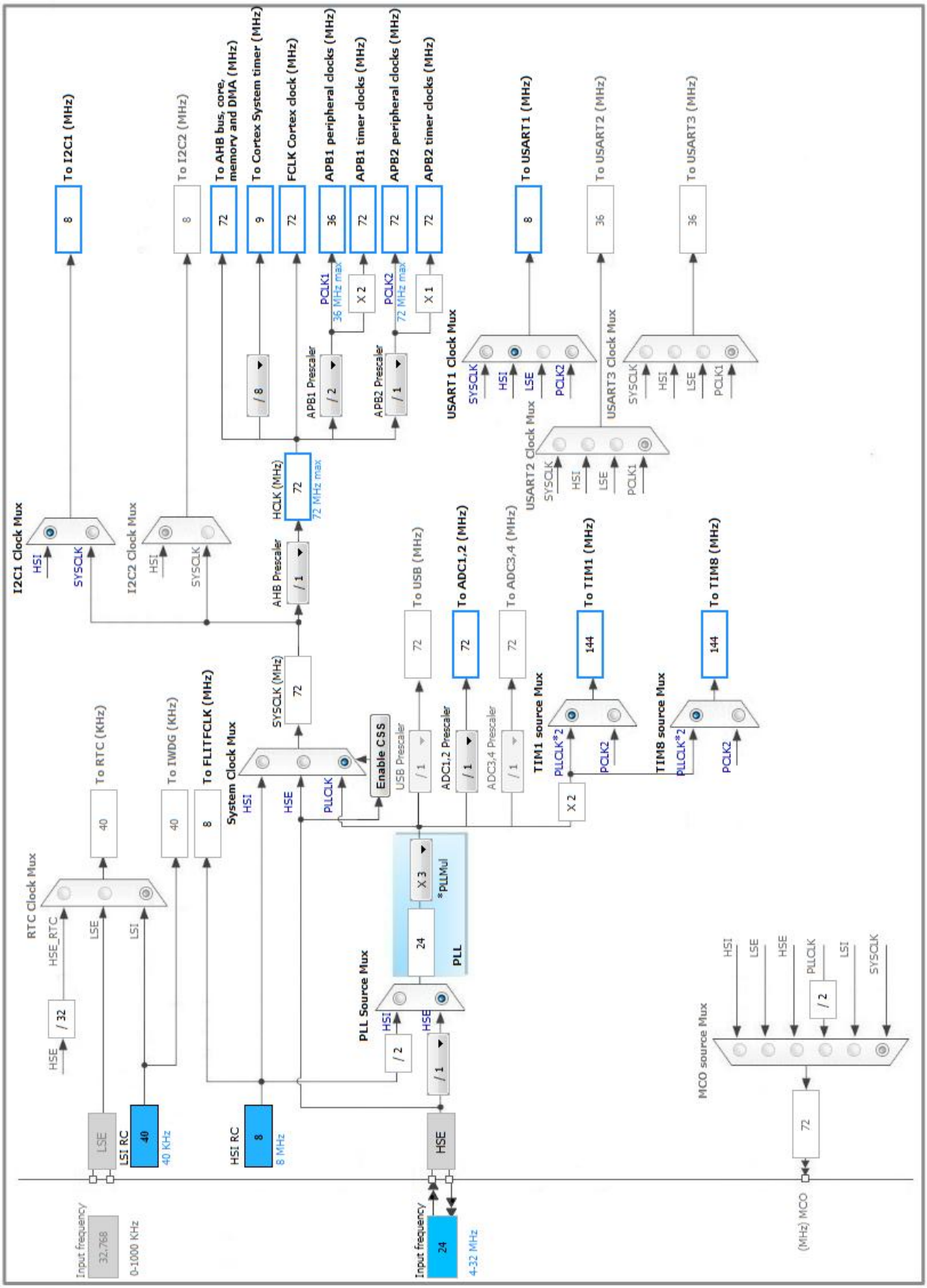


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	TIM1_CH1N	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN1	
11	PA1	I/O	OPAMP3_VINP	
12	PA2	I/O	OPAMP1_VOUT	
13	PA3	I/O	OPAMP1_VINM	
14	PA4	I/O	DAC_OUT1	
15	PA5	I/O	DAC_OUT2	
17	PA7	I/O	OPAMP1_VINP	
18	PB0	I/O	TIM1_CH2N	
19	PB1	I/O	OPAMP3_VOUT	
21	PB10	I/O	OPAMP3_VINM	
23	VSS	Power		
24	VDD	Power		
26	PB13	I/O	COMP5_INP	
27	PB14	I/O	COMP3_INP	
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
31	PA10	I/O	USART1_RX	
33	PA12	I/O	USART1_DE	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15	I/O	TIM8_CH1	
39	PB3	I/O	TIM8_CH1N	
41	PB5	I/O	TIM8_CH3N	
42	PB6	I/O	USART1_TX	
43	PB7	I/O	I2C1_SDA	
44	BOOT0	Boot		
45	PB8	I/O	I2C1_SCL	

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
46	PB9	I/O	TIM8_CH3	
47	VSS	Power		
48	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended

mode: Temperature Sensor Channel

mode: Vbat Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel Vbat ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. COMP3

mode: Input [+]

Input [-]: DAC OUT1

5.2.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed / Full Power
Interrupt Trigger Mode	None
Hysteresis Level	None
Blanking Source	None

Output Parameters:

Output Polarity	Not Inverted
Output Internal Selection	None

5.3. COMP5

mode: Input [+]

Input [-]: DAC OUT2

5.3.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed / Full Power
Interrupt Trigger Mode	None
Hysteresis Level	None
Blanking Source	None

Output Parameters:

Output Polarity	Not Inverted
Output Internal Selection	None

5.4. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

5.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

5.5. I2C1

I2C: I2C

5.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x2000090E

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.6. OPAMP1

Mode: Standalone

5.6.1. Parameter Settings:

Basic Parameters:

User Trimming	Disable

5.7. OPAMP3

Mode: Standalone

5.7.1. Parameter Settings:

Basic Parameters:

User Trimming	Disable

5.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.8.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.9. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.10. TIM1

Channel1: Output Compare CH1 CH1N
Channel2: Output Compare CH2 CH2N

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1 and 1N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 2 and 2N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.11. TIM6

mode: Activated

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.12. TIM8

Channel1: Output Compare CH1 CH1N

Channel3: Output Compare CH3 CH3N

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1 and 1N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 3 and 3N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.13. USART1

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
COMP3	PB14	COMP3_INP	Analog mode	No pull up pull down	n/a	
COMP5	PB13	COMP5_INP	Analog mode	No pull up pull down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull up pull down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull up pull down	n/a	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	Pull up	**High ***	
	PB8	I2C1_SCL	Alternate Function Open Drain	Pull up	**High ***	
OPAMP1	PA2	OPAMP1_VOUT	Analog mode	No pull up pull down	n/a	
	PA3	OPAMP1_VINM	Analog mode	No pull up pull down	n/a	
	PA7	OPAMP1_VINP	Analog mode	No pull up pull down	n/a	
OPAMP3	PA1	OPAMP3_VINP	Analog mode	No pull up pull down	n/a	
	PB1	OPAMP3_VOUT	Analog mode	No pull up pull down	n/a	
	PB10	OPAMP3_VINM	Analog mode	No pull up pull down	n/a	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PC13	TIM1_CH1N	Alternate Function Push Pull	No pull up pull down	Low	
	PB0	TIM1_CH2N	Alternate Function Push Pull	No pull up pull down	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	
TIM8	PA15	TIM8_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PB3	TIM8_CH1N	Alternate Function Push Pull	No pull up pull down	Low	
	PB5	TIM8_CH3N	Alternate Function Push Pull	No pull up pull down	Low	
	PB9	TIM8_CH3	Alternate Function Push Pull	No pull up pull down	Low	
USART1	PA10	USART1_RX	Alternate Function Push Pull	Pull up	**High ***	
	PA12	USART1_DE	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB6	USART1_TX	Alternate Function Push Pull	Pull up	**High ***	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
Timer 6 interrupt and DAC underrun interrupts	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C1 error interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
TIM8 break global interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger com interrupt	unused		
TIM8 capture compare interrupt	unused		
COMP1, COMP2 and COMP3 interrupts through EXTI lines 21, 22 and 29	unused		
COMP4, COMP5 and COMP6 interrupts through EXTI lines 30, 31 and 32	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303CBTx
Datasheet	023353_Rev13

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Cube_F303
Project Folder	E:\Alex\Dropbox\Projects\Ventmatika\Stepper\Stepper
Toolchain / IDE	Other Toolchains (GPDSC)
Firmware Package Name and Version	STM32Cube FW_F3 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No