Politecnico di Torino

Collegio di Elettronica, Telecomunicazioni e Fisica

Report for the course
Integrated Systems Architecture

Master degree in Electrical Engineering

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Contents

CHAPTER 1

Lab 1: Design and Implementation of a Digital Filter

1.1 Reference model development

1.1.1 Matlab model

The MATLAB model is crucial to understand the working principle of a FIR implementation. In our case, the filter had the following parameters:

- Number of bits: 14
- Order of the filter: 10

Through the use of this model we were able to obtain a first estimation of the frequency response (Fig. 1.1) both for the ideal case and for the 14 bits integer coefficients implementation.

The representation of the weights of the filter have one bit for the integer part and 13 bits for the fractional part. Table 1.1 reports the value obtained with this model.

1.1.2 C model for suitable precision reduction

The C model of this FIR implementations was used to analyse the behaviour of the filter and to obtain a bit-parallelism reduction in each multiplier. This was achieved using a shifting technique

Table 1.1: Matlab model estimation of the filter's coefficients

b_0	-1.12207e-4
b_1	-0.0127
b_2	-0.0248
b_3	0.0635
b_4	0.2748
b_5	0.3979
b_6	0.2748
b_7	0.0635
b_8	-0.0248
b_9	-0.0127
b_10	-1.12207e-4

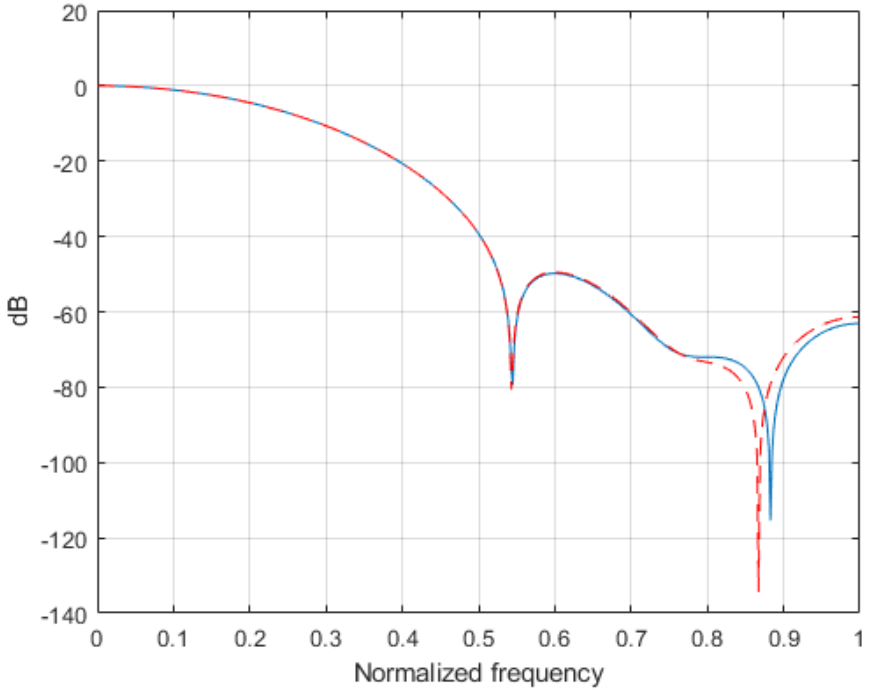

Figure 1.1: Frequency response of the FIR, in blue the ideal behaviour, in red the integer coefficients version

which reduces, in fixed point representation, the precision of the operation while maintaining the correct information.

In order to obtain an acceptable trade off, we ran a test campaign in which we progressively reduced the precision of the multiplication until we obtained a Total Harmonic Distortion (THD) close but lower than -30.

The result of this trial and error process is a precision reduction by 13 bits and the final THD is -34 dB. In fact, each input data is represented as fixed point on 14 bits, so each multiplication produces value on 28 bits. With our algorithm we managed to truncate each result to 15 bits (28 bits - 15 bits = 13 bits dropped from the result), in order to save some area for each register and by reducing the parallelism of each adder.

1.2 VLSI implementation

1.2.1 Standard architecture

The standard architecture of the filter is shown in Figure 1.2, while the timing diagram is reported in Figure 1.3 .

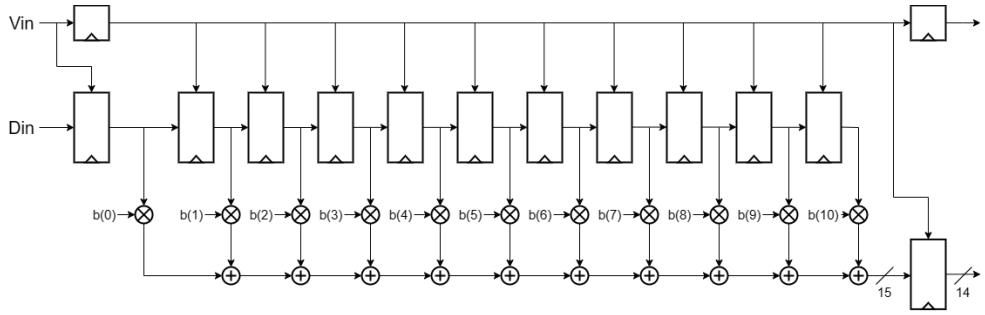

Figure 1.2: Standard architecture implementation of a FIR filter design following the specification parameters

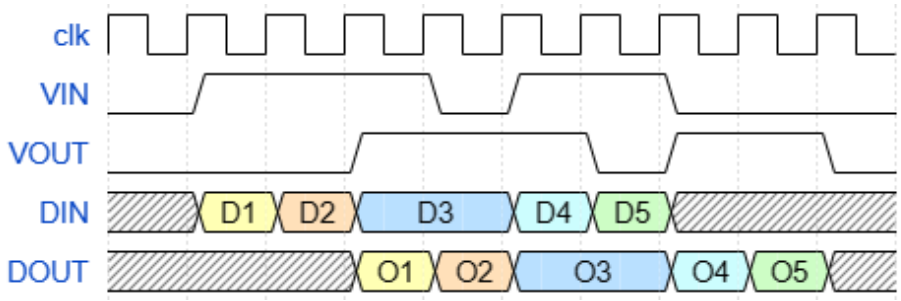

Figure 1.3: Standard architecture timing diagram

Simulation

The simulation of the FIR is crucial to validate the validity of the architecture chosen and to estimate the processing time, which in this case amounts to 40.6 us. The following figures illustrate the behaviour of the filter when its processing is activated and deactivated, i.e. when VIN moves from 0 to 1 and vice-versa. Figure 1.6 sheds a light on the truncation of the multipliers' output, which enables a precision reduction and improves the performance of the adders chain.

1.2.2 Logic synthesis

The main characteristics of the logic synthesis results are the following:

- Clock frequency: 333.33 MHz

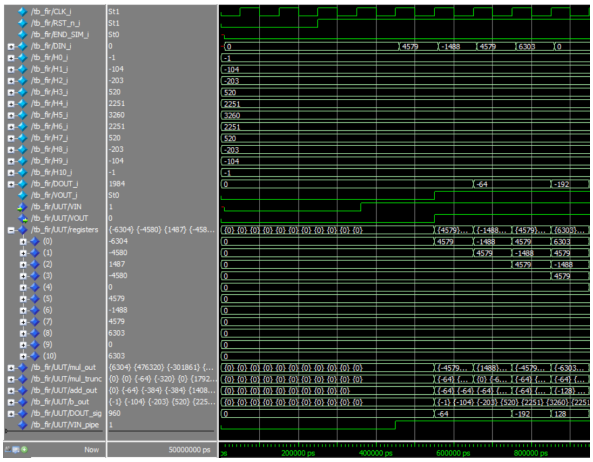

Figure 1.4: Detail on the moment FIR processing is activated. The insight of the register contents is crucial to validate the correctness of the algorithm.

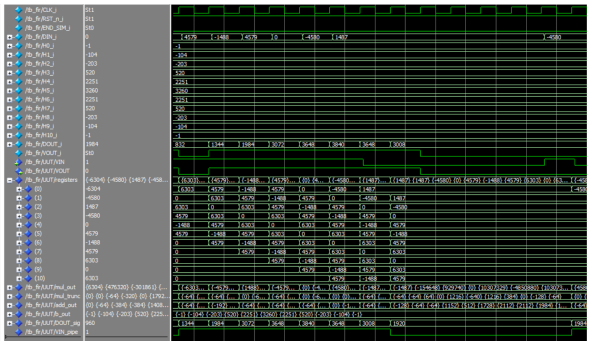

Figure 1.5: Detail on the moment FIR processing is deactivated. Note that Dout is constant during deactivation.

- Total cell area: 10880.730077
- Total Dynamic Power consumption: 90.01 uW
- Total Power consumption : 322.03 uW

The following tables highlight the result of the synthesis procedure, i.e. timing analysis in 1.2.2, resulting area in 1.2.2 and power consumption in **??**.

Timing analysis report

```
data arrival time                                          2.90

clock CLK (rise edge)                          3.00        3.00
clock network delay (ideal)                    0.00        3.00
clock uncertainty                             -0.07        2.93
DOUT_reg/reg_reg[13]/CK (DFFR_X1)              0.00        2.93 r
library setup time                            -0.03        2.90
data required time                                        2.90
-----------------------------------------------------------------------------
```

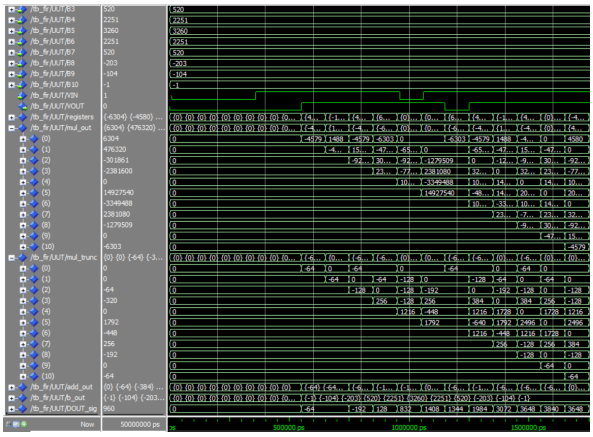

Figure 1.6: Detail on the FIR precision reduction implementation, acting on the multipliers' output

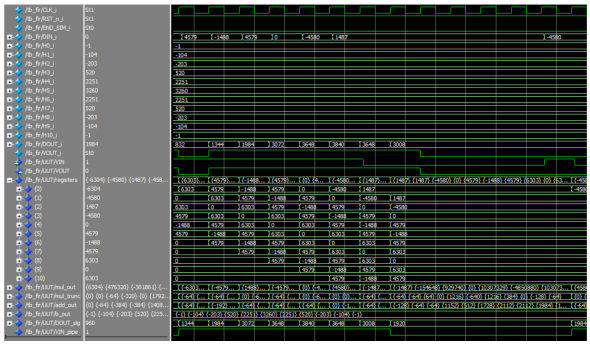

Figure 1.7: Detail on the moment FIR processing is deactivated. Note that Dout is constant during deactivation.

```
  data required time                                                    2.90
  data arrival time                                                    -2.90
  ---------------------------------------------------------------------------
  slack (MET)                                                           0.00
```

Area analysis report

```
****************************************
Report : area
Design : FIR_1
Version: S-2021.06-SP4
Date   : Mon Nov 13 11:29:58 2023
****************************************

Library(s) Used:

NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
```

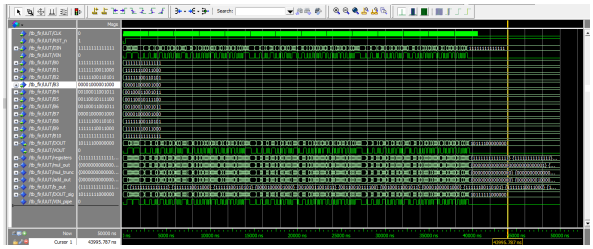

Figure 1.8: Full standard architecture simulation

```
NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         1617
Number of nets:                          7979
Number of cells:                         5865
Number of combinational cells:           5431
Number of sequential cells:               347
Number of macros/black boxes:               0
Number of buf/inv:                        659
Number of references:                      54

Combinational area:               9054.374021
Buf/Inv area:                      410.172001
Noncombinational area:            1826.356056
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 10880.730077
Total area:                 undefined
```

Power analysis report

```
****************************************
Report : power
Design : FIR
Version: S-2021.06-SP4
Date   : Mon Nov 13 20:58:35 2023
****************************************

Library(s) Used:

NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
NangateOpenCellLibrary_typical_ecsm_nowlm.db)


Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top
```

Table 1.2: POST SYNTHESIS ANALYSIS: A is the area, P is the power consumption and T is the simulation time.

$f_M = 333MHz$	$A = 10880.73um^2$	$P = 322.0314uW$	$T = 2.90ns$
$f_M/2 = 167MHz$	$A = 10882.19um^2$	$P = 288.55uW$	$T = 3.81ns$

```
Design        Wire Load Model            Library
------------------------------------------------
FIR                    5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  48.9568 uW   (54%)
  Net Switching Power  =  41.0536 uW   (46%)
                          ---------
Total Dynamic Power    =  90.0104 uW  (100%)

Cell Leakage Power     = 232.0211 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      2.8282           3.8209          1.3244e+03            7.9736  (   2.48%)
register          16.0167           5.0695          2.8755e+04           49.8409  (  15.48%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational     30.1119          32.1631          2.0194e+05          264.2169  (  82.05%)
------------------------------------------------------------------------------------------------
Total             48.9568 uW       41.0535 uW       2.3202e+05 nW       322.0314 uW
1
```

1.2.3 Explanations, comparisons and comments

As it can be observed by the provided reports' extracts and the aforementioned synthesis results, the FIR filter reaches better performance when working at the higher frequency f_M, at the cost of a higher power consumption.

For both the cell area and the delay, lower values have been achieved. On the other hand, the synthesized FIR filter provided with $f_M/2$ results to be slower and has a slightly bigger cell size, with the main achievement of a lower power dissipation. In conclusion, a possible choice between the two version could be considered as purely application-specific.

1.2.4 Place and route

Once the synthesis step is complete, we performed the Place and Route procedure which yielded the result reported in Fig.8.

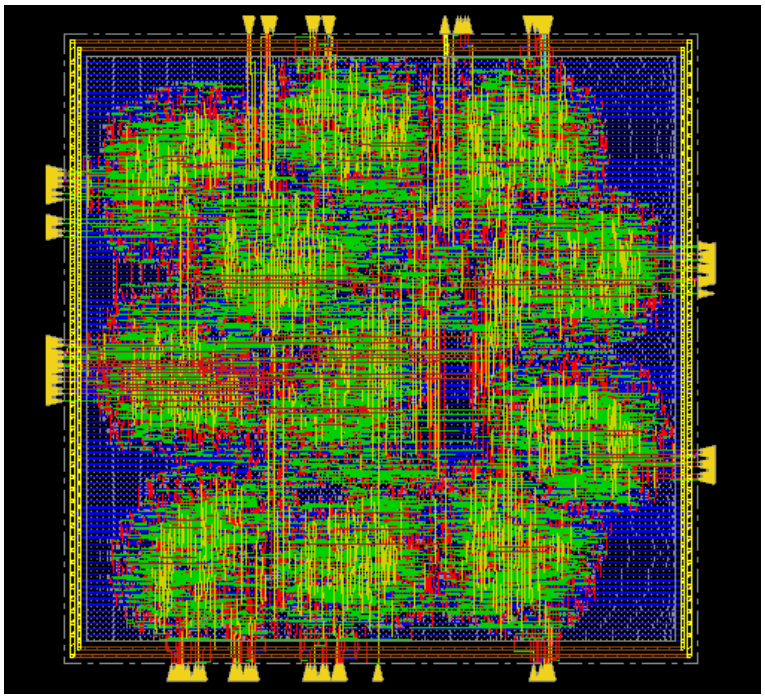

Figure 1.9: Figure 8: FIR filter - final view

The following report extracts show a correct behaviour as there are no timing violation (timeDesign Summary table for both setup and hold modes).

TimeDesign Summary - Setup mode

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg |reg2cgate| default |
+--------------------+---------+---------+---------+---------+
|           WNS (ns):|  3.555  |  3.555  |  5.606  |  5.270  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |
```

```
|    Violating Paths:|    0    |    0    |    0    |    0    |
|          All Paths:|   674   |   149   |   22    |   503   |
+--------------------+---------+---------+---------+---------+


+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 58.439%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

TimeDesign Summary: Hold mode

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg |reg2cgate| default |
+--------------------+---------+---------+---------+---------+
|           WNS (ns):|  0.141  |  0.141  |  0.279  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |
|          All Paths:|   171   |   149   |   22    |    0    |
+--------------------+---------+---------+---------+---------+

Density: 58.439%
       (100.000% with Fillers)
------------------------------------------------------------
```

The power consumption estimation has been performed after the place and route stage, too. The final results are shown in the following report extract.

Power consumption estimation post-routing

```
Design: FIR
Power Units = 1mW
Time Units = 1e-09 secs
```

Table 1.3: POST ROUTING ANALYSIS: A is the area, P is the power consumption and T is the simulation time.

$$f_M/2 = 167MHz \;\Big|\; A = 10882.19um^2 \;\Big|\; P = 318.84uW \;\Big|\; T = 3.81ns$$

```
--------------------------------------------------------------------------------

Total Power
--------------------------------------------------------------------------------
Total Internal Power:        0.05229544     16.4023%
Total Switching Power:       0.04333579     13.5921%
Total Leakage Power:         0.22319939     70.0056%
Total Power:                 0.31883062
--------------------------------------------------------------------------------
```

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.01748	0.005421	0.02836	0.05126	16.08
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.03181	0.03342	0.1934	0.2587	81.13
Clock (Combinational)	0.0002791	0.001116	8.025e-05	0.001475	0.4627
Clock (Sequential)	0.002728	0.003384	0.001316	0.007428	2.33
Total	0.0523	0.04334	0.2232	0.3188	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	1.1	0.0523	0.04334	0.2232	0.3188	100

Clock	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
CLK	0.003007	0.004499	0.001397	0.008903	2.793
Total (excluding duplicates)	0.003007	0.004499	0.001397	0.008903	2.793

Results of the place and route are shown in Table 1.5.

As shown by the data above, two power analysis have been executed, both after the Design Compiler synthesis and by the Place and Route phase through Innovus.

It is noticeable that we obtained two very similar results : 322.03 uW (by Design Vision) and 318.8 uW (by Cadence Innovus). Probably it could be stated that the second value is somewhat

more realistic due to the analysis post routing, which considers also more detailed parameters such as interconnections lines and other parasitic entities, but this proves that the first power estimation is really sophisticated.

1.3 Advanced architecture development

To improve the performance of the FIR filter, two advanced methods have been applied, concurrently:

- **Pipelining**: it consists in inserting pipeline registers along a feed-forward cutset. The goal is to reduce a critical path by breaking it into smaller paths, leading to a latency reduction and hence in a higher throughput
- **Unfolding**: it is a strategy that delves into maximizing algorithmic parallelism to optimize computational efficiency. This technique essentially entails expanding or "unfolding" the algorithm, allowing multiple instances of its computation to occur concurrently. Instead of processing a single input at a time, the algorithm is replicated and aligned to handle multiple inputs simultaneously.

The design of the advanced version of the FIR filter has been carried out in the following steps :

1. Initially, the standard FIR filter has been enhanced with an *unfolding* technique of degree 3, meaning that the overall system handles 3 inputs and produces 3 outputs at the same time, modifying the internal interconnections to exploit the commonalities among the delayed versions of the inputs (scheme is shown in Figure 1.12).

   In order to produce the architecture, a "by-hand" approach has been followed instead of the classical systematic one that involves more steps. This is due to the overall simplicity and repeatability of the structure, because although the filter is of grade 10, rewriting the equations of the 3 outputs reveals to be quite feasible.

An example is the following expression, only relative to the first output channel:

$$
\begin{aligned}
y[3k] &= b_0 \cdot x[3k] \\
&+ b_1 \cdot x[3k-1] \\
&+ b_2 \cdot x[3k-2] \\
&+ b_3 \cdot x[3k-3] \\
&+ b_4 \cdot x[3k-4] \\
&+ b_5 \cdot x[3k-5] \\
&+ b_6 \cdot x[3k-6] \\
&+ b_7 \cdot x[3k-7] \\
&+ b_8 \cdot x[3k-8] \\
&+ b_9 \cdot x[3k-9] \\
&+ b_{10} \cdot x[3k-10] \\
&\Downarrow \\
y[3k] &= b_0 \cdot x[3k] \\
&+ b_1 \cdot x[3(k-1)+2] \\
&+ b_2 \cdot x[3(k-1)+1] \\
&+ b_3 \cdot x[3(k-1)] \\
&+ b_4 \cdot x[3(k-2)+2] \\
&+ b_5 \cdot x[3(k-2)+1] \\
&+ b_6 \cdot x[3(k-2)] \\
&+ b_7 \cdot x[3(k-3)+2] \\
&+ b_8 \cdot x[3(k-3)+1] \\
&+ b_9 \cdot x[3(k-3)] \\
&+ b_{10} \cdot x[3(k-4)]
\end{aligned}
$$

It is possible to notice that the addends of the final expression are delayed versions of each of the three input channels, in alternated order. The same steps have been performed to compute the revisited expressions for the other 2 channels, highlighting the relationships with the other 2 inputs and finally coming with the correct HW implementation.

2. After the unfolding step was completed, a one-stage and a two-stage *pipelining* optimizations were implemented, as shown in Figure 1.10 and 1.11. As shown by the second picture, the aim was to split the serial chain of 10 adders into 2 shorter ones of 5 adders each, while maintaining the same idea of the other simpler implementation of separating the multiplier from the adders. However, the one-stage synthesis revealed that the critical path of the system passed through the multipliers, meaning that any further pipeline optimization efforts would result inconclusive and needlessly expensive. To demonstrate this, on the Appendix B the complete report timing of the 2-stage pipelining implementation is presented.

Finally, as just motivated, the final architecture of the advanced version of the FIR filter is shown in Figure 1.13.

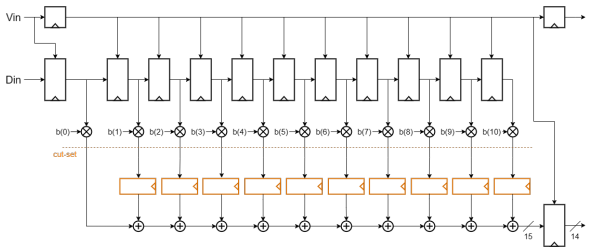

Figure 1.10: Advanced architecture implementation of a FIR filter design following the specification parameter, single-stage pipelining optimization

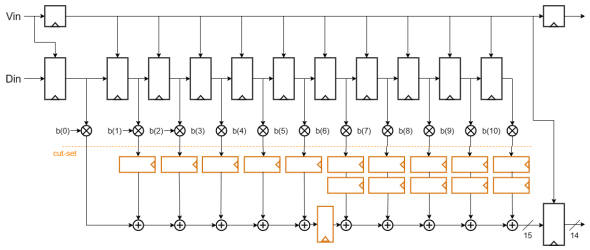

Figure 1.11: Advanced architecture implementation of a FIR filter design following the specification parameter, double-stage pipelining optimization

Simulation

To process all the samples the simulation lasts less than 15 us, demonstrating, at least logically, the great improvement in terms of throughput that the advanced architecture has produced. In fact, this version presents an overall improvement in terms of clock cycles of about 300% : in fact, the other version's simulation lasted about 40 us, while this one is about a third of it. The following figures illustrate the behaviour of the filter with a focus on the multipliers output.

1.3.1 Logic synthesis

Reports extracts showing slack met and power consumption when clock gate is enabled and frequency is equal to f_M are shown in the following extracts.

Timing Analysis: slack met detail

```
data arrival time                                          3.20

clock CLK (rise edge)                              3.30    3.30
clock network delay (ideal)                        0.00    3.30
clock uncertainty                                 -0.07    3.23
x3k2_pipe1_i_8/reg_reg[13]/CK (DFFR_X1)            0.00    3.23 r
library setup time                                -0.03    3.20
data required time                                         3.20
-----------------------------------------------------------------------
data required time                                         3.20
data arrival time                                         -3.20
-----------------------------------------------------------------------
slack (MET)                                                0.00
```

Area Analysis

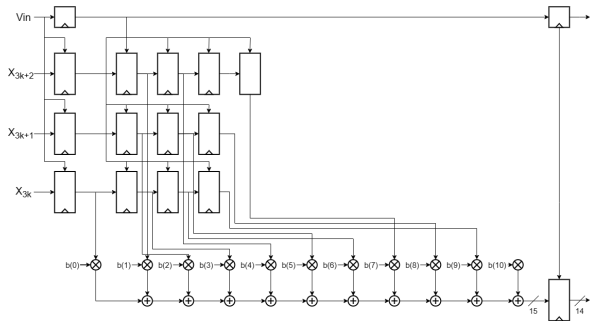

Figure 1.12: Advanced architecture implementation of a FIR filter design following the specification parameter, 3 times unfolded optimization. Here is reported only the computational section of one of the three output channels

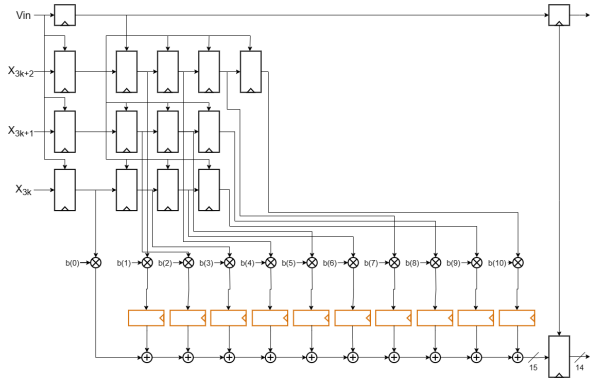

Figure 1.13: Final design of advanced architecture implementation of a FIR filter design following the specification parameter

```
Library(s) Used:

NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         5656
Number of nets:                         22670
Number of cells:                        15145
Number of combinational cells:          13897
Number of sequential cells:               965
Number of macros/black boxes:               0
Number of buf/inv:                       1883
Number of references:                     129

Combinational area:              26242.496122
Buf/Inv area:                     1112.411999
Noncombinational area:            5108.796163
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)
```

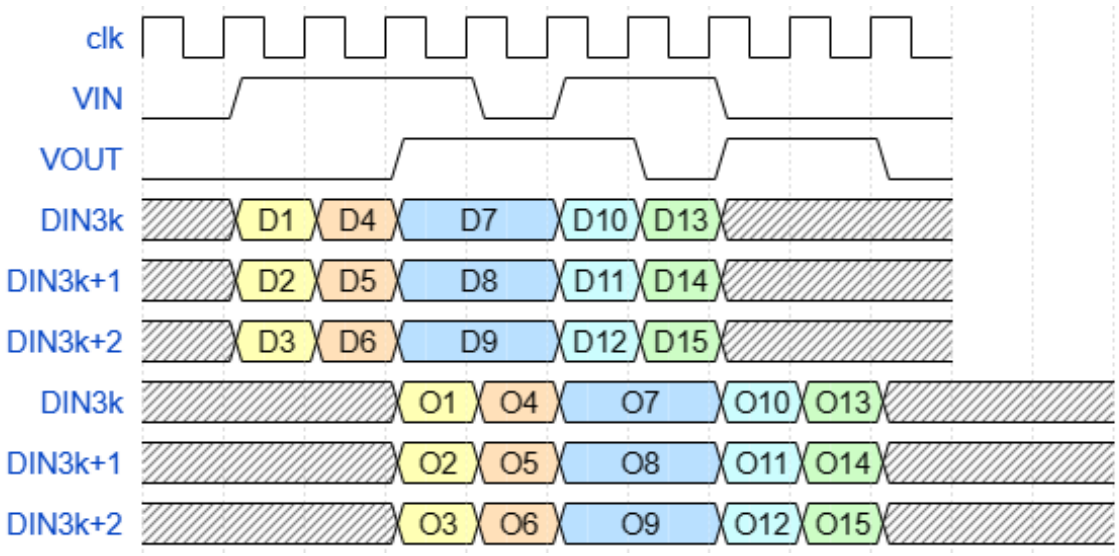

Figure 1.14: Final design timing diagram

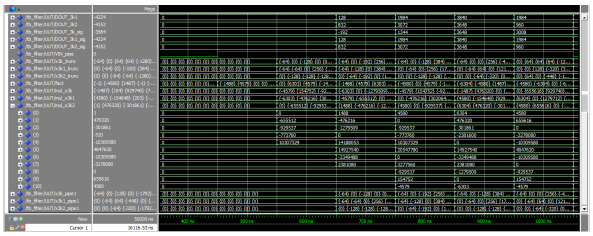

Figure 1.15: Detail on the multipliers output

```
Total cell area:                31351.292285
Total area:                   undefined
```

Power Consumption Estimation

```
Library(s) Used:

NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
NangateOpenCellLibrary_typical_ecsm_nowlm.db)


Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design         Wire Load Model             Library
------------------------------------------------
FIR_PIPE1               5K_hvratio_1_1     NangateOpenCellLibrary
```

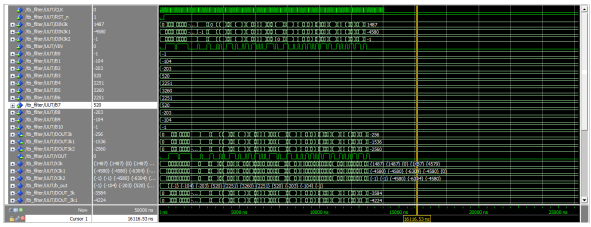

Figure 1.16: Full advanced simulation

Table 1.4: POST SYNTHESIS ANALYSIS: A is the area, P is the power consumption and T is the simulation time.

$$f_M = 303MHz \mid A = 31351.29um^2 \mid P = 897.37uW \mid T = 3.20ns$$

```
Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 150.0003 uW   (59%)
  Net Switching Power  = 104.7189 uW   (41%)
                         ---------
Total Dynamic Power    = 254.7192 uW  (100%)

Cell Leakage Power     = 642.6498 uW

Information: report_power power group summary does not include estimated
clock tree power. (PWR-789)


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    ) Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register           0.0000           0.0000              0.0000             0.0000  (   0.00%)
sequential        55.7978          27.4728          8.5721e+04           168.9920  (  18.83%)
combinational     94.2020          77.2450          5.5693e+05           728.3770  (  81.17%)
--------------------------------------------------------------------------------------------------
Total            149.9998 uW       104.7178 uW     6.4265e+05 nW        897.3690 uW
```

Results of the synthesis are shown in Table 1.4.

1.3.2 Place and route

After the Place and Route stage, the achieved result can be seen in Figures 8.

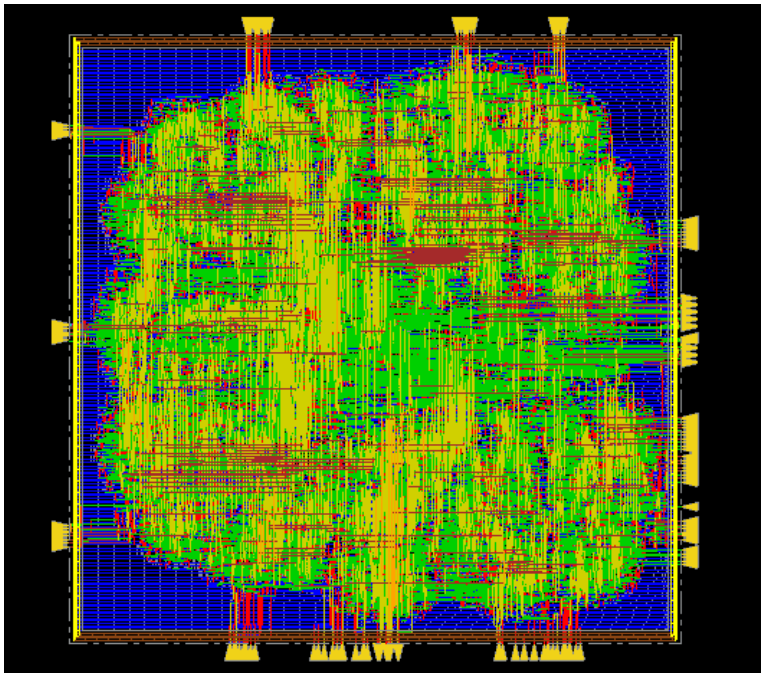

Figure 1.17: Figure 8: Advanced FIR filter - final view

Snapshots showing no timing violation (timeDesign Summary table for both setup and hold modes) and power consumption are shown in the following extracts.
TimeDesign Summary - Setup mode

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg |reg2cgate| default |
+--------------------+---------+---------+---------+---------+
|           WNS (ns):|  3.909  |  3.909  |  6.213  |  5.890  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |
|          All Paths:|  1393   |   447   |   59    |   887   |
+--------------------+---------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)       |     0       |      0 (0)       |
```

```
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 58.282%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

TimeDesign Summary: Hold mode

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------
```

Hold mode	all	reg2reg	reg2cgate	default
WNS (ns):	0.179	0.179	0.278	0.000
TNS (ns):	0.000	0.000	0.000	0.000
Violating Paths:	0	0	0	0
All Paths:	506	447	59	0

Power Consumption

```
Design: FIR_PIPE1
Power Units = 1mW
Time Units = 1e-09 secs


Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:        0.14739199     16.7768%
Total Switching Power:       0.10818836     12.3145%
Total Leakage Power:         0.62296657     70.9087%
Total Power:                 0.87854691
-----------------------------------------------------------------------------------------
```

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.04456	0.02044	0.07703	0.142	16.17
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.09521	0.07622	0.5423	0.7137	81.24
Clock (Combinational)	0.0006347	0.002769	0.0001829	0.003587	0.4082
Clock (Sequential)	0.006984	0.008763	0.003455	0.0192	2.186

Table 1.5: POST ROUTING ANALYSIS: A is the area, P is the power consumption and T is the simulation time.

$$f_M/2 = 167MHz \;\Big|\; A = 31351.29um^2 \;\Big|\; P = 878.55uW \;\Big|\; T = 3.20ns$$

```
-------------------------------------------------------------------------------------
Total                                0.1474       0.1082        0.623       0.8785          100
-------------------------------------------------------------------------------------


Rail                    Voltage   Internal   Switching     Leakage       Total  Percentage
                                  Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------
VDD                         1.1     0.1474      0.1082       0.623      0.8785          100


Clock                             Internal   Switching     Leakage       Total  Percentage
                                  Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------
CLK                               0.007619     0.01153    0.003638     0.02279       2.594
-------------------------------------------------------------------------------------
Total (excluding duplicates)      0.007619     0.01153    0.003638     0.02279       2.594
-------------------------------------------------------------------------
```

As in the previous case of the standard FIR filter, Cadence Innovus power estimator produced a very consistent result because it is very similar to the one produced by the synthesis estimator (897 uW vs 878 uW). Results of the place and route are shown in Table 1.5.

1.4 Final considerations

As expected, by the results obtained using both Design Vision and Cadence Innovus for synthesis and routing, the advanced architecture produce some very good results in terms of timing and throughput, but on the other hand the increase in area and power consumption must also be considered.

1.4.1 Timing Performance

The timing and throughput performance is obviously radically improved with the enhanced architecture, but however the critical path has increased by a non-negligible factor when the improvements have been applied. In fact, the initial architecture had a critical path of 2.90 ns, but when the first *unfolding* technique has been implemented, the critical path increased to 3.9 ns, quite unexpectedly (see Appendix A).

This is probably due to the higher fan-out that the gates must be support and the longer path the data has to pass through, hence more power is required and more propagation time as a consequence. With the aid of the *pipelining* technique however, we managed to lower the value to 3.2 ns, thanks to the splitting action between the series of adders and the multiplier.

As reported above, the 2-stage pipeline version did not bring any advantage in terms of timing since the improvements produced with the single stage were the ones already expected.

It must be also noted that, as requested, it was not possible to insert internal pipeline stages within the arithmetic units, especially the multiplier. In fact, this type of technique applied within the combinational paths would have surely offered many advantages.

1.4.2 Area

The advanced architecture reported to have almost exactly 3 times the area of the first version : this is exactly what we expected, because the unfolding method duplicates the same number of resources for the number of parallel channels. In our case we went from about 10000 cells in the first case and ended up with 31000 in the last case. The pipeline implementation does not increase much the number of cells with respect of the other method used since it only consists of adding some registers.

This is reported in the Appendix A, where the area report of the filter with only the unfolding technique is shown : 27000 cells in total, almost the ones used by the final architecture.

1.4.3 Power consumption

In the case of power consumption we fall in the same scenario of the Area estimation: the final architecture is reported to consume almost 3 times as much as the standard one (897uW vs 322 uW). This is due to the 3-fold increase in area and hence an equal factor in terms of power increase is expected.

APPENDIX A

UNFOLDING - reports

Area analysis

```
****************************************
Report : area
Design : FIR_3
Version: S-2021.06-SP4
Date   : Sat Nov 11 17:16:58 2023
****************************************

Library(s) Used:

NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         3115
Number of nets:                         18943
Number of cells:                        13988
Number of combinational cells:          13427
Number of sequential cells:               437
Number of macros/black boxes:               0
Number of buf/inv:                       1805
Number of references:                      79

Combinational area:              25192.328117
Buf/Inv area:                     1040.326002
Noncombinational area:            2343.726077
Macro/Black Box area:                0.000000
Net Interconnect area:           undefined  (Wire load has zero net area)


Total cell area:                 27536.054194
Total area:                      undefined
```

Timing analysis

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : FIR_3
Version: S-2021.06-SP4
Date   : Sat Nov 11 17:16:58 2023
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: B_1/reg_reg[3]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: DOUT3k_reg/reg_reg[13]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FIR_3              5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock CLK (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  B_1/reg_reg[3]/CK (DFFR_X1)                             0.00       0.00 r
  B_1/reg_reg[3]/Q (DFFR_X1)                              0.10       0.10 r
  B_1/data_out[3] (REG_NBIT14_28)                         0.00       0.10 r
  U198/Z (BUF_X1)                                         0.15       0.25 r
  mult_142_G2/a[3] (FIR_3_DW_mult_tc_27)                  0.00       0.25 r
  mult_142_G2/U475/ZN (INV_X1)                            0.08       0.33 f
  mult_142_G2/U439/ZN (INV_X1)                            0.14       0.46 r
  mult_142_G2/U706/ZN (XNOR2_X1)                          0.09       0.55 r
  mult_142_G2/U723/ZN (OAI22_X1)                          0.05       0.60 f
  mult_142_G2/U108/S (HA_X1)                              0.08       0.68 f
  mult_142_G2/U722/ZN (AOI222_X1)                         0.10       0.78 r
  mult_142_G2/U728/ZN (INV_X1)                            0.03       0.81 f
  mult_142_G2/U717/ZN (AOI222_X1)                         0.09       0.90 r
  mult_142_G2/U718/ZN (INV_X1)                            0.03       0.93 f
  mult_142_G2/U715/ZN (AOI222_X1)                         0.09       1.02 r
  mult_142_G2/U732/ZN (INV_X1)                            0.03       1.05 f
  mult_142_G2/U712/ZN (AOI222_X1)                         0.09       1.14 r
  mult_142_G2/U733/ZN (INV_X1)                            0.03       1.17 f
  mult_142_G2/U709/ZN (AOI222_X1)                         0.09       1.26 r
  mult_142_G2/U727/ZN (INV_X1)                            0.03       1.29 f
```

```
mult_142_G2/U726/ZN (AOI222_X1)                          0.09       1.38 r
mult_142_G2/U719/ZN (INV_X1)                             0.03       1.41 f
mult_142_G2/U704/ZN (AOI222_X1)                          0.09       1.50 r
mult_142_G2/U711/ZN (INV_X1)                             0.03       1.53 f
mult_142_G2/U710/ZN (AOI222_X1)                          0.09       1.63 r
mult_142_G2/U730/ZN (INV_X1)                             0.03       1.65 f
mult_142_G2/U705/ZN (AOI222_X1)                          0.09       1.75 r
mult_142_G2/U731/ZN (INV_X1)                             0.03       1.77 f
mult_142_G2/U707/ZN (AOI222_X1)                          0.09       1.87 r
mult_142_G2/U725/ZN (INV_X1)                             0.03       1.89 f
mult_142_G2/U724/ZN (AOI222_X1)                          0.09       1.99 r
mult_142_G2/U713/ZN (INV_X1)                             0.03       2.01 f
mult_142_G2/U708/ZN (AOI222_X1)                          0.09       2.11 r
mult_142_G2/U714/ZN (INV_X1)                             0.03       2.14 f
mult_142_G2/U716/ZN (AOI222_X1)                          0.11       2.24 r
mult_142_G2/U734/ZN (OAI222_X1)                          0.07       2.31 f
mult_142_G2/U720/ZN (AOI222_X1)                          0.11       2.42 r
mult_142_G2/U735/ZN (OAI222_X1)                          0.07       2.49 f
mult_142_G2/U11/CO (FA_X1)                               0.10       2.58 f
mult_142_G2/U10/CO (FA_X1)                               0.09       2.67 f
mult_142_G2/U9/S (FA_X1)                                 0.14       2.81 r
mult_142_G2/product[21] (FIR_3_DW_mult_tc_27)            0.00       2.81 r
add_7_root_add_0_root_add_160_10/U1_8/S (FA_X1)          0.12       2.93 f
add_2_root_add_0_root_add_160_10/U1_8/S (FA_X1)          0.15       3.08 r
add_1_root_add_0_root_add_160_10/U1_8/S (FA_X1)          0.12       3.20 f
add_0_root_add_0_root_add_160_10/U1_8/CO (FA_X1)         0.11       3.30 f
U86/Z (XOR2_X1)                                          0.08       3.39 f
U286/ZN (AOI22_X1)                                       0.06       3.45 r
U285/ZN (INV_X1)                                         0.03       3.48 f
add_0_root_add_0_root_add_160_10/U1_10/CO (FA_X1)        0.09       3.56 f
add_0_root_add_0_root_add_160_10/U1_11/CO (FA_X1)        0.09       3.66 f
add_0_root_add_0_root_add_160_10/U1_12/CO (FA_X1)        0.09       3.75 f
add_0_root_add_0_root_add_160_10/U1_13/S (FA_X1)         0.13       3.88 r
DOUT3k_reg/data_in[13] (REG_NBIT14_15)                   0.00       3.88 r
DOUT3k_reg/reg_reg[13]/D (DFFR_X1)                       0.01       3.88 r
data arrival time                                                   3.88

clock CLK (rise edge)                                    4.00       4.00
clock network delay (ideal)                              0.00       4.00
clock uncertainty                                       -0.07       3.93
DOUT3k_reg/reg_reg[13]/CK (DFFR_X1)                      0.00       3.93 r
library setup time                                      -0.03       3.90
data required time                                                  3.90
--------------------------------------------------------------------------
data required time                                                  3.90
data arrival time                                                  -3.88
--------------------------------------------------------------------------
slack (MET)                                                         0.01
```

APPENDIX B

2-STAGE PIPELINING - reports

Area analysis

```
****************************************
Report : area
Design : FIR_PIPE2
Version: S-2021.06-SP4
Date   : Mon Nov 13 15:17:38 2023
****************************************

Library(s) Used:

NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         6367
Number of nets:                         23802
Number of cells:                        15572
Number of combinational cells:          13982
Number of sequential cells:              1253
Number of macros/black boxes:               0
Number of buf/inv:                       1958
Number of references:                     148


Combinational area:              26359.536121
Buf/Inv area:                     1168.271998
Noncombinational area:            6617.016209
Macro/Black Box area:                0.000000
Net Interconnect area:           undefined  (Wire load has zero net area)


Total cell area:                 32976.552331
Total area:                      ndefined
```

Timing analysis

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : FIR_PIPE2
Version: S-2021.06-SP4
Date   : Mon Nov 13 15:17:38 2023
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: B_8/reg_reg[3]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: x3k2_pipe1_i_8/reg_reg[13]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FIR_PIPE2          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
  clock CLK (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  B_8/reg_reg[3]/CK (DFFR_X1)                              0.00       0.00 r
  B_8/reg_reg[3]/Q (DFFR_X1)                               0.10       0.10 r
  B_8/data_out[3] (REG_NBIT14_21)                          0.00       0.10 r
  U140/Z (BUF_X1)                                          0.15       0.25 r
  mult_159_G9/a[3] (FIR_PIPE2_DW_mult_tc_17)               0.00       0.25 r
  mult_159_G9/U676/ZN (INV_X1)                             0.04       0.29 f
  mult_159_G9/U445/Z (BUF_X2)                              0.05       0.34 f
  mult_159_G9/U432/ZN (INV_X1)                             0.12       0.46 r
  mult_159_G9/U687/ZN (XNOR2_X1)                           0.08       0.55 r
  mult_159_G9/U688/ZN (OAI22_X1)                           0.04       0.58 f
  mult_159_G9/U108/S (HA_X1)                               0.08       0.66 f
  mult_159_G9/U711/ZN (AOI222_X1)                          0.11       0.77 r
  mult_159_G9/U712/ZN (INV_X1)                             0.03       0.80 f
  mult_159_G9/U713/ZN (AOI222_X1)                          0.09       0.89 r
  mult_159_G9/U715/ZN (INV_X1)                             0.03       0.92 f
  mult_159_G9/U704/ZN (AOI222_X1)                          0.09       1.01 r
  mult_159_G9/U722/ZN (INV_X1)                             0.03       1.04 f
  mult_159_G9/U720/ZN (AOI222_X1)                          0.09       1.13 r
  mult_159_G9/U718/ZN (INV_X1)                             0.03       1.16 f
  mult_159_G9/U696/ZN (AOI222_X1)                          0.09       1.25 r
```

```
mult_159_G9/U706/ZN (INV_X1)                              0.03       1.28 f
mult_159_G9/U691/ZN (AOI222_X1)                           0.11       1.39 r
mult_159_G9/U695/ZN (OAI222_X1)                           0.07       1.46 f
mult_159_G9/U701/ZN (AOI222_X1)                           0.10       1.55 r
mult_159_G9/U723/ZN (INV_X1)                              0.03       1.58 f
mult_159_G9/U717/ZN (AOI222_X1)                           0.09       1.68 r
mult_159_G9/U716/ZN (INV_X1)                              0.03       1.70 f
mult_159_G9/U703/ZN (AOI222_X1)                           0.09       1.80 r
mult_159_G9/U710/ZN (INV_X1)                              0.03       1.82 f
mult_159_G9/U709/ZN (AOI222_X1)                           0.09       1.92 r
mult_159_G9/U705/ZN (INV_X1)                              0.03       1.94 f
mult_159_G9/U416/ZN (AOI222_X1)                           0.09       2.04 r
mult_159_G9/U707/ZN (INV_X1)                              0.03       2.06 f
mult_159_G9/U708/ZN (AOI222_X1)                           0.11       2.17 r
mult_159_G9/U721/ZN (OAI222_X1)                           0.07       2.24 f
mult_159_G9/U725/ZN (AOI222_X1)                           0.11       2.35 r
mult_159_G9/U724/ZN (OAI222_X1)                           0.07       2.42 f
mult_159_G9/U11/CO (FA_X1)                                0.10       2.51 f
mult_159_G9/U10/CO (FA_X1)                                0.09       2.60 f
mult_159_G9/U9/CO (FA_X1)                                 0.09       2.69 f
mult_159_G9/U8/CO (FA_X1)                                 0.09       2.79 f
mult_159_G9/U7/CO (FA_X1)                                 0.09       2.88 f
mult_159_G9/U6/CO (FA_X1)                                 0.09       2.97 f
mult_159_G9/U5/CO (FA_X1)                                 0.09       3.06 f
mult_159_G9/U4/S (FA_X1)                                  0.13       3.19 r
mult_159_G9/product[26] (FIR_PIPE2_DW_mult_tc_17)         0.00       3.19 r
x3k2_pipe1_i_8/data_in[13] (REG_NBIT15_25)                0.00       3.19 r
x3k2_pipe1_i_8/reg_reg[13]/D (DFFR_X1)                    0.01       3.20 r
data arrival time                                                    3.20

clock CLK (rise edge)                                     3.30       3.30
clock network delay (ideal)                               0.00       3.30
clock uncertainty                                        -0.07       3.23
x3k2_pipe1_i_8/reg_reg[13]/CK (DFFR_X1)                   0.00       3.23 r
library setup time                                       -0.03       3.20
data required time                                                   3.20
-----------------------------------------------------------------------------
data required time                                                   3.20
data arrival time                                                   -3.20
-----------------------------------------------------------------------------
slack (MET)                                                          0.0
```