Politecnico di Torino

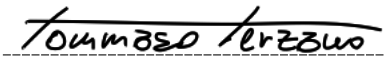
Collegio di Elettronica, Telecomunicazioni e Fisica

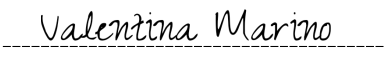
Report for the course
Integrated Systems Architecture

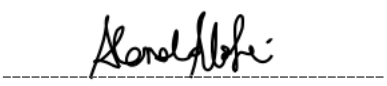
Master degree in Electrical Engineering

Group: 34

Names: A. Marchei, V. Marino, T. Terzano

Signature 1: 

Signature 2: 

Signature 3: 

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Contents

CHAPTER 1

Lab 2: digital arithmetic

1.1 FPU model

1.1.1 Simulation

The FPU has been stimulated with the following numbers, corresponding to the hexadecimal configuration shown in Table 1.1. In order to simulate a larger series of results, we modified the given testbench providing four additional value pairs, including floating point numbers.

Figure 1.1 shows a snapshot of the simulation. As it can be observed, stimulating the FPU with the numbers shown in Table 1.1 the results are exactly the expected ones.

1.1.2 Synthesis

For each one of the five required synthesis, the respective area and maximum frequency of the FPU have been found.
Table 1.2 shows the results of the experiments required in the assignment.

Table 1.1: Simulation Results

a		b		r	
15	0x4B80	204	0x5A60	3060	0x69FA
204	0x5A60	1024	0x6400	208896	0x7C00
1024	0x6400	-15	0xCB80	-15360	0xF380
-15	0xCB80	-204	0xDA60	3060	0x69FA
-204	0xDA60	-1024	0xE400	-208896	0x7C00
-1024	0xE400	15	0x4B80	-15360	0xF380
Added					
44	0x5180	-120.5	0xD788	-5304	0xED2E
-120.5	0xD788	-7	0xC700	843.5	0x6297
2.25	0x4080	44	0x5180	99	0x5630
-7	0xC700	2.25	0x4080	-15.75	0xCBE0

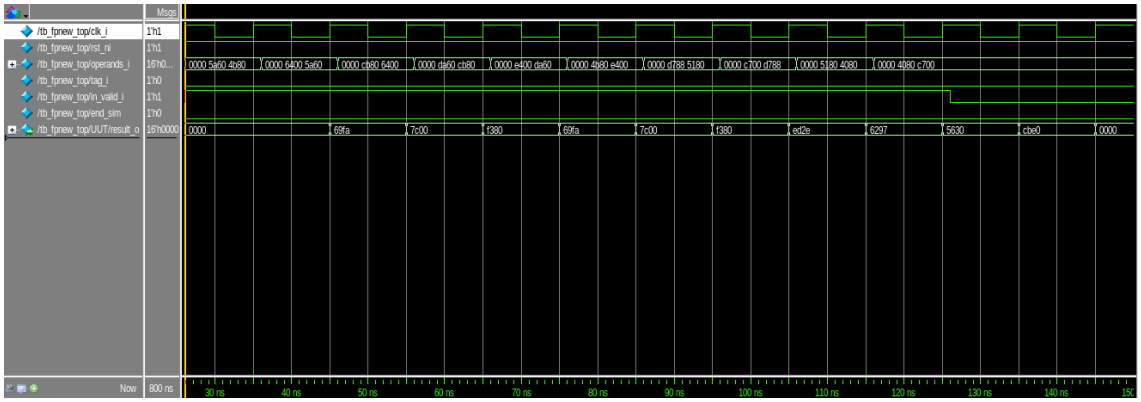

Figure 1.1: FPU simulation - waveforms

Table 1.2: Synthesis Results

Synthesis	*Area*	*Maximum Frequency*
1. *compile*	$4343.78um^2$	$285.71MHz$
2. *compile*, *optimize_registers*	$4308.93um^2$	$454.55MHz$
3. *compile_ultra*	$158.80um^2$	$757.576MHz$
4. *compile*, *optimize_register* (CSA)	$4107.31um^2$	$440.53MHz$
5. *compile*, *optimize_register* $(PPARCH)$	$4160.77um^2$	$333.33MHz$

1.1.3 Explanations, comparisons and comments

As it can be observed from the first three synthesized cases, by means of the suggested optimization commands it has been possible to reach higher maximum frequencies and lower areas.
With the *optimize_registers* command, we have been able to reach a maximum frequency about 1.6 times higher than the first general case but a slightly lower value for the occupied area. On the other hand, in the third experiment, by means of the *compile_ultra* command we reached a maximum frequency about 2.7 times higher than the one achieved in the starting synthesis and an area which is about the 3.7% of the original one.
Moreover, as it is evident from the results of the last two experiments, by optimizing the registers and forcing Design Compiler to implement the Significands multiplier as a CSA multiplier we have been able to reach a maximum frequency about 1.32 times higher and a slightly lower area than the ones reached by forcing Design Compiler to implement a PPARCH multiplier.
In both cases, the achieved results are better than the ones of the very first experiment.
The full text of the report timing, report area and report resources commands have been added in A.
In order to verify the correctness of the behaviour of the system, the simulation of all the provided post synthesis netlists has been performed by means of a proper script, resulting in a behaviour conforming to the expected one.

1.2 R4-MBE multiplier

In order to implement the multiplication in Floating Point unit, it is required to only multiply the mantissas of the 2 operands, following adjustments of the exponents and the MSB to obtain valid results. In our case, the mantissa multiplier is performed by the Modified-Booth-Encoding Radix-4 Multiplier, that substitutes the "*" operator in the original SystemVerilog description of the unit

(fpnew_fma.sv file). Since we are dealing with the FP16 standard, each operand is represented as in Figure 1.2. As shown, the numbers are represented by splitting the value into three parts, the first is the sign bit, the second are 5 bits of the exponent and the third part is the mantissa. The mantissa is made up of the last 10 bits of the number plus a further bit, always with a value of 1, which is therefore omitted in the storing (hidden bits) but which must be used during the computation of the product. This requires that the R4-MBE produces 22-bits numbers and receives two 11-bits operands, but without needing a signed operation since the sign is managed through an external logic and because the 2 mantissas are always positive by definition. In the following sections, a detailed analysis of the multiplier is reported.

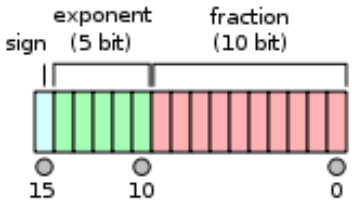

Figure 1.2: IEEE FP16 standard format

1.2.1 Radix 4 - Modified Booth Encoding

The approach of 'Booth Encoding' involves utilizing a broader range of digits for binary representation, aimed at minimizing the count of '1' bits in expressing a specific value, primarily in arithmetic computations between two numbers.

In traditional booth encoding, a series of high logic bits within a number is encoded by placing a '1' bit before (at the more significant position) the start of the sequence and a '-1' bit where the sequence concludes. By analyzing the bit values, the outcome remains consistent, but with fewer '1' bits at the logical level.

Consider the number 158, which in binary is 010011110: $(02^8) + (12^7) + (02^6) + (02^5) + (12^4) + (12^3) + (12^2) + (12^1) + (02^0)$

However, in booth encoding, it's represented as 1(-1)01000(-1)0: $(12^8) + (-12^7) + (02^6) + (12^5) + (02^4) + (02^3) + (02^2) + (-12^1) + (02^0)$

When using this number as a multiplier, reducing the '1' bits decreases the count of non-zero partial products to be summed, benefiting power efficiency, as these computations become unnecessary.

Incorporating modified booth encoding, which operates in tandem with a radix-n system (where n is greater than 2, thus encompassing a larger digit set), also enhances efficiency in terms of space. Fewer bits lead to fewer partial products and, consequently, fewer adders for these products.

Our multiplier module integrates booth encoding with a radix-4 scheme. It analyzes 3 bits of the multiplicand at a time, replacing them with an expanded set of digits: -2, -1, 0, 1, 2. This reduces the multiplicand's length to a half. The output from this encoding module includes a signal indicating the corresponding digit from the extended set (in absolute value) and another signal denoting whether the digit is positive or negative.

1.2.2 Partial Product Generator

In the preceding discussion, various multiples of the multiplicand A are necessary for the computation. For our scenario utilizing radix 4, these multiples include 0, 1A, and 2A. The multiplicand in its original form, 1A, is already available. Generating 2A is quite straightforward; it can be achieved by a single-position shift of the multiplicand. To ensure uniformity in parallel processing across all outputs

from the partial product generator, the output signal of this unit is designed to match the bit count required for the largest partial product, which is the final, or 6th, partial product. This might be 2A, but considering it is shifted two places for the earlier partial products, the total bit count becomes 11 bits (the base operand) plus 1 bit (for the possible 2A) plus 10 bits (two shifts for each of the five preceding partial products), culminating in a total of 22 bits for each partial product.

The table implemented by the Partial Product generator is shown in the following table :

X+1	X	X-1	Z	OUTPUT	SIGN
0	0	0	0	0	0
0	0	1	+A	A	0
0	1	0	+A	A	0
0	1	1	+2A	2A	0
1	0	0	-2A	$\overline{2A}$	1
1	0	1	-A	$\overline{A}$	1
1	1	0	-A	$\overline{A}$	1
1	1	1	0	0	1

Table 1.3: RADIX 4 Booth Selector Logic

The *x+1*, *x* and *x-1* represents the bits of each selected triplet of values that have to be encoded, and their output value reported in the table select a possible value for the partial product. The index of *x* at each iteration is increased by 2 with respect to the previous one, starting from the value 0 (the first *x* selects the LSB of the B operand of the multiplier). The *Output* columns specifies which value will be inserted in the corresponding row of each partial product, exploiting the fact that instead of writing the exact negative value could be instead be exploited the 2's complement by adding a 1 on the next partial product.

An example of a Modified Booth Encoder with radix-4 in case of a 16-bit operands is shown in Figure 1.3.

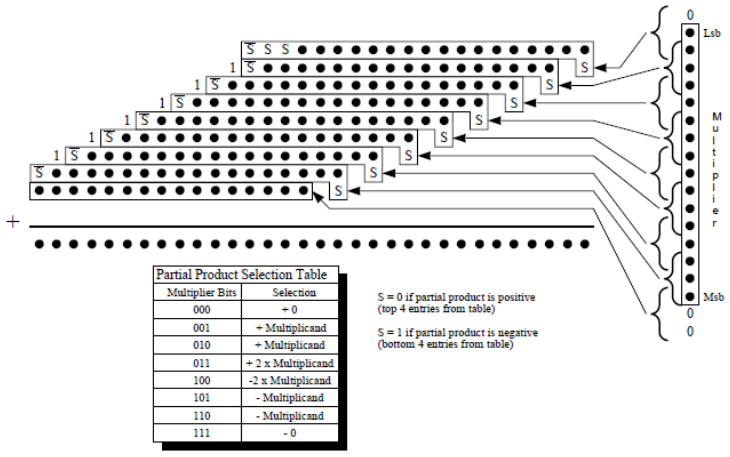

Figure 1.3: R4-MBE general implementation of 16-bits operands

In our case, since the parallelism of each input is 11 bits, 6 partial products were needed instead.

1.2.3 Dadda Tree

The process of accumulating partial products in multiplication operations can involve a variety of adder designs. This spectrum ranges from the more complex Ripple Carry Adders (RCAs), which

are characterized by their larger size and higher power requirements, to specialized tree adders such as Wallace and DADDA trees. These tree adders are particularly advantageous because they are customized to handle the exact amount of data present in the application, thereby making them not only more compact but also significantly more efficient in operation.

One of the standout features of the DADDA Tree is its strategic use of compressor elements. Unlike other methods, it employs these elements sparingly and only when they are absolutely essential. This judicious use of resources results in notable improvements in terms of both spatial efficiency and power consumption. However, this benefit comes with the trade-off of a more intricate and complex design process.

Determining when to introduce a compressor in the DADDA Tree, a key decision that impacts the number of bits, involves careful analysis. This analysis begins from the bottom or final stage and considers the maximum bit count possible at each stage. For the final calculation to be executed with a standard adder, irrespective of its specific implementation, the DADDA Tree's output must be constrained to just two numbers. This requirement limits the last stage to a maximum bit height of two. With a theoretical compression ratio of 1.5 between successive stages, it becomes possible to ascertain the maximum permissible heights for each stage. The analysis and calculations continue until identifying the first stage where the maximum size is either equal to or exceeds the number of partial products that need to be merged.

In a practical example, starting with two 11-bit numbers and representing the multiplier in Radix-4 notation leads to the creation of 6 partial products. This scenario necessitates a DADDA Tree composed of 4 stages, in addition to a final stage dedicated to summing.

The diagram that illustrates the DADDA Tree, which also finds application in the generation of SystemVerilog components, shows the inclusion of additional bits beyond the actual partial products. These extra bits are crucial as they extend the sign bit by three positions, thereby ensuring that all bits of the ensuing partial product are adequately covered. The S[x] signals, positioned on the right side of the diagram, play a vital role in the second step of generating negative numbers. These signals indicate '1' for a negative partial product and '0' for a positive one, thus integrating the sum of '1' LSB into the overall calculation and simplifying it to the extent that only one adder is required.

Our Dadda Tree implementation for the multiplier is shown in Figure 1.4.

The red rectangles represents FULL ADDERS, while the blue ones are HALF ADDERS.

A report for the number of resources used to produce 2 22-bits operands to feed the final adder is the following :

RESOURCE	#
FULL ADDER	43
HALF ADDER	12

Table 1.4: Number of resources used by the Dadda Tree

The initial phase of constructing the DADDA Tree is unique in that it is the only stage where more than one compressor is required on the same bit column. This is due to the challenge of reducing from six to four bits, which is unattainable with a single compressor. In the following phase, the objective is to decrease the number of partial products from four to three, primarily employing 3-2 compressors. However, in certain instances, these compressors are substituted with Full Adders (3-2 compressors) and Half Adders (2-2 compressors) to optimize the component area. This strategic replacement is a distinguishing characteristic of the DADDA Tree as compared to the Wallace Tree.

The final two stages of the DADDA Tree involve a progressive reduction in the height of the tree, initially to three bits and subsequently to two. This careful reduction process culminates with the production of two 22-bit numbers (with the 23rd bit discarded), which are then fed into the final adder

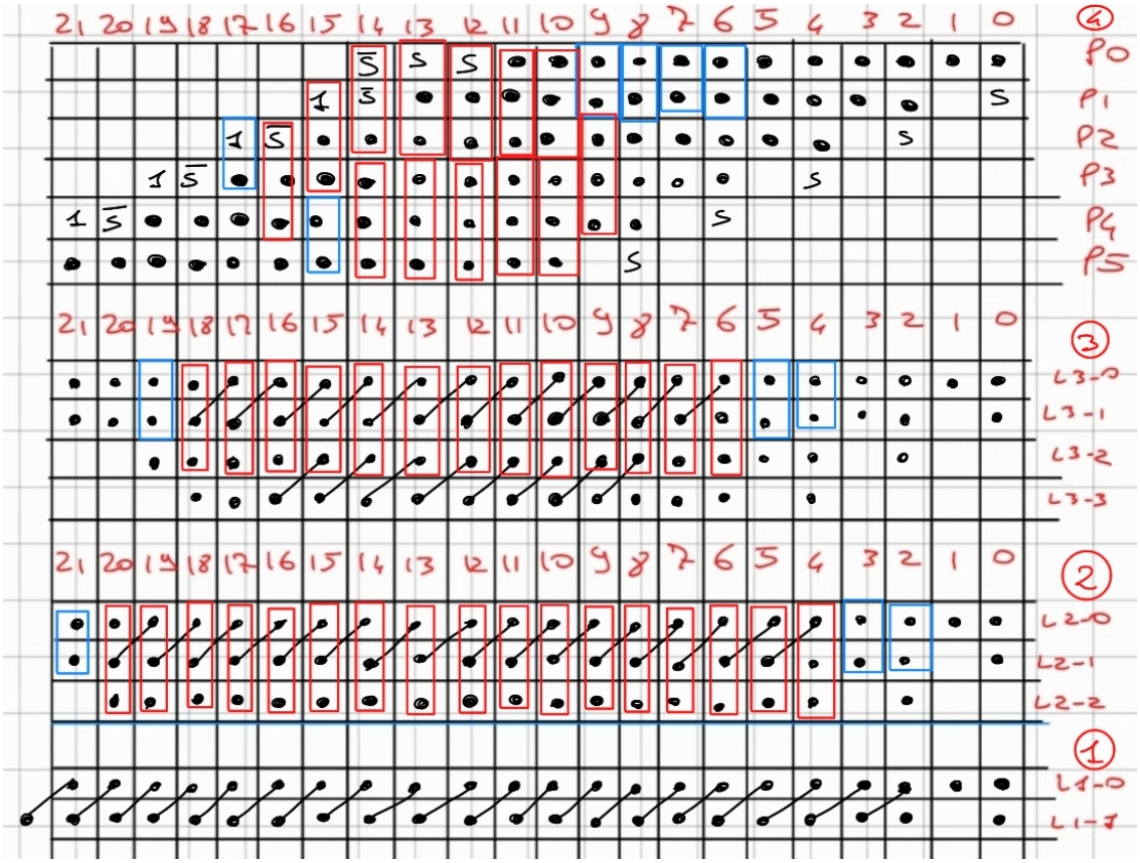

Figure 1.4: R4-MBE - Dadda Tree

for the concluding computation. This systematic approach in the DADDA Tree's design ensures a balance between computational efficiency and resource optimization.

The circuit implementing the R4-MBE is shown in Figure **??**.

1.3 Simulation

1.3.1 Standalone multiplier

Figure 1.6 shows a snapshot of a simulation for the designed multiplier as a standalone block.

To verify thoroughly the functionality of the multiplier alone, a custom testbench has been written in order to check if the produced results are correct. The code of the testbench is shown in Figure 1.7, where a series of 100 different random vectors are applied to the unit, in order to maximize the coverage.

The report of the test is shown in Appendix B.

1.3.2 Whole FPU

Figure 1.8 shows a snapshot of a simulation for the designed multiplier included in the whole FPU.

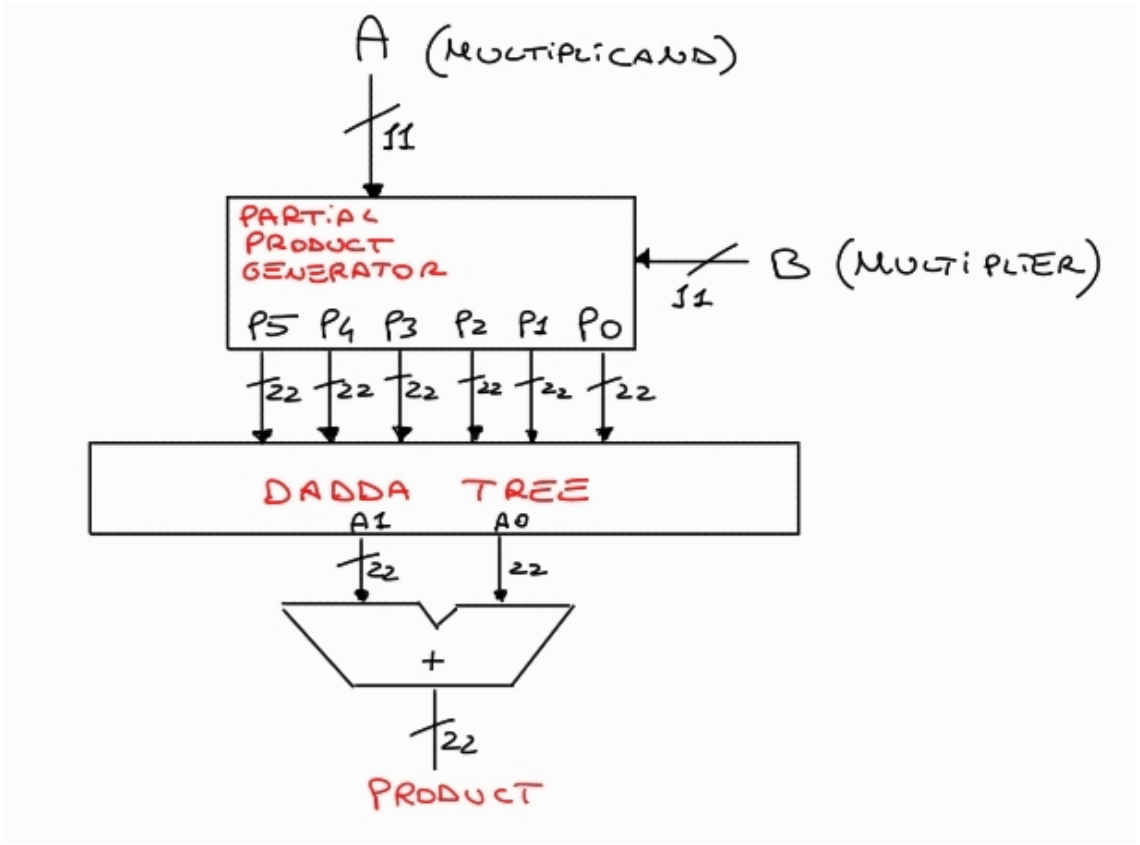

Figure 1.5: R4-MBE - Schematic

Table 1.5: FPU: Synthesis Results

Synthesis	*Area*	*Maximum Frequency*
compile_ultra	$3987.61um^2$	$370.370MHz$

Synthesis

The results of the synthesis are shown in Table 1.5.

Explanations, comparisons and comments

As it can be observed by the aforementioned table, by including the designed R4-MBE multiplier in the given Floating Point Unit it is possible to reach a maximum frequency which is about 1.3 times higher than the one reached by the very first synthesis experiment in which there was no multiplier included. It is also possible to appreciate a 10% reduction of the occupied area.
On the other hand, at a comparable optimization level (which means the same compiling command compile_ultra has been used), a considerable reduction of the resulting performance can be observed. The occupied area of the FPU with the R4-MBE is more than doubled with respect to the one from the third synthesis experiment without the mentioned multiplier, while the maximum achievable frequency is roughly half of the latter one.
The full text of the report timing and report area commands have been added in C.
In order to verify the correctness of the behaviour of the system, the simulation of all the provided post

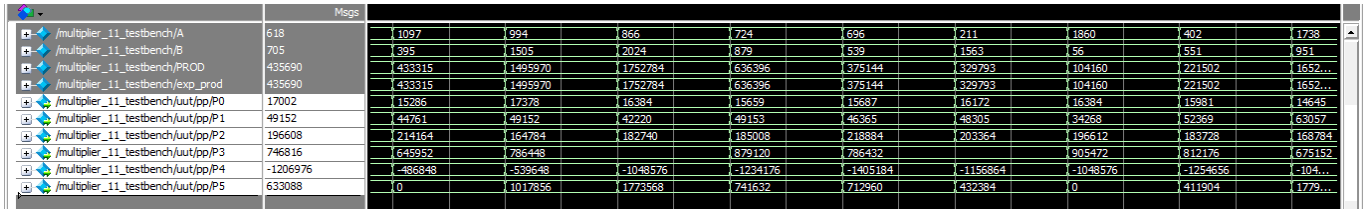

Figure 1.6: Multiplier - Simulation Results

synthesis netlists has been performed by means of a proper script, resulting in a behaviour conforming to the expected one.

src > testbench_mul11.sv

```
1   module multiplier_11_testbench();
2       logic [10:0] A, B;
3       wire [21:0] PROD;
4       integer i, output_file;
5       reg [21:0] exp_prod;
6
7       multiplier_11 uut (
8           .A_in(A),
9           .B_in(B),
10          .OUT(PROD)
11      );
12
13      initial begin
14          output_file = $fopen("mul_11_report_100vecs.txt", "w");
15
16          for (i = 0; i < 100; i++) begin
17              std::randomize(A);  //generate a random value of 11 bits
18              std::randomize(B);  //generate a random value of 11 bits
19              exp_prod = A * B;   //correct value to obtain
20              #10;                //waiting time
21
22              if (exp_prod != PROD) begin
23                  $fwrite(output_file, "%d, %d, %d, %d !\n", A, B, exp_prod, PROD);
24              end else begin
25                  $fwrite(output_file, "%d, %d, %d, %d\n", A, B, exp_prod, PROD);
26              end
27          end
28          $fclose(output_file);
29          $finish;
30      end
31  endmodule
```

Figure 1.7: Multiplier - Testbench

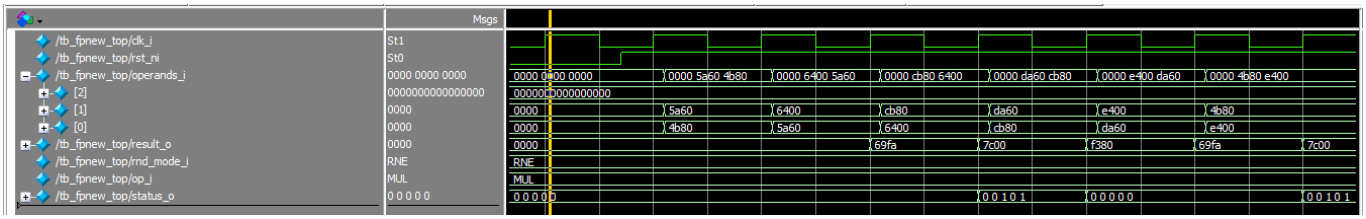

Figure 1.8: Whole FPU with MBE multiplier - Simulation Results

APPENDIX A

FPU: SYNTHESIS REPORTS

A.1 Synthesis with compile command

A.1.1 Timing Analysis

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 27 21:05:28 2023
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
      [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
      lane_instance.i_fma/inp_pipe_op_q_reg[1][3]
              (rising edge-triggered flip-flop clocked by MYCLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
      [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
      lane_instance.i_fma/mid_pipe_sum_q_reg[1][36]
            (rising edge-triggered flip-flop clocked by MYCLK)
  Path Group: MYCLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
```

—

```
clock MYCLK (rise edge)                                  0.00       0.00
clock network delay (ideal)                              0.00       0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/inp_pipe_op_q_reg[1][3]/CK (DFFR_X1)
                                                         0.00       0.00
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/inp_pipe_op_q_reg[1][3]/QN (DFFR_X1)
                                                         0.07       0.07
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U280/ZN (NAND2_X2)
                                                         0.07       0.14
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U343/ZN (INV_X1)
                                                         0.09       0.23
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U142/ZN (NAND2_X2)
                                                         0.09       0.32
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U10/ZN (NOR2_X2)
                                                         0.17       0.49
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/a[1] (
    fpnew_fma_2_00000002_3__logic_Z_1yB___logic_Z_1yB__DW_mult_uns_0)
                                                         0.00       0.49
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U302/ZN (XNOR2_X1)
                                                         0.10       0.59
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U304/ZN (INV_X1)
```

```
                                                  0.03       0.62
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U305/ZN (INV_X2)
                                                  0.07       0.69
                                                    r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U364/ZN (NOR2_X1)
                                                  0.04       0.73
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U23/CO (FA_X1)
                                                  0.11       0.83
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U22/CO (FA_X1)
                                                  0.09       0.92
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U21/CO (FA_X1)
                                                  0.09       1.01
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U20/CO (FA_X1)
                                                  0.09       1.10
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U19/CO (FA_X1)
                                                  0.09       1.19
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U18/CO (FA_X1)
                                                  0.09       1.28
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U17/CO (FA_X1)
                                                  0.09       1.37
                                                    f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
```

```
    .i_fma/mult_325/U16/CO (FA_X1)
                                                    0.09       1.47
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U15/CO (FA_X1)
                                                    0.09       1.56
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U14/CO (FA_X1)
                                                    0.09       1.65
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U13/CO (FA_X1)
                                                    0.09       1.74
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U12/CO (FA_X1)
                                                    0.09       1.83
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U11/CO (FA_X1)
                                                    0.09       1.92
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U10/CO (FA_X1)
                                                    0.10       2.02
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U309/ZN (NAND2_X1)
                                                    0.03       2.05
                                                               r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U311/ZN (NAND3_X1)
                                                    0.04       2.09
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U8/CO (FA_X1)
                                                    0.09       2.18
                                                               f
```

```
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U7/CO (FA_X1)
                                                    0.09       2.27
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U6/CO (FA_X1)
                                                    0.09       2.36
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U5/CO (FA_X1)
                                                    0.09       2.45
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U317/ZN (XNOR2_X1)
                                                    0.06       2.51
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/U312/ZN (XNOR2_X1)
                                                    0.06       2.57
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mult_325/product[21] (
    fpnew_fma_2_00000002_3__logic_Z_1yB__logic_Z_1yB__DW_mult_uns_0)
                                                    0.00       2.57
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/A[23] (
    fpnew_fma_2_00000002_3__logic_Z_1yB__logic_Z_1yB__DW01_add_6)
                                                    0.00       2.57
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/U371/ZN (NOR2_X1)
                                                    0.06       2.63
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/U494/ZN (OAI21_X1)
                                                    0.04       2.66
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
```

```
    .i_fma/add_1_root_add_368_2/U493/ZN (AOI21_X1)
                                                    0.05       2.72
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/U492/ZN (OAI21_X1)
                                                    0.03       2.75
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/U372/Z (BUF_X2)
                                                    0.06       2.81
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/U501/ZN (NAND2_X1)
                                                    0.04       2.85
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/U500/ZN (OAI21_X1)
                                                    0.03       2.88
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/U499/ZN (XNOR2_X1)
                                                    0.07       2.95
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/add_1_root_add_368_2/SUM[25] (
    fpnew_fma_2_00000002_3__logic_Z_1yB___logic_Z_1yB__DW01_add_6)
                                                    0.00       2.95
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/B[25] (
    fpnew_fma_2_00000002_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_7)
                                                    0.00       2.95
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U196/ZN (NOR2_X1)
                                                    0.06       3.01
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U197/ZN (NAND2_X1)
```

```
                                                    0.04      3.05
                                                      f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U168/ZN (NOR2_X1)
                                                    0.04      3.09
                                                      r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U167/ZN (NAND2_X1)
                                                    0.03      3.11
                                                      f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U166/ZN (NOR2_X1)
                                                    0.04      3.15
                                                      r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U157/Z (BUF_X2)
                                                    0.05      3.20
                                                      r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U230/ZN (NAND2_X1)
                                                    0.03      3.23
                                                      f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/U280/Z (XOR2_X1)
                                                    0.07      3.30
                                                      f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/sub_372/DIFF[36] (
    fpnew_fma_2_00000002_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_7)
                                                    0.00      3.30
                                                      f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U844/ZN (AOI22_X1)
                                                    0.04      3.34
                                                      r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U845/ZN (OAI21_X1)
                                                    0.03      3.38
                                                      f
```

```
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
      active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
      .i_fma/mid_pipe_sum_q_reg[1][36]/D (DFFR_X1)
                                                    0.01       3.38
                                                       f
  data arrival time                                            3.38

  clock MYCLK (rise edge)                           3.50       3.50
  clock network delay (ideal)                       0.00       3.50
  clock uncertainty                                -0.07       3.43
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
      active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
      .i_fma/mid_pipe_sum_q_reg[1][36]/CK (DFFR_X1)
                                                    0.00       3.43
                                                       r
  library setup time                                -0.04       3.39
  data required time                                           3.39
  --
    ----------------------------------------------------------------------

  data required time                                           3.39
  data arrival time                                           -3.38
  --
    ----------------------------------------------------------------------

  slack (MET)                                                  0.00
```

1

A.1.2 Area Analysis

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 27 21:05:28 2023
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
       NangateOpenCellLibrary_typical_ecsm.db)

Number of ports:                         2054
Number of nets:                          5038
Number of cells:                         3220
Number of combinational cells:           2994
Number of sequential cells:               158
```

```
Number of macros/black boxes:                0
Number of buf/inv:                         660
Number of references:                       15

Combinational area:                3500.560002
Buf/Inv area:                       397.403999
Noncombinational area:              843.220027
Macro/Black Box area:                 0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                   4343.780029
Total area:                 undefined
1
```

A.2 Synthesis with compile, optimize registers commands

A.2.1 Timing Analysis

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 27 22:06:15 2023
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/MYCLK_r_REG59_S2
              (rising edge-triggered flip-flop clocked by MYCLK)
  Endpoint: status_o[UF]
            (output port clocked by MYCLK)
  Path Group: MYCLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --
    ------------------------------------------------------------------------

  clock MYCLK (rise edge)                                 0.00       0.00
```

```
clock network delay (ideal)                                0.00       0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/MYCLK_r_REG59_S2/CK (DFFS_X1)
                                                           0.00       0.00
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/MYCLK_r_REG59_S2/Q (DFFS_X1)
                                                           0.11       0.11
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U620/ZN (NAND2_X1)
                                                           0.04       0.15
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U236/ZN (OR2_X2)
                                                           0.06       0.21
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U623/ZN (AND3_X1)
                                                           0.04       0.25
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U199/ZN (AND2_X1)
                                                           0.05       0.30
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U1013/ZN (AOI22_X1)
                                                           0.06       0.36
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U1014/ZN (OAI221_X1)
                                                           0.05       0.41
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U137/ZN (AND2_X1)
                                                           0.04       0.45
                                                              f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U639/ZN (OR2_X1)
```

0.06 0.51
f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U913/ZN (OAI22_X1)
0.06 0.57
r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U11/ZN (AOI221_X2)
0.05 0.62
f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U58/ZN (OR2_X1)
0.07 0.70
f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U257/ZN (NOR2_X1)
0.04 0.74
r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U1125/ZN (OAI222_X1)
0.04 0.78
f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U849/ZN (INV_X1)
0.03 0.81
r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U147/ZN (AND3_X2)
0.05 0.86
r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U172/ZN (OAI221_X1)
0.05 0.91
f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
.i_fma/U207/ZN (NAND2_X1)
0.04 0.96
r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance

```
    .i_fma/i_fpnew_rounding/round_sticky_bits_i[0] (
    fpnew_rounding_0000000f)
                                                    0.00       0.96
                                                               r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U38/ZN (OR2_X1)
                                                    0.04       1.00
                                                               r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U70/ZN (NAND2_X1)
                                                    0.03       1.02
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U86/ZN (OAI33_X1)
                                                    0.08       1.10
                                                               r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U87/ZN (OAI21_X1)
                                                    0.03       1.13
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U88/ZN (INV_X1)
                                                    0.04       1.17
                                                               r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U4/ZN (AND2_X2)
                                                    0.05       1.23
                                                               r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U32/ZN (NAND2_X1)
                                                    0.03       1.26
                                                               f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/U40/ZN (XNOR2_X1)
                                                    0.05       1.31
                                                               r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/i_fpnew_rounding/abs_rounded_o[12] (fpnew_rounding_0000000f)
                                                    0.00       1.31
                                                               r
```

```
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U1256/ZN (NAND4_X1)
                                                    0.04       1.35
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U1258/ZN (OAI21_X1)
                                                    0.04       1.39
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U1259/ZN (NAND2_X1)
                                                    0.03       1.42
                                                       f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U197/ZN (NAND2_X1)
                                                    0.03       1.45
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/U196/ZN (AND2_X1)
                                                    0.04       1.49
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/status_o[UF] (
    fpnew_fma_2_00000002_3__logic_Z_1yB__logic_Z_1yB_)
                                                    0.00       1.49
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/U5/ZN (AND2_X1)
                                                    0.04       1.53
                                                       r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/status_o[UF] (
    fpnew_opgroup_fmt_slice_0_2_00000010_0_00000002_3__logic_Z_1yB_)
                                                    0.00       1.53
                                                       r
gen_operation_groups[0].i_opgroup_block/i_arbiter/data_i[2][status][UF]
     (rr_arb_tree_00000005_1_346242)
                                                    0.00       1.53
                                                       r
gen_operation_groups[0].i_opgroup_block/i_arbiter/U24/ZN (AND2_X1)
                                                    0.04       1.56
                                                       r
gen_operation_groups[0].i_opgroup_block/i_arbiter/data_o[status][UF] (
    rr_arb_tree_00000005_1_346242)
```

```
                                                    0.00       1.56
                                                       r
  gen_operation_groups[0].i_opgroup_block/status_o[UF] (
      fpnew_opgroup_block_0_00000010_0_04_4_155_3__logic_Z_1yB__395949)
                                                    0.00       1.56
                                                       r
  i_arbiter/data_i[0][status][UF] (rr_arb_tree_00000004_1_532242)
                                                    0.00       1.56
                                                       r
  i_arbiter/U7/ZN (AND2_X1)                         0.04       1.61
       r
  i_arbiter/data_o[status][UF] (rr_arb_tree_00000004_1_532242)
                                                    0.00       1.61
                                                       r
  status_o[UF] (out)                                0.02       1.63
       r
  data arrival time                                            1.63

  clock MYCLK (rise edge)                           2.20       2.20
  clock network delay (ideal)                       0.00       2.20
  clock uncertainty                                -0.07       2.13
  output external delay                            -0.50       1.63
  data required time                                           1.63
  --
    ------------------------------------------------------------------------

  data required time                                           1.63
  data arrival time                                           -1.63
  --
    ------------------------------------------------------------------------

  slack (MET)                                                  0.00


1
```

A.2.2 Area Analysis

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 27 22:06:15 2023
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
       NangateOpenCellLibrary_typical_ecsm.db)
```

```
Number of ports:                         1985
Number of nets:                          4217
Number of cells:                         3228
Number of combinational cells:           2736
Number of sequential cells:               245
Number of macros/black boxes:               0
Number of buf/inv:                        683
Number of references:                      14

Combinational area:               3005.533995
Buf/Inv area:                      403.256001
Noncombinational area:            1303.400042
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  4308.934037
Total area:                 undefined
1
```

A.3 Synthesis with compile ultra command

A.3.1 Timing Analysis

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 27 20:35:00 2023
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: op_i[2] (input port clocked by MYCLK)
  Endpoint: in_ready_o (output port clocked by MYCLK)
  Path Group: MYCLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock MYCLK (rise edge)                  0.00       0.00
```

clock network delay (ideal)	0.00	0.00
input external delay	0.50	0.50 f
op_i[2] (**in**)	0.00	0.50 f
U13/ZN (INV_X1)	0.04	0.54 r
U14/ZN (NOR3_X1)	0.03	0.57 f
U39/ZN (AOI221_X1)	0.09	0.66 r
U41/ZN (OAI21_X1)	0.04	0.70 f
U42/ZN (AOI21_X1)	0.05	0.74 r
in_ready_o (**out**)	0.00	0.75 r
data arrival time		0.75
clock MYCLK (rise edge)	1.32	1.32
clock network delay (ideal)	0.00	1.32
clock uncertainty	−0.07	1.25
output external delay	−0.50	0.75
data required time		0.75
data required time		0.75
data arrival time		−0.75
slack (MET)		0.00

1

A.3.2 Area Analysis

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 27 20:35:00 2023
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
        NangateOpenCellLibrary_typical_ecsm.db)

Number of ports:                          223
Number of nets:                           435
Number of cells:                          144
Number of combinational cells:            135
Number of sequential cells:                 6
Number of macros/black boxes:               0
Number of buf/inv:                         16
Number of references:                      17

Combinational area:                148.162001
```

```
Buf/Inv area:                    9.044000
Noncombinational area:          10.640000
Macro/Black Box area:            0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:               158.802002
Total area:                 undefined

Information: This design contains black box (unknown) components. (RPT-8)
1
```

A.4 Synthesis with CSA multiplier

A.4.1 Timing Analysis

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Tue Nov 28 17:18:39 2023
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: MYCLK_r_REG138_S2
              (rising edge-triggered flip-flop clocked by MYCLK)
  Endpoint: status_o[UF]
            (output port clocked by MYCLK)
  Path Group: MYCLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --
      ------------------------------------------------------------------

  clock MYCLK (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  MYCLK_r_REG138_S2/CK (DFFR_X1)                          0.00       0.00
       r
```

```
MYCLK_r_REG138_S2/Q (DFFR_X1)                                    0.11       0.11
     r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/A[5] (fpnew_top_DW01_sub_8)
                                                                 0.00       0.11
                                                                      r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/U66/ZN (OR2_X1)
                                                                 0.04       0.15
                                                                      r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/U111/ZN (XNOR2_X1)
                                                                 0.05       0.21
                                                                      r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/DIFF[6] (fpnew_top_DW01_sub_8)
                                                                 0.00       0.21
                                                                      r
U1066/ZN (NAND4_X1)                                              0.05       0.25
     f
U1146/ZN (OAI22_X1)                                              0.06       0.31
     r
U1041/ZN (NAND2_X1)                                              0.05       0.36
     f
U1312/ZN (OAI222_X4)                                             0.11       0.47
     r
U1900/ZN (INV_X1)                                                0.04       0.51
     f
U1288/ZN (NAND2_X1)                                              0.04       0.55
     r
U1901/ZN (INV_X1)                                                0.02       0.57
     f
U752/Z (CLKBUF_X1)                                               0.07       0.65
     f
U869/ZN (AND2_X1)                                                0.06       0.71
     f
U1089/ZN (OAI33_X1)                                              0.07       0.78
     r
U1293/ZN (AOI221_X1)                                             0.03       0.81
     f
U778/ZN (OR2_X1)                                                 0.07       0.88
     f
U1224/ZN (INV_X1)                                                0.03       0.92
     r
U2077/ZN (AOI22_X1)                                              0.03       0.95
```

```
     f
U2078/ZN (OAI21_X1)                          0.03       0.98
     r
U2079/ZN (INV_X1)                            0.02       1.01
     f
U2085/ZN (NOR4_X1)                           0.09       1.10
     r
U1319/ZN (OAI221_X4)                         0.09       1.19
     f
U2179/ZN (OAI211_X1)                         0.05       1.24
     r
U1000/ZN (AND3_X1)                           0.06       1.30
     r
U799/ZN (AND3_X1)                            0.06       1.36
     r
U948/ZN (NAND2_X1)                           0.03       1.39
     f
U1307/ZN (NOR2_X1)                           0.04       1.43
     r
U1098/ZN (XNOR2_X1)                          0.06       1.49
     r
U1109/ZN (NAND3_X1)                          0.04       1.54
     f
U938/ZN (OAI21_X1)                           0.04       1.58
     r
U1052/ZN (NAND2_X1)                          0.03       1.61
     f
U1053/ZN (NAND2_X1)                          0.02       1.63
     r
U1176/ZN (AND2_X1)                           0.04       1.68
     r
status_o[UF] (out)                           0.02       1.70
     r
data arrival time                                       1.70

clock MYCLK (rise edge)                      2.27       2.27
clock network delay (ideal)                  0.00       2.27
clock uncertainty                           -0.07       2.20
output external delay                       -0.50       1.70
data required time                                      1.70
--
------------------------------------------------------------

data required time                                      1.70
data arrival time                                      -1.70
--
------------------------------------------------------------

slack (MET)                                             0.00
```

```
1
```

A.4.2 Area Analysis

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Tue Nov 28 17:18:39 2023
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
       NangateOpenCellLibrary_typical_ecsm.db)

Number of ports:                          524
Number of nets:                          3223
Number of cells:                         2660
Number of combinational cells:           2382
Number of sequential cells:               256
Number of macros/black boxes:               0
Number of buf/inv:                        542
Number of references:                      44

Combinational area:               2745.385994
Buf/Inv area:                      307.230001
Noncombinational area:            1361.920044
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  4107.306038
Total area:                 undefined
1
```

A.4.3 Resources Analysis

```
****************************************
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Tue Nov 28 17:13:00 2023
****************************************

Resource Sharing Report for design fpnew_top in file ../src/fpnew_top.sv
```

```
|          |               |            | Contained      |
                        |
| Resource | Module        | Parameters | Resources      | Contained
  Operations |
==========================================================================

| r428     | DW01_cmp2     | width=3    |                |
  gen_operation_groups[0].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                         |
|          |               |            |                |
  gen_operation_groups[0].i_opgroup_block/i_arbiter/lte_209_G4 |
| r429     | DW01_cmp2     | width=3    |                |
  gen_operation_groups[1].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                         |
|          |               |            |                |
  gen_operation_groups[1].i_opgroup_block/i_arbiter/lte_209_G4 |
| r430     | DW01_cmp2     | width=3    |                |
  gen_operation_groups[2].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                         |
|          |               |            |                |
  gen_operation_groups[2].i_opgroup_block/i_arbiter/lte_209_G4 |
| r431     | DW01_cmp2     | width=3    |                |
  gen_operation_groups[3].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                         |
|          |               |            |                |
  gen_operation_groups[3].i_opgroup_block/i_arbiter/lte_209_G4 |
| r432     | DW01_cmp2     | width=2    |                | i_arbiter/
  gt_208_G4  |
|          |               |            |                | i_arbiter/
  lte_209_G4 |
| r462     | DW01_add      | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/add_285 |
| r470     | DW01_sub      | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/sub_293 |
| r472     | DW_cmp        | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/gt_295 |
| r474     | DW_cmp        | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/lte_302 |
| r476     | DW_cmp        | width=7    |                |
```

```
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_305 |
| r478      | DW01_sub      | width=6     |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_306 |
| r480      | DW02_mult     | A_width=11 |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/mult_325 |
|
|           |               | B_width=11 |                |
                        |
| r482      | DW_rightsh    | A_width=48 |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/srl_349 |
|
|           |               | SH_width=6 |                |
                        |
| r484      | DW01_add      | width=38    |                |
    add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_368_2 |
| r486      | DW01_sub      | width=37    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_372 |
| r488      | DW_cmp        | width=7     |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510 |
| r490      | DW_cmp        | width=7     |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510_2 |
| r496      | DW_cmp        | width=9     |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gte_512 |
| r498      | DW01_add      | width=6     |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_514 |
| r504      | DW01_add      | width=6     |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_519 |
```

```
| r506      | DW_leftsh     | A_width=38 |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/sll_530 |
|
|           |               | SH_width=6 |                |
                          |
| r508      | DW_cmp        | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/gt_547 |
| r510      | DW01_inc      | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/add_542 |
| r512      | DW01_dec      | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/sub_549 |
| r514      | DW_cmp        | width=7    |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/gte_576 |
| r516      | DW01_add      | width=15   |                |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/i_fpnew_rounding/add_63 |
| r1244     | DW01_add      | width=7    |                |
  add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/
  gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].
  active_lane.lane_instance.i_fma/sub_287 |
| r1246     | DW01_sub      | width=7    |                |
  sub_2_root_add_1_root_gen_operation_groups[0].i_opgroup_block/
  gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].
  active_lane.lane_instance.i_fma/sub_287 |
| r1248     | DW01_add      | width=7    |                |
  add_0_root_add_1_root_gen_operation_groups[0].i_opgroup_block/
  gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].
  active_lane.lane_instance.i_fma/sub_287 |
| r1968     | DW01_sub      | width=8    |                |
  sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
  [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
  lane_instance.i_fma/add_512 |
| r1970     | DW01_inc      | width=9    |                |
  add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
  [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
  lane_instance.i_fma/add_512 |
| r2690     | DW01_sub      | width=7    |                |
  sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
```

```
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
| r2692     | DW01_inc      | width=7     |                |
    add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
```

Implementation **Report**

```
|                    |                    | Current             | Set
                |
| Cell               | Module             | Implementation      |
    Implementation |
| add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
|                    | DW01_inc           | pparch (speed)      |
                |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
|                    | DW01_sub           | pparch (speed)      |
                |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512 |
|                    | DW01_sub           | pparch (area,speed)
                |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_372 |
|                    | DW01_sub           | pparch (speed)      |
                |
| add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_368_2 |
|                    | DW01_add           | pparch (speed)      |
                |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_293 |
|                    | DW01_sub           | pparch (area,speed)
                |
```

```
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/mult_325 |
|                    | DW02_mult          | csa                    | csa
              |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_542 |
|                    | DW01_inc           | rpl                    |
                  |
```

1

A.5 Synthesis with PPARCH multiplier

A.5.1 Timing Analysis

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Tue Nov 28 17:06:46 2023
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: MYCLK_r_REG147_S2
              (rising edge-triggered flip-flop clocked by MYCLK)
  Endpoint: status_o[NX]
            (output port clocked by MYCLK)
  Path Group: MYCLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --
    ------------------------------------------------------------------------

  clock MYCLK (rise edge)                                 0.00       0.00
```

```
clock network delay (ideal)                                0.00       0.00
MYCLK_r_REG147_S2/CK (DFFR_X1)                             0.00       0.00
     r
MYCLK_r_REG147_S2/Q (DFFR_X1)                              0.11       0.11
     r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/A[5] (fpnew_top_DW01_sub_8)
                                                           0.00       0.11
                                                                r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/U66/ZN (OR2_X1)
                                                           0.04       0.15
                                                                r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/U114/ZN (XNOR2_X1)
                                                           0.06       0.21
                                                                r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512/DIFF[6] (fpnew_top_DW01_sub_8)
                                                           0.00       0.21
                                                                r
U1291/ZN (NAND4_X1)                                        0.04       0.25
     f
U976/ZN (OAI22_X1)                                         0.06       0.31
     r
U1835/ZN (NAND3_X1)                                        0.05       0.36
     f
U1292/ZN (OAI221_X1)                                       0.05       0.40
     r
U782/Z (CLKBUF_X1)                                         0.05       0.45
     r
U794/ZN (AND2_X2)                                          0.06       0.52
     r
U1875/ZN (AOI22_X1)                                        0.04       0.56
     f
U1876/ZN (OAI221_X1)                                       0.04       0.60
     r
U1263/ZN (NAND2_X1)                                        0.04       0.63
     f
U1121/ZN (AND4_X1)                                         0.05       0.68
     f
U1889/ZN (AOI221_X1)                                       0.08       0.76
     r
U1890/ZN (OAI211_X1)                                       0.05       0.82
     f
```

```
U1891/ZN (INV_X1)                                  0.04       0.86
     r
U1029/ZN (AND2_X2)                                 0.05       0.91
     r
U1933/ZN (AOI22_X1)                                0.04       0.95
     f
U1934/ZN (OAI21_X1)                                0.04       0.99
     r
U1935/ZN (INV_X1)                                  0.02       1.01
     f
U1940/ZN (NOR4_X1)                                 0.09       1.10
     r
U983/ZN (OAI211_X1)                                0.06       1.16
     f
U779/Z (BUF_X2)                                    0.06       1.21
     f
U2030/ZN (OAI211_X1)                               0.04       1.26
     r
U854/ZN (AND3_X1)                                  0.07       1.33
     r
U1074/ZN (AND4_X2)                                 0.06       1.39
     r
U855/ZN (NAND3_X1)                                 0.04       1.44
     f
U1161/ZN (XNOR2_X1)                                0.05       1.48
     r
U2138/ZN (NAND3_X1)                                0.03       1.52
     f
U2141/ZN (NOR3_X1)                                 0.05       1.56
     r
U2143/ZN (OAI21_X1)                                0.04       1.60
     f
U2147/ZN (NAND2_X1)                                0.03       1.63
     r
status_o[NX] (out)                                 0.00       1.63
     r
data arrival time                                             1.63

clock MYCLK (rise edge)                            2.20       2.20
clock network delay (ideal)                        0.00       2.20
clock uncertainty                                 -0.07       2.13
output external delay                             -0.50       1.63
data required time                                            1.63
--
```

```
data required time                                            1.63
data arrival time                                            -1.63
--
```

```
  slack (MET)                                                    0.00


1
```

A.5.2 Area Analysis

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Tue Nov 28 17:06:46 2023
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
       NangateOpenCellLibrary_typical_ecsm.db)

Number of ports:                          462
Number of nets:                          3215
Number of cells:                         2755
Number of combinational cells:           2478
Number of sequential cells:               259
Number of macros/black boxes:               0
Number of buf/inv:                        576
Number of references:                      46

Combinational area:               2782.891993
Buf/Inv area:                      337.288000
Noncombinational area:            1377.880044
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  4160.772038
Total area:                 undefined
1
```

A.5.3 Resources Analysis

```
****************************************
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Tue Nov 28 17:00:02 2023
****************************************
```

```
Resource Sharing Report for design fpnew_top in file ../src/fpnew_top.sv

================================================================================

|          |              |            | Contained     |
                        |
| Resource | Module       | Parameters | Resources     | Contained
  Operations |
================================================================================

| r429     | DW01_cmp2    | width=3    |               |
  gen_operation_groups[0].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                        |
|          |              |            |               |
  gen_operation_groups[0].i_opgroup_block/i_arbiter/lte_209_G4 |
| r430     | DW01_cmp2    | width=3    |               |
  gen_operation_groups[1].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                        |
|          |              |            |               |
  gen_operation_groups[1].i_opgroup_block/i_arbiter/lte_209_G4 |
| r431     | DW01_cmp2    | width=3    |               |
  gen_operation_groups[2].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                        |
|          |              |            |               |
  gen_operation_groups[2].i_opgroup_block/i_arbiter/lte_209_G4 |
| r432     | DW01_cmp2    | width=3    |               |
  gen_operation_groups[3].i_opgroup_block/i_arbiter/gt_208_G4 |
|              |                        |
|          |              |            |               |
  gen_operation_groups[3].i_opgroup_block/i_arbiter/lte_209_G4 |
| r433     | DW01_cmp2    | width=2    |               | i_arbiter/
  gt_208_G4  |
|          |              |            |               | i_arbiter/
  lte_209_G4 |
| r463     | DW01_add     | width=7    |               |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/add_285 |
| r471     | DW01_sub     | width=7    |               |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/sub_293 |
| r473     | DW_cmp       | width=7    |               |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
  active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
  i_fma/gt_295 |
| r475     | DW_cmp       | width=7    |               |
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
```

```
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_302 |
| r477      | DW_cmp       | width=7    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_305 |
| r479      | DW01_sub     | width=6    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_306 |
| r481      | DW02_mult    | A_width=11 |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/mult_325 |
|
|           |              | B_width=11 |                |
                        |
| r483      | DW_rightsh   | A_width=48 |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/srl_349 |
|
|           |              | SH_width=6 |                |
                       |
| r485      | DW01_add     | width=38   |                |
    add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_368_2 |
| r487      | DW01_sub     | width=37   |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_372 |
| r489      | DW_cmp       | width=7    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510 |
| r491      | DW_cmp       | width=7    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510_2 |
| r497      | DW_cmp       | width=9    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gte_512 |
| r499      | DW01_add     | width=6    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_514 |
| r505      | DW01_add     | width=6    |                |
```

```
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_519 |
| r507      | DW_leftsh     | A_width=38 |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sll_530 |
|
|           |               | SH_width=6 |                |
                          |
| r509      | DW_cmp        | width=7    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gt_547 |
| r511      | DW01_inc      | width=7    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_542 |
| r513      | DW01_dec      | width=7    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_549 |
| r515      | DW_cmp        | width=7    |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gte_576 |
| r517      | DW01_add      | width=15   |                |
    gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/i_fpnew_rounding/add_63 |
| r1245     | DW01_add      | width=7    |                |
    add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_287 |
| r1247     | DW01_sub      | width=7    |                |
    sub_2_root_add_1_root_gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_287 |
| r1249     | DW01_add      | width=7    |                |
    add_0_root_add_1_root_gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_287 |
| r1969     | DW01_sub      | width=8    |                |
    sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512 |
| r1971     | DW01_inc      | width=9    |                |
    add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
```

```
    lane_instance.i_fma/add_512 |
| r2691     | DW01_sub     | width=7    |                |
    sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
| r2693     | DW01_inc     | width=7    |                |
    add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
```

Implementation **Report**

```
|                    |                  | Current              | Set
                |
| Cell               | Module           | Implementation       |
    Implementation |
```

```
| add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
|                    | DW01_inc         | pparch (speed)       |
                  |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
|                    | DW01_sub         | pparch (speed)       |
                  |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512 |
|                    | DW01_sub         | pparch (area,speed)
                   |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_372 |
|                    | DW01_sub         | pparch (speed)       |
                  |
| add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
    [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_368_2 |
|                    | DW01_add         | pparch (speed)       |
                  |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
```

```
    i_fma/sub_293 |
|                       | DW01_sub          | pparch (area,speed)
                    |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/mult_325 |
|                       | DW02_mult         | pparch (area)       | pparch
            |
|                       |                   | mult_arch: benc_radix4
                  |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_542 |
|                       | DW01_inc          | rpl                 |
                    |
```

1

APPENDIX B

Simulation result of the Multiplier

B.1 TXT Report

The following .txt contains the list of 100 random couples of input vectors applied to the multiplier. The columns are ordered in the following order : A B Expected_output Obtained_output. In case of a line where the expected output differs from the one obtained from the multiplier, a "!" is written in the same line, but as shown in the file, no errors are detected so the multiplier behaves in a correct manner.

```
   A  ,     B  , EXPECTED,  OBTAINED

 952,  1062,  1011024,  1011024
 358,   950,   340100,   340100
 198,  1606,   317988,   317988
1906,   814,  1551484,  1551484
1127,  1338,  1507926,  1507926
1130,   436,   492680,   492680
 623,   598,   372554,   372554
1589,  2004,  3184356,  3184356
 174,   381,    66294,    66294
2011,  1541,  3098951,  3098951
1763,   800,  1410400,  1410400
1509,  1797,  2711673,  2711673
1317,  1769,  2329773,  2329773
1117,  1418,  1583906,  1583906
 344,   395,   135880,   135880
 342,   969,   331398,   331398
 697,   320,   223040,   223040
1920,  1550,  2976000,  2976000
 212,   398,    84376,    84376
1216,   407,   494912,   494912
 293,   967,   283331,   283331
 600,   337,   202200,   202200
 306,  1571,   480726,   480726
 852,   435,   370620,   370620
1626,   742,  1206492,  1206492
```

```
1526,  613,  935438,  935438
1514,  783, 1185462, 1185462
 239, 1092,  260988,  260988
1481,  203,  300643,  300643
 839,  711,  596529,  596529
1522,  993, 1511346, 1511346
 901,  816,  735216,  735216
 630,  285,  179550,  179550
1490, 1814, 2702860, 2702860
1755,  832, 1460160, 1460160
 693,  657,  455301,  455301
1907,  160,  305120,  305120
1367, 1053, 1439451, 1439451
 980, 2013, 1972740, 1972740
 410,  132,   54120,   54120
 951, 1161, 1104111, 1104111
 266,  725,  192850,  192850
1278, 1612, 2060136, 2060136
1534,  707, 1084538, 1084538
1928, 1468, 2830304, 2830304
1435,  755, 1083425, 1083425
1583, 1463, 2315929, 2315929
 267,  743,  198381,  198381
1280,  265,  339200,  339200
 618,  705,  435690,  435690
1540, 1888, 2907520, 2907520
 943, 1391, 1311713, 1311713
 325, 1997,  649025,  649025
1900, 1744, 3313600, 3313600
 169, 1532,  258908,  258908
 741,  167,  123747,  123747
  59,  190,   11210,   11210
 673, 1413,  950949,  950949
1934, 1952, 3775168, 3775168
 277,    0,       0,       0
 452, 1931,  872812,  872812
 168, 1725,  289800,  289800
 620,  893,  553660,  553660
1707,  426,  727182,  727182
1377,  690,  950130,  950130
 342,  582,  199044,  199044
 212,  737,  156244,  156244
2004, 1057, 2118228, 2118228
 352, 1897,  667744,  667744
1542, 2036, 3139512, 3139512
1662, 1226, 2037612, 2037612
 552,    3,    1656,    1656
1455, 1004, 1460820, 1460820
 894, 1094,  978036,  978036
```

```
 328, 1733,  568424,  568424
2046, 1700, 3478200, 3478200
1397,   13,   18161,   18161
1654, 1149, 1900446, 1900446
1311, 1529, 2004519, 2004519
 633,  545,  344985,  344985
 109,  733,   79897,   79897
 719, 1009,  725471,  725471
1637, 1434, 2347458, 2347458
1904,  936, 1782144, 1782144
1910, 1006, 1921460, 1921460
 436,  280,  122080,  122080
 593,  636,  377148,  377148
 845, 1217, 1028365, 1028365
1719,  582, 1000458, 1000458
1776,  295,  523920,  523920
 371, 1852,  687092,  687092
1174, 1736, 2038064, 2038064
1858, 1318, 2448844, 2448844
 569,  883,  502427,  502427
1967,  436,  857612,  857612
 359,  200,   71800,   71800
2027, 1106, 2241862, 2241862
 394, 1358,  535052,  535052
  44, 1503,   66132,   66132
 711, 1169,  831159,  831159
```

APPENDIX C

FPU with R4-MBE: SYNTHESIS REPORTS

C.1 Timing Analysis

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Sun Dec 17 14:26:12 2023
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Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
      [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
      lane_instance.i_fma/inp_pipe_operands_q_reg[1][1][1]
              (rising edge-triggered flip-flop clocked by MYCLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices
      [2].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
      lane_instance.i_fma/mid_pipe_sum_q_reg[1][26]
            (rising edge-triggered flip-flop clocked by MYCLK)
  Path Group: MYCLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --
```

```
clock MYCLK (rise edge)                                  0.00       0.00
clock network delay (ideal)                              0.00       0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/inp_pipe_operands_q_reg[1][1][1]/CK (DFFR_X2)
                                                         0.00       0.00
                                                              r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/inp_pipe_operands_q_reg[1][1][1]/Q (DFFR_X2)
                                                         0.14       0.14
                                                              r
U1430/ZN (OR2_X1)                                        0.06       0.20
     r
U1420/ZN (AND3_X1)                                       0.08       0.28
     r
U2564/ZN (INV_X1)                                        0.05       0.33
     f
U2750/ZN (OAI211_X1)                                     0.06       0.39
     r
U1413/ZN (AND2_X1)                                       0.06       0.45
     r
U2754/ZN (NOR2_X1)                                       0.03       0.48
     f
U2107/ZN (OAI21_X1)                                      0.03       0.52
     r
U2129/ZN (NAND2_X1)                                      0.03       0.55
     f
U3053/CO (FA_X1)                                         0.09       0.64
     f
U3051/CO (FA_X1)                                         0.09       0.73
     f
U3050/CO (FA_X1)                                         0.09       0.82
     f
U3060/CO (FA_X1)                                         0.09       0.91
     f
U3061/CO (FA_X1)                                         0.09       1.00
     f
U3057/CO (FA_X1)                                         0.09       1.09
     f
U3056/CO (FA_X1)                                         0.09       1.18
     f
U3069/CO (FA_X1)                                         0.09       1.27
     f
U3065/CO (FA_X1)                                         0.09       1.36
     f
U3067/CO (FA_X1)                                         0.09       1.45
     f
```

```
U3074/CO (FA_X1)                                        0.09       1.54
     f
U2985/CO (FA_X1)                                        0.09       1.63
     f
U2986/CO (FA_X1)                                        0.09       1.72
     f
U2960/CO (FA_X1)                                        0.09       1.81
     f
U3078/S (FA_X1)                                         0.14       1.95
     r
U2171/ZN (NOR2_X1)                                      0.04       1.99
     f
U1537/ZN (OR2_X1)                                       0.06       2.05
     f
U1762/ZN (AND2_X1)                                      0.04       2.09
     f
U2067/ZN (AND2_X1)                                      0.04       2.13
     f
U2170/ZN (NAND2_X1)                                     0.03       2.16
     r
U2186/ZN (NAND3_X1)                                     0.03       2.19
     f
U2215/ZN (NAND2_X1)                                     0.03       2.23
     r
U2094/ZN (NAND2_X1)                                     0.03       2.26
     f
U2176/ZN (AOI21_X1)                                     0.05       2.30
     r
U2225/ZN (INV_X1)                                       0.03       2.33
     f
U2141/ZN (NAND2_X2)                                     0.06       2.39
     r
U2144/ZN (NAND2_X1)                                     0.04       2.43
     f
U2058/ZN (XNOR2_X1)                                     0.06       2.49
     f
U2173/ZN (OAI21_X1)                                     0.05       2.53
     r
U2270/ZN (INV_X1)                                       0.02       2.55
     f
U2269/ZN (OAI21_X1)                                     0.03       2.58
     r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
    .i_fma/mid_pipe_sum_q_reg[1][26]/D (DFFR_X1)
                                                        0.01       2.59
                                                             r
data arrival time                                                  2.59
```

```
  clock MYCLK (rise edge)                                  2.70       2.70
  clock network delay (ideal)                              0.00       2.70
  clock uncertainty                                       -0.07       2.63
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].
      active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance
      .i_fma/mid_pipe_sum_q_reg[1][26]/CK (DFFR_X1)
                                                           0.00       2.63
                                                              r
  library setup time                                      -0.04       2.59
  data required time                                                  2.59
  --
      ------------------------------------------------------------------------


  data required time                                                  2.59
  data arrival time                                                  -2.59
  --
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  slack (MET)                                                         0.00
```

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C.2 Area Analysis

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Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Sun Dec 17 14:26:12 2023
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Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
       NangateOpenCellLibrary_typical_ecsm.db)

Number of ports:                        96
Number of nets:                       3464
Number of cells:                      3240
Number of combinational cells:        3105
Number of sequential cells:            133
Number of macros/black boxes:            0
Number of buf/inv:                     538
Number of references:                   43

Combinational area:            3276.853994
Buf/Inv area:                   302.176002
```

```
Noncombinational area:           710.752023
Macro/Black Box area:              0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                3987.606017
Total area:                 undefined
1
```