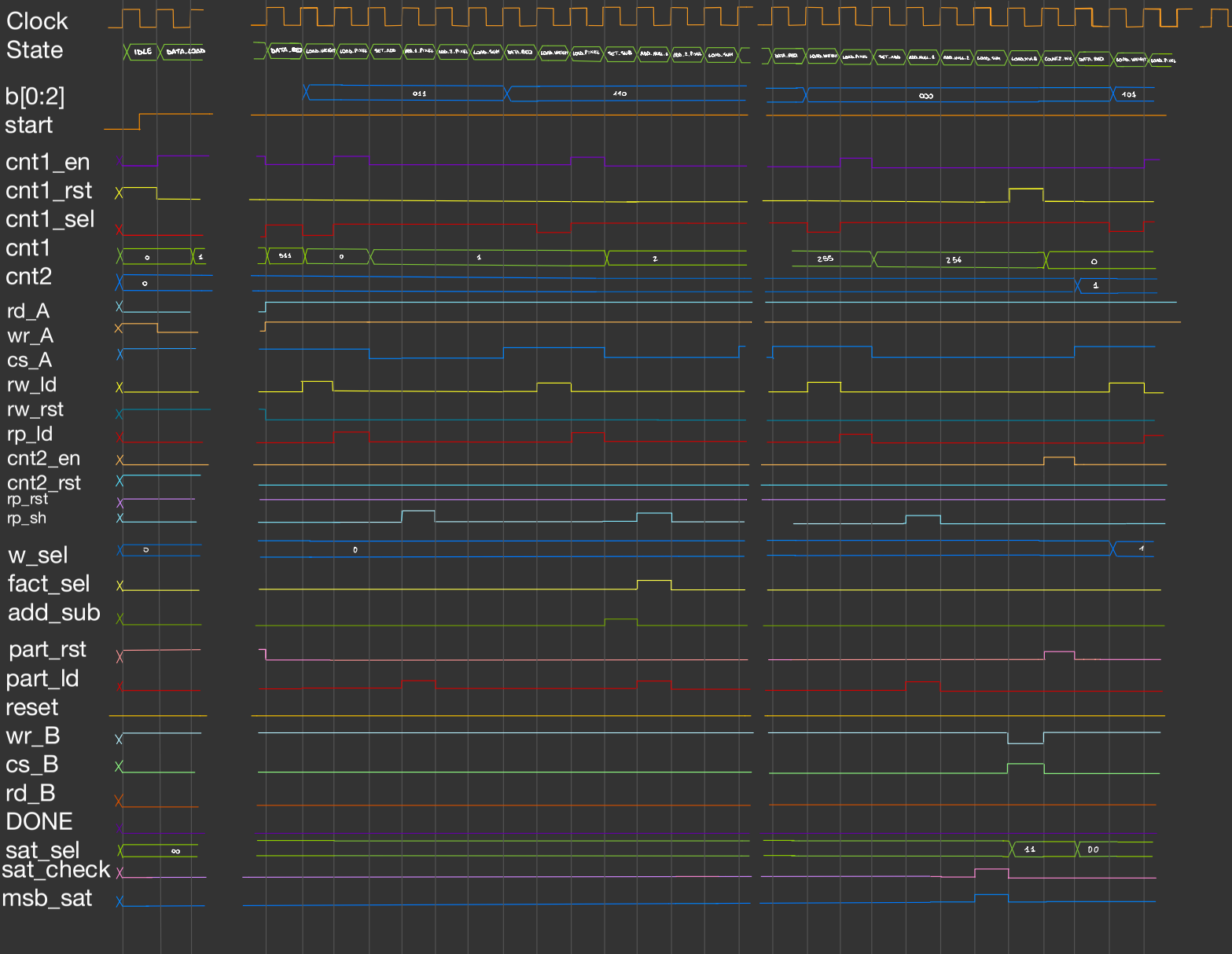
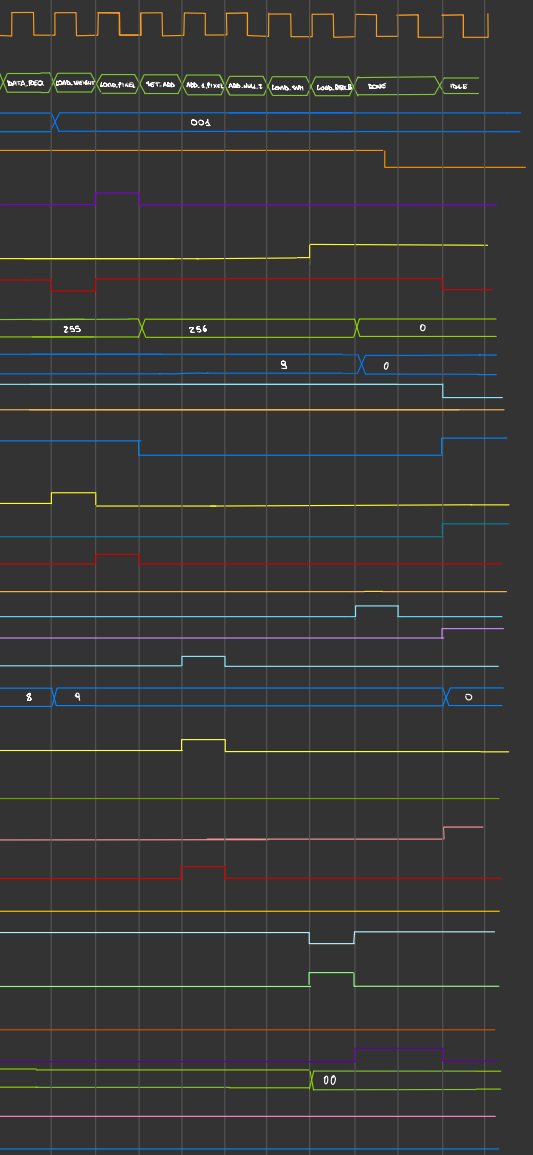

Clock
State
IDLE
DATA_LOAD
DATA_RED
LOAD.WEIGHT
LOAD.PIXEL
SET.ADD
ADD.1.PIXEL
ADD.2.PIXEL
LOAD.SUM
DATA.RED
LOAD.WEIGHT
LOAD.PIXEL
SET.SUB
ADD.ABS.1
ADD.2.PIXEL
LOAD.SUM
DATA.RED
LOAD.WEIGHT
LOAD.PIXEL
SET.ADD
ADD.ABS.1
ADD.ABS.2
LOAD.SUM
LOAD.MAX
COUNT2.INC
DATA.RED
LOAD.WEIGHT
LOAD.PIXEL
b[0:2]
011
110
000
101
start
cnt1_en
cnt1_rst
cnt1_sel
cnt1
0
1
341
0
1
2
255
256
0
cnt2
0
1
rd_A
wr_A
cs_A
rw_ld
rw_rst
rp_ld
cnt2_en
cnt2_rst
rp_rst
rp_sh
w_sel
0
0
1
fact_sel
add_sub
part_rst
part_ld
reset
wr_B
cs_B
rd_B
DONE
sat_sel
00
11
00
sat_check
msb_sat


DATA_REQ
LOAD_WEIGHT
LOAD_PIXEL
RST. ADD
ADD. 1 PIXEL
ADD. HALF
LOAD. WIN
LOAD. BIAS
DONE
IDLE
001
255
256
0
9
0
8
9
0
00