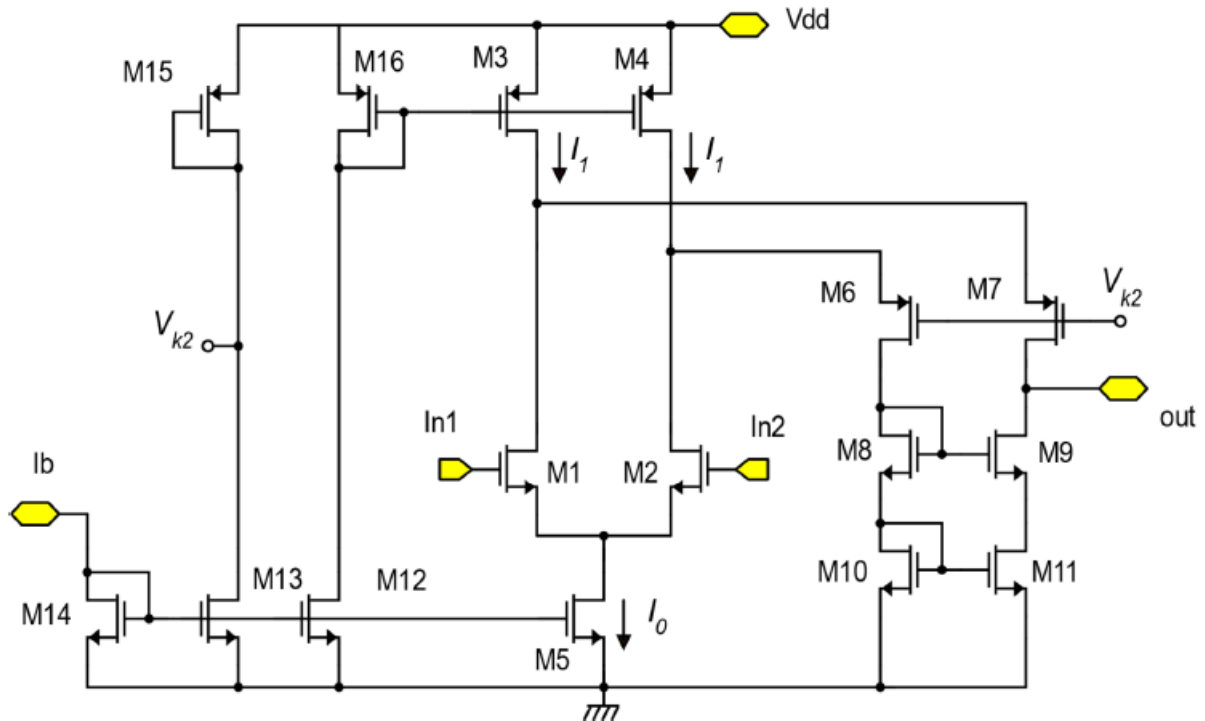


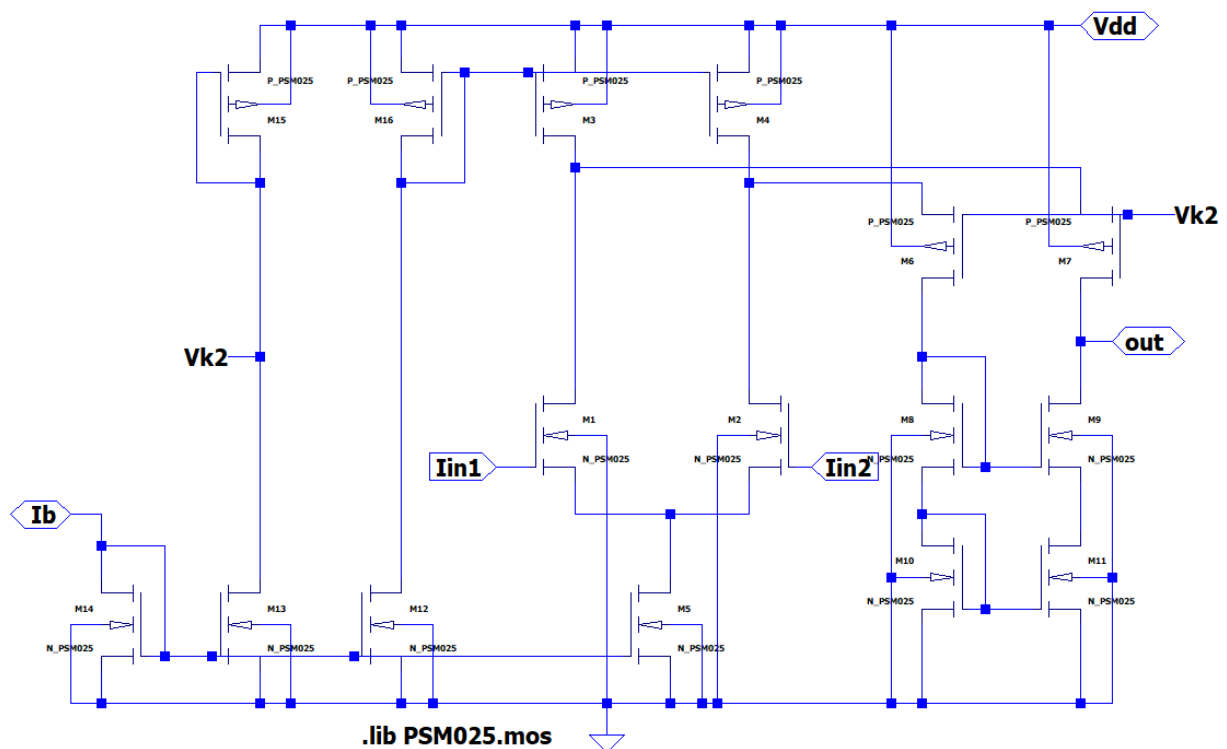
## Folded Cascode CMOS con ingresso n

*Report Preliminare*

Si riporta il circuito da progettare



Di seguito si riporta lo schematico su LTSpice

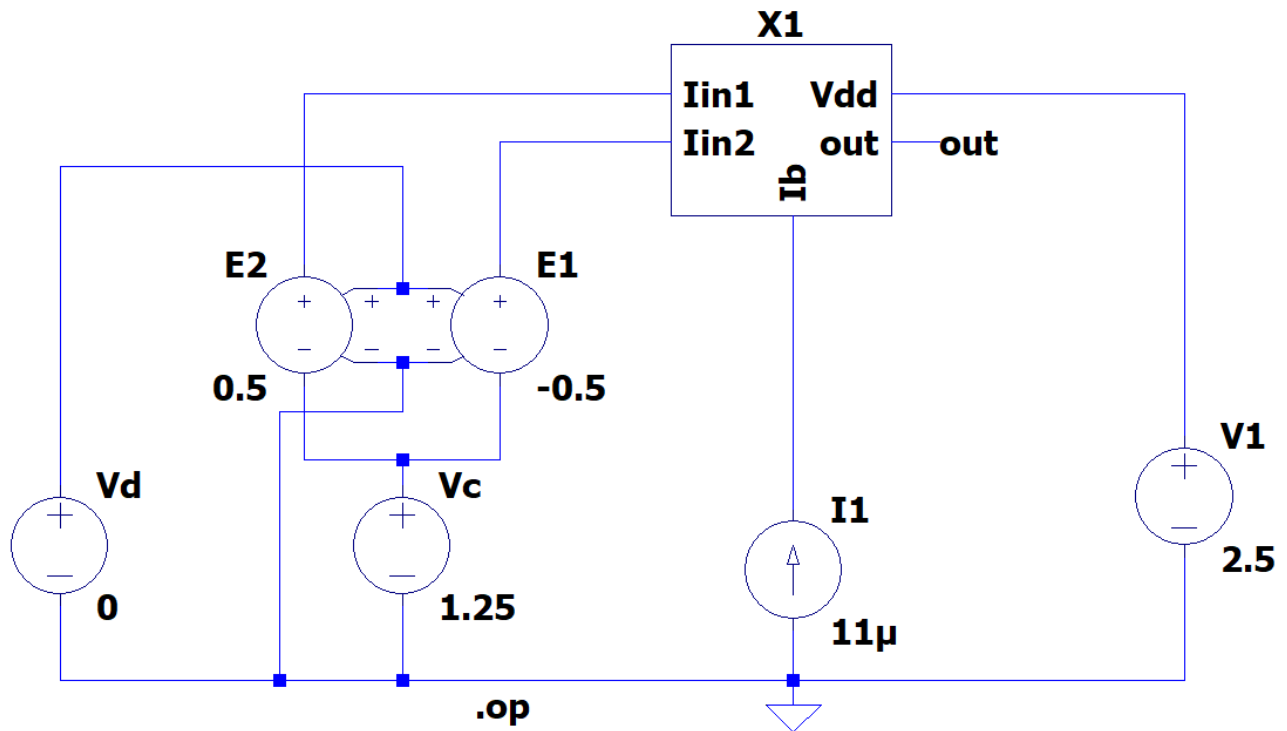


Le condizioni per il progetto sono:

V<sub>dd</sub>=2.5 V

$$I_b = 11 \mu A, I_0 = 22 \mu A, I_1 = 22 \mu A, I_{D12} = I_b, I_{D13} = 3 I_b$$

Facendo riferimento al seguente test-bench



Si effettua una preliminare analisi del punto di riposo (.op) e si verifica che i transistori siano in saturazione e che le  $V_{GS}-V_t$  siano vicine a quelle richieste.

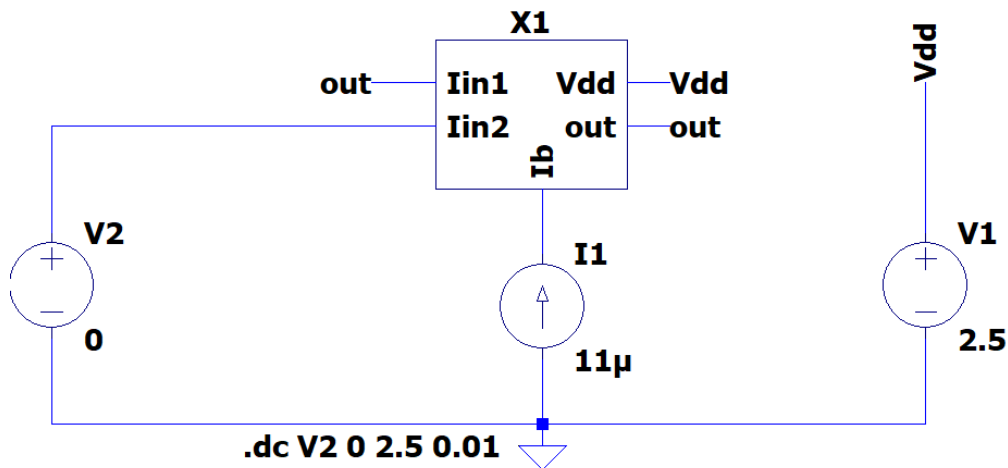
Tramite lo “Spice Error Log” si ottiene

Name:	m:x1:5	m:x1:8	m:x1:9	m:x1:10	m:x1:11	Name:	m:x1:14	m:x1:13	m:x1:12	m:x1:1	m:x1:2
Model:	x1:n_psm025	x1:n_psm025	x1:n_psm025	x1:n_psm025	x1:n_psm025	Model:	x1:n_psm025	x1:n_psm025	x1:n_psm025	x1:n_psm025	x1:n_psm025
Id:	2.12e-05	1.27e-05	1.27e-05	1.27e-05	1.27e-05	Id:	1.10e-05	3.43e-05	1.21e-05	1.06e-05	1.06e-05
Vgs:	6.51e-01	7.92e-01	7.92e-01	6.69e-01	6.69e-01	Vgs:	6.51e-01	6.51e-01	6.51e-01	7.34e-01	7.34e-01
Vds:	5.16e-01	7.92e-01	7.92e-01	6.69e-01	6.69e-01	Vds:	6.51e-01	1.42e+00	1.75e+00	1.74e+00	1.74e+00
Vbs:	0.00e+00	-6.69e-01	-6.69e-01	0.00e+00	0.00e+00	Vbs:	0.00e+00	0.00e+00	0.00e+00	-5.16e-01	-5.16e-01
Vth:	4.24e-01	5.58e-01	5.58e-01	4.20e-01	4.20e-01	Vth:	4.21e-01	4.18e-01	4.12e-01	5.23e-01	5.23e-01
Vdsat:	1.89e-01	2.11e-01	2.11e-01	2.04e-01	2.04e-01	Vdsat:	1.92e-01	1.93e-01	1.97e-01	1.91e-01	1.91e-01
Gm:	1.78e-04	1.00e-04	1.00e-04	9.82e-05	9.82e-05	Gm:	9.15e-05	2.81e-04	9.69e-05	9.20e-05	9.20e-05
Gds:	2.81e-06	1.20e-06	1.20e-06	1.33e-06	1.33e-06	Gds:	1.21e-06	2.85e-06	9.61e-07	8.91e-07	8.91e-07
Gmb:	3.79e-05	1.67e-05	1.67e-05	2.06e-05	2.06e-05	Gmb:	1.92e-05	6.01e-05	2.04e-05	1.61e-05	1.61e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	2.46e-15	1.23e-15	1.23e-15	1.23e-15	1.23e-15	Cgsov:	1.23e-15	3.70e-15	1.23e-15	1.23e-15	1.23e-15
Cgdov:	2.46e-15	1.23e-15	1.23e-15	1.23e-15	1.23e-15	Cgdov:	1.23e-15	3.70e-15	1.23e-15	1.23e-15	1.23e-15
Cgbov:	1.00e-18	1.00e-18	1.00e-18	1.00e-18	1.00e-18	Cgbov:	1.00e-18	1.00e-18	1.00e-18	1.00e-18	1.00e-18
dQgdVgb:	2.65e-14	1.30e-14	1.30e-14	1.32e-14	1.32e-14	dQgdVgb:	1.32e-14	3.97e-14	1.32e-14	1.30e-14	1.30e-14
dQgdVdb:	-2.37e-15	-1.18e-15	-1.18e-15	-1.18e-15	-1.18e-15	dQgdVdb:	-1.18e-15	-3.52e-15	-1.17e-15	-1.17e-15	-1.17e-15
dQgdVsb:	-2.30e-14	-1.13e-14	-1.13e-14	-1.15e-14	-1.15e-14	dQgdVsb:	-1.15e-14	-3.45e-14	-1.15e-14	-1.13e-14	-1.13e-14
dQddVgb:	-1.13e-14	-5.65e-15	-5.65e-15	-5.65e-15	-5.65e-15	dQddVgb:	-5.65e-15	-1.69e-14	-5.64e-15	-5.64e-15	-5.64e-15
dQddVdb:	2.42e-15	1.20e-15	1.20e-15	1.20e-15	1.20e-15	dQddVdb:	1.20e-15	3.60e-15	1.20e-15	1.20e-15	1.20e-15
dQddVsb:	1.11e-14	5.24e-15	5.24e-15	5.52e-15	5.52e-15	dQddVsb:	5.51e-15	1.66e-14	5.51e-15	5.28e-15	5.28e-15
dQbdVgb:	-3.87e-15	-1.68e-15	-1.68e-15	-1.94e-15	-1.94e-15	dQbdVgb:	-1.94e-15	-5.85e-15	-1.95e-15	-1.73e-15	-1.73e-15
dQbdVdb:	-7.29e-18	7.45e-19	7.45e-19	1.10e-18	1.10e-18	dQbdVdb:	1.23e-18	1.48e-17	5.12e-18	2.99e-18	2.99e-18
dQbdVsb:	-1.57e-15	-4.04e-16	-4.04e-16	-7.76e-16	-7.76e-16	dQbdVsb:	-7.84e-16	-2.34e-15	-7.86e-16	-4.73e-16	-4.73e-16

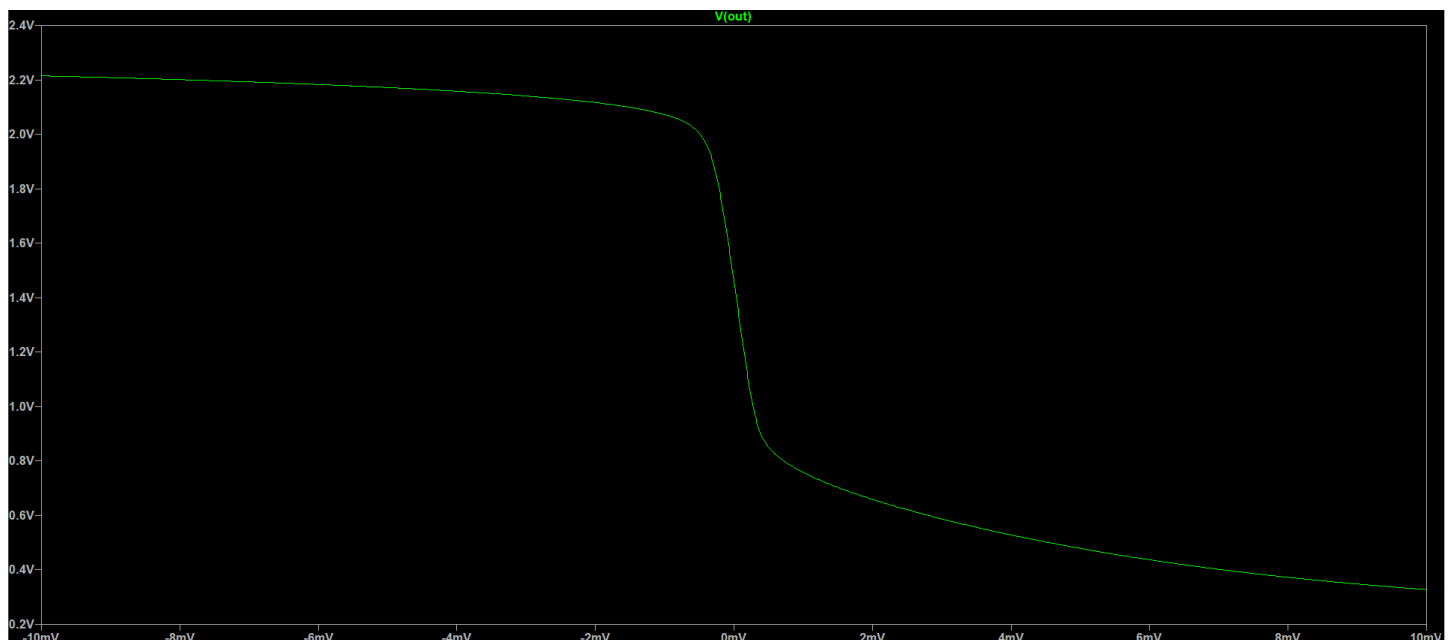
Name:	m:x1:15	m:x1:16	m:x1:3	m:x1:4	m:x1:6	m:x1:7
Model:	x1:p_psm025	x1:p_psm025	x1:p_psm025	x1:p_psm025	x1:p_psm025	x1:p_psm025
Id:	-3.43e-05	-1.21e-05	-2.33e-05	-2.33e-05	-1.27e-05	-1.27e-05
Vgs:	-1.08e+00	-7.54e-01	-7.54e-01	-7.54e-01	-8.35e-01	-8.35e-01
Vds:	-1.08e+00	-7.54e-01	-2.46e-01	-2.46e-01	-7.93e-01	-7.93e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	2.46e-01	2.46e-01
Vth:	-5.67e-01	-5.67e-01	-5.67e-01	-5.67e-01	-6.41e-01	-6.41e-01
Vdsat:	-4.34e-01	-1.89e-01	-1.90e-01	-1.90e-01	-1.98e-01	-1.98e-01
Gm:	1.19e-04	1.06e-04	2.00e-04	2.00e-04	1.09e-04	1.09e-04
Gds:	1.12e-06	6.03e-07	7.90e-06	7.90e-06	6.07e-07	6.07e-07
Gmb:	3.85e-05	3.43e-05	6.54e-05	6.54e-05	3.14e-05	3.14e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	3.64e-15	7.57e-15	1.51e-14	1.51e-14	7.57e-15	7.57e-15
Cgdov:	3.64e-15	7.57e-15	1.51e-14	1.51e-14	7.57e-15	7.57e-15
Cgbov:	9.36e-19	9.36e-19	9.36e-19	9.36e-19	9.36e-19	9.36e-19
dQgdVgb:	3.26e-14	6.76e-14	1.36e-13	1.36e-13	6.72e-14	6.72e-14
dQgdVdb:	-3.65e-15	-7.58e-15	-1.66e-14	-1.66e-14	-7.58e-15	-7.58e-15
dQgdVsb:	-2.72e-14	-5.57e-14	-1.12e-13	-1.12e-13	-5.57e-14	-5.57e-14
dQddVgb:	-1.42e-14	-2.95e-14	-6.02e-14	-6.02e-14	-2.95e-14	-2.95e-14
dQddVdb:	3.64e-15	7.58e-15	1.63e-14	1.63e-14	7.58e-15	7.58e-15
dQddVsb:	1.39e-14	2.89e-14	5.84e-14	5.84e-14	2.82e-14	2.82e-14
dQbdVgb:	-4.14e-15	-8.56e-15	-1.60e-14	-1.60e-14	-8.12e-15	-8.12e-15
dQbdVdb:	-6.40e-18	-8.12e-18	-8.66e-16	-8.66e-16	-7.02e-18	-7.02e-18
dQbdVsb:	-4.31e-15	-9.74e-15	-2.02e-14	-2.02e-14	-8.18e-15	-8.18e-15

Si può notare che le  $V_{GS}-V_t$  dei transistor rientrano nel range richiesto  $200\text{mV} \pm 20\text{mV}$ , mentre per quanto riguarda il transistor M15, che dovrebbe avere  $V_{GS}-V_t = 500\text{mV}$ , si ottiene un valore di  $434\text{mV}$ .

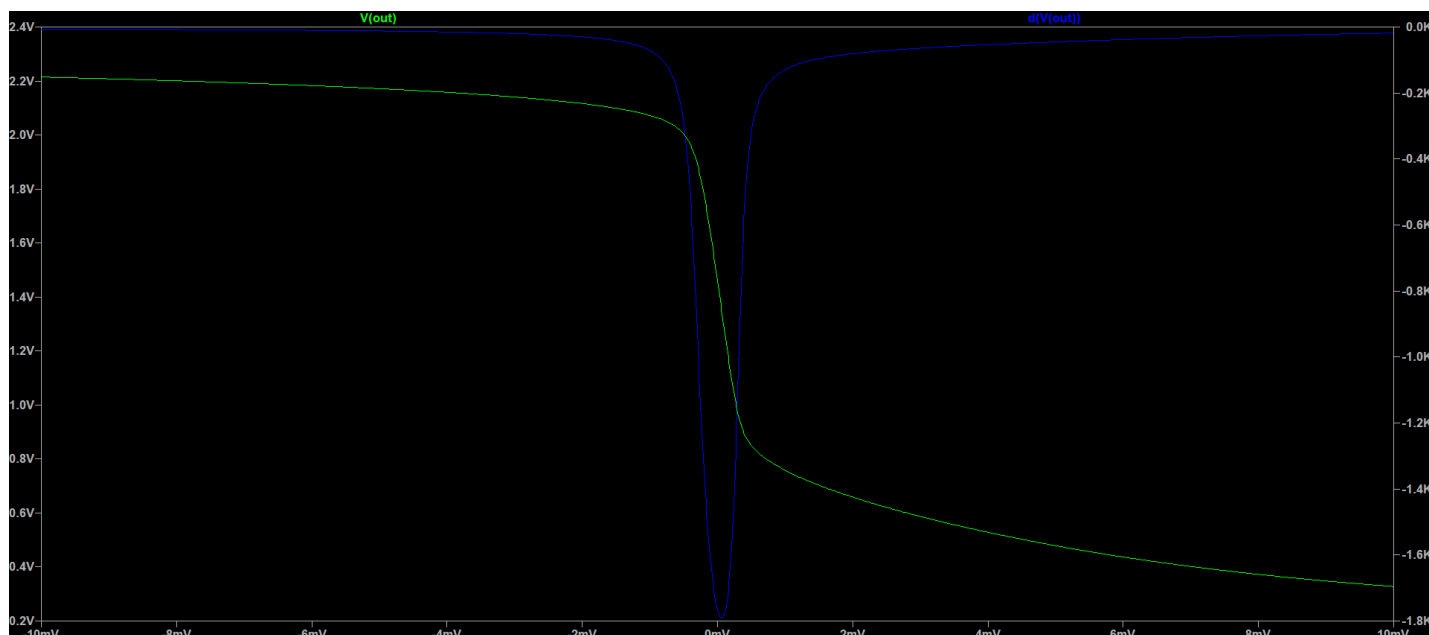
La seconda simulazione da effettuare è stata realizzata con la stessa test-bench, ma realizzando un dc sweep della tensione  $V_d$  tra  $-10\text{mV}$  e  $+10\text{mV}$  con un passo di  $10\text{ }\mu\text{V}$  mantenendo  $V_C$  a  $1.25\text{ V}$  (.dc  $V_d -10\text{m} 10\text{m} 10\text{u}$ )



Di seguito riporta il grafico della corrispondente tensione di uscita



Per una stima dell'amplificazione si riporta il grafico di  $d(V(out))/d(V_d)$



Cursor 1	
d(V(out))	
Horz:	0V
Vert:	-1.7687201K
Cursor 2	
Horz:	-- N/A--
Vert:	-- N/A--
Diff (Cursor2 - Cursor1)	
Horz:	-- N/A--
Vert:	-- N/A--
Slope:	
-- N/A--	

Grazie al cursore si ha un guadagno  $A_d \approx 1768$ , valore che rientra nelle specifiche ( $>1000$ ).

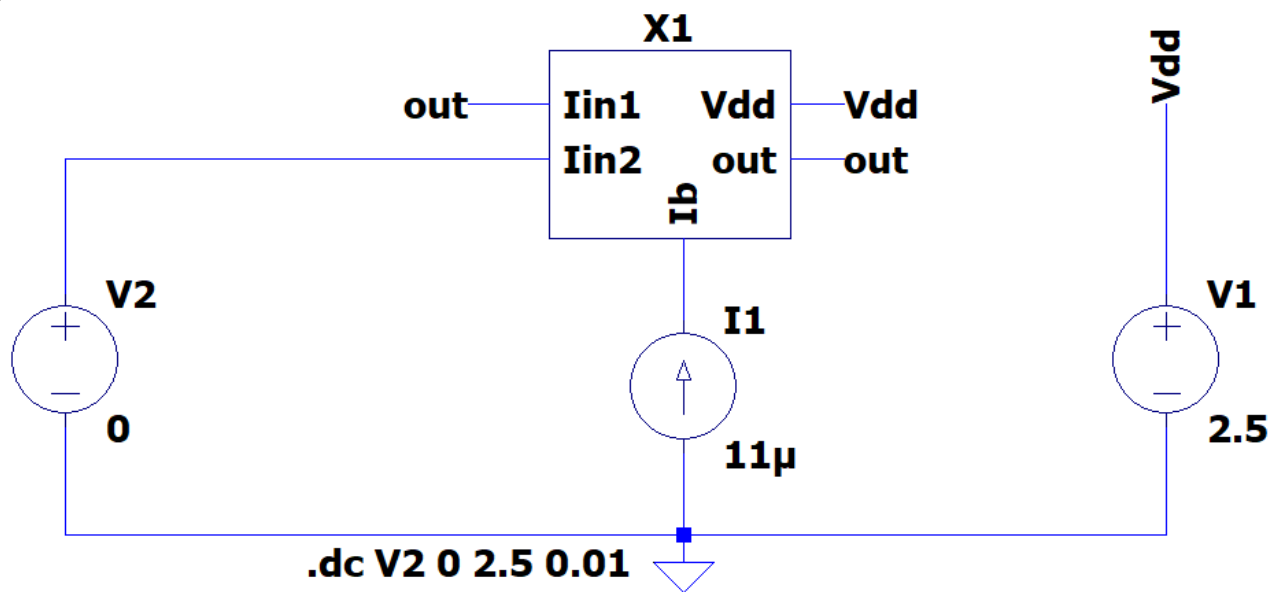
La seconda stima da effettuare è quella relativa alla tensione di offset sistematica dello stadio, un secondo cursore fornisce

Cursor 1	
V(out)	
Horz:	120 $\mu$ V
Vert:	1.2464658V
Cursor 2	
Horz:	-- N/A--
Vert:	-- N/A--
Diff (Cursor2 - Cursor1)	
Horz:	-- N/A--
Vert:	-- N/A--
Slope:	
-- N/A--	

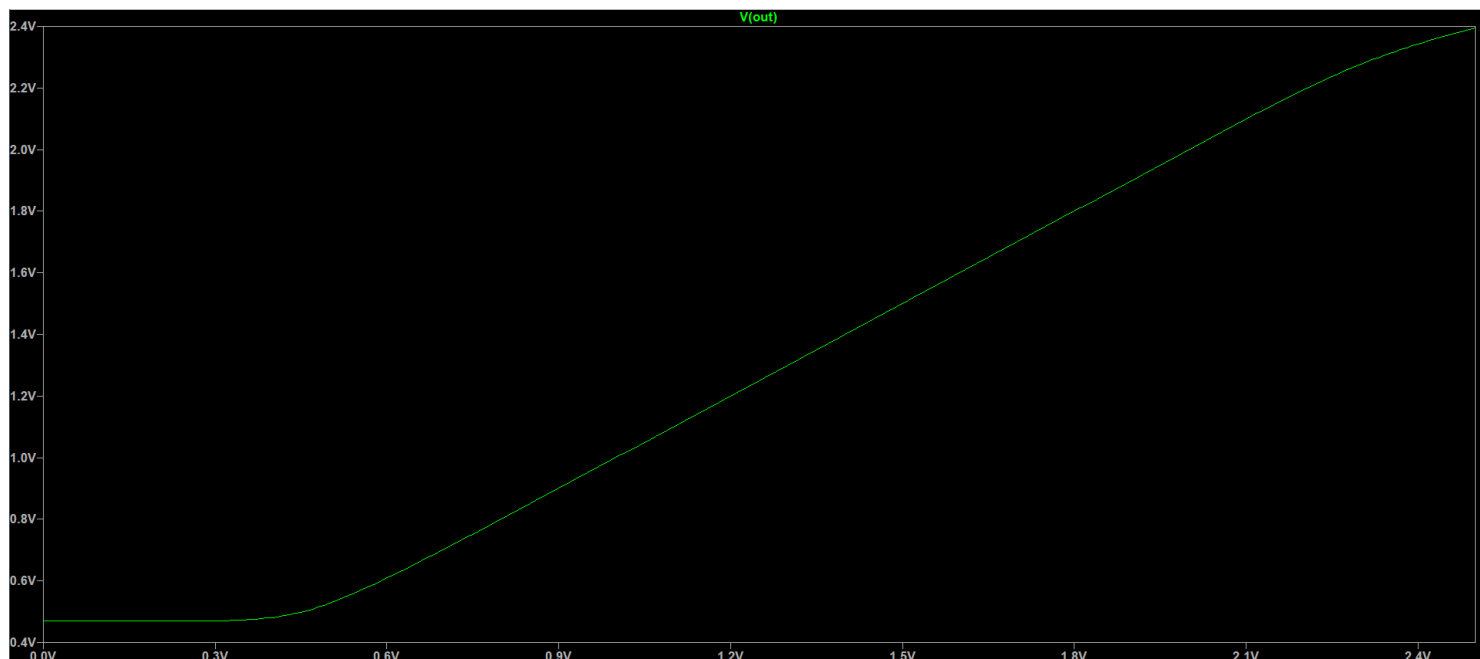
Si ha un offset sistematico pari a 120  $\mu$ V, valore che non rientra nelle specifiche richieste ( $<100 \mu$ V). Tale risultato è frutto di alcuni tentativi di dimensionamento per cercare di avvicinarsi alle specifiche richieste e rappresenta il miglior risultato che si è riusciti ad ottenere.

Come simulazione finale si chiede si collegare l'amplificatore operazionale a formare un buffer ed effettuare un dc sweep della tensione da 0 a Vdd con step 0.01V (.dc V2 0 2.5 0.01).

Si riporta la test-bench utilizzata



Il risultato della simulazione è il seguente



Cursor 1	
V(out)	
Horz: 2.29V	Vert: 2.2692878V
Cursor 2	
V(out)	
Horz: 600mV	Vert: 609.31259mV
Diff (Cursor2 - Cursor1)	
Horz: -1.69V	Vert: -1.6599752V
Slope: 0.982234	

Il range di linearità misurato risulta pari a:

$$600 \text{ mV} < V_{in} < 2.29 \text{ V}$$