Politecnico di Torino

III Facoltà di Ingegneria

Synthesizable LBIST for RI5CY processor Testing and Fault Tolerance

Master degree in Electronic Engineering

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1 LBIST

1.1 Specifications

The LBIST interacts with a RI5CY processor, which has been modified inserting 20 scan chains in order to improve the testability of the system. Furthermore additional test points have been added in order to increase the controllability and observability of random resistant pins. Two additional signals have been added:

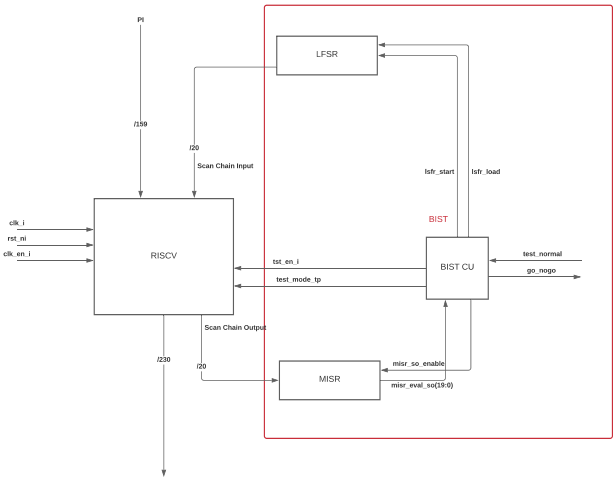
- *test_mode_tp*: used in order to enable the test point itself
- *test_en_i*: used in order to enable scan chains

Here it's reported the scan chain implementation result:

Scan_path	Len	ScanDataIn	ScanDataOut	ScanEnable	MasterClock	SlaveClock
I 1	152	test_si1	test_so1	test_en_i	clk_i	-
I 2	152	test_si2	test_so2	test_en_i	clk_i	-
I 3	152	test_si3	test_so3	test_en_i	clk_i	-
I 4	152	test_si4	test_so4	test_en_i	clk_i	-
I 5	152	test_si5	test_so5	test_en_i	clk_i	-
I 6	152	test_si6	test_so6	test_en_i	clk_i	-
I 7	152	test_si7	test_so7	test_en_i	clk_i	-
I 8	152	test_si8	test_so8	test_en_i	clk_i	-
I 9	152	test_si9	data_we_o	test_en_i	clk_i	-
I 10	152	test_si10	irq_id_o[4]	test_en_i	clk_i	-
I 11	152	test_si11	test_so11	test_en_i	clk_i	-
I 12	152	test_si12	test_so12	test_en_i	clk_i	-
I 13	152	test_si13	test_so13	test_en_i	clk_i	-
I 14	152	test_si14	test_so14	test_en_i	clk_i	-
I 15	152	test_si15	test_so15	test_en_i	clk_i	-
I 16	152	test_si16	test_so16	test_en_i	clk_i	-
I 17	152	test_si17	test_so17	test_en_i	clk_i	-
I 18	151	test_si18	test_so18	test_en_i	clk_i	-
I 19	151	test_si19	test_so19	test_en_i	clk_i	-
I 20	151	test_si20	test_so20	test_en_i	clk_i	-

The LBIST applies 10 000 different patterns to the system, with an expected fault coverage of around 80%. In the result section it's reported the fault coverage with 100 vectors, but the 80% value has been estimated starting from the 10 000 and 1 million random vectors fault simulation.

1.2 Architecture



The LBIST is composed by three main blocks:

- BIST Controller
- LFSR
- MISR

1.2.1 BIST Controller

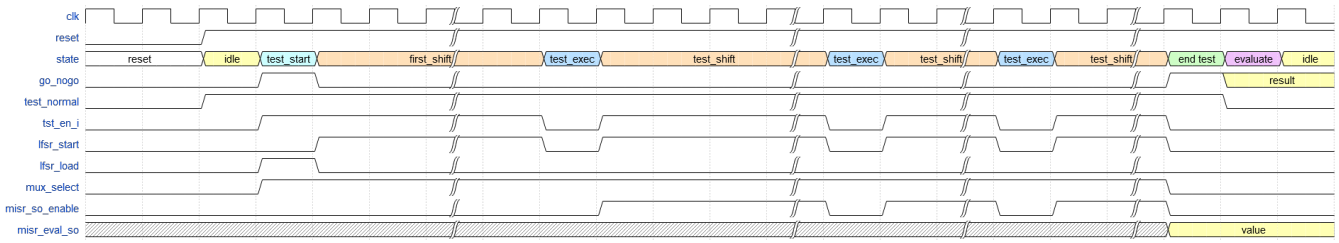


Figure 1: Expected Behaviour

It's the core of the LBIST, his task is to communicate with the different modules, the RI5CY and the outside.To do so it uses the following signals:

- **lfsr_load**: used to load in the LFSR the starting seed. In this HW the selected seed is "0x00001";
- **lfsr_start**: used to enable the LFSR shift, so that it doesn't change value during the execution phase, and allows to use every pattern generated with that specific seed;
- **misr_so_enable**: used to enable the MISR during the *shift out* phase, meanwhile it keeps it disabled during the other phases;
- **misr_so_eval(19:0)**: signal containing the signature, it's compared to the golden signature at the end of the test;
- **test_en_i**: used in order to enable the scan chains during the test phase, it goes to zero during the execution phase;
- **test_mode_tp**: used in order to enable the test points during the test;
- **test_normal**: signal coming from the outside to control the test start. It's expected to stay at '1' during the whole test;
- **go_nogo**: goes to '1' one clock cycle after the test is started, then goes to '1' at the end of the test to signal that the following value is going to be the result of the test:
  - '1' if the signature is equal to the golden signature: no failures detected;
  - '0' otherwise, it means that there is a failure in the system.

The test is divided in different phases:

1. **test_start:**The LSFR is loaded with the seed, and go_nogo is put to '1' to signal the beginning of the test
2. **test_shift:**The system executes at the same time the shift in and shift out of the values in the scan chains (lasts 152 clock cycle, as the longest scan chain)
3. **test_exec:**LFSR and MISR are stopped;test mode is disabled, in order to have an execution in normal mode
4. **end_test,evaluate:**The result is communicated to the outside

1.2.2 LFSR

The LFSR is used to generate the random patterns, used as inputs for the scan chains. The primitive polynomial used in order to build it is:

$$x^{20} + x^3 + 1 \tag{1}$$

Which means that the system is able to generate up to 2^{20} unique values.

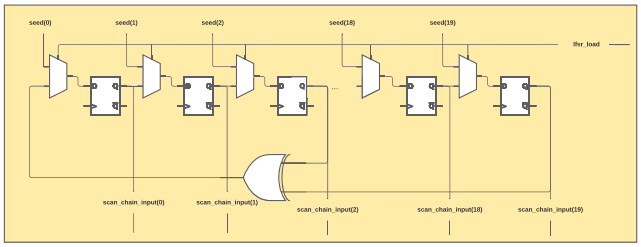


Figure 2: LFSR

1.2.3 MISR

A MISR is used as Output Data Evaluator, in particular we use a MISR associated to the primitive polynomial:

$$x^{20} + x^3 + 1 \tag{2}$$

It's shown in the following picture:

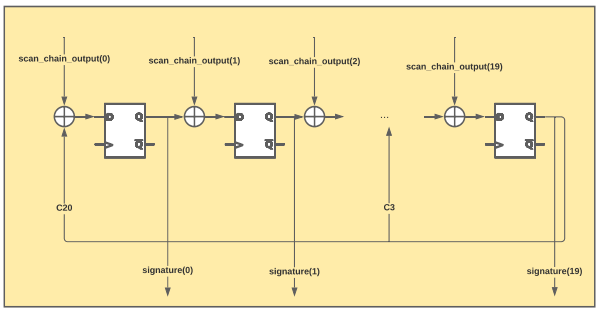


Figure 3: MISR

For readability purposes there are only the first and last flip flops reported, but the chain continues in the dotted section. C3 is used as input for the XOR having as inputs also scan_chain_output(17) and the output of the 17th flipflop. At the end of the test the signature is compared to the golden one by the LBIST controller. Here it's reported the golden signature for a test of 10 000 patterns:

$$\textbf{golden\_signature} = 0x2EAE6$$

1.3 Simulation Results

The following two waves show the behaviour of the LBIST in case of a correct signature and a wrong signature. The LBIST go_nogo signal follows the communication protocol described before. As soon as the test finishes it rises the signal to '1' for a clock cycle and the following clock cycle it changes it value to either '1' in case of correct signature or '0' in case of wrong signature (faulty system).

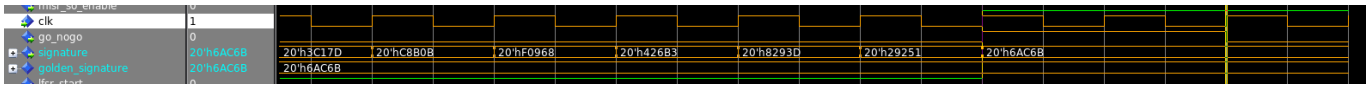


Figure 4: Correct Signature go_nogo = '1' -> '1'

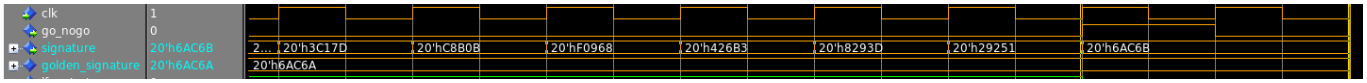


Figure 5: Wrong Signature go_nogo = '1' -> '0'

Here it is reported the signals of a full example test of one vector, which matches the expected waveform designed in the introductory phase:

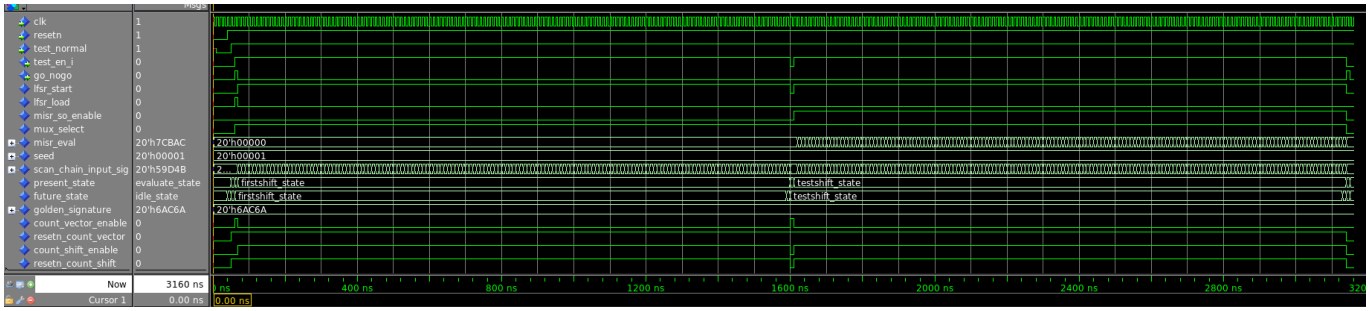


Figure 6: Single Execution Simulation

2 Results

2.1 Fault Coverage with a random pattern generation using TetraMAX

Here is reported the fault coverage with 10 000 and 1 million random vectors:

10k Vectors:

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT     235461
  detected_by_simulation         DS    (210597)
  detected_by_implication        DI     (24864)
Possibly detected                PT          0
Undetectable                     UD        212
  undetectable-unused            UU         (86)
  undetectable-tied              UT        (126)
ATPG untestable                  AU         25
  atpg_untestable-not_detected   AN         (25)
Not detected                     ND      59846
  not-controlled                 NC       (8517)
  not-observed                   NO      (51329)
-----------------------------------------------
total faults                             295544
test coverage                             79.73%
fault coverage                            79.67%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                            0
-----------------------------------------------
```

1M vectors:

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT     253934
  detected_by_simulation         DS    (229071)
  detected_by_implication        DI     (24863)
Possibly detected                PT          0
Undetectable                     UD        212
  undetectable-unused            UU         (86)
  undetectable-tied              UT        (126)
ATPG untestable                  AU         33
  atpg_untestable-not_detected   AN         (33)
Not detected                     ND      41365
  not-controlled                 NC       (6671)
  not-observed                   NO      (34694)
-----------------------------------------------
total faults                             295544
test coverage                             85.98%
fault coverage                            85.92%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                            0
-----------------------------------------------
```

It's noticeable that by increasing greatly the number of vectors the fault coverage doesn't increase as much.

2.2 Fault Coverage using vectors generated by the LBIST vs ATPG

Here is reported the fault coverage obtained starting from 100 vectors generated from our LFSR:

LBIST:

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT     164526
  detected_by_simulation         DS    (139662)
  detected_by_implication        DI     (24864)
Possibly detected                PT       3933
  not_analyzed-pos_detected      NP      (3933)
Undetectable                     UD        212
  undetectable-unused            UU         (86)
  undetectable-tied              UT        (126)
ATPG untestable                  AU          0
Not detected                     ND     126873
  not-controlled                 NC      (6994)
  not-observed                   NO    (119879)
-----------------------------------------------
total faults                             295544
test coverage                             56.37%
fault coverage                            56.33%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                           0
#external patterns (run/riscv_dumpports_100.vcd.fixed)  15403
    #full_sequential patterns            15403
-----------------------------------------------
```

ATPG:

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT     293594
Possibly detected                PT          0
Undetectable                     UD       1201
ATPG untestable                  AU        630
Not detected                     ND         37
-----------------------------------------------
total faults                             295462
test coverage                             99.77%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                        2437
    #basic_scan patterns                  2410
    #full_sequential patterns               27
-----------------------------------------------
```

It's noticeable that with 100 vectors the fault coverage for the stuck-at faults is discreetly good. The actual fault coverage using 10 000 vectors, as in the final version of the LBIST, is likely going to be close to the value obtained before, around 80% with the random patterns. The ATPG results arrive close to 100% coverage.

2.3 Test Application Time

The test duration (considering a t_{clk} of 10 ns, so a f_{clk} of 100Mhz) is given by the simple equation:

$$t_{test} = ((scan\_cells\_longest\_chain + 1) \cdot vectors + scan\_cells\_longest\_chain) \cdot t_{clk} =$$

$$((152 + 1) \cdot 10000 + 152) \cdot 10ns = 15301520ns$$

Which is equal to around 15.3 ms.

2.4 Area Overhead

As expected, the area overhead caused by the LBIST hardware is negligible with respect to the area of the RI5CY processor.

```
****************************************
Report : area
Design : riscv_core_0_128_1_16_1_1_0_0_0_0_0_0_0_0_0_
3_6_15_5_1a110800
Version: R-2020.09-SP2
Date   : Thu Jan 13 15:49:19 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /home/s287758/tft-hw-assignment/
syn/techlib/NangateOpenCellLibrary_typical_ccs_scan.db)

Number of ports:                         8930
Number of nets:                         51427
Number of cells:                        39701
Number of combinational cells:          36411
Number of sequential cells:              3135
Number of macros/black boxes:               0
Number of buf/inv:                       6075
Number of references:                      18

Combinational area:              40202.442097
Buf/Inv area:                     3526.894016
Noncombinational area:           20692.672204
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 60895.114301
Total area:                 undefined
1
```

```
****************************************
Report : area
Design : bist
Version: R-2020.09-SP2
Date   : Fri Jan 14 18:26:18 2022
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    NangateOpenCellLibrary (File: /home/s287758/tft-hw-assignment/syn_system/techlib/
NangateOpenCellLibrary_typical_ccs_scan.db)

Number of ports:                          223
Number of nets:                           586
Number of cells:                          359
Number of combinational cells:            272
Number of sequential cells:                63
Number of macros/black boxes:               0
Number of buf/inv:                         20
Number of references:                       3

Combinational area:                298.984000
Buf/Inv area:                       11.172000
Noncombinational area:             284.885990
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                   583.869990
Total area:                 undefined
1
```