Product Errata
December 6, 2023

VA416xx

Radiation Hardened VA416XX

32-Bit Arm® Cortex®-M4

Errata (Rev. B silicon)

VOR-ER1004: Serial Wire Debug		
Description	**Workaround**	**Comment**
Serial Wire Debug (SWD) is not functioning as intended without code in boot memory.	VA41630: Will ship devices with code in NVM. Do not erase internal NVM and leave blank VA41620/28/29: External memory must have code programmed into it.	Present in VA416xx Rev B silicon.
VOR-ER1008: True Random Number Generator (TRNG)		
Description	**Workaround**	**Comment**
A read of EHR_DATA[5] will always return a value of 0x0000_0000 and will automatically clear the contents of EHR_DATA[4:0]	Do not read EHR_DATA[5] until after EHR_DATA[4:0] has been read	Present in VA416xx Rev A/B silicon
VOR-ER1009: Internal Voltage Regulator		
Description	**Workaround**	**Comment**
The use of the internal 1.5V digital and analog regulators can cause an unreliable power-up condition	An external 3.3V and 1.5V supply must be applied to the device	Present in VA416xx Rev A/B silicon
VOR-ER1010: TMR Refresh Issue with UART0 and UART1		
Description	**Workaround**	**Comment**
UART errors (on UART0 and UART1 only) may occur if the TMR refresh rate is set to any number higher than 0 (for refresh every clock cycle)	Set the DIVCOUNT_L value in the REFRESH_CONFIG_L Register to 0x0000	Present in VA416xx Rev B silicon
VOR-ER1011: TRSTn pull resistor direction		
Description	**Workaround**	**Comment**
Pulling the TRSTn up through a 10k Ohm resistor may	For proper programming operation of the MCU, pin TRSTn should be	Present in VA416xx Rev B silicon

result in NVM programming issues	pulled down through a 10k Ohm resistor	
VOR-ER1012: Internal Band-Gap Measurement		
Description	**Workaround**	**Comment**
Performing an ADC conversion on ADC channels 11 or 12 can cause the MCU to reset	Do not set up the ADC to perform an ADC conversion on either the Bandgap 1.0V (channel 11) or the Bandgap 1.5V (channel 12)	Present in VA416xx Rev B silicon
VOR-ER1013: External Bus Interface (EBI) Wait States		
Description	**Workaround**	**Comment**
Extra wait states are required for EBI reads above 70MHz	Program the CFGWRITECYCLE in the EBICFG[3:0] registers to a value of 3 or higher for bus frequencies of 70MHz or higher	Present in VA416xx Rev B silicon
VOR-ER1014: Ethernet 10/100 MAC does not work at 100Mbps		
Description	**Workaround**	**Comment**
Ethernet peripheral encounters an excessive number of errors at 100Mbps	Ethernet peripheral encounters an excessive number of errors at 100Mbps	Present in VA416xx, both Rev A and Rev B.
VOR-ER1015: EDAC SBE/MBE count registers are not addressed correctly for writes		
Description	**Workaround**	**Comment**
In the SYSCONFIG block, data written to RAM1_SBE is miswritten to RAM0_MBE and data written to RAM0_MBE is incorrectly written to RAM1_SBE. The reads of the counts from RAMx_MBE and RAMx_SBE registers are correct and the EDAC circuitry correctly updates these register counts.	Must compensate for this in the application firmware.	Present in VA416xx Rev A/B silicon
VOR-ER1016: SPI RX FIFO		
Description	**Workaround**	**Comment**
While using block mode SPI transfers, failing to close the block (setting BMSTOP bit in the last transmitted	To ensure all SPI words are received, close the block by appending the BMSTOP bit to the last data word transmitted.	Present in VA416xx, both Rev A & Rev B.

word) will result in the last received word not being registered into the receive FIFO.		
VOR-ER1017: SPI block mode SCK glitch		
Description	**Workaround**	**Comment**
When the SPI is set up with SPH = 0, BMSTALL = 1, and BLOCKMODE = 1, writing BMSTOP + BMSKIPDATA causes a glitch on SCK if the SPI peripheral is stalled (block is open and the TX FIFO is empty).	Close a SPI block by appending the BMSTOP bit on the last data word instead of using BMSTOP + BMSKIPDATA on its own.	Present in VA416xx, both Rev A & Rev B.

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VORAGO Technologies
1501 S. MOPAC Expressway, Suite #350
Austin, TX 78746
www.voragotech.com
Email: info@voragotech.com
Phone: (512) 347-1800