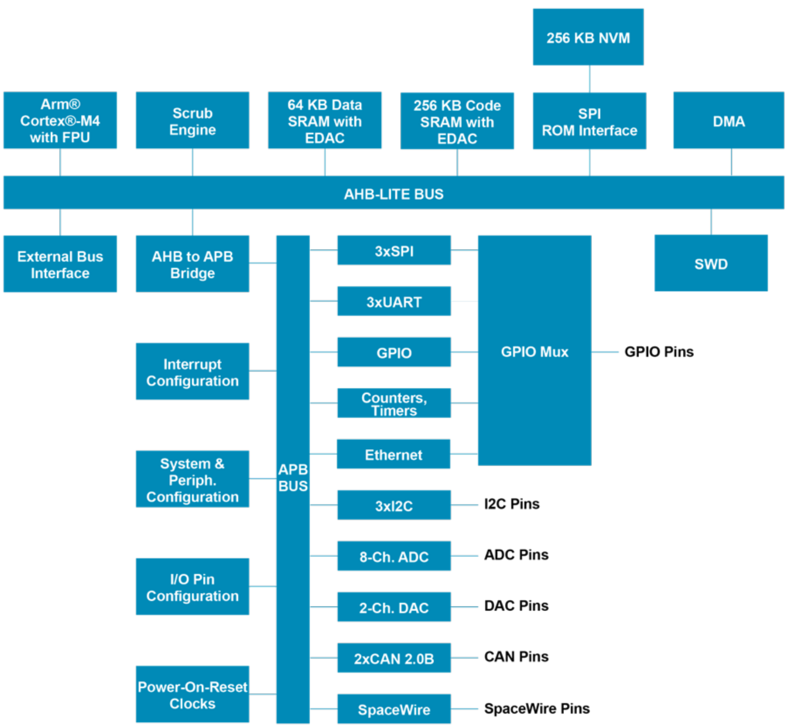
Radiation Hardened VA416X0

32-Bit Arm® Cortex®-M4 (with FPU) microcontroller manufactured with HARDSIL® technology offering best in class radiation performance and latch-up immunity.



MEMORY CONFIGURATION OPTIONS

- Internal FRAM (VA41630 only)
- External SPI NVM (for code boot)
- External parallel NVM (for code boot)
- External memory bus interface (EBI for code or data)

RADIATION HARDENED PERFORMANCE

- VA41620 Total Ionizing Dose (TID) > 300 krad(Si)
- VA41630 Total Ionizing Dose (TID) > 200 krad(Si)[1]
- Soft Error Rate (SER) < 1E-15 errors / bit-day w/ EDAC & Scrub enabled (See Section 7 for details)
- Single-Event Latch-Up (SEL) immunity to LET > 110 MeVcm^2 / mg

KEY FEATURES

- Manufactured with HARDSIL® technology
- RAD hardened Registers with Triple-Mode Redundancy (TMR)
- 32-bit Arm® Cortex®-M4 processor
  - Single-Precision Floating-Point Unit (FPU)
  - SWD based debug interface
- Operating voltages
  - GPIO 3.3 ± 10% V
  - Core 1.5 ± 10% V
- Clock rate up to 100 MHz
  - Internal 20 MHz oscillator for fail-safe clocking
- Memory
  - 64 Kbyte on-chip data and 256 Kbyte on-chip program memory SRAM
  - 256 Kbyte SPI FRAM (VA41630 only)
  - Error Detection and Correction (EDAC)
  - Built-in Scrub Engine
- Peripherals
  - 104 Configurable GPIO pins
  - 3 UART interfaces
  - 3 I^{2}C interfaces
  - 3 SPI interfaces
  - 2 CAN 2.0B
  - Ethernet MAC
  - SpaceWire interface
  - DMA controller
  - 8-Ch 12-bit ADC
  - 2-Ch 12-bit DAC
  - Temperature sensor
- External Asynchronous Parallel Bus Interface (EBI)
  - 8-bit or 16-bit memory support
  - Four chip selects of up to 16 Mbytes each
- Timer System
  - 24 configurable 32-bit counters / timers
  - Input capture, Output compares
  - PWMs, Pulse Counters, Watchdog timer
- Packages
  - 196 BGA (12mm x 12mm)
  - 176 QFP (20mm x 20mm)

SUPPORT

- PEB1 development board
- BSP and drivers
- See product errata in Section 13
- [1] Refer to Infineon-CYPT15B102Q-GGMB-Datasheet for FRAM radiation data.

Features

- Performance
  - 100 MHz Arm® Cortex®-M4 processor with Single-Precision Floating-Point Unit (FPU)
- On-Chip Memory
  - 256 Kbyte Non-Volatile Memory (Infineon FRAM) (VA41630 only)
  - 256 Kbyte Program SRAM
  - 64 Kbyte Data SRAM
  - On-chip Error Detection and Correction (EDAC) and Scrub Engine
- General-purpose I/O (GPIO) pins
  - Configurable direction
  - Configurable pull-up/down resistors
  - Configurable as edge or level sensitive interrupt sources
- 24 General-purpose counter/timers
  - Configurable interrupt sources
  - Can be triggered from multiple sources (GPIO or other counter/timers)
  - Each counter/timer has an independent 32-bit counter
  - Configurable as PWM, capture or compare
- 3 x UARTS
  - Internal FIFO
  - Transmit or receive interrupt source
- 3 x Serial Peripheral Interface (SPI) ports
  - Internal FIFO
  - Transmit or receive interrupt source
  - Multiple chip select outputs
- 3 x I^2C ports
  - Internal FIFO
  - Master and Slave mode on all ports
  - Standard and Fast mode support
- System-level Triple-Mode Redundancy (TMR) on critical internal registers
- 8-Channel, 12-bit ADC
- 2-Channel, 12-bit DAC
- 2 x CAN 2.0B controllers
- Ethernet MAC
- SpaceWire controller with LVDS interface
- Random Number Generator
- Temperature sensor
- Serial Wire Debug (SWD) based debug controller (JTAG is for factory test only)
- Parallel external memory bus interface (EBI)

1 Functional Description

The VA416X0 is optimized for radiation environments and consists of an Arm® Cortex®-M4 CPU core and a related set of peripherals. It includes Error Detection and Correction (EDAC) logic on the internal memories. The program space EDAC is 16-bit word-based for optimum performance and reliability. The data space EDAC is 8-bit to allow reliable byte size data manipulation. In addition, the VA416X0 includes Triple-Mode Redundancy (TMR) with voting on select internal flip-flop storage elements.

1.1 Related Documentation

The following associated documents will help understand this device:

- Arm® Documents (Available from http://infocenter.arm.com)
    - Cortex®-M4 Generic User Guide
    - Cortex®-M4 Technical Reference Manual
    - AMBA® 3 AHB-Lite™ Protocol Specification
    - AMBA® 3 APB Protocol Specification
    - Arm® TrustZone® True Random Number Generator Technical Reference Manual
    - Arm® PrimeCell® External Bus Interface Technical Reference Manual
    - Arm® PrimeCell® DMA Technical Reference Manual
- NXP Documents
    - I^2C-bus Specification
- Infineon Documents
    - FM25V20A FRAM Datasheet
- VORAGO Documents
    - VA416XX Programmer's Guide

1.2 Feature Summary

- Processor Core
    - Arm® Cortex®-M4 processor
        - Up to 100 MHz operation
        - SysTick Counter
        - Single Cycle Multiply-and-accumulate
        - Hardware divide (2 to 12 cycles)
        - Single-precision IEEE 754 compliant HW Floating Point Unit (FPU)
        - Bit-Banding region for registers and data SRAM

- Arm® Cortex®-M4 built-in Nested Vectored Interrupt Controller (NVIC)
  - 240 Interrupt sources with a unique 3-bit priority level (176 of these are used)
  - External Non-Maskable Interrupt (NMI) pin
  - Tail chaining supported
- Arm® CoreSight™ debug and trace technology
  - SWD: Serial Wire Debug
  - DAP: Debug Access Port
  - Four Breakpoint Comparators
  - Two Data Watch Point Comparators

- Memory
  - 64 Kbyte SRAM Data Memory (32 Kbyte on Data bus and 32 Kbyte on System bus)
    - Byte-level Error Detection and Correction (EDAC) logic on Data memory
  - 256 Kbyte SRAM Instruction Memory
    - Loaded from Serial Peripheral Interface (SPI) based memory or from external memory on the External Bus interface at startup
    - Configurable boot delay, boot speed, and error checking
    - 16-bit level EDAC on instruction memory
  - Programmable Scrub Engine for both Data and Instruction memory
  - Utility peripheral
    - Provides means of injecting single and multi-bit errors to check error handling routines.
  - 256 Kbyte serial FRAM in package (VA41630 only)
- System Integration Peripherals
  - System Configuration
    - Memory Control
      - Data memory clear on reset
      - Code memory reload on reset
      - Code memory write protect
      - Code/Data memory Scrub rate
      - Code/Data memory SBE/MBE counters
      - Code/Data memory SBE/MBE Interrupt control
    - GPIO Glitch Filter rate control
    - Peripheral Configuration
      - Clock gating and Reset control of individual peripherals

- Interrupt Router
  - Maps interrupt sources to timers, ADC, DAC, and DMA for flexible event triggers
- Four-Channel DMA
  - Allows CPU independent data movement from memory to memory, peripherals to memory, or memory to peripherals.

- Analog Peripherals
  - 12-bit SAR ADC
    - Eight channels on dedicated pins
    - Internal temperature sensor connection
    - 600 kps maximum sampling rate
    - Triggerable by a timer event
  - Digital to Analog Converter (DAC)
    - Two independent channels on dedicated pins
    - 12-bit resolution
    - 0.5 mA drive capability
    - DMA connection allows waveform generation
- Serial Communication Peripherals
  - Three UARTs
    - 16-word Transmit and Receive FIFOs
    - Fractional baud rate generation
    - Supports:
      - 5, 6, 7, 8, and 9 bits
      - Even, Odd and None parity
      - Stop Bits 1 or 2
      - Break generation and detection
    - Error detection
      - FIFO overflow
      - Framing error
      - Parity error
      - Break detection
    - Configurable Interrupt generation
      - FIFO level (fully configurable)
      - Receive Timeout
      - Error
  - Three SPI Ports (Fourth SPI used only to program Boot SPI FRAM)
    - Supports all four modes of SPI operation
    - Data size of 4 to 16 bits
    - 16-word Transmit and Receive FIFOs

        - Block mode support for larger Frame sizes
        - Master-mode clock rates up to 1/4 System clock (3.125 Mbytes/s)
        - Slave-mode clock rates up to 1/24 System clock (520 kbytes/s)
        - Configurable Interrupt generation for transmitting and receiving
            - FIFO level (fully configurable)
            - FIFO Overflow
            - Receive Timeout
    - Three I^2C Ports
        - Standard I^2C-compliant bus interface
        - Dedicated open-drain pins supporting I^2C Fast mode
        - Configurable as Master or Slave
        - 16-byte Transmit and Receive FIFOs
        - Configurable Interrupt generation
            - FIFO level (fully configurable)
    - Ethernet Media Access Controller (MAC)
        - Supports 10/100BASE-T
        - Media-Independent interface (MII)
    - Two Controller Area Network (CAN) Ports
        - Supports CAN 2.0B
        - Two-wire interface to external Physical Layer (PHY)
    - SpaceWire port
        - Supports SpaceWire standard ECSS-E-ST-50-12C
        - 1k byte receive FIFO
        - 1k byte transmit FIFO
- System Connection Peripherals
    - GPIO
        - Seven GPIO Ports with up to 104 pins total
            - 16-bit ports A-F
            - 8-bit port G
        - Configurable direction control of individual bits
        - Bit-level mask register allows single instruction setting or clearing of any bits in one port.
        - Configurable interrupt generation on ports A-F
            - Level or Edge sensitive
        - Configurable Pulse mode on individual bits
        - Configurable (0 to 3) cycle delay filtering on individual bits

- I/O Configuration
  - Manages programmable function selects of each pin to allow peripherals to be mapped to GPIO
  - Sets electrical parameters:
    - Glitch filters
    - Pull-up/Pull-down resistors
    - Signal inversion
    - Pseudo open-drain
- Timers
  - Twenty-four 32-bit timers
  - Advanced trigger modes using cascade feature
    - Separate Start/Stop based on other timers or interrupt signals
    - Multiple trigger sources from GPIO or other timers
  - Configurable output event
    - One cycle pulse when timer equal to zero detected
    - Active mode
    - Divide by two for square wave creation
    - Two PWM modes: single edge and double edge detection (supports center alignment)
- External Bus interface
  - Asynchronous with 16-bit or 8-bit data width
  - Double mapped in memory to allow Instruction or Data access
  - 16 Mbyte memory space with four chip selects
  - Configurable wait states

- Power supplies
  - Configured for use with dual supplies
    - 3.3 V for I/O
    - 1.5 V for logic
- Radiation Hardness
  - Latch-up immunity in extreme environments
  - Built to be resistant to Single Event Upsets (SEU)
  - Built with VORAGO proprietary HARDSIL® technology
  - Designed with Dual-Interlocked Storage Cells (DICE) and Triple-Mode Redundancy (TMR) on key register elements.

1.3 Boot Sequence

The VA416XX can boot from one of two sources: an internal/external Serial Peripheral Interface (SPI) peripheral connected to the ROM SPI interface or via the External Parallel Bus Interface (EBI). The boot mode is selected with the EBI_BOOT pin. The clock source for boot operation is a 20 MHz internally generated oscillator (HBO)

If EBI_BOOT=0, The VA416X0 begins operation by loading the internal SRAM code memory from an SPI memory (internal/external) via a connected Serial Peripheral Interface (SPI)

If EBI_BOOT=1, The VA416X0 will load the internal code memory from an external memory device via the External Bus Interface.

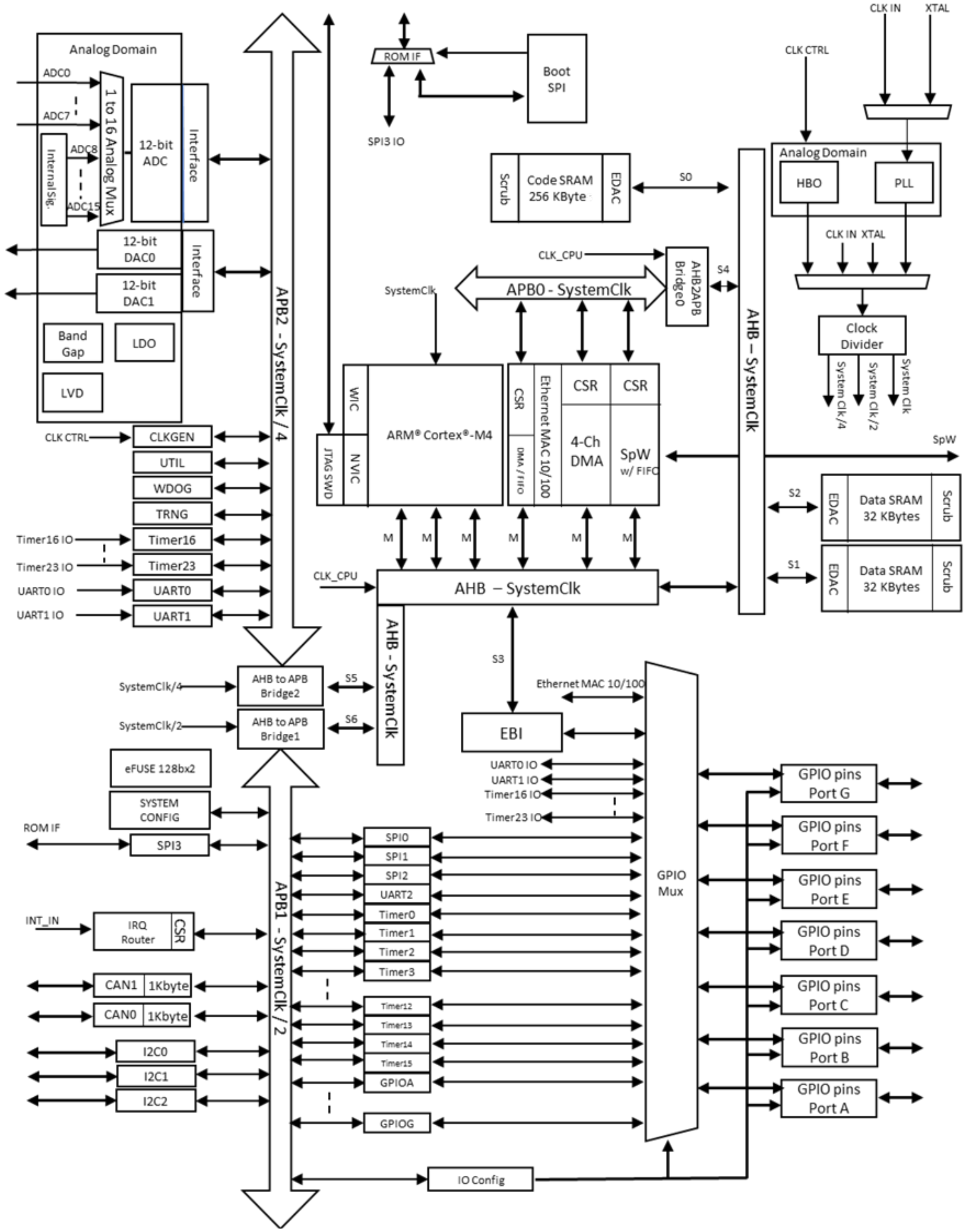
After loading the code memory, the processor follows a typical Arm® Cortex®-M4 start sequence.

1.4 Resets

In addition to the Power-on reset, the device can be reset from other events:

- EXTRESETn pin
- SYSRESETREQ from software
- Hardware events configured by IRQ Selector Peripheral or the System Controller Peripheral:
    - Watchdog Timer
    - Memory Errors (Single or Multi-bit errors from the EDAC memory controller)

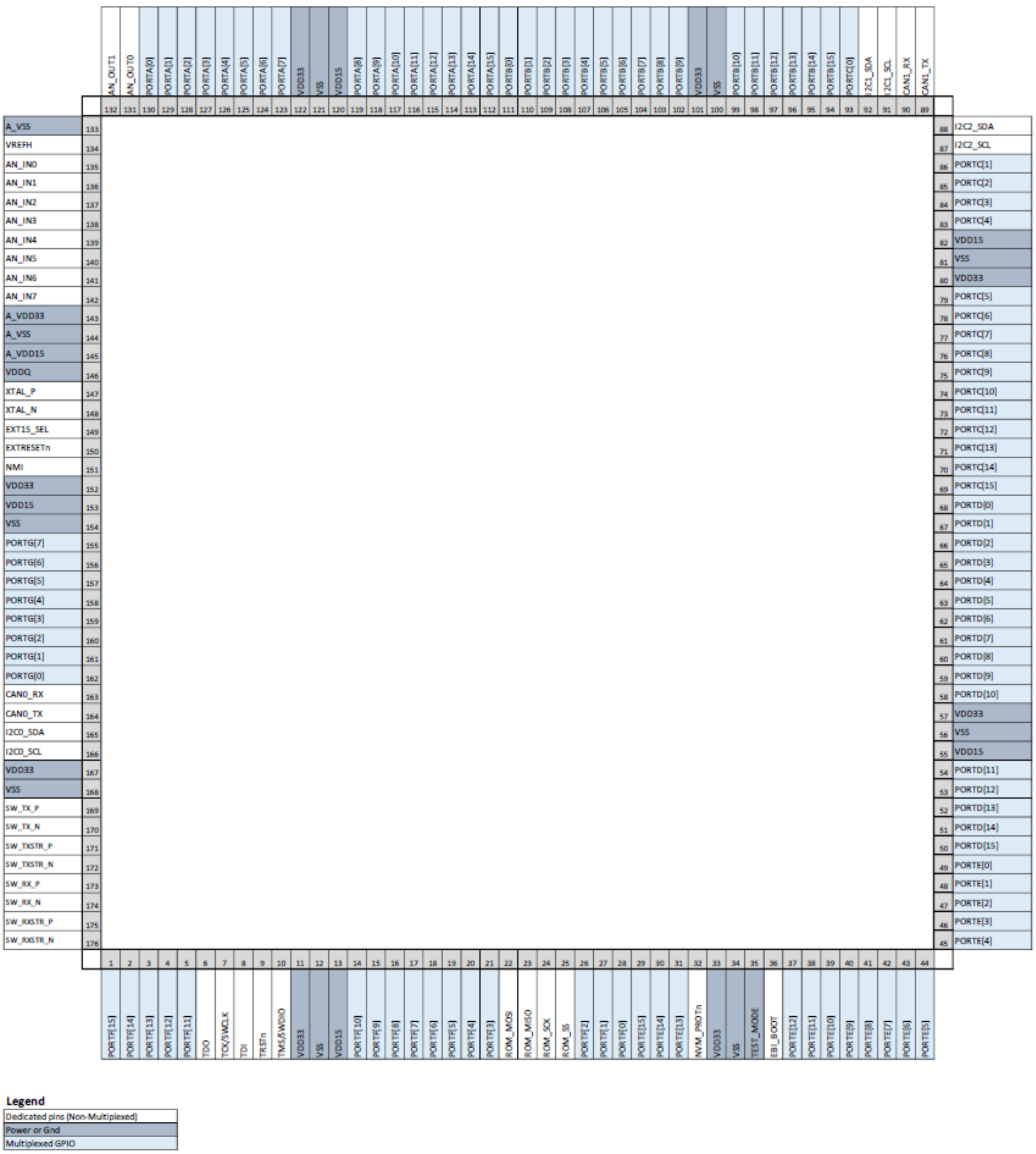
2 Block Diagram



3 Pinout

The VA416X0 is available in a choice of packages: 176-pin plastic QFP, 176-pin ceramic QFP, and 196-pin plastic BGA.

3.1 176-pin QFP pinout



3.2 Pin Descriptions

Pin Type	Description	Type	Internal Pull-up/down
	System Pins		
XTAL_P	Crystal Oscillator Output	Out	None
XTAL_N	Crystal Oscillator Input	In	None
EXTRESETn	External System Reset, active low. Resets the processor and all peripherals. This signal is internally synchronized before being used. Any reset will cause this pin to pull low during the reset sequence.	Async In / Open drain Out	Pull-up
NMI	Non-maskable Interrupt – active high	Async In	None
EBI_BOOT	When high, this signal enables software boot from the EBI port rather than the SPI ROM interface.	In	None
EXT15_SEL	When high, this signal disables the internal 1.5 V regulator, and 1.5 V must be applied externally to all VDD15 pins and A_VDD15.	In	None
NVM_PROTn	When low, this signal inhibits the programming of the internal FRAM (VA41630 only).	In	None
TEST_MODE	For factory use only. Must be tied to VSS with a 10k resistor.	In	None
	General-Purpose I/O Pins		
PORTA[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, Timers, and Ethernet pins.	Sync I/O	Software configurable
PORTB[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, Timers, and Ethernet pins.	Sync I/O	Software configurable
PORTC[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, Timers, and EBI pins.	Sync I/O	Software configurable
PORTD[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, Timers, and EBI pins.	Sync I/O	Software configurable
PORTE[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, Timers, and EBI pins.	Sync I/O	Software configurable

Pin Type	Description	Type	Internal Pull-up/down
PORTF[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, Timers, and EBI pins.	Sync I/O	Software configurable
PORTG[7:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, and Timer pins.	Sync I/O	Software configurable
	SPI ROM pins		
ROM_SCK	SPI Clock to Boot ROM.	Sync Out	None
ROM_SS	SPI Chip Select to Boot ROM (Active Low).	Sync Out	None
ROM_MOSI	SPI Data Out to Boot ROM.	Sync Out	None
ROM_MISO	SPI Data In from Boot ROM (must be tied to VSS for VA41630 devices with an internal FRAM).	Sync In	Pull-down
	I^2C Pins		
I2C0_SCL	I^2C0 Clock	Open drain	None
I2C0_SDA	I^2C0 Data	Open drain	None
I2C1_SCL	I^2C1 Clock	Open drain	None
I2C1_SDA	I^2C1 Data	Open drain	None
I2C2_SCL	I^2C2 Clock	Open drain	None
I2C2_SDA	I^2C2 Data	Open drain	None
	CAN Pins		
CAN0_RX	CAN0 Receive	Sync In	None
CAN0_TX	CAN0 Transmit	Sync Out	None
CAN1_RX	CAN1 Receive	Sync In	None
CAN1_TX	CAN1 Transmit	Sync Out	None
	SWD Pins		
TCK/SWCK	Test Clock/Serial Wire Debug Clock	Clock	None
TMS/SWDIO	Test Mode Select/Serial Wire Debug Data IO	Sync In/Out	Pull-up
TRSTn	Test Reset, active low	Sync In	None
TDI	Test Data In	Sync In	None
TDO	Test Data Out	Sync Out	None
	SpaceWire Pins		
SW_RXSTR_N	Receive strobe negative signal	LVDS	None
SW_RXSTR_P	Receive strobe positive signal	LVDS	None
SW_RX_N	Receive data negative signal	LVDS	None

Pin Type	Description	Type	Internal Pull-up/down
SW_RX_P	Receive data positive signal	LVDS	None
SW_TXSTR_N	Transmit strobe negative signal	LVDS	None
SW_TXSTR_P	Transmit strobe positive signal	LVDS	None
SW_TX_N	Transmit data negative signal	LVDS	None
SW_TX_P	Transit data positive signal	LVDS	None
	Analog pins		
AN_IN0	Analog to digital converter input	In	None
AN_IN1	Analog to digital converter input	In	None
AN_IN2	Analog to digital converter input	In	None
AN_IN3	Analog to digital converter input	In	None
AN_IN4	Analog to digital converter input	In	None
AN_IN5	Analog to digital converter input	In	None
AN_IN6	Analog to digital converter input	In	None
AN_IN7	Analog to digital converter input	In	None
AN_OUT0	Digital to analog converter output	Out	None
AN_OUT1	Digital to analog converter output	Out	None
VREFH	Analog reference	Power	N/A
	Power/Ground/Analog pins		
VDD15	1.5 V Core power (must be supplied externally if EXT15_SEL=1)	Power	N/A
VSS	Ground	Ground	N/A
VDD33	3.3 V IO power	Power	N/A
A_VDD15	1.5 V Analog power (must be supplied externally if EXT15_SEL=1)	Power	N/A
A_VSS	Analog Ground	Ground	N/A
A_VDD33	3.3 V Analog IO power	Power	N/A
VDDQ	For factory use only. Must be tied to VSS	Power	N/A

3.3 GPIO Pin Alternative Functions

GPIO pins can be configured for various peripherals on the VA416X0 MCU. The default configuration is for all the pins to be assigned as GPIO. Please refer to the VA416XX Programmer's Guide for more information about the usage of GPIO pins and their alternative functions.

Port pin default function FUNSEL[1:0]=00	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTA[0]	TIM[0]	SPI2_SSn4	UART0_RTSn
PORTA[1]	TIM[1]	SPI2_SSn3	UART0_CTSn

Port pin default function FUNSEL[1:0]=00	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTA[2]	TIM[2]	SPI2_SSn2	UART0_TX
PORTA[3]	TIM[3]	SPI2_SSn1	UART0_RX
PORTA[4]	TIM[4]	SPI2_SSn0	Not assigned
PORTA[5]	TIM[5]	SPI2_SCK	Not assigned
PORTA[6]	TIM[6]	SPI2_MISO	Not assigned
PORTA[7]	TIM[7]	SPI2_MOSI	Not assigned
PORTA[8]	ETH_MDIO	SPI2_SSn6	TIM[8]
PORTA[9]	ETH_MDC	SPI2_SSn5	Not assigned
PORTA[10]	ETH_RxD3	TIM[23]	Not assigned
PORTA[11]	ETH_RxD2	TIM[22]	Not assigned
PORTA[12]	ETH_RxD1	TIM[21]	Not assigned
PORTA[13]	ETH_RxD0	TIM[20]	Not assigned
PORTA[14]	ETH_Rx_DV	TIM[19]	Not assigned
PORTA[15]	ETH_Rx_CLK	TIM[18]	Not assigned
PORTB[0]	ETH_Rx_ER	TIM[17]	SPI1_SSn7
PORTB[1]	ETH_Tx_ER	TIM[16]	SPI1_SSn6
PORTB[2]	ETH_Tx_CLK	TIM[15]	SPI1_SSn5
PORTB[3]	ETH_Tx_EN	TIM[14]	SPI1_SSn4
PORTB[4]	ETH_TxD0	TIM[13]	SPI1_SSn3
PORTB[5]	ETH_TxD1	TIM[12]	SPI1_SSn2
PORTB[6]	ETH_TxD2	TIM[11]	SPI1_SSn1
PORTB[7]	ETH_TxD3	TIM[10]	SPI1_SSn0
PORTB[8]	ETH_COL	TIM[9]	SPI1_SCK
PORTB[9]	ETH_CRS	TIM[8]	SPI1_MISO
PORTB[10]	ETH_PPS_OUT	TIM[7]	SPI1_MOSI
PORTB[11]	SPI0_SSn3	TIM[6]	Not assigned
PORTB[12]	SPI0_SSn2	TIM[5]	UART1_RTSn
PORTB[13]	SPI0_SSn1	TIM[4]	UART1_CTSn
PORTB[14]	SPI0_SSn0	TIM[3]	UART1_TX
PORTB[15]	SPI0_SCK	TIM[2]	UART1_RX
PORTC[0]	SPI0_MISO	TIM[1]	Not assigned
PORTC[1]	SPI0_MOSI	TIM[0]	Not assigned
PORTC[2]	EBI_A[0][1]	UART0_RTSn	Not assigned
PORTC[3]	EBI_A[1][1]	UART0_CTSn	Not assigned
PORTC[4]	EBI_A[2][1]	UART0_TX	Not assigned
PORTC[5]	EBI_A[3][1]	UART0_RX	Not assigned
PORTC[6]	EBI_A[4][1]	Not assigned	Not assigned

Port pin default function FUNSEL[1:0]=00	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTC[7]	EBI_A[5] [1]	SPI1_SSn1	Not assigned
PORTC[8]	EBI_A[6] [1]	SPI1_SSn0	Not assigned
PORTC[9]	EBI_A[7] [1]	SPI1_SCK	Not assigned
PORTC[10]	EBI_A[8] [1]	SPI1_MISO	Not assigned
PORTC[11]	EBI_A[9] [1]	SPI1_MOSI	Not assigned
PORTC[12]	EBI_A[10] [1]	UART2_RTSn	Not assigned
PORTC[13]	EBI_A[11] [1]	UART2_CTSn	Not assigned
PORTC[14]	EBI_A[12] [1]	UART2_TX	Not assigned
PORTC[15]	EBI_A[13] [1]	UART2_RX	Not assigned
PORTD[0]	EBI_A[14] [1]	TIM[0]	Not assigned
PORTD[1]	EBI_A[15] [1]	TIM[1]	Not assigned
PORTD[2]	EBI_A[16] [1]	TIM[2]	Not assigned
PORTD[3]	EBI_A[17] [1]	TIM[3]	Not assigned
PORTD[4]	EBI_A[18] [1]	TIM[4]	Not assigned
PORTD[5]	EBI_A[19] [1]	TIM[5]	Not assigned
PORTD[6]	EBI_A[20] [1]	TIM[6]	Not assigned
PORTD[7]	EBI_A[21] [1]	TIM[7]	Not assigned
PORTD[8]	EBI_A[22] [1]	TIM[8]	Not assigned
PORTD[9]	EBI_A[23] [1]	TIM[9]	UART1_RTSn
PORTD[10]	EBI_D[15] [1]	TIM[10]	UART1_CTSn
PORTD[11]	EBI_D[14] [1]	TIM[11]	UART1_TX
PORTD[12]	EBI_D[13] [1]	TIM[12]	UART1_RX
PORTD[13]	EBI_D[12] [1]	TIM[13]	Not assigned
PORTD[14]	EBI_D[11] [1]	TIM[14]	Not assigned
PORTD[15]	EBI_D[10] [1]	TIM[15]	Not assigned
PORTE[0]	EBI_D[9] [1]	TIM[16]	UART0_RTSn
PORTE[1]	EBI_D[8] [1]	TIM[17]	UART0_CTSn
PORTE[2]	EBI_D[7] [1]	TIM[18]	UART0_TX
PORTE[3]	EBI_D[6] [1]	TIM[19]	UART0_RX
PORTE[4]	EBI_D[5] [1]	TIM[20]	Not assigned
PORTE[5]	EBI_D[4] [1]	TIM[21]	SPI1_SSn7
PORTE[6]	EBI_D[3] [1]	TIM[22]	SPI1_SSn6
PORTE[7]	EBI_D[2] [1]	TIM[23]	SPI1_SSn5
PORTE[8]	EBI_D[1] [1]	SPI1_SSn4	TIM[16]
PORTE[9]	EBI_D[0] [1]	SPI1_SSn3	TIM[17]
PORTE[10]	Not assigned	SPI1_SSn2	TIM[18]
PORTE[11]	Not assigned	SPI1_SSn1	TIM[19]

Port pin default function FUNSEL[1:0]=00	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTE[12]	EBI_CEn[0] [1]	SPI1_SSn0	TIM[20]
PORTE[13]	EBI_CEn[1] [1]	SPI1_SCK	TIM[21]
PORTE[14]	EBI_CEn[2] [1]	SPI1_MISO	TIM[22]
PORTE[15]	EBI_CEn[3] [1]	SPI1_MOSI	TIM[23]
PORTF[0]	EBI_OEn[1]	SPI2_SSn4	TIM[0]
PORTF[1]	EBI_WEn[1]	SPI2_SSn3	TIM[1]
PORTF[2]	SPI1_SSn0	SPI2_SSn2	TIM[2]
PORTF[3]	SPI1_SCK	SPI2_SSn1	TIM[3]
PORTF[4]	SPI1_MISO	SPI2_SSn0	TIM[4]
PORTF[5]	SPI1_MOSI	SPI2_SCK	TIM[5]
PORTF[6]	UART2_RTSn	SPI2_MISO	TIM[6]
PORTF[7]	UART2_CTSn	SPI2_MOSI	TIM[7]
PORTF[8]	UART2_TX	Not assigned	TIM[8]
PORTF[9]	UART2_RX	Not assigned	TIM[9]
PORTF[10]	UART1_RTSn	Not assigned	TIM[10]
PORTF[11]	UART1_CTSn	Not assigned	TIM[11]
PORTF[12]	UART1_TX	Not assigned	TIM[12]
PORTF[13]	UART1_RX	TIM[19]	Not assigned
PORTF[14]	UART0_RTSn	TIM[20]	Not assigned
PORTF[15]	UART0_CTSn	TIM[21]	Not assigned
PORTG[0]	UART0_TX	TIM[22]	Not assigned
PORTG[1]	UART0_RX	TIM[23]	Not assigned
PORTG[2]	TIM[9]	SPI1_SSn0	Not assigned
PORTG[3]	TIM[10]	SPI1_SCK	Not assigned
PORTG[4]	SPI1_SSn3	SPI1_MISO	Not assigned
PORTG[5]	SPI1_SSn2	Not assigned	Not assigned
PORTG[6]	SPI1_SSn1	TIM[12]	Not assigned
PORTG[7]	Not assigned	Not assigned	Not assigned

3.4 196-Pin Plastic BGA Ball-Map Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PF15	NC	SRXSN	SRXN	STXSN	STXN	SDA0	PG01	PG05	NC	XTALp	AN7	AN3	VREFH
B	PF11	PF14	SRXSP	SRXP	STXSP	SCL0	PG00	PG04	NMI	XTALn	A3V3	AN4	AN0	DAC0
C	TRST	TDO	PF13	STXP	3V3	CRX0	PG03	PG07	E1V5	A1V5	AN5	AN1	DAC1	ATOUT
D	PF08	TMS	TCK	PF12	CTX0	PG02	PG06	RSTn	VDDQ	AN6	AN2	PA03	PA01	PA00
E	PF04	PF07	PF10	TDI	1V5	VSS	3V3	1V5	VSS	3V3	PA09	PA06	PA04	PA02
F	SCK	PF03	PF06	PF09	VSS	VSS	3V3	1V5	VSS	VSS	PA13	PA10	PA07	PA05
G	PF01	CSn	MOSI	PF05	1V5	1V5	VSS	VSS	3V3	3V3	PB01	PA14	PA11	PA08
H	PE13	PF00	F_SO	MISO	3V3	3V3	VSS	VSS	1V5	1V5	PB04	NC	PA15	PA12
J	EBI	WPn	PE15	PF02	VSS	VSS	1V5	3V3	VSS	VSS	PB08	PB05	PB02	PB00
K	PE10	PE12	TEST	PE14	3V3	VSS	1V5	3V3	VSS	1V5	PB12	PB09	PB06	PB03
L	PE08	PE09	PE11	PE01	PD13	PD09	PD05	PD01	PC13	PC10	PC00	PB13	PB10	PB07
M	PE06	PE07	PE02	PD14	PD10	PD06	PD02	PC14	NC	PC07	PC04	SDA1	PB14	PB11
N	PE05	PE03	PD15	PD11	PD07	PD03	PC15	PC11	PC08	PC05	PC02	SCL2	SCL1	PB15
P	PE04	PE00	PD12	PD08	PD04	PD00	PC12	PC09	PC06	PC03	PC01	SDA2	CTX1	CRX1

3.5 196-Pin Plastic BGA Ball Description

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
A01	PF15	PORTF[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
A02	NC	No connect
A03	SRXSN	SpaceWire Rx strobe -
A04	SRXN	SpaceWire Rx -
A05	STXSN	SpaceWire Tx strobe -
A06	STXN	SpaceWire Tx -
A07	SDA0	I^2C0 Data
A08	PG01	PORTG[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
A09	PG05	PORTG[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
A10	NC	No connect
A11	XTALp	Crystal Oscillator Output
A12	AN7	Analog input channel 7
A13	AN3	Analog input channel 3
A14	VREFH	Analog Reference (3.3 V)
B01	PF11	PORTF[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B02	PF14	PORTF[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B03	SRXSP	SpaceWire Rx strobe +
B04	SRXP	SpaceWire Rx +
B05	STXSP	SpaceWire Tx strobe +
B06	SCL0	I^2C0 Clock
B07	PG00	PORTG[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B08	PG04	PORTG[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B09	NMI	Non-maskable Interrupt – active high
B10	XTALn	Crystal Oscillator Input
B11	A3V3	3.3 V Analog IO power

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
B12	AN4	Analog input channel 4
B13	AN0	Analog input channel 0
B14	DAC0	Digital to analog output 0
C01	TRST	Test Reset, active low
C02	TDO	Test Data Out
C03	PF13	PORTF[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
C04	STXP	SpaceWire Tx +
C05	3V3	3.3 V power
C06	CRX0	CAN0 RX
C07	PG03	PORTG[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
C08	PG07	PORTG[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
C09	E1V5	When high, this signal disables the internal 1.5 V regulator, and 1.5 V must be applied externally to all 1V5 pins and A1V5.
C10	A1V5	1.5 V Analog power (must be supplied externally if EXT15_SEL=1)
C11	AN5	Analog input channel 5
C12	AN1	Analog input channel 1
C13	DAC1	Digital to analog output 1
C14	ATOUT	For factory use only. Must be pulled to VSS
D01	PF08	PORTF[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D02	TMS	Test Mode Select/Serial Wire Debug Data IO
D03	TCK	Test Clock/Serial Wire Debug Clock
D04	PF12	PORTF[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D05	CTX0	CAN0 TX
D06	PG02	PORTG[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D07	PG06	PORTG[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D08	RSTn	External System Reset, active low. Resets the processor and all peripherals. Any reset will cause this pin to drive low during the reset sequence. (Must have external pull-up)

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
D09	VDDQ	For factory use only. Must be tied to VSS
D10	AN6	Analog input channel 6
D11	AN2	Analog input channel 2
D12	PA03	PORTA[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D13	PA01	PORTA[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D14	PA00	PORTA[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E01	PF04	PORTF[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E02	PF07	PORTF[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E03	PF10	PORTF[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E04	TDI	Test Data In
E05	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
E06	VSS	Ground
E07	3V3	3.3 V power
E08	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
E09	VSS	Ground
E10	3V3	3.3 V power
E11	PA09	PORTA[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E12	PA06	PORTA[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E13	PA04	PORTA[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E14	PA02	PORTA[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F01	SCK	SPI Clock to Boot ROM.
F02	PF03	PORTF[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F03	PF06	PORTF[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F04	PF09	PORTF[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
F05	VSS	Ground
F06	VSS	Ground
F07	3V3	3.3 V power
F08	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
F09	VSS	Ground
F10	VSS	Ground
F11	PA13	PORTA[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F12	PA10	PORTA[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F13	PA07	PORTA[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F14	PA05	PORTA[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G01	PF01	PORTF[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G02	CSn	SPI Chip Select to Boot ROM (Active Low).
G03	MOSI	SPI Data Out to Boot ROM.
G04	PF05	PORTF[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G05	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
G06	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
G07	VSS	Ground
G08	VSS	Ground
G09	3V3	3.3 V power
G10	3V3	3.3 V power
G11	PB01	PORTB[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G12	PA14	PORTA[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G13	PA11	PORTA[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G14	PA08	PORTA[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H01	PE13	PORTE[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
H02	PF00	PORTF[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H03	F_SO	SPI Data In from Boot ROM. Must be connected to H04
H04	MISO	SPI Data In from Boot ROM. Must be connected to H03
H05	3V3	3.3 V power
H06	3V3	3.3 V power
H07	VSS	Ground
H08	VSS	Ground
H09	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
H10	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
H11	PB04	PORTB[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H12	NC	No connect
H13	PA15	PORTA[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H14	PA12	PORTA[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J01	EBI	Expanded Bus Boot Mode
J02	WPn	Nonvolatile memory write protection
J03	PE15	PORTE[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J04	PF02	PORTF[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J05	VSS	Ground
J06	VSS	Ground
J07	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
J08	3V3	3.3 V power
J09	VSS	Ground
J10	VSS	Ground
J11	PB08	PORTB[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J12	PB05	PORTB[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J13	PB02	PORTB[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
J14	PB00	PORTB[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K01	PE10	PORTE[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K02	PE12	PORTE[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K03	TEST	For factory use only. Must be tied to ground with a 10k resistor.
K04	PE14	PORTE[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K05	3V3	3.3 V power
K06	VSS	Ground
K07	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
K08	3V3	3.3 V power
K09	VSS	Ground
K10	1V5	1.5 V power (must be supplied externally if EXT15_SEL=1)
K11	PB12	PORTB[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K12	PB09	PORTB[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K13	PB06	PORTB[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K14	PB03	PORTB[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L01	PE08	PORTE[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L02	PE09	PORTE[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L03	PE11	PORTE[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L04	PE01	PORTE[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L05	PD13	PORTD[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L06	PD09	PORTD[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L07	PD05	PORTD[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L08	PD01	PORTD[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
L09	PC13	PORTC[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L10	PC10	PORTC[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L11	PC00	PORTC[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L12	PB13	PORTB[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L13	PB10	PORTB[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L14	PB07	PORTB[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M01	PE06	PORTE[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M02	PE07	PORTE[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M03	PE02	PORTE[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M04	PD14	PORTD[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M05	PD10	PORTD[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M06	PD06	PORTD[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M07	PD02	PORTD[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M08	PC14	PORTC[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M09	NC	No connect
M10	PC07	PORTC[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M11	PC04	PORTC[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M12	SDA1	I^2C1 Data
M13	PB14	PORTB[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M14	PB11	PORTB[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N01	PE05	PORTE[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N02	PE03	PORTE[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
N03	PD15	PORTD[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N04	PD11	PORTD[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N05	PD07	PORTD[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N06	PD03	PORTD[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N07	PC15	PORTC[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N08	PC11	PORTC[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N09	PC08	PORTC[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N10	PC05	PORTC[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N11	PC02	PORTC[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N12	SCL2	I^2C2 Clock
N13	SCL1	I^2C1 Clock
N14	PB15	PORTB[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P01	PE04	PORTE[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P02	PE00	PORTE[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P03	PD12	PORTD[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P04	PD08	PORTD[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P05	PD04	PORTD[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P06	PD00	PORTD[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P07	PC12	PORTC[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P08	PC09	PORTC[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P09	PC06	PORTC[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P10	PC03	PORTC[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
P11	PC01	PORTC[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P12	SDA2	I^2C2 Data
P13	CTX1	CAN1 TX
P14	CRX1	CAN1 RX

Note: When the EBI peripheral is used to access external memory, all GPIO pins associated with the EBI can only be used for EBI functions. These pins cannot be used as a GPIO or other alternative functions. This applies whether the VA416x0 booting from the EBI pins (EBI_BOOT=1) or the ROM SPI pins (EBI_BOOT=0).

4 Peripheral Summary

4.1 Serial Peripheral Interface (SPI)

The VA416X0 contains three general-purpose Serial Peripheral Interface (SPI) blocks. A fourth master only SPI is dedicated to the boot memory and uses a dedicated set of pins. The other three use pins shared with various GPIOs. Please refer to the VA416XX Programmer's Guide for more information about the usage of the SPI.
The SPI peripheral supports the following features:

- Master mode
- Slave mode
- Buffered RX/TX operation with dual four entry FIFOs
- Serial clock (SCK) with programmable polarity (SPO) and phase (SPH)
- SPI0 has up to 4 chip selects
- SPI1 has up to 8 chip selects
- SPI2 has up to 7 chip selects
- SPI3 is Master only and shares its pins with the SPI ROM pins (ROM_SCK, ROM_MOSI, ROM_MISO, ROM_SS)
- Interrupt conditions:
  - TX FIFO is at least half empty (TXIM)
  - RX FIFO is at least half full (RXIM)
  - RX Timeout (RTIM)
  - RX FIFO overrun (RORIM)

4.2 Universal Asynchronous Receiver/Transmitter (UART)

The VA416X0 contains three Universal Asynchronous Receiver/Transmitter (UART) interface blocks with an independent Transmit and Receive section, each with a 16-byte FIFO. The UART pins are shared with various GPIO pins. Please refer to the VA416XX Programmer's Guide for more information about the usage of the UART.

The UART peripheral supports the following features:

- Selectable even, odd, or no parity
- Selectable one or two stop bits
- Word sizes from 5 to 8 bits
- 9-bit address mode
- Baud rates from 300 to 115,200 bps (or up to 2 Mbps)
- 16-byte RX and TX FIFO
- Detection of Framing, Parity, and Overrun errors

- Full Duplex or Half Duplex operation
- Break signal generation and detection
- Interrupt conditions:
  - Receive FIFO at least half full (IRQ_RX)
  - Receive FIFO overflow, receive frame error, receive parity error, or receive break condition (IRQ_RX_STATUS)
  - Receive timeout (IRQ_RX_TO)
  - Transmit FIFO at least half empty (IRQ_TX)
  - Transmit FIFO overflow (IRQ_TX_STATUS)
  - Transmit FIFO empty (IRQ_TX_EMPTY)
  - Transmitter interrupt when CTSn changes value (IRQ_TX_CTS)

4.3 Inter-Integrated Circuit (I^{2}C)

The VA416X0 contains three Inter-Integrated Circuit (I^{2}C) interface blocks. Please refer to the VA416XX Programmer's Guide for more information about I^{2}C usage.

The I^{2}C peripheral supports the following features:

- Standard I^{2}C-compliant bus interface
- Configurable as Master or Slave
- Dedicated open-drain pins
- 16-word FIFO for both transmit and receive
- Programmable clock rate for normal 100 kHz mode or 400 kHz mode
- Interrupt conditions:
  - TX FIFO ready (TXREADY)
  - TX FIFO empty (TXEMPTY)
  - TX FIFO overflow (TXOVERFLOW)
  - RX FIFO full (RXFULL)
  - RX FIFO ready (RXREADY)
  - RX FIFO overflow (RXOVERFLOW)
  - Clock low timeout (CLKLOTO)
  - I^{2}C Status (STATUS)

4.4 SpaceWire (SpW)

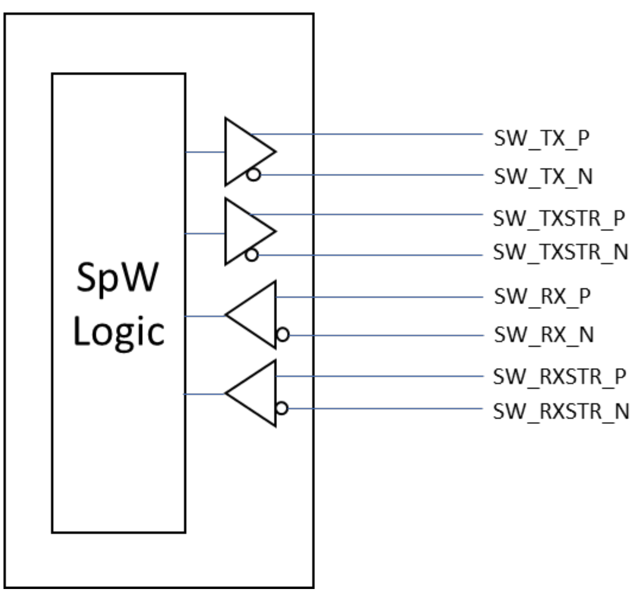
The VA416X0 contains a single SpaceWire interface block. Please refer to the VA416XX Programmer's Guide for more information about SpaceWire usage.

The SpaceWire interface supports the following features:

- Full implementation of SpaceWire standard ECSS-E-ST-50-12C
- Protocol ID extension ECSS-E-ST-50-11C
- RMAP protocol ECSS-E-ST-50-11C
- AMBA AHB backend with DMA
- Descriptor-based autonomous multi-packet transfer
- 1 Kbyte receive FIFO
- 1 Kbyte transmit FIFO

This interface implements the SpaceWire Time Distribution Protocol (TDP). The protocol provides the capability to transfer time values and synchronize them between onboard users of the SpaceWire network. The time values are transferred as CCSDS Time Codes, and synchronization is performed through SpaceWire Time Codes.

The SpaceWire interface consists of four differential pairs (two inputs and two outputs), as shown in the figure. The VA416X0 incorporates the Low Voltage Differential Signal (LVDS) driver and receiver structures. External LVDS circuits are not required.



4.5 Controller Area Network (CAN)

The VA416X0 contains two CAN interface blocks. Please refer to the VA416XX Programmer's Guide for more information about CAN usage.

The CAN Controller implements the following features:

Compliant to CAN Specification 2.0B
- Standard data and remote frames
- Extended data and remote frames
- Up to 8 bytes data length
- Programmable bit rate of up to 1 Mbps

15 message buffers, each configurable as a receive or transmit buffer
- Message buffers are 16-bit oriented as dual-port RAM
- One buffer may be used as a basic CAN path

Remote frame support
- Automatic transmission after reception of a Remote Transmission Request (RTR)
- Auto receive after transmission of an RTR

Acceptance filtering
- Two filtering capabilities: global acceptance mask and individual buffer identifiers
- One of the buffers uses an independent acceptance filtering procedure

Programmable transmit priority

Interrupt capability
- One interrupt vector for all message buffers (receive/transmit/error)
- Each interrupt source can be enabled/disabled

16-bit counter with time stamp capability on successful message reception or transmission

Push-pull capable output pins

Diagnostic functions
- Error identification
- Loopback and listen-only features for test and initialization purposes

An external CAN transceiver is required to connect the VA416X0 to a CAN interface bus.

4.6 General Purpose 4-Channel DMA

The VA416X0 supports a single DMA interface to allow the MCU to transfer data from a peripheral to memory or memory to a peripheral, independent of the Arm® CPU. The Ethernet and SpaceWire peripherals have their own DMA and will not use the general-purpose DMA. Please refer to the VA416XX Programmer's Guide for more information about the usage of the DMA.

The DMA controller implements the following features:

- Each DMA channel has dedicated handshake signals
- Each DMA channel has a programmable priority level
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel
- Support for multiple transfer types:
    - Memory-to-memory
    - Memory-to-peripheral
    - Peripheral-to-memory
- Support for multiple DMA transfer data widths
- The number of transfers in a single DMA cycle is programmable from 1 to 1024

Typical use cases for the DMA are:

- ADC routing results to RAM buffer
- SPI/UART emptying own FIFO into RAM buffer or vice versa
- Moving external EBI Memory to on-chip SRAM

4.7 Ethernet Media Access Control (MAC)

The VA416X0 contains an Ethernet interface block. Please refer to the VA416XX Programmer's Guide for more information about the usage of the Ethernet.

MAC General features:

- Compliant with the full IEEE 802.3-2002 specifications
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Support of CSMA/CD protocol for half-duplex operation
- Supports full-duplex only configuration
- Supports IEEE 802.3x flow control for full-duplex operation
- Supports backpressure for flow control in half-duplex mode

- Optional forwarding of received pause frames to the user application when operating in full-duplex mode
- Automatic CRC and pad generation controllable on a per-frame basis
- Optional Automatic Pad Stripping on the receive frames
- Programmable frame length to support standard Ethernet frames 16KB in size
- Programmable inter-frame gap to 40 to 96-bit times (steps of 8)
- Supports a variety of flexible address filtering modes
- Checksum options:
  - Offload Engine for Ipv4, Ipv6, TCP, UDP, ICMP
  - Insertion in transmit frames
  - Check of received frames
- Support for IEEE 1588-2002 time-stamping of transmitted and received frames

External PHY interface features:

- Supports industry-standard MII
- MDIO master interface for PHY device configuration and management

Ethernet DMA features:

- Four single-channel transmit and receive engines
- Fully synchronous design operating on a single system clock
- 32/64/128-bit data transfers
- Optimized for packet-oriented DMA transfers with frame delimiters
- Byte-aligned addressing for data buffers supported
- Dual-buffer (ring) and linked-list (chained) descriptor chaining
- Descriptor architecture allows large blocks of data transfer with minimum CPU intervention
- Each descriptor can transfer up to 16 Kbyte of data
- Comprehensive status reporting for normal operation and transfers with errors
- Programmable burst size for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-frame transmit/receive complete interrupt control
- Round-robin or fixed-priority arbitration between receive and transmit engines
- Start/stop modes

Ethernet FIFO:

- 2 Kbyte transmit buffer
- 2 Kbyte receive buffer

An external Ethernet PHY is required to connect the VA416X0 to an Ethernet bus.

4.8 Analog to Digital Converter (ADC)

The VA416X0 Analog to Digital Converter (ADC) is a general-purpose 12-bit successive approximation architecture. Please refer to the VA416XX Programmer's Guide for more information about the usage of the ADC.

ADC feature summary:

- Resolution: 12-bit
- 600k samples per second
- Eight external input channels
- Eight internal channels, including a temperature sensor
- 32-word FIFO for storing continuous mode conversion
- Timers can trigger conversion events
- DMA connection for moving data from ADC to data SRAM
- Interrupt capability on conversion complete
- Optional sweep mode will automatically convert from a single channel to up to eight channels repeatedly and store the results in the FIFO
- Operating supply range from 3.0 to 3.6 V
- Integrated temperature sensor (uncalibrated to ±5°C)
- Programmable conversion clock

4.9 Digital to Analog Converter (DAC)

The VA416X0 Digital-to-Analog Converter (DAC) is a general-purpose 12-bit voltage output block. Please refer to the VA416XX Programmer's Guide for more information about the usage of the DAC.

DAC feature summary:

- Resolution: 12-bit
- Rail to rail voltage output
- 32-word FIFO
- Power-on reset output = 0 V
- Operating supply range from 3.0 to 3.6 V
- 2 Independent DAC outputs
- Close coupling to the interrupt controller and MCU that allows periodic updates

Power up and Reset Behavior of DAC:
If the DAC is enabled in software, the output of the DAC will be set to a zero volt reading following a reset.

4.10 Timers/Counters (TIM)

The VA416X0 contains 24 general-purpose Timer/Counter interface blocks. These can be configured as timers or event counters. They can be free-running or triggered by system events. Timer pins are shared with various GPIO pins. Please refer to the VA416XX Programmer's Guide for more information about the usage of the Timers.

Timer feature summary:

- Advanced trigger modes
  - Start/Stop based on other Counter/Timers or GPIO signals
  - Multiple trigger sources
- Configurable output event
  - One cycle zero detect when a timer equal to zero is detected
  - Active mode
  - Divide by two for square wave generation
  - Two PWM modes: Single edge and double edge detection

4.11 General-Purpose Input/Output Ports (GPIO)

The VA416X0 contains seven GPIO banks providing a total of 104 GPIO pins. GPIO pins can be configured as inputs or outputs. Please refer to the VA416XX Programmer's Guide for more information about the usage of the GPIO.

- PORTA[15:0]
- PORTB[15:0]
- PORTC[15:0]
- PORTD[15:0]
- PORTE[15:0]
- PORTF[15:0]
- PORTG[7:0]
- Interrupt capability on Ports A to F
- Selectable edge or level interrupts
- Programmable pull-up or pull-down resistors
- Programmable output inversion
- Selectable input filtering
- Pseudo open-drain capability

- Alternative functions available on many GPIO pins

4.12 External Parallel Bus Interface (EBI)

The EBI peripheral is used to interface multiple external memories to the VA416X0. The EBI can connect to an 8-bit or 16-bit external asynchronous memory of up to 16 Mbytes and supports up to four external memory devices. Each external memory will be sharing memory interface signals such as data, address, and write/read. Each memory will have its own chip enable pin (EBI_CEn[3:0]).

The External Bus Interface can be used to load the Instruction code into the internal SRAM (if EBI_BOOT=1). Please refer to the VA416XX Programmer's Guide for more information about the usage of the External Parallel Bus Interface.

When the EBI peripheral is used to access external memory, all GPIO pins associated with the EBI can only be used for EBI functions. These pins cannot be used as a GPIO or other alternative functions. This applies whether the VA416x0 is booting from the EBI pins (EBI_BOOT=1) or booting from the ROM SPI pins (EBI_BOOT=0)

4.13 True Random Number Generator (TRNG)

The Arm® TrustZone TRNG offers these two components:

- The TRNG that conforms to the following standards and drafts:
    - NIST SP800-90B
    - NIST SP800-22
    - FIPS 140-2
    - BSI AIS-31
- A software-implemented Deterministic Random Bit Generator (DRBG) which follows NIST SP 800-90A (making the entire RNG flow SP 800-90C compliant)

For more detailed information, see the Arm® TrustZone True Random Number Generator, Technical Reference Manual.

4.14 Debug and programing interface (DBG)

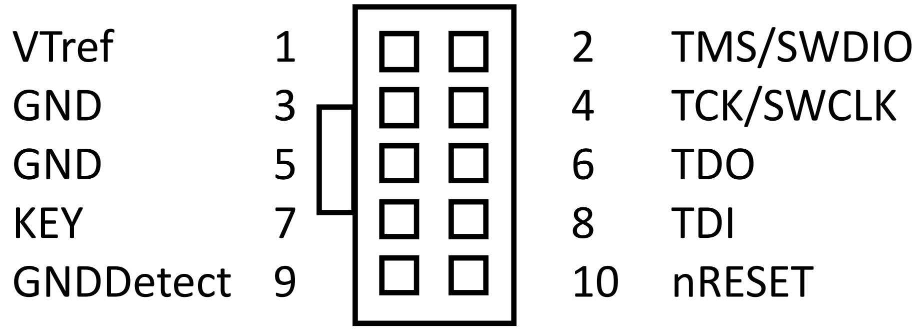
ARM's Serial Wire Debug (SWD) replaces the traditional 5-pin JTAG debug interface by introducing a 2-pin interface with a clock (SWDCLK) and a single bi-directional data pin (SWDIO), providing all the normal JTAG debug and test functionality, although daisy-chaining devices as via JTAG is not possible. SWDIO and SWCLK are overlaid on the TMS and TCK pins, allowing the same connector to be used for JTAG and SWD (JTAG is not supported in user mode for the VA416xx). To communicate with a device via SWD, data is sent on SWDIO, synchronous to the SWCLK. With every rising edge of SWCLK, one bit of data is transmitted or received on the SWDIO pin.

SWD Pins

Pin	Type	Explanation
SWCLK	Input	The clock signal to the target CPU. This pin is recommended to be pulled to a defined state on the target board.
SWDIO	I/O	Bi-directional data pin. This pin should be pulled up on the target board.

JTAG/SWD Pod Signal	Purpose	Connects to:
VTref	This is the target reference voltage. It is used to check if the target board has power.	It is normally fed from VDD of the target board and must not have a series resistor.
GND	Target ground.	MCU VSS.
KEY	Physical key to aid in cable placement.	No electrical connection.
GNDDetect	Debugger ground detect.	Use a 10k pull-up resistor to VDD33.
TMS/SWDIO	SWDIO is bi-directional data line.	MCU pin TMS/SWDIO. Use 10K Ohm pull-up resistor to VDD33.
TCK/SWCLK	Test Clock pin	MCU pin TCK/SWCLK. Use a 10k pull-down resistor to GND.
TDO	Test Data Output pin	MCU pin TDO. Not used with SWD and may be left floating.
TDI	Test Data Input pin	MCU pin TDI. Not used with SWD. Use at 10k pull-up resistor to VDD33
nRESET	Reset pin	MCU pin EXTRESETn. Connected to active low EXTRESETn input pin of the MCU so the debugger can reset the MCU.

The most common interface connector is a Samtec 10-pin: FTSH-105-01-L-DV-007-K connector. Shown below is the pinout.


VTref 1
GND 3
GND 5
KEY 7
GNDDetect 9
2 TMS/SWDIO
4 TCK/SWCLK
6 TDO
8 TDI
10 nRESET

5 DC Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Rating	Hi-Rel	Unit
V_{DD33}	DC supply voltage (I/O)	-0.3 to 3.8	V
V_{DD15}	DC supply voltage (core)	-0.3 to 1.8	V
A_V_{DD33}	DC supply voltage (analog)	-0.3 to 3.8	V
A_V_{DD15}	DC supply voltage (analog)	-0.3 to 1.8	V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8	V
T_{CASE}	Operating temperature	-55 to 125	°C
T_{BIAS}	Temperature under bias	-55 to 125	°C
T_{STG}	Storage temperature	-55 to 125	°C

5.2 Recommended Supply Conditions

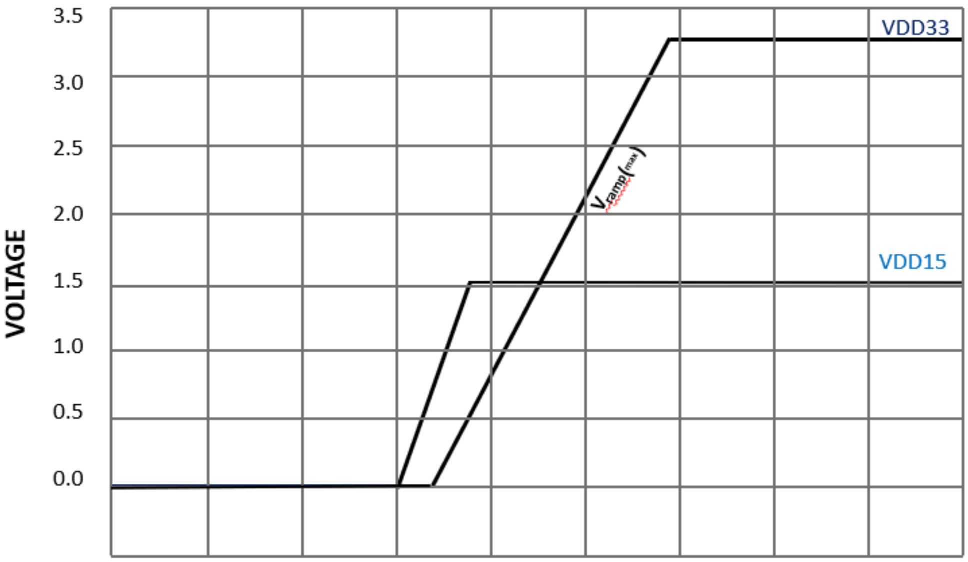
Symbol	Parameter	Min	Typ	Max	Unit
V_{DD33}	I/O supply voltage	3.0	3.3	3.6	V
V_{DD15}	Core supply voltage (if supplied externally)	1.35	1.5	1.65	V
A_V_{DD33}	Analog supply voltage	3.0	3.3	3.6	V
A_V_{DD15}	Analog supply voltage (must be supplied externally)	1.35	1.5	1.65	V
V_{SS}	Ground	-	0	-	V
V_{ramp}	V_{DD15}/V_{DD33} supply ramp rate[1,4]	0.5 V/ms	-	100 V/us	–
V_{PROFF}	V_{DD33} level at which the Power-on reset is released when voltage is rising[2]	2.65	2.8	2.95	V
V_{PRON}	V_{DD33} level at which the Power-on reset is activated when voltage is falling[3]	-	2.7	-	V

Notes:

1. V_{Ramp} time is the time from V_{DD} = 0 V until it reaches the operating range.
2. V_{PROFF} is the voltage at which the internal Power-on reset is released when power is rising.
3. V_{PRON} is the voltage at which the internal Power-on reset is activated.
4. See additional requirements for VDD15/VDD33 power supply relationship in the graph below

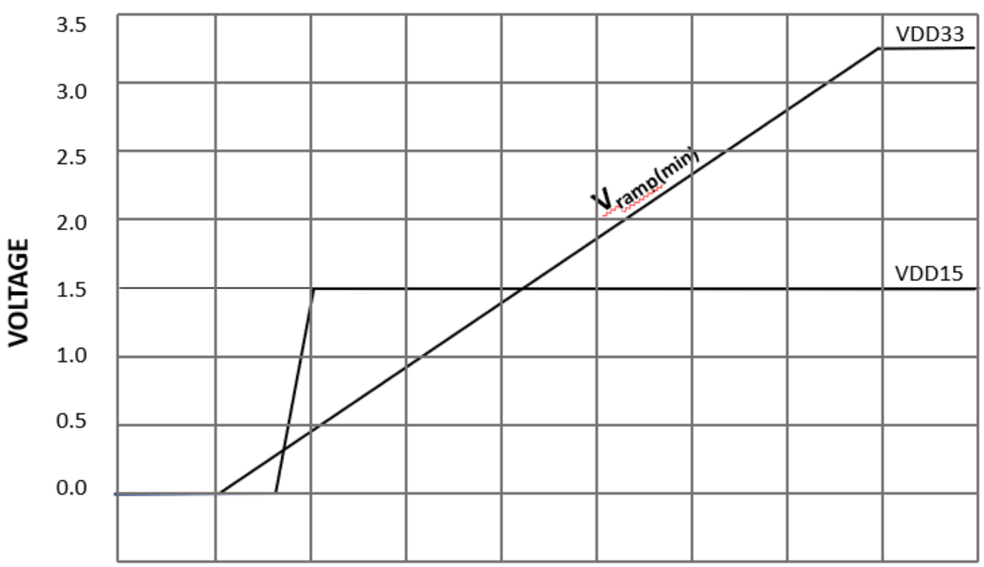
5.3 Required Power Supply Sequencing

For reliable boot operation, the VDD15 ramp must be faster than the VDD33 ramp to ensure that VDD33 is less than VDD15 until VDD15 reaches 1.5V.



Power sequencing for case of maximum VDD33 ramp.

To meet this requirement, the ramp rate of the VDD33 can be adjusted to slow the rise of the VDD33 relative to VDD15. This is shown in the figure below.



Power sequencing for case of minimum VDD33 ramp.

5.4 DC Current Consumption

Core Supply Current (VDD15)

The typical core supply current is approximately 1.2mA/MHz

System clock frequency (MHz)[1]	Min	Typ[2]	Max[3]	Units
10	-	20	-	mA
20	-	35	-	mA
50	-	65	-	mA
100	-	125	-	mA

Notes:

1. Maximum activity is measured with all internal counters running at the maximum rate, all I^2C interfaces active in Fast mode and loopback mode, all SPI interfaces active in master mode at 16x clock divide rate, and all UARTs active in loopback mode at 1M Baud rate, and the CPU running multiply operations.
2. Measured at nominal VDD and 25°C.
3. Measured at maximum VDD and 125°C.

I/O Supply Current[1] (V_{DD33}) I_{DD33}

Run I_{DD}[1]	Max	Units
Overall maximum I/O current	200	mA
Maximum I/O current per side of the device	100	mA

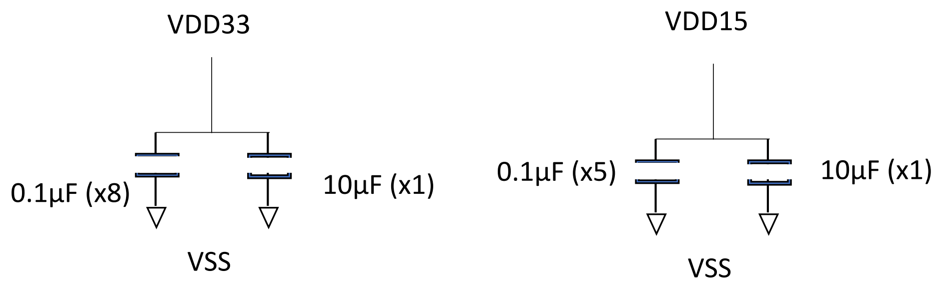
Notes:

1. Although each GPIO can source or sink up to 8mA, the maximum current allowed per package side of the device is 100mA. The maximum allowable current into VDD33 (I_{DD33}) is 200mA. I/O supply current is entirely application dependent. It is the sum of all the GPIO outputs switching, the switching frequency of those outputs, and the capacitive loading on each pin.
2. Not a tested parameter

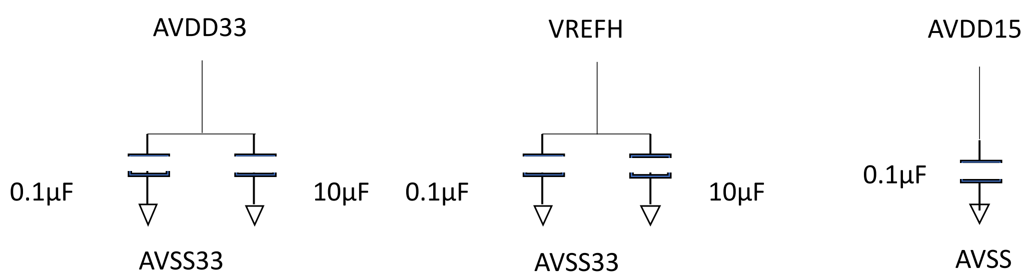
5.5 Power Supply Decoupling

Each power supply pair (VDD33/VSS, VDD15/VSS, A_VDD33/A_VSS, A_VDD15/A_VSS) must be decoupled with filtering ceramic capacitors, as shown. These capacitors must be placed as close as possible to the corresponding supply pins to ensure proper operation of the MCU. Capacitors can also be placed on the bottom side of a PC board for convenience.

Digital Supplies



Analog Supplies



5.6 General Purpose I/O

Input/Output and Input-Only Pads

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IL}	Input Low Voltage	VDD33=Max	-0.3	-	0.3 x V_{DD33}	V
V_{IH}	Input High Voltage	VDD33=Max	0.7 x V_{DD33}	-	V_{DD33} + 0.3	V
V_{hys}[2]	Hysteresis of Schmitt trigger	VDD33=Max	-	450	-	mV

Notes:

1. Typ for –55° to 125°C measured at 25°C
2. The following input buffers have Schmitt Trigger Inputs: TCK, TRSTn, TDI, TMS, ROM_MISO, NVM_PROTn, TEST_MODE, NMI, CAN0_RX, CAN1_RX, EBI_BOOT, and all GPIO

Input/Output and Output-Only Pads

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{OL}	Output voltage (Low)	Load I = 8 mA V_{DD33} = Min	-	0.25	0.4	V
V_{OH}	Output voltage (High)	Load I = -8 mA V_{DD33} = Min	0.8 x V_{DD33}	3.0	-	V

Notes:

1. Typical for –55° to 125°C measured at 25°C

Leakage Current Input/Output and Input-Only Pads

See Pin Descriptions in Section 3 for more information.

Symbol	Parameter	Pins	Test Condition	Min	Typ[1]	Max
I_{in}	Input leakage current (V_{in} low)	Pins with configurable pull-up or pull-down	V_{in} = 0 V	-1 µA	10 nA	-
		Pins with internal pull-down always enabled	V_{in} = 0 V	-65 µA	-50 µA	-
		Tri-state Pins	V_{in} = 0 V	-1 µA	10 nA	-
	Input leakage current (V_{in} high)	Pins with configurable pull-up or pull-down	V_{in} = V_{DD33}	-	10 nA	1 µA
		Pins with internal pull-down always enabled	V_{in} = V_{DD33}	-	10 nA	1 µA
		Tri-state Pins	V_{in} = V_{DD33}	-	10 nA	1 µA

Notes:

1. Typical for -55° to 125°C measured at 25°C

Open Drain I²C Pads

Open Drain I²C pad specifications apply to pads: I2Cx_SCL, I2Cx_SDA.

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IL}	Input low voltage		-0.3		0.3 x $V_{DD33MAX}$	V
V_{IH}	Input high voltage		0.7 x $V_{DD33MIN}$		V_{DD33} + 0.3	V

V_{hys}	Hysteresis of Schmitt trigger		-	450	-	mV
I_{in}	Input leakage current (high)	$V_{in} = V_{DD33}$	-1 μA	10 nA	1 μA	
V_{OL}	Output voltage (low)	Load I = -8 mA, V_{DD33} = Min	-	0.25	0.4	V

Notes:

1. Typical for –55° to 125°C measured at 25°C

5.7 SpaceWire Pads

SpaceWire Low Voltage Differential Signaling (LVDS) Receive Pads[1]

LVDS TX specifications apply to pads: SW_RX_N, SW_RX_P, SW_RXSTR_N, and SW_RXSTR_P.
An internal 100Ω load is provided between SW_RX_N and SW_RX_P and between SW_RXSTR_N and SW_RXSTR_P.

Symbol	Parameter	Min	Typ	Max	Unit
$\|V_{ID}\|$	Input differential voltage	75	100	-	mV
V_{CM}	Input common mode voltage	0.2	1.2	2.8	V
I_{IC}	Input current, single ended	92	114	160	μA
C_{in}	Input capacitance at pad (when disabled)	-	0.9	1	pF
R_{in}	Terminating resistance	-	100	-	Ω

Note:

1. Guaranteed by design

SpaceWire Low Voltage Differential Signaling (LVDS) Transmit Pads[1]

LVDS RX specifications apply to pads: SW_TX_N, SW_TX_P, SW_TXSTR_N, and SW_TXSTR_P.
An internal 100 Ω load is assumed between SW_RX_N and SW_RX_P and between SW_RXSTR_N and SW_RXSTR_P at the receiving end.

Symbol	Parameter	Min	Typ	Max	Unit
$\lvert V_{OD} \rvert$	Output differential voltage	270	350	410	mV
V_{OM}	Output common-mode voltage (V_{DD33} = 3.3 V)	1.22	1.25	1.26	V
V_{OCM}	Output common mode voltage	1.09	1.25	1.38	V
I_{OC}	Output current	2.7	3.5	4.1	mA
t_{skd}	Differential pulse skew	0	0.025	0.1	ns
C_{in}	Input capacitance at pad (when disabled)	-	0.9	1	pF

Note: Guaranteed by design

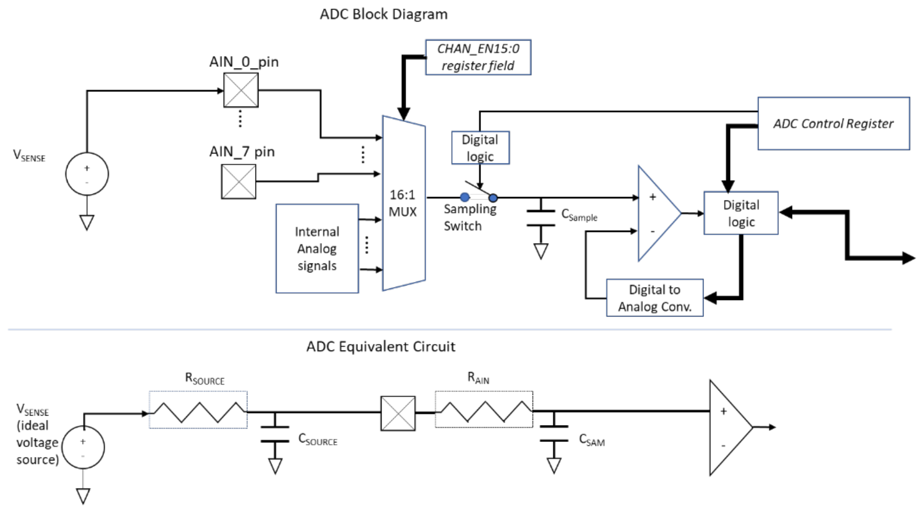
5.8 ADC Operating Conditions

The following table lists the operating conditions that must be maintained for the ADC to achieve the performance, as stated in ADC Operating Performance Table. Unless specified, the temperature range is –55°C to 125°C.

Symbol	Parameter	Min	Typ	Max	Unit
A_V_{DD33}	Analog supply voltage	3.0	3.3	3.6	V
A_I_{DD33}	Analog supply current	-	17	25	mA
A_V_{DD15}	Analog supply voltage	1.35	1.5	1.65	V
A_I_{DD15}	Analog supply current	-	400	-	µA
V_{REFH}	Reference voltage	2.0	-	A_V_{DD33}	V
I_{REFH}	Analog reference current	-	-	100	µA
V_{ADIN}	Analog input voltage range	0	-	V_{REFH}	V
A_V_{SS}	Ground	-	0	-	V
C_{SAM}[1]	Sample capacitance	-	10	-	pF
R_{AIN}[1]	Series resistance	-	1700	-	Ω
F_{ADC}	ADC conversion clock frequency	2.5	-	12.5	MHz
R_{Source}	Source series resistance	-	2000	-	Ω

Notes:

1. This is an internal circuit. Parameter guaranteed by design.



ADC Block Diagram and Equivalent Circuit

5.9 ADC Operating Performance

The following behavioral information applies to the operating conditions. Unless specified, the temperature range is –55°C to 125°C. For maximum accuracy, VORAGO recommends using software that will sample the ADC input pins several (two to four) times to determine an average value for the ADC input voltage. Having a filter capacitor (C_{SOURCE}) can help reduce electrical noise and lower the source impedance. Choose a value as large as the input signal bandwidth will allow and place it very close to the ADC input pin.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Resolution		12	-	-	Bits
INL[1]	Integral non-linearity	f_{ADC} = 2.5 MHz	-	±7	-	LSB
		f_{ADC} = 12.5 MHz	-	±3	-	LSB
DNL	Differential non-linearity	f_{ADC} = 2.5 MHz	-	11	-	LSB
		f_{ADC} = 12.5 MHz	-	±3	-	LSB
ZE	Zero-scale error	f_{ADC} = 2.5 MHz	-	-6 / +1	-	LSB
		f_{ADC} = 12.5 MHz	-	-1 / +3	-	LSB
FE	Full-scale error	f_{ADC} = 2.5 MHz	-	-4 / 0	-	LSB
		f_{ADC} = 12.5 MHz	-	-1 / 2	-	LSB

Notes:

1. INL is calculated using the least-squares method.

5.10 Post-TID ADC Operating Performance

The following information applies to the operating conditions after 300 krad (Si) of radiation exposure. Unless specified, the temperature range is –55°C to 125°C. Specification derated to reflect total dose exposure to 300krad (Si) at 100rad (Si)/s and 25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ZE	Zero-scale error	f_{ADC} = 2.5 MHz	-1	-	+1	%FS
FE	Full-scale error	f_{ADC} = 2.5 MHz	-2	-	+2	%FS

5.11 Internal Temperature Sensor

VA416X0 has a temperature sensor that can be accessed via an internal ADC channel. The temperature sensor is referenced from VREFH.

Symbol	Parameter	Typ	Unit
T_L	Linearity with temperature	+/- 0.5	°C
V_{ROOM}	25°C voltage reading	1.48	V
T_{VALUE}	25°C ADC Count	0x0730	Hex value

A read of the temperature sensor voltage can be converted to a temperature in degrees C by using the following equation:

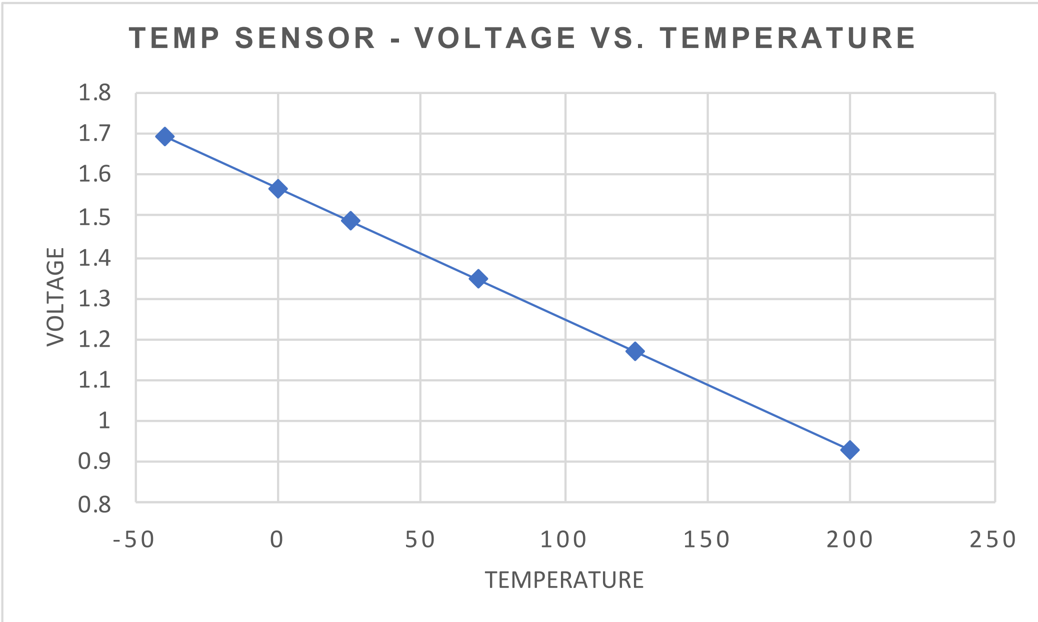
$$\text{Voltage} = -0.0032(\text{Temperature}) + 1.5685$$

OR

$$\text{Temperature} = (\text{Voltage} - 1.5685) / -0.0032$$

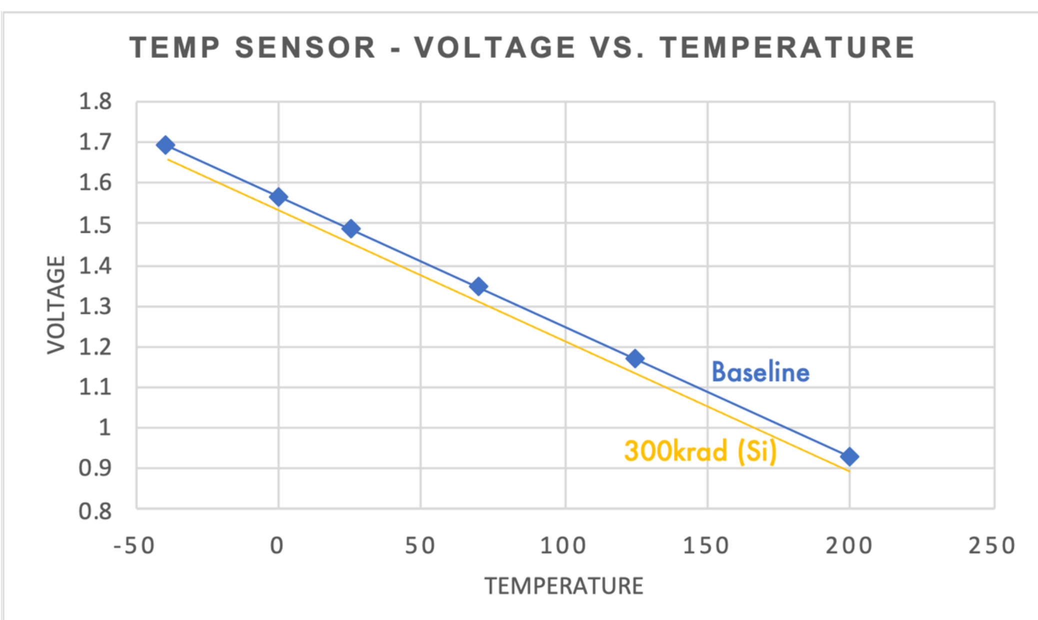
Degrees_C = ((ADC_data_reading_in_decimal / 4096 * VREFH) – 1.5685) / -0.0032)

Using VREFH=VDD33=3.3V, typical room temperature reading of 0x730 (1840 decimal):
Degrees_C = ((1840 / 4096 * 3.3V) – 1.5685) / -0.0032 = 26.9 C



5.12 Post-TID Internal Temperature Sensor

Following TID radiation exposure, the VA416X0 internal temperature sensor that can shift up to 8°C at room temperature. The graph below shows baseline temperature sensor data, as well as post-TID temperature sensor data after 300krad (Si) at 10rad (Si)/s.



5.13 DAC Operating Conditions

The following table lists the operating conditions that must be maintained for the DAC to achieve the performance, as stated in DAC Operating Performance Table. Unless specified, the temperature range is –55°C to 125°C.

Symbol	Parameter	Min	Typ	Max	Unit
A_V_{DD33}	Supply voltage	3.0	3.3	3.6	V
V_{REFH}	Reference voltage	2.0	-	A_V_{DD33} – 0.3	V
A_V_{SS}	Ground	-	0	-	V
R_{IN}	Input resistance	-	2	-	kΩ
C_L	Output load capacitance	-	100	-	pF
I_L	Output load current	-	0.5	-	mA

5.14 DAC Operating Performance

The following behavioral information applies to the operating conditions outline in the above table.

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
	Resolution		12			Bits
INL	Integral non-linearity			±4		LSB
DNL	Differential non-linearity	AV_{DD33} 3.0 V to 3.6 V		±1		LSB

Notes:

1. Typical for –55° to 125°C measured at 25°C

5.15 Low-Voltage Detect Circuit

Refer to the VA416XX Programmer's Guide for more information.

Low-Voltage Detect Level	LVL_SLCT[1] Value	Min	Typ	Max	Units
Low-voltage detect rising	-	2.85	2.9	2.95	V
Low-voltage detect falling	00	2.75	2.8	2.85	V
	01	-	2.9	-	V
	10	-	3.0	-	V
	11	-	3.1	-	V

Notes:

1. LVL_ SLCT is set to the lowest possible setting on power-up to keep the low voltage detect circuit from resetting the device.

5.16 Internal Pull-up/Pull-down Resistors

Pull direction	Min	Typ	Max	Units
Pull-up[1]	45	55	65	kΩ
Pull-down[2]	45	55	65	kΩ

Notes:

1. Pins with dedicated Pull-ups: EXTRESETn, TMS/SWDIO
2. Pins with dedicated Pull-downs: ROM_MISO, TMS

5.17 Pin Capacitance

Symbol	Parameter	Conditions	Max	Unit
C_{IN}[1]	Input pin capacitance	V_{in} = 3.3 V	6	pF
$C_{I/O}$[2]	I/O pin capacitance	V_{out} = 3.3 V	10	pF
C_{OD}[3]	Open drain pin capacitance	V_{out} = 0V	10	pF

Notes:

1. Input only pins: XTAL_N, ROM_MISO, TCK, TRSTn, TDI, CAN0_RX, CAN1_RX, NMI, EBI_BOOT, NVM_PROTn, EXT15_SEL, TEST_MODE
2. Bidirectional pins: PORTA[15:0], PORTB[15:0], PORTC[15:0], PORTD[15:0], PORTE[15:0], PORTF[15:0], PORTG[7:0], TMS/SWDIO
3. Open-drain pins: EXTRESETn, I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, I2C2_SCL, and I2C2_SDA.

6 AC Electrical Characteristics

6.1 AC Timing Conditions

V_{DD33}	3.3 V ± 0.3 V
Input swing levels	0 to 3.3 V
Input rise/fall times[1]	4 ns[1]
Input timing reference levels	1.65 V
Output timing reference levels	1.65 V
AC test load	15 pF

Notes:

1. Rise/Fall times are measured from 20% to 80% of V_{DD33}

6.2 Internal 20 MHz Oscillator

The internal 20 MHz oscillator is used for boot and Power-Up delay timing. If the system clock drops below 1MHz, the system clock will automatically switch over to the internal 20MHz oscillator as a system fail-safe mechanism.

Parameter	Description	Min	Typ	Max	Unit
t_{CYC}	Clock cycle time	40	50	66.7	ns
t_{FREQ}	Clock frequency	15	20	25	MHz
-	Cycle time accuracy	-25	-	25	%

6.3 External Clock Signals

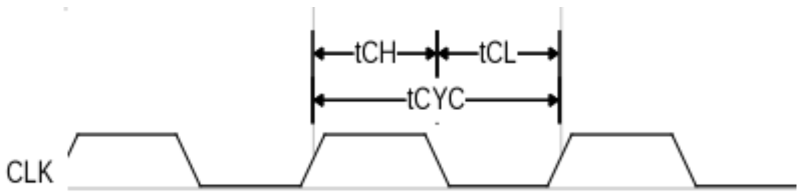
The VA416X0 can be clocked in several different ways.

- Internal oscillator
- 4 to 10 MHz external crystal with PLL or without PLL enabled
- 4 to 100 MHz external square wave with PLL enabled
- 0 to 100 MHz external square wave without PLL enabled

External Clock Signal

An external clock can be used to drive the XTAL_N input with the XTAL_P pin left unconnected. The clock signal must adhere to the following table.

Parameter	Description	Time	Unit
t_{CYC}	Clock cycle time (min)	10	ns
t_{CH}	Clock high (min)	4	ns
t_{CL}	Clock low (min)	4	ns



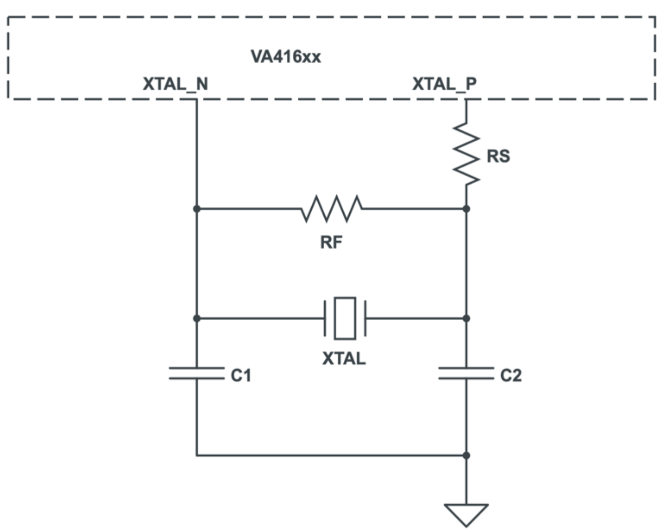
External Crystal Oscillator

Parameter	Description	Min	Typ	Max	Unit
f_{XTAL}	Crystal frequency	4	-	10	MHz
R_F	Feedback resistor	-	1M	-	Ω
R_S	Series resistor	1k	-	20k	Ω
t_S	Startup time	-	10	15	ms

Note: PC board trace lengths for the oscillator circuit should be as short as possible

Example External Crystal Oscillator Circuit

If an external crystal oscillator circuit is used, please refer to the crystal oscillator manufacturer's data sheet for exact values of resistors and capacitors for proper oscillation at the fundamental frequency, reliable startup, and to maximize stability.



6.4 Phased Locked Loop (PLL)

The VA416X0 contains an internal PLL circuit that can be used to generate internal frequencies higher than the input clock. The PLL clock can be used as the MCU system clock. Please refer to the VA416XX Programmer's Guide for more information on the usage of the PLL.

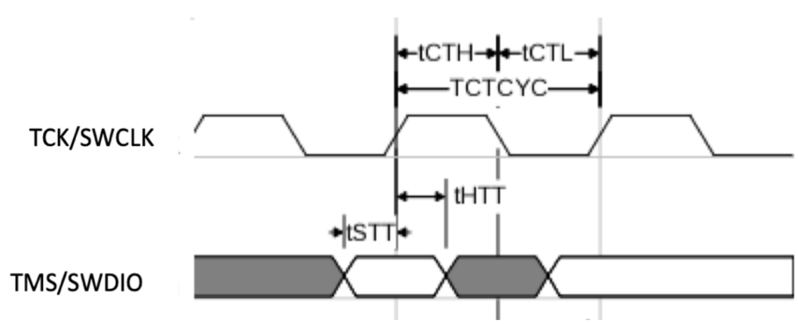
Parameter	Description	Typ	Max	Unit
f_{in}	Input frequency	4	100	MHz
f_{out}	Output frequency	-	100	MHz
t_{LOCK}	PLL lock time	10	100	µs
Jitter	PLL clock jitter (percentage of input frequency)	3	-	%
t_{CL}	Clock low (min)	4	-	ns

Note: Guaranteed by design

6.5 Serial Wire Debug (SWD)

The Serial Wire Debug interface allows access to the Arm® Debug Access Port (DAP). The TMS/SWDIO pin is bi-directional data, and the TCK/SWCLK pin is a clock input to the VA416X0.

Parameter	Description	Typ	Unit
t_{CTCYC}	TCK/SWCLK cycle time (min)[2]	60	ns
t_{CTH}	TCK/SWCLK high (min) [2]	20	ns
t_{CTL}	TCK/SWCLK low (min) [2]	20	ns
t_{STT}	TMS/SWDIO setup time to TCK/SWCLK rise	2.0	ns
t_{HTT}	TMS/SWDIO hold time to TCK/SWCLK rise	6.0	ns



6.6 Low Voltage Differential Signaling (LVDS)

LVDS Receiver Timing Specifications

Symbol	Description	Min	Typ	Max	Unit
F	Operating frequency	-	100	100	MHz
t_{pHLr}	Input differential propagation delay high to low		2.3		ns
t_{pLHr}	Input differential propagation delay low to high		2.3		ns

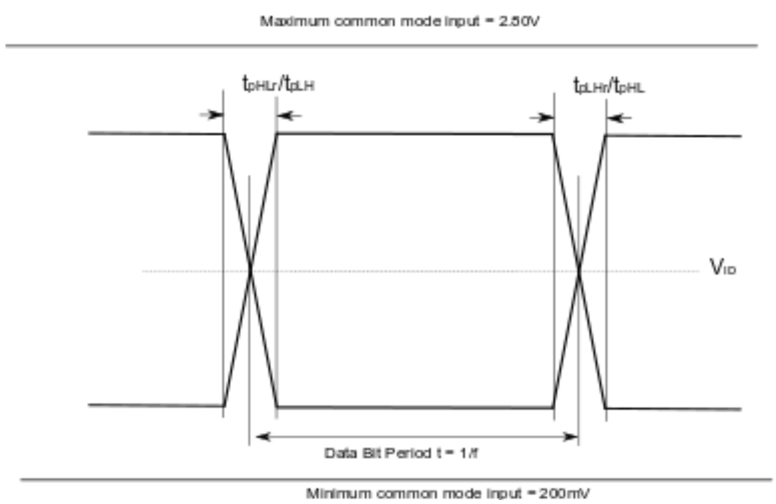
Note: Guaranteed by design

LVDS Transmitter Timing Specifications

Symbol	Description	Min	Typ	Max	Unit
F	Operating frequency	-	100	-	MHz
t_{pHL}	Output differential propagation delay high to low		1.5		ns
t_{pLH}	Output differential propagation delay low to high		1.5		ns

Note: Guaranteed by design

LVDS Timing

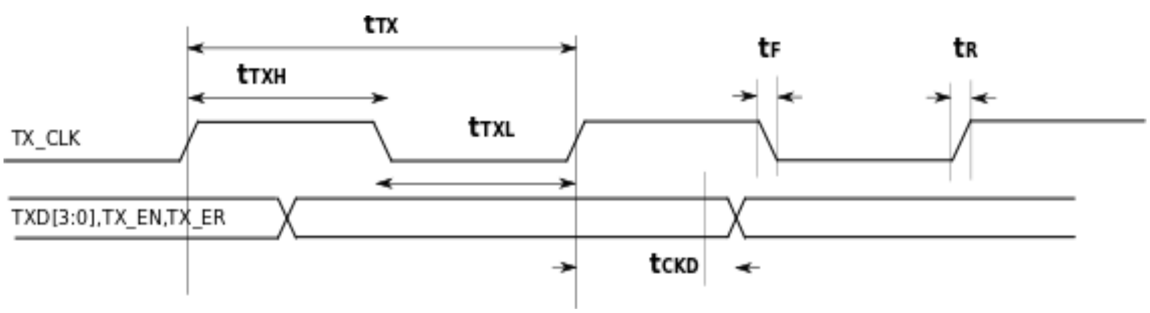


6.7 Ethernet MII Timing

Parameter	Description	Min	Typ	Max	Unit
t_{TX}	Transmit clock period for 10 Mbps	-	400	-	ns
t_{TX}	Transmit clock period for 100 Mbps	-	40	-	ns
$t_{TXH/TXL}$	Transmit clock duty cycle	35	-	65	%
t_{CKD}	Transmit clock to MII data delay	1	5	15	ns
t_R, t_F	Transmit clock rise and fall time	1	-	4	ns

Note: Guaranteed by design

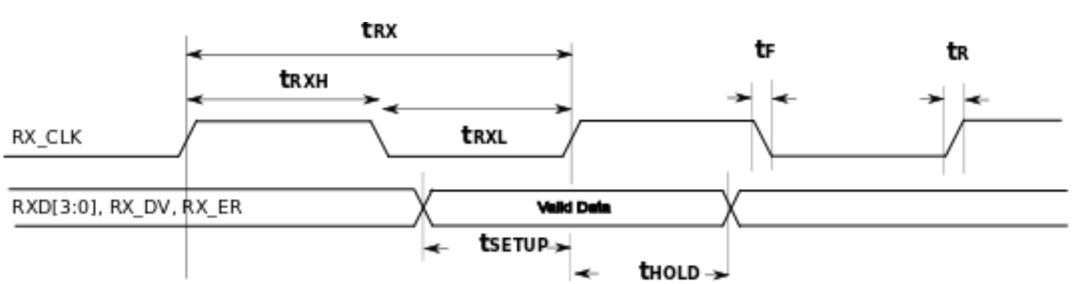
Transmit timing



Parameter	Description	Min	Typ	Max	Unit
t_{RX}	Receive clock period for 10 Mbps	-	400	-	ns
t_{RX}	Receive clock period for 100 Mbps	-	40	-	ns
$t_{RXH/RXL}$	Receive clock duty cycle	35	-	65	%
t_{SETUP}	Receive data set up time to receive clock	10	-	-	ns
t_{HOLD}	Receive data hold time to receive clock	10	-	-	ns
t_R, t_F	Receive clock rise and fall time	1	-	4	ns

Note: Guaranteed by design

Receive timing

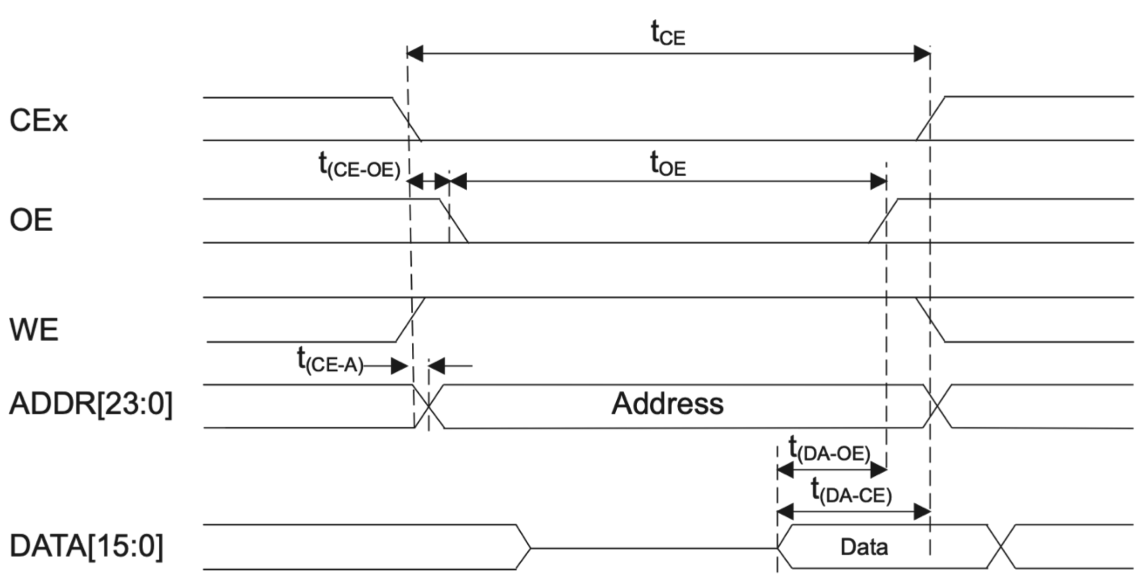


6.8 External Bus Interface (EBI) Timing

In all timing tables, the t_{HCLK} is the MCU system clock. The External Bus Interface is designed to be timing compatible with industry standard memories.

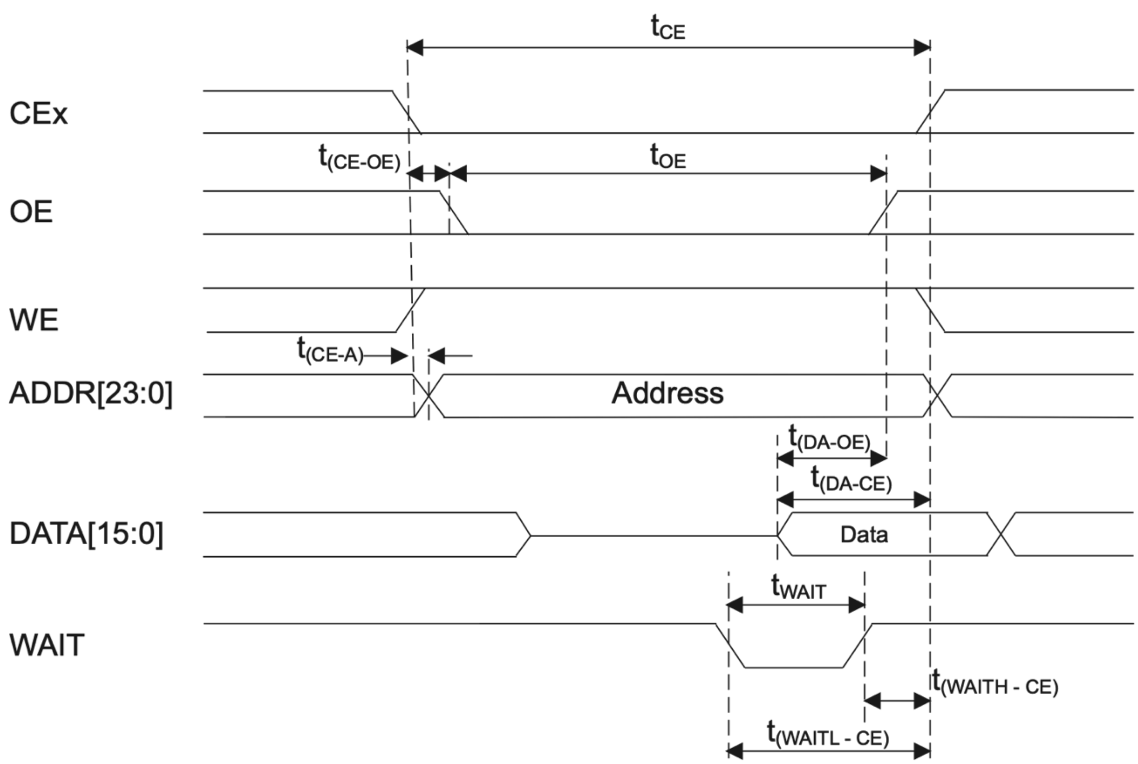
Read timing (no wait states)

Parameter	Description	Min	Typ	Max	Unit
t_{CE}	Chip select low time	2 t_{HCLK} - 2	-	2 t_{HCLK} + 0.5	ns
t_{CE} to t_{OE}	Chip select low to output enable low set-up time	0	-	1	ns
t_{OE}	Output enable low time	2 t_{HCLK} - 1	-	2 t_{HCLK} + 0.5	ns
t_{OE} to t_{CE}	Output enable high to chip select high hold time	0	-	-	ns
t_{CE} to t_A	Chip select low to address valid set-up time	-	-	0.5	ns
t_{OE} to t_A	Address hold time after output enable high	0	-	-	ns
t_{DATA} to t_{CE}	Data to chip select high set-up time	2 t_{HCLK} – 2	-	-	ns
t_{DATA} to t_{OE}	Data to output enable high set-up time	2 t_{HCLK} – 2	-	-	ns
t_{OE} to t_{DATA}	Data hold time after output enable high	0	-	-	ns
t_{CE} to t_{DATA}	Data hold time after chip select high	0	-	-	ns



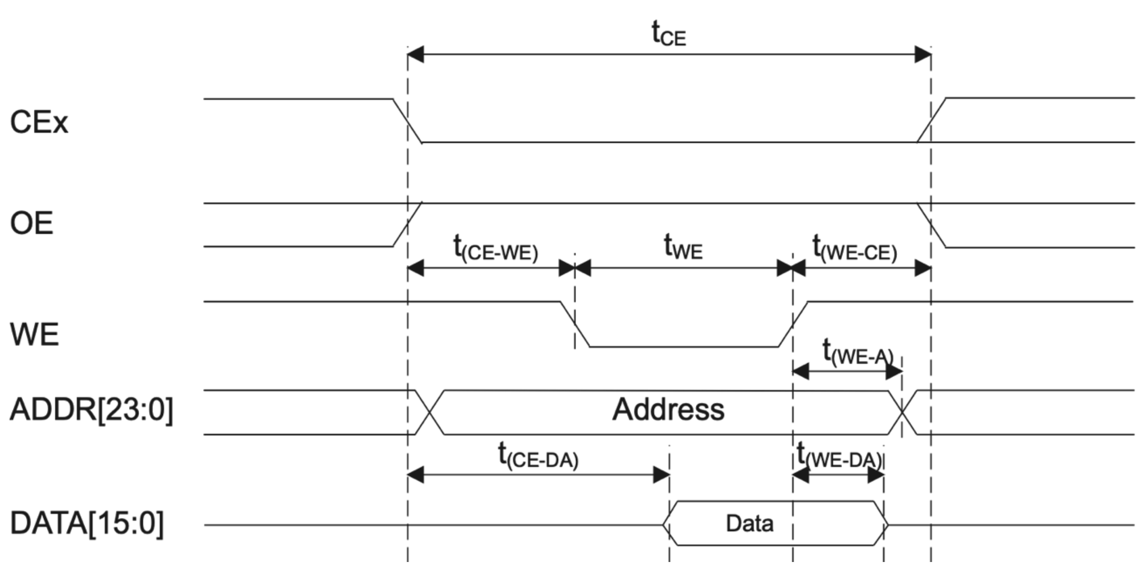
Read timing (with wait states)

Parameter	Description	Min	Typ	Max	Unit
t_{CE}	Chip select low time	7 t_{HCLK} + 1	-	7 t_{HCLK}	ns
t_{OE}	Output enable low time	5 t_{HCLK} - 1	-	5 t_{HCLK} + 1	ns
t_{WAIT}	Wait signal low time	t_{HCLK} - 0.5	-	-	ns
t_{CE} to t_A	Chip select low to address valid set-up time	-	-	0.5	ns
t_{WAITL} to t_{CE}	Wait signal valid before chip select high	5 t_{HCLK} + 1.5	-	-	ns
t_{WAITH} to t_{CE}	Chip select hold time after wait signal invalid	4 t_{HCLK} + 1	-	-	ns



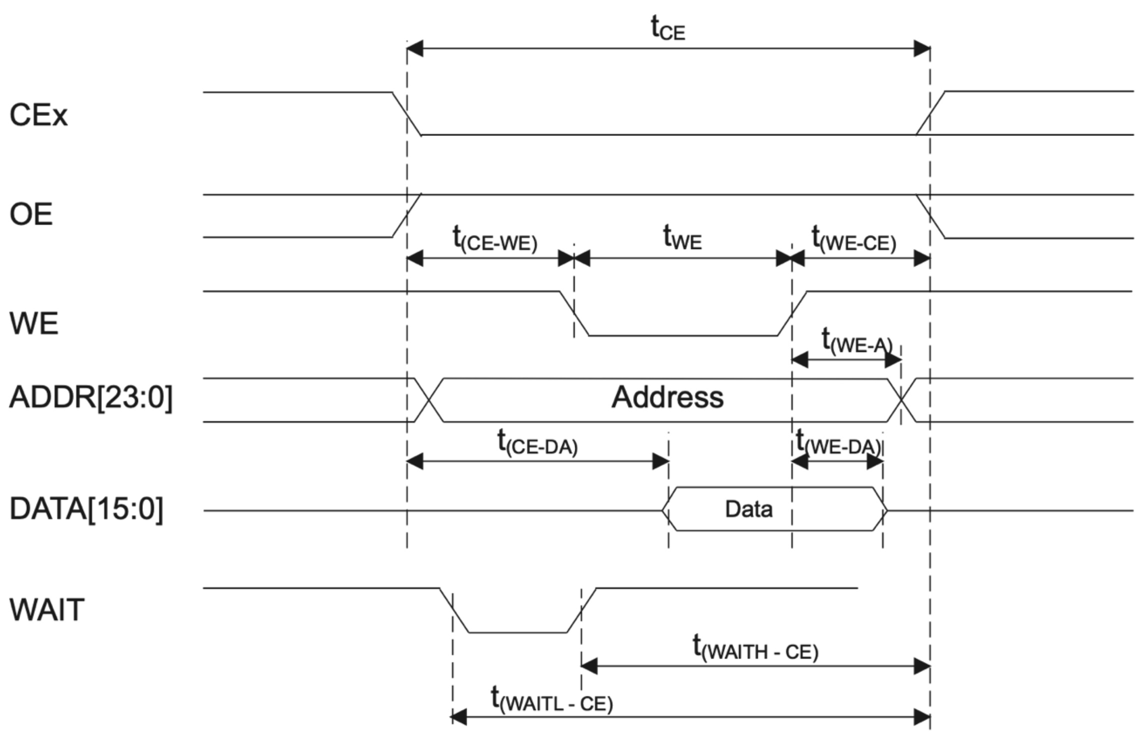
Write timing (no wait states)

Parameter	Description	Min	Typ	Max	Unit
t_{CE}	Chip select low time	3 t_{HCLK} - 2	-	3 t_{HCLK} + 0.5	ns
t_{CE} to t_{OE}	Chip select low to output enable low set-up time	t_{HCLK} - 0.5	-	t_{HCLK} + 0.5	ns
t_{WE}	Write enable low time	t_{HCLK}	-	t_{HCLK} + 0.5	ns
t_{WE} to t_{CE}	Write enable high to chip select high hold time	t_{HCLK} + 0.5	-	-	ns
t_{CE} to t_{A}	Chip select low to address valid set-up time	-	-	0	ns
t_{WE} to t_{A}	Address hold time after write enable high	t_{HCLK} + 0.5	-	-	ns
t_{CE} to t_{DATA}	Chip select low to data valid time	-	-	t_{HCLK} + 2	ns
t_{DATA} to t_{WE}	Data hold time after write enable high	t_{HCLK} + 0.5	-	-	ns



Write timing (with wait states)

Parameter	Description	Min	Typ	Max	Unit
t_{CE}	Chip select low time	8 t_{HCLK} - 0.5	-	8 t_{HCLK} + 1	ns
t_{WE}	Write enable low time	6 t_{HCLK} - 0.5	-	6 t_{HCLK} + 1	ns
t_{WAITL} to t_{CE}	Wait signal valid before chip select high	6 t_{HCLK} - 0.5	-	-	ns
t_{WAITH} to t_{CE}	Chip select hold time after wait signal invalid	4 t_{HCLK} + 2	-	-	ns



7 Electrostatic Discharge (ESD)

ESD testing is done in conformance with MIL-PRF-38534 and applies to all pads.

Parameter	Test Conditions	Value	Unit
ESD for Human Body Model (HBM)	All pins	2000	V
ESD for field-induced Charged Device Model (CDM)	All pins	500	V

8 Radiation Hardened Performance Targets

Parameter	Description	Min	Typ	Max	Unit
TID	Total ionizing dose (VA41620)	-	-	300	krad(Si)
TID	Total ionizing dose (VA41630)	-	-	200	krad(Si)
SER	Soft error rate (EDAC & Scrub[1] enabled)	-	1E-15	-	error bit per day[2]
SEL	Linear energy transfer (latch-up immunity)	110	-	-	MeV * cm^2 / mg

Notes:

1. Running at an appropriate frequency to prevent the accumulation of errors in the memory to achieve consistently low SER over time.
2. In geosynchronous orbit, solar min, and 100 mils of aluminum shielding.

9 Thermal Resistance Characteristics

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

176-pin plastic QFP package thermal resistance data

Thermal Parameter	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1,2]	Four-layer board (2s2p); Still air	θ_{JA}	30.81	°C/W
	Four-layer board (2s2p); air flow 1 m/s	θ_{JA}	27.62	°C/W
	Four-layer board (2s2p); air flow 2 m/s	θ_{JA}	26.49	°C/W
Junction to Case[3,4]	–	θ_{JC}	6.01	°C/W
Junction to Board[5]	–	θ_{JB}	23.67	°C/W

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance,

mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Simulation models are setup following the EIA/JESD51-2 for still air condition and following the EIA/JESD51-6 for moving air condition. The package is placed with horizontal orientation.
3. The model and boundary condition intend to simulate the θ_{JC} test conditions. A cold plate and the grease between package and cold plate are modeled.
4. θ_{JC} represents the thermal resistance between the chip to package top case.
5. The model and boundary conditions intend to simulate the test conditions specified in EIA/JESD51-8.

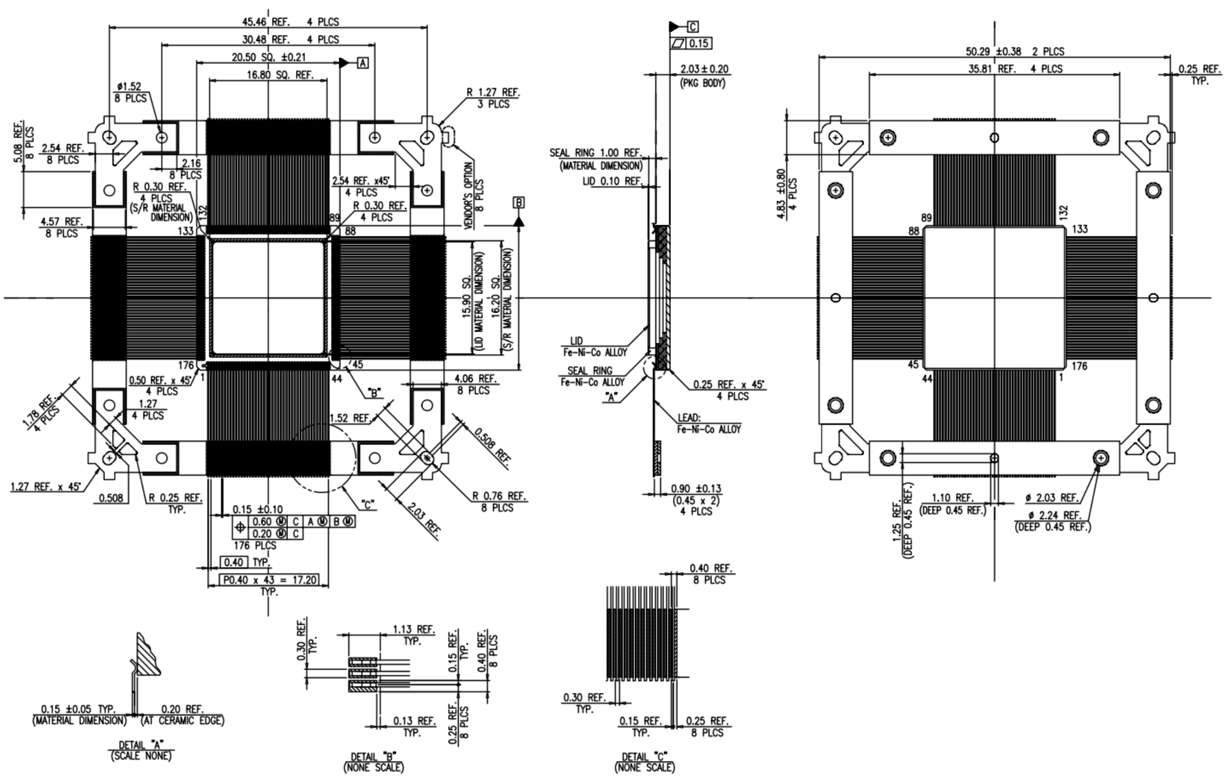
196- pin BGA package thermal resistance data

Thermal Parameter	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1,2]	Four-layer board (2s2p); Still air	θ_{JA}	18.74	°C/W
	Four-layer board (2s2p); air flow 1 m/s	θ_{JA}	16.72	°C/W
	Four-layer board (2s2p); air flow 2 m/s	θ_{JA}	15.95	°C/W
Junction to Case[3,4]	–	θ_{JC}	6.49	°C/W
Junction to Board[5]	–	θ_{JB}	8.17	°C/W

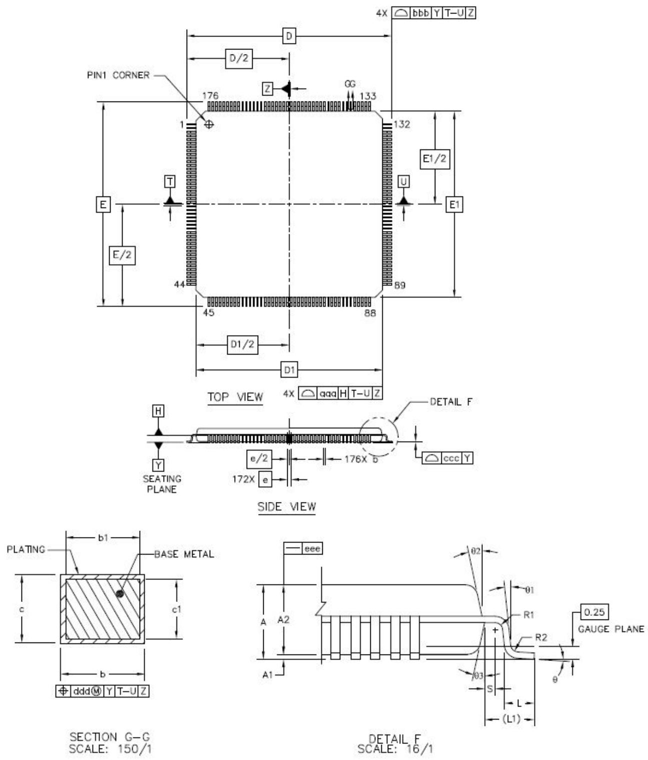
Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. The simulation models are setup following the EIA/JESD51-2 for still air condition and following the EIA/JESD51-6 for moving air condition. The package is placed with horizontal orientation.
3. The model and boundary condition intend to simulate the θ_{JC} test conditions. A cold plate and the grease between package and cold plate are modeled.
4. θ_{JC} represents the thermal resistance between the chip to package top case.
5. The model and boundary conditions intend to simulate the test conditions specified in EIA/JESD51-8.

10 Package Mechanical Information

10.1 176-Pin Ceramic QFP

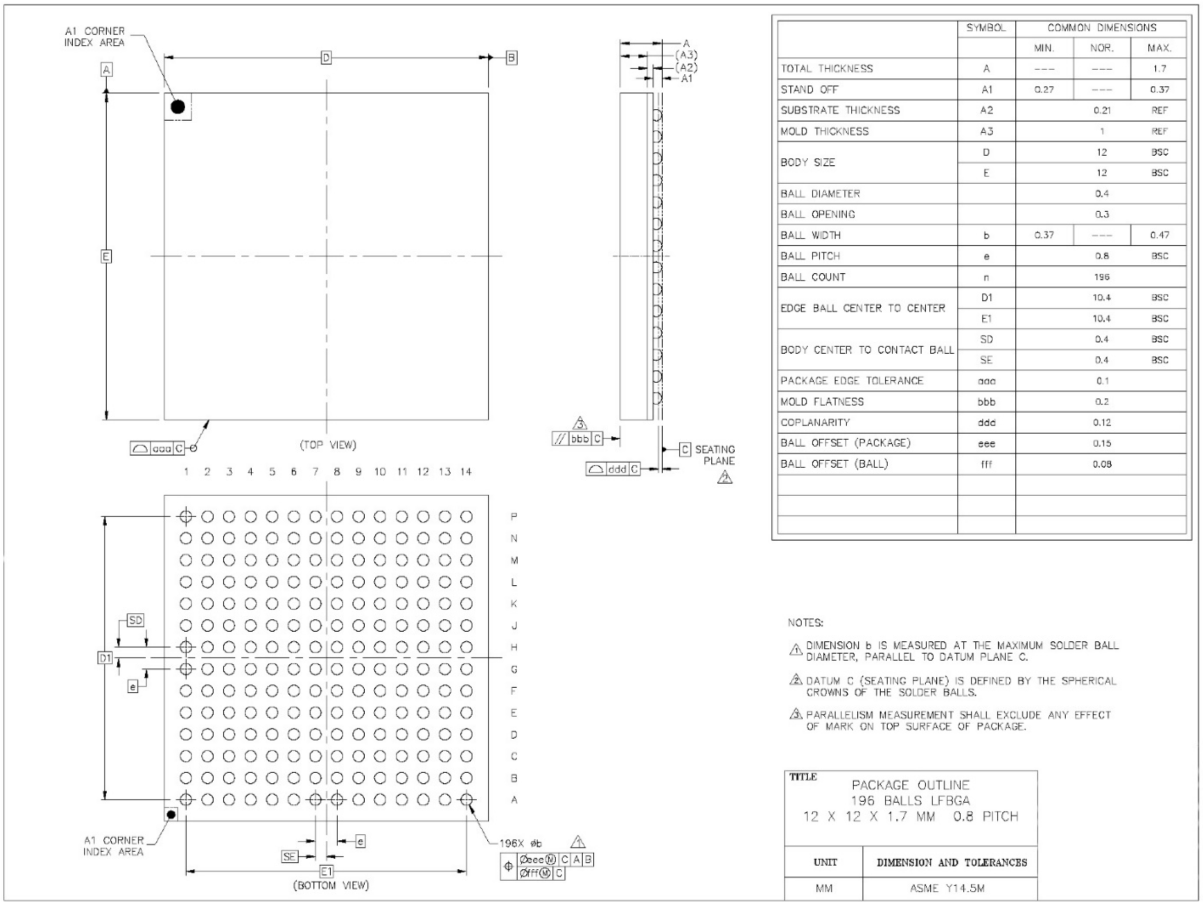


10.2 176-Pin Plastic QFP



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	22 BSC		
	Y	E	22 BSC		
BODY SIZE	X	D1	20 BSC		
	Y	E1	20 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

10.3 196-Pin Plastic BGA



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.7
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		1	REF
BODY SIZE	D		12	BSC
	E		12	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.3	
BALL WIDTH	b	0.37	---	0.47
BALL PITCH	e		0.8	BSC
BALL COUNT	n		196	
EDGE BALL CENTER TO CENTER	D1		10.4	BSC
	E1		10.4	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.12	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

10.4 Package Pin Metallization

Package	Material
176-pin plastic	100% Matte Tin
176-pin ceramic (including QML devices)	99.9% Gold
196-pin BGA	63% Tin / 37% Lead

10.5 Reflow / Soldering Conditions

To prevent potential memory corruption of the FRAM, soldering conditions for the VA41630 must not exceed 260°C for 3 seconds.

11 Ordering Information

Part Number	Package	NVM	Qualification
VA41630-CQ176F0EBA	Ceramic 176 QFP	256 Kbyte on-chip FRAM	Engineering Sample
VA41630-CQ176FKQBA	Ceramic 176 QFP	256 Kbyte on-chip FRAM	MIL-PRF-38534 Class K
VA41630-CQ176FQQBA	Ceramic 176 QFP	256 Kbyte on-chip FRAM	MIL-PRF-38535 Class Q+
VA41630-PQ176F0PBA	Plastic 176 QFP	256 Kbyte on-chip FRAM	VORAGO HiRel Qual
VA41630-PG196F0PBA	Plastic 196 BGA	256 Kbyte on-chip FRAM	VORAGO HiRel Qual
VA41630-PG196F0PBB	Plastic 196 BGA	256 Kbyte on-chip FRAM	VORAGO HiRel Qual
VA41620-CQ176F0EBA	Ceramic 176 QFP	External NVM (parallel or SPI)	Engineering Sample
VA41620-PQ176F0PBA	Plastic 176 QFP	External NVM (parallel or SPI)	VORAGO HiRel Qual
VA41620-PG196F0PBB	Plastic 196 BGA	External NVM (parallel or SPI)	VORAGO HiRel Qual

12 Development Kit Ordering Information

Description	Part number	Features
Development Board	PEB1-VA41630	Supported by Keil™ MDK-Arm® Microcontroller Software Kit Board Support Package (BSP) includes example software for peripherals Includes Segger J-Link OB
Development Board	PEB1-VA41620	Supported by Keil™ MDK-Arm® Microcontroller Software Kit Board Support Package (BSP) includes example software for peripherals Includes Segger J-Link OB

13 VA416X0 Errata

VOR-ER1004: Serial Wire Debug		
Description	**Workaround**	**Comment**
Serial Wire Debug (SWD) is not functioning as intended without code in boot memory	VA41630: Will ship devices with code in NVM. Do not erase internal NVM and leave blank VA41620/28/29: External memory must have code programmed into it	Present in VA416xx Rev B silicon
VOR-ER1008: True Random Number Generator (TRNG)		
Description	**Workaround**	**Comment**
A read of I_DATA[5] will always return a value of 0x0000_0000 and will automatically clear the contents of I_DATA[4:0]	Do not read I_DATA[5] until after I_DATA[4:0] has been read	Present in VA416xx Rev A/B silicon
VOR-ER1009: Internal Voltage Regulator		
Description	**Workaround**	**Comment**
The use of the internal 1.5V digital and analog regulators can cause an unreliable power-up condition	An external 3.3V and 1.5V supply must be applied to the device	Present in VA416xx Rev A/B silicon
VOR-ER1010: TMR Refresh Issue with UART0 and UART1		
Description	**Workaround**	**Comment**
UART errors (on UART0 and UART1 only) may occur if the TMR refresh rate is set to any number higher than 0 (for refresh every clock cycle)	Set the DIVCOUNT_L value in the REFRESH_CONFIG_L Register to 0x0000	Present in VA416xx Rev B silicon
VOR-ER1011: TRSTn pull resistor direction		
Description	**Workaround**	**Comment**
Pulling the TRSTn up through a 10k Ohm resistor may result in NVM programming issues	For proper programming operation of the MCU, pin TRSTn should be pulled down through a 10k Ohm resistor	Present in VA416xx Rev B silicon
VOR-ER1012: Internal Band-Gap Measurement		
Description	**Workaround**	**Comment**
Performing an ADC conversion on ADC channels 11 or 12 can cause the MCU to reset	Do not set up the ADC to perform an ADC conversion on either the Bandgap 1.0V (channel 11) or the Bandgap 1.5V (channel 12)	Present in VA416xx Rev B silicon
VOR-ER1013: External Bus Interface (EBI) Wait States		
Description	**Workaround**	**Comment**

Extra wait states are required for EBI reads above 70MHz	Program the CFGWRITECYCLE in the EBICFG[3:0] registers to a value of 3 or higher for bus frequencies of 70MHz or higher	Present in VA416xx Rev B silicon
VOR-ER1014: Ethernet 10/100 MAC does not work at 100Mbps		
Description	**Workaround**	**Comment**
Ethernet peripheral encounters an excessive number of errors at 100Mbps	Operate the Ethernet peripheral at 10Mbps	Present in VA416xx Rev B silicon
VOR-ER1015: EDAC SBE/MBE count registers are not addressed correctly for writes		
Description	**Workaround**	**Comment**
In the SYSCONFIG block, data written to RAM1_SBE is miswritten to RAM0_MBE and data written to RAM0_MBE is incorrectly written to RAM1_SBE. The reads of the counts from RAMx_MBE and RAMx_SBE registers are correct and the EDAC circuitry correctly updates these register counts.	Must compensate for this in the application firmware.	Present in VA416xx Rev A/B silicon
VOR-ER1016: SPI RX FIFO		
Description	**Workaround**	**Comment**
While using block mode SPI transfers, failing to close the block (setting BMSTOP bit in the last transmitted word) will result in the last received word not being registered into the receive FIFO.	To ensure all SPI words are received, close the block by appending the BMSTOP bit to the last data word transmitted.	Present in VA416xx, both Rev A & Rev B.
VOR-ER1017: SPI block mode SCK glitch		
Description	**Workaround**	**Comment**
When the SPI is set up with SPH = 0, BMSTALL = 1, and BLOCKMODE = 1, writing BMSTOP + BMSKIPDATA causes a glitch on SCK if the SPI peripheral is stalled (block is open and the TX FIFO is empty).	Close a SPI block by appending the BMSTOP bit on the last data word instead of using BMSTOP + BMSKIPDATA on its own.	Present in VA416xx, both Rev A & Rev B.

14 Disclaimer

IMPORTANT NOTICE – PLEASE READ CAREFULLY

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15 Revision History

Date	Version	Page Locations	Description
05/22/2017	0.1	All	Initial draft
06/20/2018	0.2	4,5,10,33	Fixed typos. Updated block diagram
06/21/2018	0.3	11	Updated pinout
07/06/2018	0.4	11	Added pin description table
08/01/2018	0.5	30-42	Replaced tables, added PTG[7] in pin diagram and function select table, added plastic package information
11/12/2018	0.6	11	updated the pinout diagram to show V_{DD33} and V_{DD15} instead of V_{DDIO} and V_{DD}
12/03/2018	0.7	41	Changed 1 MHz internal clock timing to 20 MHz
02/20/2019	0.8	11-14	Updated the pinout diagram and updated some pin names. Reconfigured some section numbers and replaced peripheral block diagrams. Added die pad coordinates.
06/26/2019	0.9	All	Reconfigured some sections, updated formatting and symbols throughout, added electrical tables, and replaced several feature descriptions.
07/19/2019	0.92	35-47	Cleaned up some figures and tables, added deep-sleep information, EBI specifications, and removed some redundant information
11/12/2019	0.93	12, 53	Corrected pin names and updated ceramic package drawing.
03/11/2020	0.94	35-43	Updated electrical specifications for VOL, VOH, and removed VOH for the I^2C pins. Also, minor corrections were made throughout the text.
03/26/2020	0.94A	All	Grammar and punctuation scrub, and clarification for readability and understanding. Added EBI timing diagrams and LVDS pin electrical specifications.
04/20/2020	0.95	14, 52	Moved die pad information to Section 9.
06/30/2020	0.96	51	Added improved IDD specs and information.
07/28/2020	0.97	12	Corrected pinout diagram, pin 146
08/07/2020	0.98	13-16, 52, 60	added BGA package
09/15/2020	0.99	13, 19, 60	Added pins VDDQ and TEST_MODE
01/27/2021	0.991	18, 39	TMS has a pull-down, not pull-up
4/21/2021	0.992	41	Corrected typo in the table in Section 6.3.
6/9/2021	0.995	33, 38, 46-49	Corrected power supply decoupling, updated the temperature sensor graph, updated the EBI timing diagrams, and cleaned up ADC and DAC tables.
6/30/2021	1.0	All	Removed "Preliminary" from each page.
7/16/2021	1.1	63	Updated part numbers
8/5/21	1.2	1	Updated radiation data verbiage
8/23/21	1.3	All	Edited header to be consistent with other datasheets. Updated package options.

Date	Version	Page Locations	Description
10/6/21	1.4	64	Removed bare die as package option.
12/21/21	1.5	1, 53	Updated block diagram to be consistent with other VORAGO datasheets. Updated notes to SER data.
3/2/22	1.6	1, 20	Replaced JTAG with SWD on block diagram. Removed JTAG from BGA ball descriptions table.
3/28/22	1.7	1, 56	Minor edits to cover page, for consistency with other VORAGO datasheets. Added required soldering conditions.
4/13/22	1.8	65, 66	Added VA416XX errata.
7/13/22	1.9	1,9,12,35,37	Page 1 added reference to errata in support box Page 9 added section. 1.3 Boot Sequence Page 12 updated section. 3.2 196-Pin Plastic BGA Ball-Map diagram, updated VA416x0 Description Page 35 added section. 4.14 Debug and programing interface (DBG) Page 37 added section. 5.3 Required Power Supply Sequencing
10/21/22	2.0	12, 68	Corrected BGA ball L06, now PD09 was NC. Updated ordering info with production part numbers
3/3/23	2.1	66	Added VA41630 QML-V part to Section 9 Ordering Information.
4/10/23	2.2	42, 63, 71	Removed deep sleep mode table. Added package thermal information, added Ethernet erratum, and some other minor changes.
7/12/23	2.3	67	Corrected 9.4 Pin Metallization Table.
8/7/23	2.4	1, 9, 23, 48, 49, 66, 69	Replaced block diagram with blue box version for compatibility with other data sheets and to show 8 ADC channels. Added reference to Infineon FRAM datasheet for FRAM radiation data. Removed "Option for use with a single 3.3 V supply". TMS has an internal pull-up resistor. Added verbiage to the temp sensor example. Added post-TID ADC performance table & post-TID internal temp sensor chart. Updated metallization table. Added VOR-ER1015 EDAC register address erratum. A few font changes for consistency.
12/11/23	2.5	67	Added part numbers VA41630-PG196F0PBB & VA41620-PG196F0PBB.
1/4/24	2.6	1, 48, 69 All (misc & formatting)	Blue bock diagram for consistency across datasheets. Updated post-TID ADC performance table. Added errata VOR-ER1016: SPI RX FIFO & VOR-ER1017: SPI block mode SCK glitch. Minor miscellaneous updates & formatting changes for consistency across datasheets.
2/16/24	2.7	66	Updated ordering table. Removed VA41630-PQ176F0PBB & added correct part number VA41630-PG196F0PBB. Removed VA41630-PG196PBA (PCN

Date	Version	Page Locations	Description
			issued). Replaced VA41630-CQ176VBA with VA41630-CQ176FQQBA.