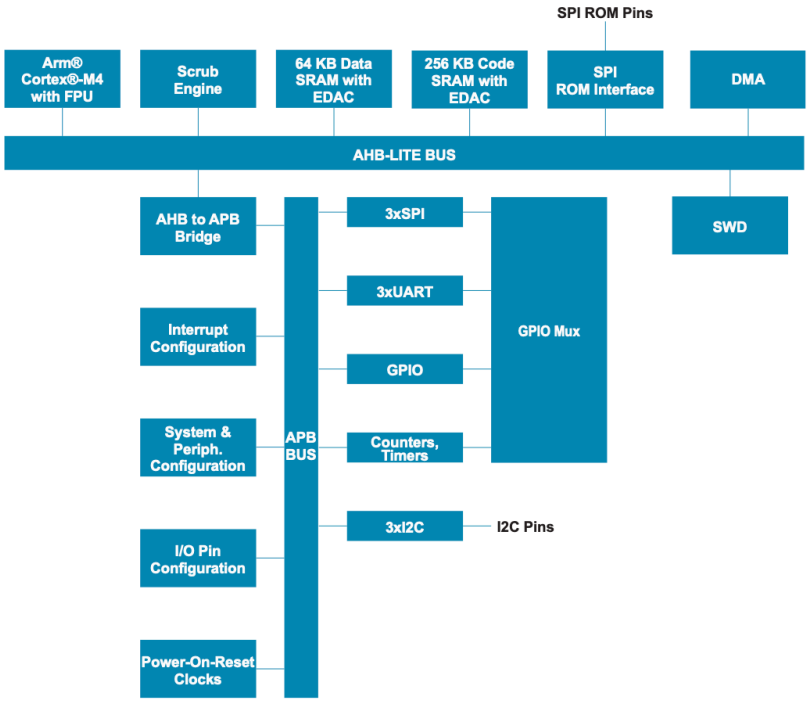
VA41628

Radiation Hardened VA41628

32-Bit Arm® Cortex®-M4 (with FPU) microcontroller manufactured with HARDSIL® technology offering best in class radiation performance and latch-up immunity.



KEY FEATURES

- Manufactured with HARDSIL® technology
- RAD hardened Registers with Triple-Mode Redundancy (TMR)
- 32-bit Arm® Cortex®-M4 processor
  - Single-Precision Floating-Point Unit (FPU)
  - SWD based debug interface
- Operating voltages
  - GPIO 3.3 ± 10% V
  - Core 1.5 ± 10% V
- Clock rate up to 50MHz
  - Internal 20MHz oscillator for fail-safe clocking
- Memory
  - 64 Kbyte on-chip data and 256 Kbyte on-chip program memory SRAM
  - Error Detection and Correction (EDAC)
  - Built in Scrub Engine
- Peripherals
  - 75 Configurable GPIO pins
  - 3 UART interfaces
  - 3 I^2C interfaces
  - 3 SPI interface
  - DMA controller
- Timer System
  - 24 configurable 32-bit counters / timers
  - Input capture, Output compares
  - PWMs, Pulse Counters, Watchdog timer
- Package
  - 128 CQFP (14mm x 14mm)
  - 196 BGA (12mm x 12mm)

MEMORY CONFIGURATION OPTIONS

- External SPI NVM (for code boot)

RADIATION HARDENED PERFORMANCE

- VA41628 Total Ionizing Dose (TID) > 300 krad(Si)
- Soft Error Rate (SER) < 1E-15 errors/bit-day w/ EDAC & Scrub enabled (See Section 6 for details)
- Single-Event Latch-Up (SEL) immunity to ion LETs > 110 MeVcm^2/mg (at 125°C)

SUPPORT

- PEB3 development board
- BSP and drivers
- See product errata in Section 10

Features

- Performance
  - 50 MHz Arm® Cortex®-M4 processor with Single-Precision Floating-Point Unit (FPU)
- On-Chip Memory
  - 256 Kbyte Program SRAM
  - 64 Kbyte Data SRAM
  - On-chip Error Detection and Correction (EDAC) and Scrub Engine
- General-purpose I/O (GPIO) pins
  - Configurable direction
  - Configurable pull-up/down resistors
  - Configurable as edge or level sensitive interrupt sources
- 24 General-purpose counter/timers
  - Configurable interrupt sources
  - Can be triggered from multiple sources (GPIO or other counter/timers)
  - Each counter/timer has an independent 32-bit counter
  - Configurable as PWM, capture or compare
- 3 x UART
  - Internal FIFO
  - Transmit or receive interrupt source
- 3 x Serial Peripheral Interface (SPI) ports
  - Internal FIFO
  - Transmit or receive interrupt source
  - Multiple chip-select outputs
- 3 x I^2C ports
  - Internal FIFO
  - Master and Slave mode on all ports
  - Standard and Fast mode support
- System-level Triple-Mode Redundancy (TMR) on critical internal registers
- Random Number Generator
- Serial Wire Debug (SWD) based debug controller

1 Functional Description

The VA41628 is optimized for radiation environments and consists of an Arm® Cortex®-M4 CPU core and a related set of peripherals. It includes Error Detection and Correction (EDAC) logic on the internal memories. The program space EDAC is 16-bit word-based for optimum performance and reliability. The data space EDAC is 8-bit to allow reliable byte size data manipulation. In addition, the VA41628 includes Triple-Mode Redundancy (TMR) with voting on select internal flip-flop storage elements.

1.1 Related Documentation

The following associated documents will help understand this device:

- Arm® Documents (Available from http://infocenter.arm.com)
  - Cortex®-M4 Generic User Guide
  - Cortex®-M4 Technical Reference Manual
  - AMBA® 3 AHB-Lite™ Protocol Specification
  - AMBA® 3 APB Protocol Specification
  - Arm® TrustZone® True Random Number Generator Technical Reference Manual
  - Arm® PrimeCell® External Bus Interface Technical Reference Manual
  - Arm® PrimeCell® DMA Technical Reference Manual
- NXP Documents (Available from http://www.nxp.com)
  - I²C-bus Specification and User Manual
- VORAGO Documents
  - VA416XX Programmer's Guide

1.2 Feature Summary

- Processor Core
  - Arm® Cortex®-M4 processor
    - Up to 50MHz operation
    - SysTick Counter
    - Single Cycle Multiply-and-accumulate
    - Hardware divide (2 to 12 cycles)
    - Single-precision IEEE 754 compliant HW Floating Point Unit (FPU)
    - Bit-Banding region for registers and data SRAM

- Arm® Cortex®-M4 built-in Nested Vectored Interrupt Controller (NVIC)
  - Interrupt sources with a unique 8-bit priority level
  - Tail chaining supported
- Arm® CoreSight™ debug and trace technology
  - SWD: Serial Wire Debug
  - DAP: Debug Access Port
  - Four Breakpoint Comparators
  - Two Data Watch Point Comparators

- Memory
  - 64 Kbyte SRAM Data Memory (32 Kbyte on Data bus and 32 Kbyte on System bus)
    - Byte-level Error Detection and Correction (EDAC) logic on Data memory
  - 256 Kbyte SRAM Instruction Memory
    - Loaded from Serial Peripheral Interface (SPI) based memory at startup
    - Configurable boot delay, boot speed, and error checking
    - 16-bit level EDAC on instruction memory
  - Programmable Scrub Engine for both Data and Instruction memory
  - Utility peripheral
    - Provides means of injecting single and multi-bit errors to check error handling routines.
- System Integration Peripherals
  - System Configuration
    - Memory Control
      - Data memory clear on reset
      - Code memory reload on reset
      - Code memory write protect
      - Code/Data memory Scrub rate
      - Code/Data memory SBE/MBE counters
      - Code/Data memory SBE/MBE Interrupt control
    - GPIO Glitch Filter rate control
    - Peripheral Configuration
      - Clock gating and Reset control of individual peripherals
  - Interrupt Router
    - Maps interrupt sources to timers and DMA for flexible event triggers

- Four-Channel DMA
  - Allows CPU independent data movement from memory to memory, peripherals to memory, or memory to peripherals.

- Serial Communication Peripherals
  - Three UARTs
    - 16-word Transmit and Receive FIFOs
    - Fractional baud rate generation
      - Supports baud rates up to 115,200 with system clocks above 2MHz
    - Supports:
      - 5, 6, 7, 8 and 9 bits
      - Even, Odd and None parity
      - Stop Bits 1 or 2
      - Break generation and detection
    - Error detection
      - FIFO overflow
      - Framing error
      - Parity error
      - Break detection
    - Configurable Interrupt generation
      - FIFO level (fully configurable)
      - Receive Timeout
      - Error
  - Three SPI Ports (Fourth SPI used only to boot SPI NVM)
    - Supports all four modes of SPI operation
    - Data size of 4 to 16 bits
    - 16-word Transmit and Receive FIFOs
    - Block mode support for larger Frame sizes
    - Master-mode clock rates up to 1/8 System clock (1.56 Mbit/s)
    - Slave-mode clock rates up to 1/24 System clock (520 kbit/s)
    - Configurable Interrupt generation for transmitting and receiving
      - FIFO level (fully configurable)
      - FIFO Overflow
      - Receive Timeout
  - Three I^2C Ports
    - Standard I^2C-compliant bus interface
    - Dedicated open-drain pins supporting I^2C Fast mode

        - Configurable as Master or Slave
        - 16-byte Transmit and Receive FIFOs
        - Configurable Interrupt generation
            - FIFO level (fully configurable)
- System Connection Peripherals
    - GPIO
        - Seven GPIO Ports with up to 75 pins total
            - 16-bit ports A
            - 9-bit ports B
            - 14-bit ports C
            - 6-bit ports D
            - 14-bit ports E
            - 8-bit ports F
            - 8-bit port G
        - Configurable direction control of individual bits
        - Bit-level mask register allows single instruction setting or clearing of any bits in one port.
        - Configurable interrupt generation on ports A-F
            - Level or Edge sensitive
        - Configurable Pulse mode on individual bits
        - Configurable (0 to 3) cycle delay filtering on individual bits
    - I/O Configuration
        - Manages programmable function selects of each pin to allow peripherals to be mapped to GPIO
        - Sets electrical parameters:
            - Glitch filters
            - Pull-up/Pull-down resistors
            - Signal inversion
            - Pseudo open-drain
    - Timers
        - Twenty-three 32-bit timers
        - Advanced trigger modes using cascade feature
            - Separate Start/Stop based on other timers or interrupt signals
            - Multiple trigger sources from GPIO or other timers
        - Configurable output event

- One cycle pulse when timer equal to zero detected
- Active mode
- Divide by two for square wave creation
- Two PWM modes: single edge and double edge detection (supports center alignment)

- Power supplies
  - Configured for use with dual supplies
    - 3.3 V for I/O
    - 1.5 V for logic
- Radiation Hardness
  - Latch-up immunity in extreme environments
  - Built to be resistant to Single Event Upsets (SEU)
  - Built with VORAGO proprietary HARDSIL® technology
  - Designed with Dual-Interlocked Storage Cells (DICE) and Triple-Mode Redundancy (TMR) on key register elements.

1.3 Power-Up Sequence

The VA41629 begins operation by loading the internal SRAM code memory from an external SPI non-volatile memory connected to the ROM SPI interface. The clock source for boot operation is a 20 MHz internally generated oscillator (HBO).

After loading the code memory, the processor follows a typical Arm® Cortex®-M4 start sequence.

1.4 Resets

In addition to the Power-on reset, the device can be reset from other events:

- EXTRESETn pin
- SYSRESETREQ from software
- Hardware events configured by IRQ Selector Peripheral or the System Controller Peripheral:
  - Processor Lockup
  - Watchdog Timer
  - Memory Errors (Single or Multi-bit errors from the EDAC memory controller)

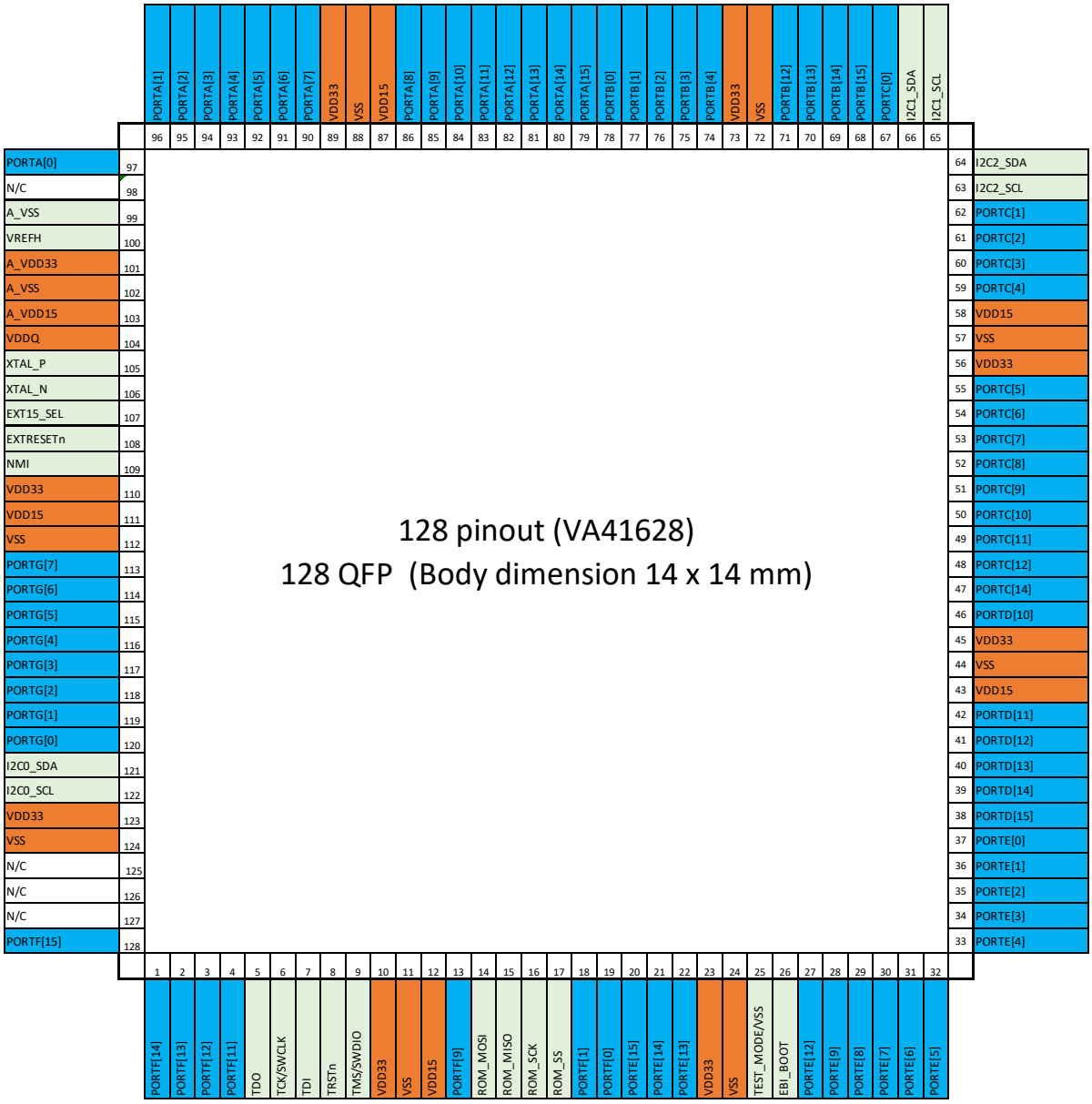
1.5 Inter-Integrated Circuit (I^2C) pins

The VA41628 contains three sets of dedicated I^2C pins and related I^2C controllers. Each controller can act as both an I^2C master and an I^2C slave simultaneously. These interfaces are capable of operating up to 100 kbps in Standard mode and up to 400 kbps in Fast mode.

2 Pinout and Ball Mapping

The VA41628 is available in128-pin ceramic QFP and 196-ball plastic BGA.

2.1 128-pin CQFP



2.2 Pin Descriptions

Pin Type	Description	Type	Internal Pull-up/down
System Pins			
XTAL_N	Crystal Oscillator Input	In	None
XTAL_P	Crystal Oscillator Output	Out	None
EXTRESETn	External System Reset, active low. Resets the processor and all peripherals. This signal is internally synchronized before being used. Any reset will cause this pin to pull low during the reset sequence.	ASync In / Open drain Out	Pull-up
NMI	Non-maskable Interrupt – active high	ASync In	None
EBI_BOOT	Used for factory test purposes only. Must be tied to VSS.	In	None
EXT15_SEL	Must be tied to VDD33. This signal disables the internal 1.5 V regulator, and 1.5 V must be applied externally to all VDD15 pins and A_VDD15.	In	None
TEST_MODE	For factory use only. Must be tied to VSS with a 10k resistor.	In	None
General-Purpose I/O Pins			
PORTA[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers.	Sync I/O	Software configurable
PORTB[15:12, 4:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers.	Sync I/O	Software configurable
PORTC[14,12:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers.	Sync I/O	Software configurable
PORTD[15:10]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers.	Sync I/O	Software configurable
PORTE[15:12, 9:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers.	Sync I/O	Software configurable

Pin Type	Description	Type	Internal Pull-up/down
PORTF[15:11, 9, 1:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers.	Sync I/O	Software configurable
PORTG[7:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers.	Sync I/O	Software configurable
SPI ROM pins			
ROM_SCK	SPI Clock to Boot ROM.	Sync Out	None
ROM_SS	SPI Chip Select to Boot ROM (Active Low).	Sync Out	None
ROM_MOSI	SPI Data Out to Boot ROM.	Sync Out	None
ROM_MISO	SPI Data In from Boot ROM.	Sync In	Pull-down
I^2C Pins			
I2C0_SCL	I^2C0 Clock	Open drain	None
I2C0_SDA	I^2C0 Data	Open drain	None
I2C1_SCL	I^2C1 Clock	Open drain	None
I2C1_SDA	I^2C1 Data	Open drain	None
I2C2_SCL	I^2C2 Clock	Open drain	None
I2C2_SDA	I^2C2 Data	Open drain	None
SWD Pins			
TCK/SWCK	Test Clock/Serial Wire Debug Clock	Clock	None
TMS/SWDIO	Test Mode Select/Serial Wire Debug Data IO	Sync In/Out	Pull-down
TRSTn	Test Reset, active low	Sync In	None
TDI	Test Data In	Sync In	None
TDO	Test Data Out	Sync Out	None

Pin Type	Description	Type	Internal Pull-up/down
Power/Ground pins			
VDD15	1.5 V Core power (must be supplied externally)	Power	N/A
VSS	Ground	Ground	N/A
VDD33	3.3 V IO power	Power	N/A
A_VDD15	1.5 V Analog power (must be tied to VDD15)	Power	N/A
A_VSS	Analog Ground (must be tied to VSS)	Ground	N/A
A_VDD33	3.3 V Analog IO power (must be tied to VDD33)	Power	N/A
VREFH	Analog reference (must be tied to VDD33)	Power	N/A
VDDQ	For factory use only (must be tied to VSS)	Power	N/A

2.3 GPIO Pin Alternative Functions

GPIO pins can be configured for various peripherals on the VA41628 MCU. The default configuration is for all the pins to be assigned as GPIO. Please refer to the VA416XX Programmer's Guide for more information about the usage of GPIO pins and their alternative functions.

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTA[0]	TIM[0]	SPI2_SSn4	UART0_RTSn
PORTA[1]	TIM[1]	SPI2_SSn3	UART0_CTSn
PORTA[2]	TIM[2]	SPI2_SSn2	UART0_TX
PORTA[3]	TIM[3]	SPI2_SSn1	UART0_RX
PORTA[4]	TIM[4]	SPI2_SSn0	Not assigned
PORTA[5]	TIM[5]	SPI2_SCK	Not assigned
PORTA[6]	TIM[6]	SPI2_MISO	Not assigned
PORTA[7]	TIM[7]	SPI2_MOSI	Not assigned
PORTA[8]	Not assigned	SPI2_SSn6	TIM[8]
PORTA[9]	Not assigned	SPI2_SSn5	Not assigned
PORTA[10]	Not assigned	TIM[23]	Not assigned
PORTA[11]	Not assigned	TIM[22]	Not assigned
PORTA[12]	Not assigned	TIM[21]	Not assigned
PORTA[13]	Not assigned	TIM[20]	Not assigned

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTA[14]	Not assigned	TIM[19]	Not assigned
PORTA[15]	Not assigned	TIM[18]	Not assigned
PORTB[0]	Not assigned	TIM[17]	SPI1_SSn7
PORTB[1]	Not assigned	TIM[16]	SPI1_SSn6
PORTB[2]	Not assigned	TIM[15]	SPI1_SSn5
PORTB[3]	Not assigned	TIM[14]	SPI1_SSn4
PORTB[4]	Not assigned	TIM[13]	SPI1_SSn3
PORTB[12]	SPI0_SSn2	TIM[5]	UART1_RTSn
PORTB[13]	SPI0_SSn1	TIM[4]	UART1_CTSn
PORTB[14]	SPI0_SSn0	TIM[3]	UART1_TX
PORTB[15]	SPI0_SCK	TIM[2]	UART1_RX
PORTC[0]	SPI0_MISO	TIM[1]	Not assigned
PORTC[1]	SPI0_MOSI	TIM[0]	Not assigned
PORTC[2]	Not assigned	UART0_RTSn	Not assigned
PORTC[3]	Not assigned	UART0_CTSn	Not assigned
PORTC[4]	Not assigned	UART0_TX	Not assigned
PORTC[5]	Not assigned	UART0_RX	Not assigned
PORTC[6]	Not assigned	Not assigned	Not assigned
PORTC[7]	Not assigned	SPI1_SSn1	Not assigned
PORTC[8]	Not assigned	SPI1_SSn0	Not assigned
PORTC[9]	Not assigned	SPI1_SCK	Not assigned
PORTC[10]	Not assigned	SPI1_MISO	Not assigned
PORTC[11]	Not assigned	SPI1_MOSI	Not assigned
PORTC[12]	Not assigned	Not assigned	Not assigned
PORTC[14]	Not assigned	UART2_TX	Not assigned
PORTD[10]	Not assigned	TIM[10]	UART1_CTSn
PORTD[11]	Not assigned	TIM[11]	UART1_TX
PORTD[12]	Not assigned	TIM[12]	UART1_RX
PORTD[13]	Not assigned	TIM[13]	Not assigned
PORTD[14]	Not assigned	TIM[14]	Not assigned
PORTD[15]	Not assigned	TIM[15]	Not assigned
PORTE[0]	Not assigned	TIM[16]	UART0_RTSn
PORTE[1]	Not assigned	TIM[17]	UART0_CTSn
PORTE[2]	Not assigned	TIM[18]	UART0_TX
PORTE[3]	Not assigned	TIM[19]	UART0_RX

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTE[4]	Not assigned	TIM[20]	Not assigned
PORTE[5]	Not assigned	TIM[21]	SPI1_SSn7
PORTE[6]	Not assigned	TIM[22]	SPI1_SSn6
PORTE[7]	Not assigned	TIM[23]	SPI1_SSn5
PORTE[8]	Not assigned	SPI1_SSn4	TIM[16]
PORTE[9]	Not assigned	SPI1_SSn3	TIM[17]
PORTE[12]	Not assigned	SPI1_SSn0	TIM[20]
PORTE[13]	Not assigned	SPI1_SCK	TIM[21]
PORTE[14]	Not assigned	SPI1_MISO	TIM[22]
PORTE[15]	Not assigned	SPI1_MOSI	TIM[23]
PORTF[0]	Not assigned	SPI2_SSn4	TIM[0]
PORTF[1]	Not assigned	SPI2_SSn3	TIM[1]
PORTF[9]	UART2_RX	Not assigned	TIM[9]
PORTF[11]	UART1_CTSn	Not assigned	TIM[11]
PORTF[12]	UART1_TX	Not assigned	TIM[12]
PORTF[13]	UART1_RX	TIM[19]	Not assigned
PORTF[14]	UART0_RTSn	TIM[20]	Not assigned
PORTF[15]	UART0_CTSn	TIM[21]	Not assigned
PORTG[0]	UART0_TX	TIM[22]	Not assigned
PORTG[1]	UART0_RX	TIM[23]	Not assigned
PORTG[2]	TIM[9]	SPI1_SSn0	Not assigned
PORTG[3]	TIM[10]	SPI1_SCK	Not assigned
PORTG[4]	SPI1_SSn3	SPI1_MISO	Not assigned
PORTG[5]	SPI1_SSn2	Not assigned	Not assigned
PORTG[6]	SPI1_SSn1	TIM[12]	Not assigned
PORTG[7]	Not assigned	Not assigned	Not assigned

2.4 196-Ball PBGA Ball Mapping

VA41628 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PF15	NC	NC	NC	NC	NC	SDA0	PG01	PG05	NC	XTALp	NC	NC	A3V3
B	PF11	PF14	NC	NC	NC	SCL0	PG00	PG04	NMI	XTALn	A3V3	NC	NC	NC
C	TRST	TDO	PF13	NC	3V3	VSS	PG03	PG07	E1V5	A1V5	NC	NC	NC	ATOUT
D	NC	TMS	TCK	PF12	NC	PG02	PG06	RSTn	VDDQ	NC	NC	PA03	PA01	PA00
E	NC	NC	NC	TDI	1V5	VSS	3V3	1V5	VSS	3V3	PA09	PA06	PA04	PA02
F	SCK	NC	NC	PF09	VSS	VSS	3V3	1V5	VSS	VSS	PA13	PA10	PA07	PA05
G	PF01	CSn	MOSI	NC	1V5	1V5	VSS	VSS	3V3	3V3	PB01	PA14	PA11	PA08
H	PE13	PF00	F_SO	MISO	3V3	3V3	VSS	VSS	1V5	1V5	PB04	NC	PA15	PA12
J	VSS	WPn	PE15	NC	VSS	VSS	1V5	3V3	VSS	VSS	NC	NC	PB02	PB00
K	NC	PE12	TEST	PE14	3V3	VSS	1V5	3V3	VSS	1V5	PB12	NC	NC	PB03
L	PE08	PE09	NC	PE01	PD13	NC	NC	NC	NC	PC10	PC00	PB13	NC	NC
M	PE06	PE07	PE02	PD14	PD10	NC	NC	PC14	NC	PC07	PC04	SDA1	PB14	NC
N	PE05	PE03	PD15	PD11	NC	NC	NC	PC11	PC08	PC05	PC02	SCL2	SCL1	PB15
P	PE04	PE00	PD12	NC	NC	NC	PC12	PC09	PC06	PC03	PC01	SDA2	NC	VSS

2.5 Ball Descriptions

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
A01	PF15	PORTF[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
A02	NC	No connect
A03	NC	No connect
A04	NC	No connect
A05	NC	No connect
A06	NC	No connect
A07	SDA0	I^2C0 Data
A08	PG01	PORTG[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
A09	PG05	PORTG[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
A10	NC	No connect
A11	XTALp	Crystal Oscillator Output
A12	NC	No connect
A13	NC	No connect
A14	A3V3	3.3 V Analog IO power
B01	PF11	PORTF[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B02	PF14	PORTF[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B03	NC	No connect
B04	NC	No connect
B05	NC	No connect
B06	SCL0	I^2C0 Clock
B07	PG00	PORTG[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B08	PG04	PORTG[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
B09	NMI	Non-maskable Interrupt – active high

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
B10	XTALn	Crystal Oscillator Input
B11	A3V3	3.3 V Analog IO power
B12	NC	No connect
B13	NC	No connect
B14	NC	No connect
C01	TRST	Test Reset, active low
C02	TDO	Test Data Out
C03	PF13	PORTF[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
C04	NC	No connect
C05	3V3	3.3 V power
C06	VSS	Tie to ground
C07	PG03	PORTG[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
C08	PG07	PORTG[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
C09	E1V5	When high, this signal disables the internal 1.5 V regulator, and 1.5 V must be applied externally to all 1V5 pins and A1V5.
C10	A1V5	1.5 V Analog power (must be supplied externally)
C11	NC	No connect
C12	NC	No connect
C13	NC	No connect
C14	ATOUT	For factory use only. Must be pulled to VSS
D01	NC	No connect
D02	TMS	Test Mode Select/Serial Wire Debug Data IO
D03	TCK	Test Clock/Serial Wire Debug Clock
D04	PF12	PORTF[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D05	NC	No connect
D06	PG02	PORTG[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D07	PG06	PORTG[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D08	RSTn	External System Reset, active low. Resets the processor and all peripherals. This signal is internally synchronized before being used. Any reset will cause this pin to pull low during the reset sequence.
D09	VDDQ	For factory use only. Must be tied to VSS
D10	NC	No connect
D11	NC	No connect

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
D12	PA03	PORTA[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D13	PA01	PORTA[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
D14	PA00	PORTA[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E01	NC	No connect
E02	NC	No connect
E03	NC	No connect
E04	TDI	Test Data In
E05	1V5	1.5 V power (must be supplied externally)
E06	VSS	Ground
E07	3V3	3.3 V power
E08	1V5	1.5 V power (must be supplied externally)
E09	VSS	Ground
E10	3V3	3.3 V power
E11	PA09	PORTA[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E12	PA06	PORTA[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E13	PA04	PORTA[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
E14	PA02	PORTA[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F01	SCK	SPI Clock to Boot ROM.
F02	NC	No connect
F03	NC	No connect
F04	PF09	PORTF[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F05	VSS	Ground
F06	VSS	Ground
F07	3V3	3.3 V power
F08	1V5	1.5 V power (must be supplied externally)
F09	VSS	Ground
F10	VSS	Ground
F11	PA13	PORTA[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F12	PA10	PORTA[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
F13	PA07	PORTA[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
F14	PA05	PORTA[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G01	PF01	PORTF[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G02	CSn	SPI Chip Select to Boot ROM (Active Low).
G03	MOSI	SPI Data Out to Boot ROM.
G04	NC	No connect
G05	1V5	1.5 V power (must be supplied externally)
G06	1V5	1.5 V power (must be supplied externally)
G07	VSS	Ground
G08	VSS	Ground
G09	3V3	3.3 V power
G10	3V3	3.3 V power
G11	PB01	PORTB[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G12	PA14	PORTA[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G13	PA11	PORTA[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
G14	PA08	PORTA[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H01	PE13	PORTE[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H02	PF00	PORTF[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H03	F_SO	Must be tied to H03
H04	MISO	Must be tied to H04
H05	3V3	3.3 V power
H06	3V3	3.3 V power
H07	VSS	Ground
H08	VSS	Ground
H09	1V5	1.5 V power (must be supplied externally)
H10	1V5	1.5 V power (must be supplied externally)
H11	PB04	PORTB[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
H12	NC	No connect
H13	PA15	PORTA[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
H14	PA12	PORTA[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J01	VSS	Factory test only. Must be tied to ground.
J02	WPn	Tie to 3.3V power.
J03	PE15	PORTE[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J04	NC	No connect
J05	VSS	Ground
J06	VSS	Ground
J07	1V5	1.5 V power (must be supplied externally)
J08	3V3	3.3 V power
J09	VSS	Ground
J10	VSS	Ground
J11	NC	No connect
J12	NC	No connect
J13	PB02	PORTB[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
J14	PB00	PORTB[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K01	NC	No connect
K02	PE12	PORTE[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K03	TEST	For factory use only. Must be tied to ground with a 10k resistor.
K04	PE14	PORTE[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K05	3V3	3.3 V power
K06	VSS	Ground
K07	1V5	1.5 V power (must be supplied externally)
K08	3V3	3.3 V power
K09	VSS	Ground
K10	1V5	1.5 V power (must be supplied externally)
K11	PB12	PORTB[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
K12	NC	No connect
K13	NC	No connect
K14	PB03	PORTB[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L01	PE08	PORTE[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
L02	PE09	PORTE[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L03	NC	No connect
L04	PE01	PORTE[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L05	PD13	PORTD[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L06	NC	No connect
L07	NC	No connect
L08	NC	No connect
L09	NC	No connect
L10	PC10	PORTC[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L11	PC00	PORTC[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L12	PB13	PORTB[13] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
L13	NC	No connect
L14	NC	No connect
M01	PE06	PORTE[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M02	PE07	PORTE[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M03	PE02	PORTE[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M04	PD14	PORTD[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M05	PD10	PORTD[10] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M06	NC	No connect
M07	NC	No connect
M08	PC14	PORTC[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M09	NC	No connect
M10	PC07	PORTC[7] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M11	PC04	PORTC[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M12	SDA1	I^2C1 Data

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
M13	PB14	PORTB[14] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
M14	NC	No connect
N01	PE05	PORTE[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N02	PE03	PORTE[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N03	PD15	PORTD[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N04	PD11	PORTD[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N05	NC	No connect
N06	NC	No connect
N07	NC	No connect
N08	PC11	PORTC[11] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N09	PC08	PORTC[8] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N10	PC05	PORTC[5] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N11	PC02	PORTC[2] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
N12	SCL2	I^2C2 Clock
N13	SCL1	I^2C1 Clock
N14	PB15	PORTB[15] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P01	PE04	PORTE[4] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P02	PE00	PORTE[0] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P03	PD12	PORTD[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P04	NC	No connect
P05	NC	No connect
P06	NC	No connect
P07	PC12	PORTC[12] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P08	PC09	PORTC[9] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.

PBGA Ball #	PBGA Ball Name	PBGA Ball Description
P09	PC06	PORTC[6] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P10	PC03	PORTC[3] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P11	PC01	PORTC[1] Software configurable general-purpose I/O. Software configurable for direction, interrupt sources, and counter/timer triggers.
P12	SDA2	I^2C2 Data
P13	NC	No connect
P14	VSS	Tie to ground.

3 Peripheral Summary

3.1 Serial Peripheral Interface (SPI)

The VA41628 contains three general purpose Serial Peripheral Interface (SPI) blocks. A fourth SPI is dedicated to the boot memory and uses a dedicated set of pins. The other three use pins shared with various GPIOs. Please refer to the VA416XX Programmer's Guide for more information about the SPI usage.
The SPI peripheral supports the following features:

- Master mode
- Slave mode
- Buffered RX/TX operation with dual four entry FIFOs
- Serial clock (SCK) with programmable polarity (SPO) and phase (SPH)
- SPI0 has up to 3 chip selects
- SPI1 has up to 8 chip selects
- SPI2 has up to 7 chip selects
- SPI3 is Master only and shares its pins with the SPI ROM pins (ROM_SCK, ROM_MOSI, ROM_MISO, ROM_SS)
- Interrupt conditions:
    - TX FIFO is at least half empty (TXIM)
    - RX FIFO is at least half full (RXIM)
    - RX Timeout (RTIM)
    - RX FIFO overrun (RORIM)

3.2 Universal Asynchronous Receiver/Transmitter (UART)

The VA41628 contains three Universal Asynchronous Receiver/Transmitter (UART) interface blocks with an independent Transmit and Receive section, each with a 16-byte FIFO. The UART pins are shared with various GPIO pins. Please refer to the VA416XX Programmer's Guide for more information about the UART usage.
The UART peripheral supports the following features:

- Selectable even, odd or no parity
- Selectable one or two stop bits
- Word sizes from 5 to 8 bits
- 9-bit address mode
- Baud rates from 300 to 115,200 bps (or up to 2 Mbps)

- 16-byte RX and TX FIFO
- Detection of Framing, Parity and Overrun errors
- Full Duplex or Half Duplex operation
- Break signal generation and detection
- Interrupt conditions:
  - Receive FIFO at least half full (IRQ_RX)
  - Receive FIFO overflow, receive frame error, receive parity error, or receive break condition (IRQ_RX_STATUS)
  - Receive timeout (IRQ_RX_TO)
  - Transmit FIFO at least half empty (IRQ_TX)
  - Transmit FIFO overflow (IRQ_TX_STATUS)
  - Transmit FIFO empty (IRQ_TX_EMPTY)
  - Transmitter interrupt when CTSn changes value (IRQ_TX_CTS)

3.3 Inter-Integrated Circuit (I^2C)

The VA41628 contains three Inter-Integrated Circuit (I^2C) interface blocks. Please refer to the VA416XX Programmer's Guide for more information about I^2C usage.
The I^2C peripheral supports the following features:

- Standard I^2C-compliant bus interface
- Configurable as Master or Slave
- Dedicated open-drain pins
- 16-word FIFO for both transmit and receive
- Programmable clock rate for standard 100 kHz mode or 400 kHz mode
- Interrupt conditions:
  - TX FIFO ready (TXREADY)
  - TX FIFO empty (TXEMPTY)
  - TX FIFO overflow (TXOVERFLOW)
  - RX FIFO full (RXFULL)
  - RX FIFO ready (RXREADY)
  - RX FIFO overflow (RXOVERFLOW)
  - Clock low timeout (CLKLOTO)
  - I^2C Status (STATUS)

3.4 General Purpose 4-Channel DMA

The VA41628 supports a single DMA interface to allow the MCU to transfer data from a peripheral to memory or memory to peripheral, independent of the Arm® CPU. Please refer to the VA416XX Programmer's Guide for more information about DMA usage.
The DMA controller implements the following features:

- Each DMA channel has dedicated handshake signals
- Each DMA channel has a programmable priority level
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel
- Support for multiple transfer types:
    - Memory-to-memory
    - Memory-to-peripheral
    - Peripheral-to-memory
- Support for multiple DMA transfer data widths
- The number of transfers in a single DMA cycle is programmable from 1 to 1024

A typical use case for the DMA is listed below:

- SPI/UART emptying own FIFO into RAM buffer or vice versa

3.5 Timers/Counters (TIM)

The VA41628 contains 24 general-purpose Timer/Counter interface blocks. These can be configured as timers or event counters. They can be free-running or triggered by system events. Timer pins are shared with various GPIO pins. Please refer to the VA416XX Programmer's Guide for more information about Timers usage.

Timer feature summary

- Advanced trigger modes
    - Start/Stop based on other Counter/Timers or GPIO signals
    - Multiple trigger sources
- Configurable output event
    - One cycle zero detect when timer equal to zero is detected
    - Active mode
    - Divide by two for square wave generation
      Two PWM modes: Single edge and double edge detection

3.6 General-Purpose Input/Output Ports (GPIO)

The VA41628 contains seven GPIO banks providing a total of 75 GPIO pins. GPIO pins can be configured as inputs or outputs. Please refer to the VA416XX Programmer's Guide for more information about GPIO usage.

- PORTA[15:0]
- PORTB[15:12, 4:0]
- PORTC[14,12:0]
- PORTD[15:10]
- PORTE[15:12, 9:0]
- PORTF[15:11, 9, 1:0]
- PORTG[7:0]
- Interrupt capability on Ports A to F
- Selectable edge or level interrupts
- Programmable pull-up or pull-down resistors
- Programmable output inversion
- Selectable input filtering
- Pseudo open-drain capability
- Alternative functions available on many GPIO pins

3.7 True Random Number Generator (TRNG)

The Arm® TrustZone TRNG offers these two components:

- The TRNG that conforms to the following standards and drafts:
  - NIST SP800-90B
  - NIST SP800-22
  - FIPS 140-2
  - BSI AIS-31
- A software-implemented Deterministic Random Bit Generator (DRBG) which follows NIST SP 800-90A (making the entire RNG flow SP 800-90C compliant)

For more detailed information, see the Arm® TrustZone True Random Number Generator, Technical Reference Manual.

3.8 Debug and Programming Interface (DBG)

ARM's Serial Wire Debug (SWD) replaces the traditional 5-pin JTAG debug interface by introducing a 2-pin interface with a clock (SWDCLK) and a single bi-directional data pin (SWDIO), providing all the normal JTAG debug and test functionality, although daisy-chaining devices as via JTAG is not possible. SWDIO and SWCLK are overlaid on the TMS and TCK pins, allowing the same connector to be used for JTAG and SWD (JTAG is not supported in user mode for VA41628). To communicate with a device via SWD, data is sent on SWDIO, synchronous to the SWCLK. With every rising edge of SWCLK, one bit of data is transmitted or received on the SWDIO pin.

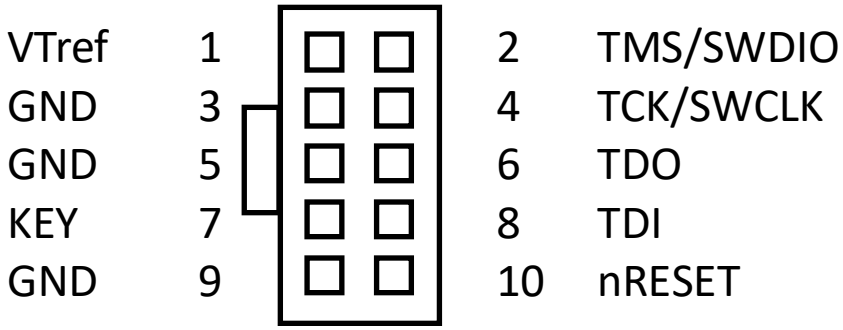
SWD Pins

Pin	Type	Explanation
SWCLK	Input	The clock signal to the target CPU. This pin is recommended to be pulled to a defined state on the target board.
SWDIO	I/O	Bi-directional data pin. This pin should be pulled up on the target board.

JTAG/SWD Pod Signal	Purpose	Connects to:
VTref	This is the target reference voltage. It is used to check if the target board has power.	It is normally fed from VDD of the target board and must not have a series resistor.
GND	Target ground.	MCU VSS.
KEY	Physical key to aid in cable placement.	No electrical connection.
GND	Debugger ground detect.	MCU VSS.
TMS/SWDIO	SWDIO is bi-directional data line.	MCU pin TMS/SWDIO. Use 10K Ohm pull-up resistor to VDD33.
TCK/SWCLK	Test Clock pin	MCU pin TCK/SWCLK. Use a 10k pull-down resistor to GND.

TDO	Test Data Output pin	MCU pin TDO. Not used with SWD and may be left floating.
TDI	Test Data Input pin	MCU pin TDI. Not used with SWD. Use at 10k pull-up resistor to VDD33
nRESET	Reset pin	MCU pin EXTRESETn. Connected to active low EXTRESETn input pin of the MCU so the debugger can reset the MCU.

The most common interface connector is a Samtec 10-pin: FTSH-105-01-L-DV-007-K connector. Shown below is the pinout.



4 DC Electrical Characteristics

4.1 Absolute Maximum Ratings

Symbol	Rating	Hi-Rel	Unit
V_{DD33}	DC supply voltage (I/O)	-0.3 to 3.8	V
V_{DD15}	DC supply voltage (core)	-0.3 to 1.8	V
A_V_{DD33}	DC supply voltage (analog)	-0.3 to 3.8	V
A_V_{DD15}	DC supply voltage (analog)	-0.3 to 1.8	V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8	V
T_{CASE}	Operating temperature	-55 to 125	°C
T_{BIAS}	Temperature under bias	-55 to 125	°C
T_{STG}	Storage temperature	-55 to 125	°C

4.2 Recommended Supply Conditions

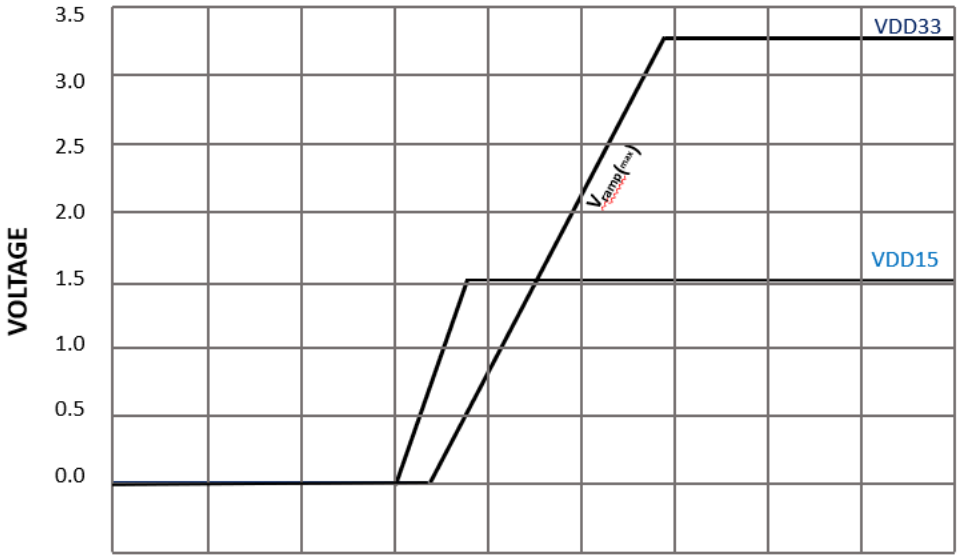
Symbol	Parameter	Min	Typ	Max	Unit
V_{DD33}	I/O supply voltage	3.0	3.3	3.6	V
V_{DD15}	Core supply voltage (must be supplied externally)	1.35	1.5	1.65	V
A_V_{DD33}	Analog supply voltage	3.0	3.3	3.6	V
A_V_{DD15}	Analog supply voltage (must be supplied externally)	1.35	1.5	1.65	V
V_{SS}	Ground	-	0	-	V
V_{ramp}	V_{DD33} voltage ramp rate[1,4]	0.5 V/ms	-	100 V/µs	-
V_{PROFF}	V_{DD33} level at which the Power-on reset is released when voltage is rising[2]	2.65	2.8	2.95	V
V_{PRON}	V_{DD33} level at which the Power-on reset is activated when voltage is falling[3]	-	2.7	-	V

Notes:

1. V_{Ramp} time is the time from V_{DD} at 0 V until it reaches the operating range.
2. V_{PROFF} is the voltage at which the internal Power-on reset is released when power is rising.
3. V_{PRON} is the voltage at which the internal Power-on reset is activated.
4. See additional requirements for VDD15/VDD33 power supply relationship in the graph below.

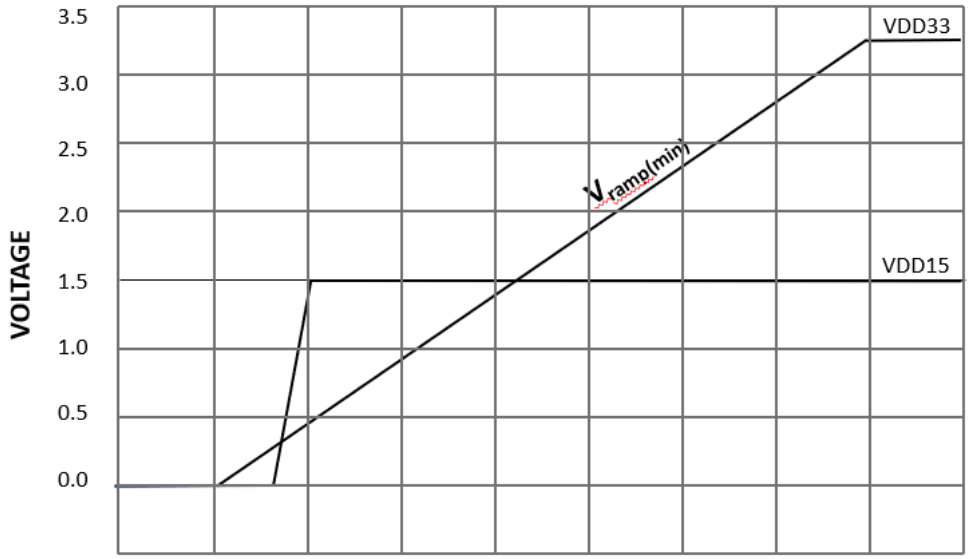
4.3 Required Power Supply Sequencing

For reliable boot operation, the VDD15 ramp must be faster than the VDD33 ramp to ensure that VDD33 is less than VDD15 until VDD15 reaches 1.5V.



Power sequencing for case of maximum VDD33 ramp.

To meet this requirement, the ramp rate of the VDD33 can be adjusted to slow the rise of the VDD33 relative to VDD15. This is shown in the figure below.



Power sequencing for case of minimum VDD33 ramp.

4.4 DC Current Consumption

Core Supply Current (VDD15)

The typical core supply current is approximately 1.2mA/MHz.

System clock frequency (MHz)[1]	Min	Typ[2]	Max[3]	Units
10	-	20	-	mA
20	-	35	-	mA
50	-	65	-	mA

Notes:

1. Maximum activity is measured with all internal counters running at the maximum rate, all I^2C interfaces active in Fast mode and loopback mode, all SPI interfaces active in master mode at 16x clock divide rate, all UARTs active in loopback mode at 1MHz Baud rate, and the CPU running multiply operations.
2. Measured at nominal VDD and 25C.
3. Measured at maximum VDD and 125C.

I/O Supply Current[1] (V_{DD33}) I_{DD33}

Run I_{DD}[1]	Max	Units
Overall maximum I/O current	200	mA
Maximum I/O current per side of the device	100	mA

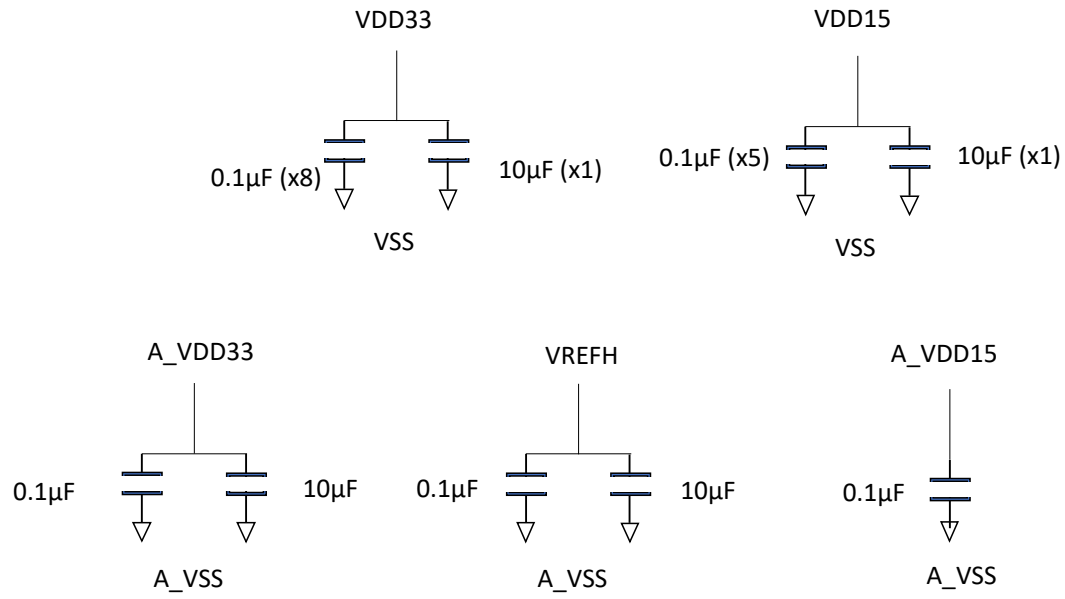
Notes:

1. Although each GPIO can source or sink up to 8mA, the maximum current allowed per package side of the device is 100mA. The maximum allowable current into VDD33 (I_{DD33}) is 200mA. I/O supply current is entirely application dependent. It is the sum of all the GPIO outputs switching, the switching frequency of those out outputs, and the capacitive loading on each pin.

4.5 Power Supply Decoupling

Each power supply pair (VDD33/VSS, VDD15/VSS, A_VDD33/A_VSS, A_VDD15/A_VSS) and VREFH must be decoupled with filtering ceramic capacitors, as shown. These capacitors must be placed as close as possible to the corresponding supply pins to ensure proper operation of the MCU. Capacitors can also be placed on the bottom side of a PC board for convenience.

Digital and Analog Supplies



4.6 Electrostatic Discharge (ESD)

ESD testing is done in conformance with MIL-PRF-38534 and applies to all pads.

Parameter	Test Conditions	Value	Unit
ESD for Human Body Model (HBM)	All pins	2000	V
ESD for field-induced Charged Device Model (CDM)	All pins	500	V

4.7 General Purpose I/O

Input/Output and Input-Only Pads

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IL}	Input Low Voltage	VDD33=Max	-0.3	-	0.3 x V_{DD33}	V
V_{IH}	Input High Voltage	VDD33=Max	0.7 x V_{DD33}	-	V_{DD33} + 0.3	V
V_{hys}[2]	Hysteresis of Schmitt trigger	VDD33=Max	-	450	-	mV

Notes:

1. Typ for –55° to 125°C measured at 25°C
2. The following input buffers have Schmitt Trigger Inputs: TCK, TRSTn, TDI, TMS, ROM_MISO, NVM_PROTn, TEST_MODE, NMI, CAN0_RX, CAN1_RX, EBI_BOOT, and all GPIO

Input/Output and Output-Only Pads

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{OL}	Output voltage (Low)	Load I = 8 mA V_{DD33} = Min	-	0.25	0.4	V
V_{OH}	Output voltage (High)	Load I = -8 mA V_{DD33} = Min	0.8 x V_{DD33}	3.0	-	V

Notes:

1. Typ for –55° to 125°C measured at 25°C

Leakage Current Input/Output and Input-Only Pads (At Temperature –55 to 125°C).

See Pin Descriptions in Section 3 for more information.

Symbol	Parameter	Pins	Test Condition	Min	Typ[1]	Max
I_{in}	Input leakage current (V_{in} low)	Pins with configurable pull-up or pull-down	V_{in} = 0 V	-1 µA	10 nA	-
		Pins with internal pull-down always enabled	V_{in} = 0 V	-65 µA	-50 µA	-
		Tri-state Pins	V_{in} = 0 V	-1 µA	10 nA	-

Symbol	Parameter	Pins	Test Condition	Min	Typ[1]	Max
	Input leakage current (V_{in} high)	Pins with configurable pull-up or pull-down	$V_{in} = V_{DD33}$	-	10 nA	1µA
		Pins with internal pull-down always enabled	$V_{in} = V_{DD33}$	-	10 nA	1µA
		Tri-state Pins	$V_{in} = V_{DD33}$	-	10 nA	1 µA

Notes:

1. TYP for -55° to 125°C measured at 25°C

Open Drain I²C Pads

Open Drain I²C pad specifications apply to pads: I2Cx_SCL, I2Cx_SDA.

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IL}	Input low voltage		-0.3		0.3 x $V_{DD33MAX}$	V
V_{IH}	Input high voltage		0.7 x $V_{DD33MIN}$		V_{DD33} + 0.3	V
V_{hys}	Hysteresis of Schmitt trigger		-	450	-	mV
I_{in}	Input leakage current (high)	$V_{in} = V_{DD33}$	-1 µA	10 nA	1 µA	
V_{OL}	Output voltage (low)	Load I = -8 mA, V_{DD33} = Min	-	0.25	0.4	V

Notes:

1. Typ for –55° to 125°C measured at 25°C

4.8 Low-Voltage Detect Circuit

Refer to the VA416XX Programmer's Guide for more information.

Low-Voltage Detect Level	LVL_SLCT[1] Value	Min	Typ[2]	Max	Units
Low-voltage detect rising	-	2.85	2.9	2.95	V
Low-voltage detect falling	00	2.75	2.8	2.85	V
	01	-	2.9	-	V
	10	-	3.0	-	V
	11	-	3.1	-	V

Notes:

1. LVL_ SLCT is set to the lowest possible setting on power-up to keep the low voltage detect circuit from resetting the device.
2. Typ for –55° to 125°C measured at 25°C

4.9 Internal Pull-up/Pull-down Resistors

Pull direction	Min	Typ	Max	Units
Pull-up[1]	45	55	65	kΩ
Pull-down[2]	45	55	65	kΩ

Notes:

1. Pins with dedicated Pull-ups: EXTRESETn
2. Pins with dedicated Pull-downs: ROM_MISO, TMS

4.10 Pin Capacitance

Symbol	Parameter[4]	Conditions	Max	Unit
C_{IN}[1]	Input pin capacitance	V_{in} = 3.3 V	6	pF
$C_{I/O}$[2]	I/O pin capacitance	V_{out} = 3.3 V	10	pF
C_{PD}[3]	Open drain pin capacitance	V_{out} = 0V	10	pF

Notes:

1. Input only pins: XTAL_N, ROM_MISO, TCK, TRSTn, TDI, NMI, EBI_BOOT, EXT15_SEL
2. Bidirectional pins: PORTA, PORTB, PORTC, PORTD, PORTE, PORTF, PORTG, TMS/SWDIO, EXTRESETn
3. Open-drain pins: I2Cx_SCL, I2Cx_SDA
4. This is an internal circuit and is guaranteed by design.

5 AC Electrical Characteristics

5.1 AC Timing Conditions

V_{DD33}	3.3 V ± 0.3 V
Input swing levels	0 to 3.3 V
Input rise/fall times[1]	4 ns[1]
Input timing reference levels	1.65 V
Output timing reference levels	1.65 V
AC test load	15 pF

Notes:

1. Rise/Fall times are measured from 20% to 80% of V_{DD33}

5.2 Internal 20MHz Oscillator

The internal 20MHz oscillator is used for boot and Power-Up delay timing. If the system clock drops below 1MHz, the system clock will automatically switch over to the internal 20MHz oscillator as a system fail-safe mechanism.

Parameter	Description	Min	Typ	Max	Unit
t_{CYC}	Clock cycle time	40	50	66.7	ns
t_{FREQ}	Clock frequency	15	20	25	MHz
-	Cycle time accuracy	-25	-	25	%

5.3 Clock Signals

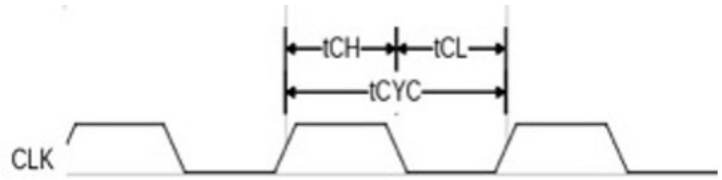
The VA41628 can be clocked in several different ways.

- Internal oscillator
- 4 to 10MHz external crystal oscillator with PLL or without PLL enabled
- 4 to 50MHz external square wave with PLL enabled
- Up to 50MHz external square wave without PLL enabled

External Clock Signal

An external clock can be used to drive the XTAL_N input with the XTAL_P pin left unconnected. The clock signal must adhere to the following table.

Parameter	Description	Time	Unit
t_{CYC}	Clock cycle time (min)	10	ns
t_{CH}	Clock high (min)	4	ns
t_{CL}	Clock low (min)	4	ns



External Crystal Oscillator

If an external crystal oscillator circuit is used, please refer to the crystal oscillator manufacturer's data sheet for exact values of resistors and capacitors for proper oscillation at the fundamental frequency, reliable start-up, and to maximize stability.

Parameter	Description	Min	Typ	Max	Unit
f_{XTAL}	Crystal frequency	4	-	10	MHz
R_F	Feedback resistor	-	1M	-	Ω
R_S	Series resistor	1k	-	20k	Ω
t_S	Start-up time	-	10	15	ms

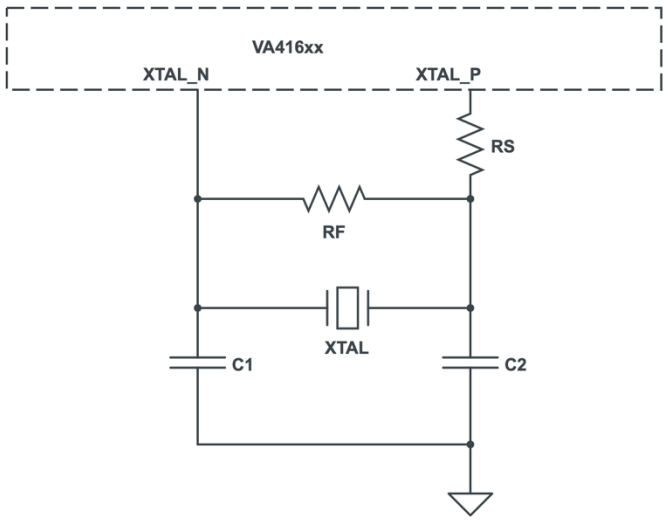
Note:

PC board trace lengths for the oscillator circuit should be as short as possible

Example External Crystal Oscillator Circuit

If an external crystal oscillator circuit is used, please refer to the crystal oscillator manufacturer's data sheet for exact values of resistors and capacitors for proper oscillation at the fundamental frequency, reliable startup, and to maximize stability.

External Oscillator



5.4 Phased Locked Loop (PLL)

The VA41628 contains an internal PLL circuit that can be used to generate internal frequencies higher than the input clock (either driven by an external clock or an external crystal oscillator). The PLL clock can be used as the MCU system clock. Please refer to the VA416XX Programmer's Guide for more information on the usage of the PLL.

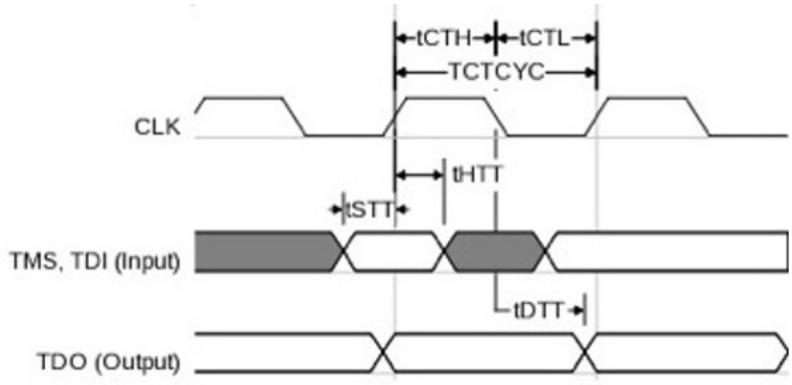
Parameter	Description	Typ	Max	Unit
f_{in}	Input frequency	4	50	MHz
f_{out}	Output frequency	50	-	MHz
t_{LOCK}	PLL lock time	10	100	µs
Jitter	PLL clock jitter (percentage of input frequency)	3	-	%
t_{CL}	Clock low (min)	4	-	ns

Note: Guaranteed by design

5.5 Serial Wire Debug (SWD)

The Serial Wire Debug interface allows access to the Arm® Debug Access Port (DAP). The TMS/SWDIO pin is bi-directional data, and the TCK/SWCLK pin is a clock input to the VA41628.

Parameter	Description	Typ	Unit
t_{CTCYC}	TCK/SWCLK cycle time (min)	60	ns
t_{CTH}	TCK/SWCLK high (min)	20	ns
t_{CTL}	TCK/SWCLK low (min)	20	ns
t_{DTT}	SWDIO/TDO output change from TCK/SWCLK fall	9	ns
t_{STT}	TMS/SWDIO and TDI setup time to TCK/SWCLK rise	2.0	ns
t_{HTT}	TMS/SWDIO and TDI hold time to TCK/SWCLK rise	6.0	ns



6 Radiation Hardened Performance Targets

Parameter	Description	Min	Typ	Max	Unit
TID	Total ionizing dose	-	-	300	krad(Si)
SER	Soft error rate (EDAC & Scrub[1] enabled)	-	1E-15	-	error bit per day[2]
SEL	Linear energy transfer (latch-up immunity)	110	-	-	MeV * cm^2 / mg

Notes:

1. Running at an appropriate frequency to prevent the accumulation of errors in the memory to achieve consistently low SER over time.
2. In geosynchronous orbit, solar min, and 100 mils of aluminum shielding.

7 Thermal Resistance Characteristics

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

196- pin BGA package thermal resistance data

Thermal Parameter	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1,2]	Four-layer board (2s2p); Still air	θ_{JA}	18.74	°C/W
	Four-layer board (2s2p); air flow 1 m/s	θ_{JA}	16.72	°C/W
	Four-layer board (2s2p); air flow 2 m/s	θ_{JA}	15.95	°C/W
Junction to Case[3,4]	–	θ_{JC}	6.49	°C/W
Junction to Board[5]	–	θ_{JB}	8.17	°C/W

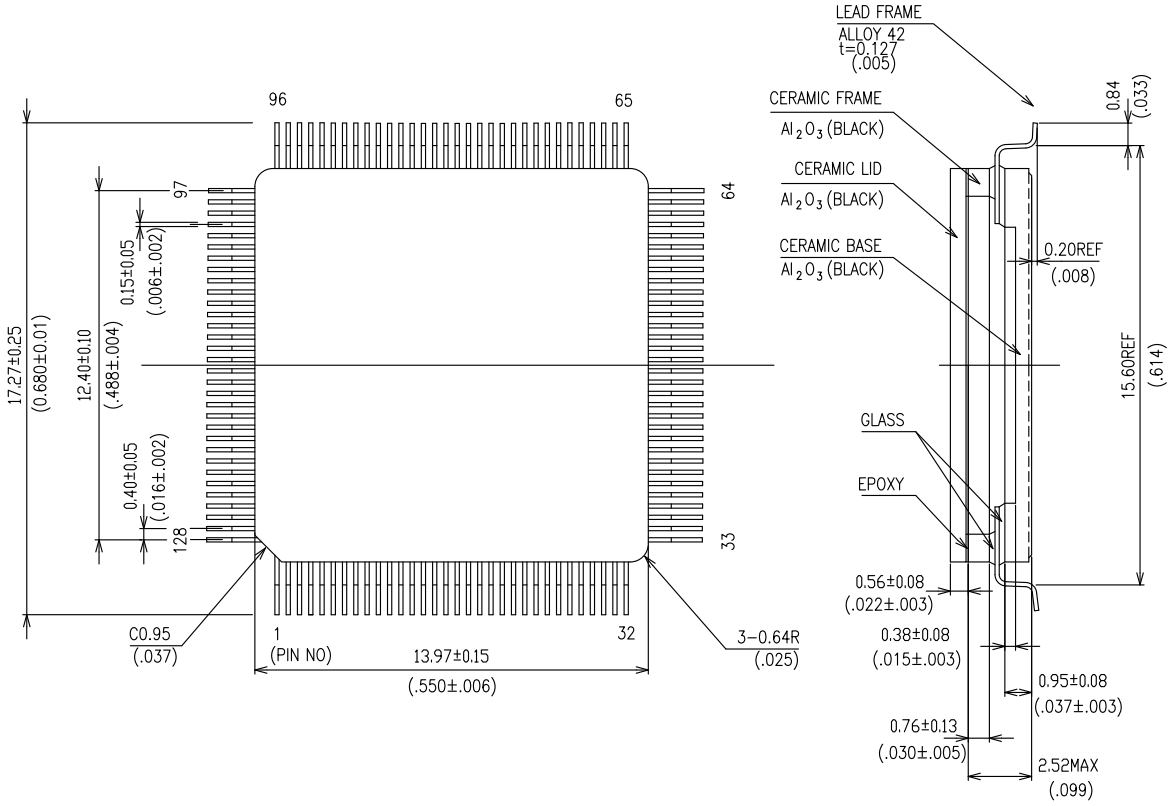
Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. The simulation models are setup following the EIA/JESD51-2 for still air condition and following the EIA/JESD51-6 for moving air condition. The package is placed with horizontal orientation.
3. The model and boundary condition intend to simulate the θ_{JC} test conditions. A cold plate and the grease between package and cold plate are modeled.
4. θ_{JC} represents the thermal resistance between the chip to package top case.
5. The model and boundary conditions intend to simulate the test conditions specified in EIA/JESD51-8.

8 Package Mechanical Information

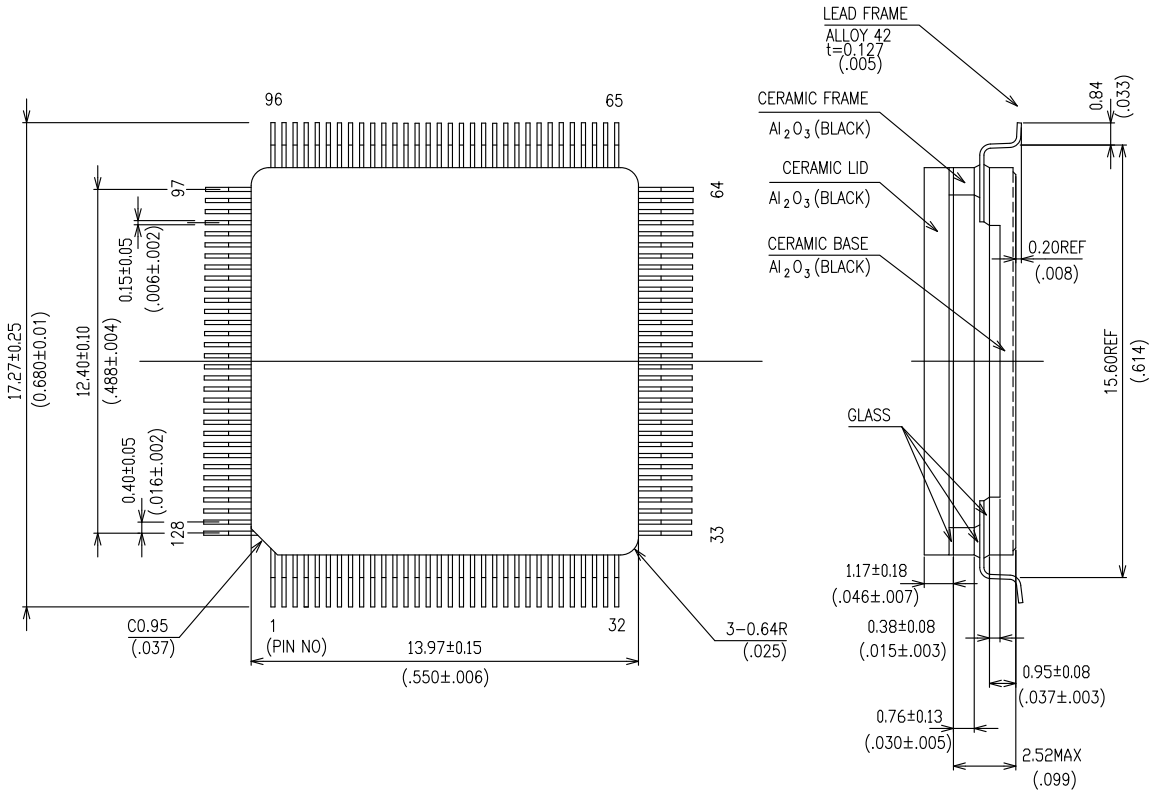
8.1 128-Pin Ceramic LQFP – Rev A

Rev A: Au-plated leads with epoxy lids, plating is Au 1.5um MIN.

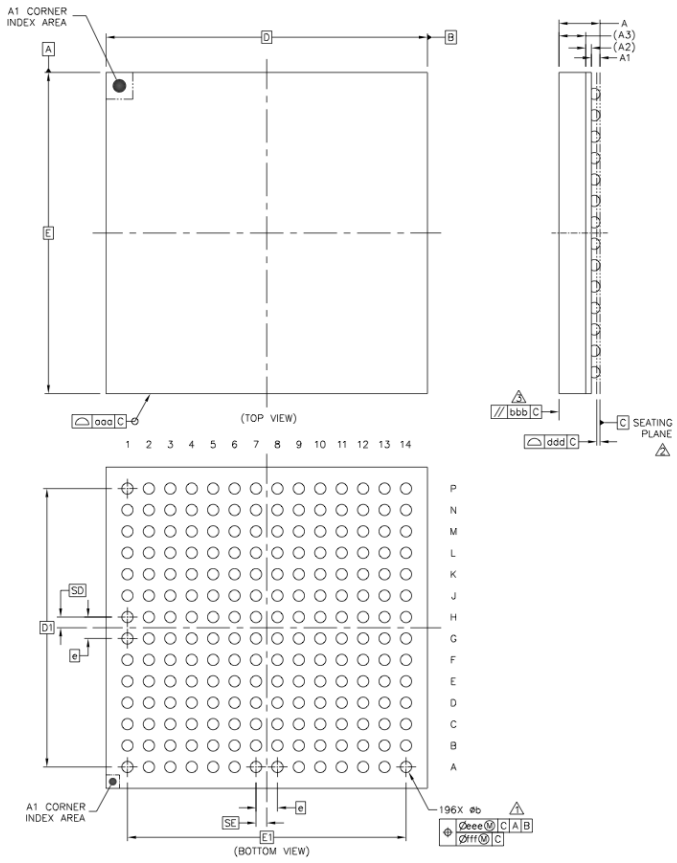


8.2 128-Pin Ceramic LQFP – Rev B

Rev B: Al-plated leads with glass lids, plating is Al 2.5um MIN target 4um.



8.3 196-Ball Plastic BGA



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.7
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		1	REF
BODY SIZE	D		12	BSC
	E		12	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.3	
BALL WIDTH	b	0.37	---	0.47
BALL PITCH	e		0.8	BSC
BALL COUNT	n		196	
EDGE BALL CENTER TO CENTER	D1		10.4	BSC
	E1		10.4	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.12	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

8.4 Package Pin Metallization

Package	Material
128-pin ceramic w/ Au-plated leads, epoxy lids	99.9% Gold
128-pin ceramic w/ Al-plated leads, glass lids	63% Tin / 37% Lead
196-pin BGA	63% Tin / 37% Lead

9 Ordering Information

Part Number	Package	Qualification
VA41628-CQ128F0PBA	Ceramic 128 QFP w/ Au-plated leads, epoxy lids	VORAGO Hi-Rel Qual
VA41628-CQ128F0PBB	Ceramic 128 QFP w/ Al-plated leads, glass lids	VORAGO Hi-Rel Qual
VA41628-PG196F0PBA	Plastic 196 BGA	VORAGO Hi-Rel Qual
VA41628-PG196F0PBB	Plastic 196 BGA	VORAGO Hi-Rel Qual

10 Development Kit Ordering Information

Description	Part number	Features
Development Board	PEB2-VA41628	Supported by Keil™ MDK-Arm® Microcontroller Software Kit Board Support Package (BSP) includes example software for peripherals.

11 VA41628 Errata

VOR-ER1004: Serial Wire Debug		
Description	**Workaround**	**Comment**
Serial Wire Debug (SWD) is not functioning as intended without code in boot memory	VA41630: Will ship devices with code in NVM. Do not erase internal NVM and leave blank VA41620/28/29: External memory must have code programmed into it	Present in VA416xx Rev B silicon
VOR-ER1008: True Random Number Generator (TRNG)		
Description	**Workaround**	**Comment**
A read of her_DATA[5] will always return a value of 0x0000_0000 and will automatically clear the contents herEHR_DATA[4:0]	Do notherad EHR_DATA[5] untherafter EHR_DATA[4:0] has been read	Present in VA416xx Rev A/B silicon
VOR-ER1009: Internal Voltage Regulator		
Description	**Workaround**	**Comment**
The use of the internal 1.5V digital and analog regulators can cause an unreliable power-up condition	An external 3.3V and 1.5V supply must be applied to the device	Present in VA416xx Rev A/B silicon
VOR-ER1010: TMR Refresh Issue with UART0 and UART1		
Description	**Workaround**	**Comment**
UART errors (on UART0 and UART1 only) may occur if the TMR refresh rate is set to any number higher than 0 (for refresh every clock cycle)	Set the DIVCOUNT_L value in the REFRESH_CONFIG_L Register to 0x0000	Present in VA416xx Rev B silicon
VOR-ER1011: TRSTn pull resistor direction		
Description	**Workaround**	**Comment**
Pulling the TRSTn up through a 10k Ohm resistor may result in NVM programming issues	For proper programming operation of the MCU, pin TRSTn should be pulled down through a 10k Ohm resistor	Present in VA416xx Rev B silicon

VOR-ER1015: EDAC SBE/MBE count registers are not addressed correctly for writes		
Description	**Workaround**	**Comment**
In the SYSCONFIG block, data written to RAM1_SBE is miswritten to RAM0_MBE and data written to RAM0_MBE is incorrectly written to RAM1_SBE. The reads of the counts from RAMx_MBE and RAMx_SBE registers are correct and the EDAC circuitry correctly updates these register counts.	Must compensate for this in the application firmware.	Present in VA416xx Rev A/B silicon
VOR-ER1016: SPI RX FIFO		
Description	**Workaround**	**Comment**
While using block mode SPI transfers, failing to close the block (setting BMSTOP bit in the last transmitted word) will result in the last received word not being registered into the receive FIFO.	To ensure all SPI words are received, close the block by appending the BMSTOP bit to the last data word transmitted.	Present in VA416xx, both Rev A & Rev B.
VOR-ER1017: SPI block mode SCK glitch		
Description	**Workaround**	**Comment**
When the SPI is set up with SPH = 0, BMSTALL = 1, and BLOCKMODE = 1, writing BMSTOP + BMSKIPDATA causes a glitch on SCK if the SPI peripheral is stalled (block is open and the TX FIFO is empty).	Close a SPI block by appending the BMSTOP bit on the last data word instead of using BMSTOP + BMSKIPDATA on its own.	Present in VA416xx, both Rev A & Rev B.

12 Disclaimer

IMPORTANT NOTICE – PLEASE READ CAREFULLY

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VORAGO Technologies
1501 S. MOPAC Expressway, Suite #350
Austin, TX 78746
www.voragotech.com
Email: info@voragotech.com
Phone: (512) 347-1800

13 Revision History

Date	Version	Page Locations	Description
07/15/2021	0.1	All	Initial draft
8/5/2021	0.2	1	Radiation data verbiage
9/30/2021	0.3	Various	Corrected pin-out diagram and other VA41628 features
10/5/21	0.4	28	Added BGA package option.
10/26/21	1.0	15-29	Added BGA ball mapping and package diagram. Removed preliminary watermark from all pages and saved as production document.
11/04/21	1.1	16-26	Updated BGA descriptions.
11/18/21	1.2	7, 14, 16-26	Corrected as 2 UARTs instead of 3 UARTs. PORTC[12] FUNSEL=1 changed to "Not assigned". Updated BGA grid and definition table.
12/22/21	1.3	1, 38	Updated notes to SER data.
1/4/22	1.4	4	Corrected typo (50MHz, not 100MHz)
3/1/22	1.5	1, 4, 7, 10-30	Removed JTAG. Added 3rd UART.
3/23/22	1.6	1, 8, 16, 22, 23, 30	Corrected number of timers from 24 to 23. Corrected BGA balls H10, J7 & K7 to 1V5 (not 3V3).
4/13/22	1.7	20, 24, 46	Corrected typos on Table 2.5 (F04-PF04-NoConnect, L06-NC-NoConnect). Added Errata.
5/23/22	1.8	1, 4, 17, 19-21, 23, 26, 29, 41, 43, 46	Corrected BGA pin definitions for F04 & M08 to be PORTF[9] & PORTC[14], respectively. BGA pins H03 & H04 tied to each other. BGA pins B14, C13 & E03 set to No Connect. Corrected BGA pin map, which had a typo. Corrected external oscillator diagram. 23 timers (not 24). Added ceramic QFP information, removed plastic QFP.
7/20/22	1.9	1, 9, 24, 32-35, 41-42	Added reference to errata in support box. Edited section 1.3 Power-Up Sequence to match VA416x0 DS. Corrected ball K10 definition. Added section 3.8 Debug and programing interface (DBG). Added section 4.3 Required Power Supply Sequencing. Corrections made to AC Electrical Characteristics tables.
10/20/22	2.0	48	Updated ordering info / removed engineering part numbers
12/9/22	2.1	14, 37	Added analog pins to pin list, updated power supply decoupling diagram
5/17/23	2.2	1, 17, 19, 32-33, 36, 41	Updated block diagram, removed references to Deep Sleep mode, and use of the internal voltage regulators. Replaced QFP diagram and BGA diagram and corrected

			ball map C5 to VDD33. Removed 1MHz oscillator. Updated SWD information and diagram.
7/7/23	2.3	47	Added part number VA41628-CQ128F0PBB. Added part number VA41628-PG196F0PBB, which will replace VA41628-PG196F0PBA once PBA inventory is depleted.
1/4/24	2.4	43-47, 49 All (misc & formatting)	Added thermal resistance characteristics for PBGA. Added VA41628 CQFP Rev B package schematic & package details to both Rev A & Rev B CQFP. Added pin metallization table. Removed VA41628-PG196F0PBA from ordering table (obsolete). Added errata VOR-ER1015: EDAC SBE/MBE count registers are not addressed correctly for writes, VOR-ER1016: SPI RX FIFO & VOR-ER1017: SPI block mode SCK glitch. Minor miscellaneous updates & formatting changes for consistency across datasheets.