centre frequency is minimal (maximum Q) as expected, as the tank circuit operates at its peak Q. The noise bandwidth increases as the frequency moves away from the centre frequency. As the CPSO always operates at its free-running frequency, where the injected frequency is equal to the free-running frequency, it always has maximum noise rejection. When the free-running frequency of the CPSO is changed by varying the bias of transistor T_1, a new tracking curve is established. Therefore, the CPSO tracking range is formed by an infinite number of bias levels, each one having a tracking range $\Delta\omega$. Individual tracking ranges do not have any significance in the operation of the CPSO, as the CPSO always operates at its free-running frequency. For convenience we will define the total tracking range of the CPSO as $N\ \Delta\omega$, knowing that under each tracking curve $\Delta\omega$ there are an infinite number of operating points, each corresponding to the free-running frequency of the CPSO.

In Fig. 1, the ϕ-correction network should establish a bias for transistor T_1, which will change the free-running frequency of the CPSO to correspond to the injected frequency. The generation of such a bias locus by the ϕ-correction network is not a straightforward procedure but requires a skilful mapping if absolute coherency is to be achieved.

Calibration of the phase correction network: The ϕ-correction network, in Fig. 1, is disconnected from the base of transistor T_1 and terminated in R_T, which is approximately equal to the input resistance of transistor T_1, at point D, as shown in Fig. 3. A new resistor R_B is connected to the base of T_1 and

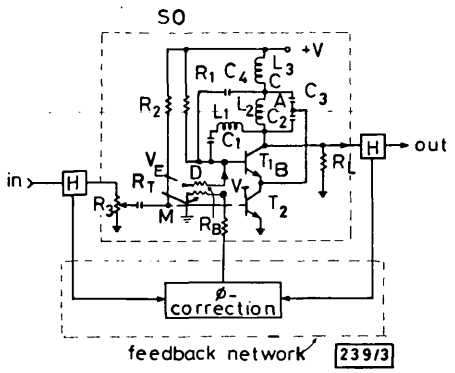

Fig. 3 *Bias calibration of a CPSO*

is applied to a variable voltage source V_E. We identify the frequency range at which the CPSO should operate, say $\omega_1 - \omega_2$, and determine the change in V_E which moves the free-running frequency of the CPSO from ω_1 to ω_2. This procedure enables us to draw the bias/frequency curve shown in Fig. 4. The phase correction network, when connected back

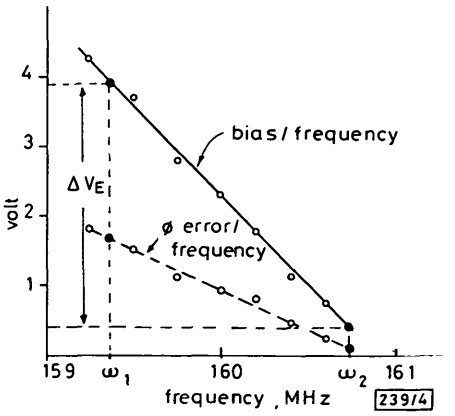

Fig. 4 *Bias and phase-error curves for a CPSO*

to the base of T_1, must supply the same voltage change ΔV_E between ω_1 and ω_2 for the CPSO to operate absolutely coherently. To determine the ϕ-error voltage delivered by the ϕ-correction network we remove V_E and apply $\omega_1 - \omega_2$ in steps of, say, 50 kHz to the input of the CPSO and determine the open-loop output voltage of the ϕ-correction network at point V_T. This enables us to draw the ϕ-error curve shown in Fig. 4. This curve must be mapped into the bias/frequency curve for the CPSO to operate in absolute coherency. A computer algorithm should be developed to perform the mapping. When the ϕ-correction network is connected back to the base of T_1, we assume that the error voltage associated between the open loop and closed loop is negligible or may need some slight adjustment. Experiments have confirmed these assumptions.

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METHOD TO REDUCE THE SIGN BIT EXTENSION IN A MULTIPLIER THAT USES THE MODIFIED BOOTH ALGORITHM

Indexing terms: Computers, Binary multiplication, Modified Booth algorithm

A technique that reduces the number of full adders that are used to implement the modified Booth algorithm is described. This technique is based on the need to extend the sign bit of the partial products and on the redundancy that is implicit in this operation.

Introduction: The modified Booth algorithm (MBA) basically consists of two steps: first obtain the partial products from the multiplicands and second add these partial products in an array of full adders.[1,2]

The second step, the summation in an array, has to be done with sign bit extension, because it is a signed multiplication.

The redundancy of the sign bit extension can be eliminated by a simple method, i.e. reducing the number of variable inputs to the array, thus making it possible to reduce the number of full adders involved.

The technique will be illustrated by an example.

Description: Let X and Y be the numbers to be multiplied, in 2-complement notation:

$$X = x_3 x_2 x_1 x_0$$

$$Y = y_3 y_2 y_1 y_0$$

x_3 and y_3 are the sign bits of x and y, respectively.

Analysing three bits of Y at a time, in accordance with the MBA, the partial products are

$$A = (-8x_3 + 4x_2 + 2x_1 + x_0) \cdot (-2y_1 + y_0 + y_{-1}) \quad (1)$$

$$B = (-8x_3 + 4x_2 + 2x_1 + x_0) \cdot (-2y_3 + y_2 + y_1) \quad (2)$$

The MBA algorithm requires that the multiplier Y be padded with a zero to the right of the least significant bit, i.e. $y_{-1} = 0$.

The partial products A and B are 6-bit numbers:

$$A = A_4 A_3 A_2 A_1 A_0 \cdot A_{-1}$$

$$B = B_4 B_3 B_2 B_1 B_0 \cdot B_{-1}$$

The pad bits A_{-1} and B_{-1} are always zero, so they will no longer be considered here. A_4 and B_4 are the sign bits. To perform a correct 2-complement operation y_1 and y_3 have to be added to the LSBs of the partial products.

A and B have to be added with sign extension:

$$\begin{array}{l} A_4\,A_4\,A_4\,A_4\,A_3\,A_2\,A_1\,A_0 \qquad\qquad y_1 \\ B_4\,B_4\,B_3\,B_2\,B_1\,B_0 \qquad\qquad y_3 \\ \hline P_7\,P_6\,P_5\,P_4\,P_3\,P_2\,P_1\,P_0 \end{array}$$

The physical implementation of the summation with full adders is shown in Fig. 1.

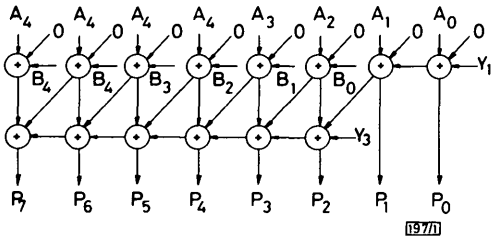

Fig. 1 *Conventional implementation of partial product summation*

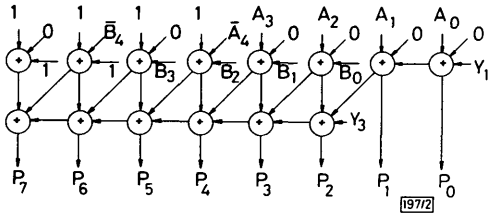

Fig. 2 *Replacement of sign bit extension according to eqns. 3 and 4*

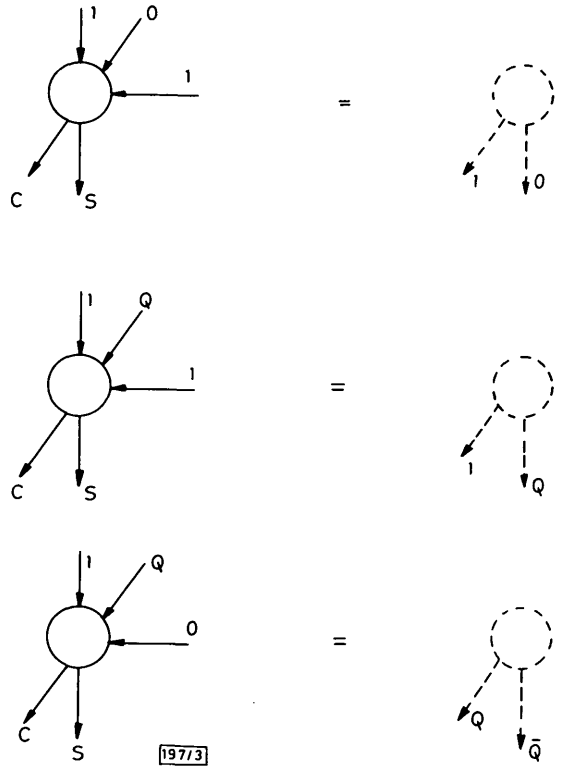

Fig. 3 *Procedure for elimination of full adders*

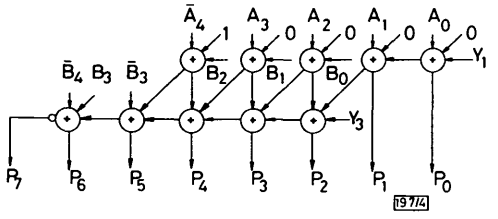

Fig. 4 *Partial product summation with a reduced array of full adders*

If we note that

$$A_4\,A_4\,A_4\,A_4 = (1\ 1\ 1\ 1 + \bar{A}_4) \bmod 16 \tag{3}$$

$$B_4\,B_4 \qquad = (1\ 1 \qquad + \bar{B}_4) \bmod 4 \tag{4}$$

the summing of the partial products is now

$$\begin{array}{cccccccc} 1 & 1 & 1 & \underline{1} & A_3 & A_2 & A_1 & A_0 \\ & & & \bar{A}_4 & & & & y_1 \\ 1 & \underline{1} & B_3 & B_2 & B_1 & B_0 & & \\ & \bar{B}_4 & & & & y_3 & & \\ \hline P_7 & P_6 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0 \end{array}$$

thus eliminating the redundancy of the sign bit extension. The implementation is shown in Fig. 2.

Some full adders of the array can be eliminated as shown in Fig. 3 and the resulting implementation of the multiplier is shown in Fig. 4.

The number of full adders can be reduced significantly with the technique described. It can be extended for multipliers with different numbers of bits. To illustrate this, Table 1

Table 1 COMPARISON OF ARRAY SIZE WITH AND WITHOUT REDUCTION TECHNIQUE

No. of bits	Normal MBA	Reduced MBA
4 × 4	14	10
6 × 6	30	21
8 × 8	52	36

shows the difference between the sizes of the array with and without the reduction technique.

The technique described can also be used in other cases where sign bit extension is involved. It is not restricted to the modified Booth algorithm.

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12th August 1986

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MECHANISM OF CARRIER LIFETIME INCREASE IN ION BEAM SYNTHESISED SOI STRUCTURES

Indexing terms: Semiconductor devices and materials, Silicon-on-insulator structures

Carrier lifetimes were measured in epitaxial silicon layers which were deposited on silicon wafers implanted with different nitrogen doses at 330 keV. At doses greater than $10^{16}\,cm^{-2}$ the lifetime was more than one order of magnitude higher on the implanted part of the wafers ($\sim 300\,\mu s$). The mechanism responsible for this effect is connected with the gettering efficiency for heavy metals of a precipitation-rich dislocation network in the implanted silicon.

Introduction: In a recent letter we have reported on relatively high values of the minority carrier generation lifetime in epitaxial silicon layers deposited above ion beam synthesised buried silicon nitride SOI (silicon-on-insulator) structures.[1] Two causes to explain this effect were given there:

Thesis 1: neutralisation of crystal defects in the epitaxial layer by nitrogen diffusing out of the buried nitride system