PIC24FV16KM204 FAMILY

General Purpose, 16-Bit Flash Microcontrollers with XLP Technology Data Sheet

Analog Peripheral Features

- Up to Two 8-Bit Digital-to-Analog Converters (DACs):
  - Soft Reset disable function allows DAC to retain its output value through non-VDD Resets
  - Support for Idle mode
  - Support for left and right justified input data
- Two Operational Amplifiers (Op Amps):
  - Differential inputs
  - Selectable power/speed levels:
    - Low power/low speed
    - High power/high speed
- Up to 22-Channel, 10/12-Bit Analog-to-Digital Converter:
  - 100k samples/second at 12-bit conversion rate (single Sample-and-Hold)
  - Auto-scan with Threshold Detect
  - Can operate during Sleep
  - Dedicated band gap reference and temperature sensor input
- Up to Three Rail-to-Rail Analog Comparators:
  - Programmable reference voltage for comparators
  - Band gap reference input
  - Flexible input multiplexing
  - Low-power or high-speed selection options
- Charge Time Measurement Unit (CTMU):
  - Capacitive measurement, up to 22 channels
  - Time measurement down to 200 ps resolution
  - Up to 16 external trigger pairs
- Internal Temperature Sensor with Dedicated A/D Converter Input

High-Performance RISC CPU

- Modified Harvard Architecture
- Operating Speed:
  - DC – 32 MHz clock input
  - 16 MIPS at 32 MHz clock input
- 8 MHz Internal Oscillator:
  - 4x PLL option
  - Multiple clock divide options
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture
- 24-Bit Wide Instructions
- 16-Bit Wide Data Path
- Linear Program Memory Addressing, Up to 6 Mbytes
- Linear Data Memory Addressing, Up to 64 Kbytes
- Two Address Generation Units (AGUs) for Separate Read and Write Addressing of Data Memory

Multiple/Single Capture Compare Peripheral (MCCP/SCCP) Features

- 16 or 32-Bit Time Base
- 16 or 32-Bit Capture:
  - 4-deep capture buffer
- 16 or 32-Bit Compare:
  - Single Edge Compare modes
  - Dual Edge Compare/PWM modes
  - Center-Aligned Compare mode
  - Variable Frequency Pulse mode
- Single Output Steerable mode (MCCP only)
- Brush DC Forward and Reverse modes (MCCP only)
- Half-Bridge with Dead-Time Delay (MCCP only)
- Push-Pull PWM mode (MCCP only)
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

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Device	Pins	Memory			Voltage Range (V)	Peripherals											ICD BRKPT
		Flash Program (bytes)	SRAM (bytes)	EE Data (bytes)		16-Bit Timer	16-Bit MCCP/SCCP	MSSP	UART	12-Bit A/D Channels	8-Bit DAC	Op Amp	Comparators	CTMU	RTCC	CLC	
5V Devices																	
PIC24FV16KM204	44	16K	2K	512	2.0-5.5	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24FV16KM202	28	16K	2K	512	2.0-5.5	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24FV08KM204	44	8K	2K	512	2.0-5.5	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24FV08KM202	28	8K	2K	512	2.0-5.5	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24FV16KM104	44	16K	1K	512	2.0-5.5	1	1/1	1	1	22	—	—	1	Yes	—	1	3
PIC24FV16KM102	28	16K	1K	512	2.0-5.5	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24FV08KM102	28	8K	1K	512	2.0-5.5	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24FV08KM101	20	8K	1K	512	2.0-5.5	1	1/1	1	1	16	—	—	1	Yes	—	1	3
3V Devices																	
PIC24F16KM204	44	16K	2K	512	1.8-3.6	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24F16KM202	28	16K	2K	512	1.8-3.6	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24F08KM204	44	8K	2K	512	1.8-3.6	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24F08KM202	28	8K	2K	512	1.8-3.6	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24F16KM104	44	16K	1K	512	1.8-3.6	1	1/1	1	1	22	—	—	1	Yes	—	1	3
PIC24F16KM102	28	16K	1K	512	1.8-3.6	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24F08KM102	28	8K	1K	512	1.8-3.6	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24F08KM101	20	8K	1K	512	1.8-3.6	1	1/1	1	1	16	—	—	1	Yes	—	1	3

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Peripheral Features

- High-Current Sink/Source, 18 mA/18 mA All Ports
- Independent Ultra-Low Power, 32 kHz Timer Oscillator
- Up to Two Master Synchronous Serial Ports (MSSPs) with SPI and I^2C modes:
  - In SPI mode:
    - User-configurable SCKx and SDOx pin outputs
    - Daisy-chaining of SPI Slave devices
  - In I^2C mode:
    - Serial clock synchronization (clock stretching)
    - Bus collision detection and will arbitrate accordingly
    - Support for 16-bit read/write interface
- Up to Two Enhanced Addressable UARTs:
  - LIN/J2602 bus support (auto-wake-up, Auto-Baud Detect, Break character support)
  - High and low speed (SCI)
  - IrDA® mode (hardware encoder/decoder function)
- Two External Interrupt Pins
- Hardware Real-Time Clock and Calendar (RTCC)
- Configurable Reference Clock Output (REFO)
- Two Configurable Logic Cells (CLCs)
- Up to Two Single Output Capture/Compare/PWM (SCCP) modules and Up to Three Multiple Output Capture/Compare/PWM (MCCP) modules

Special Microcontroller Features

- Wide Operating Voltage Range Options:
  - 1.8V to 3.6V (PIC24F devices)
  - 2.0V to 5.0V (PIC24FV devices)
- Selectable Power Management modes:
  - Idle: CPU shuts down, allowing for significant power reduction
  - Sleep: CPU and peripherals shut down for substantial power reduction and fast wake-up
  - Retention Sleep mode: PIC24FV devices can enter Sleep mode, employing the Retention Regulator, further reducing power consumption
  - Doze: CPU can run at a lower frequency than peripherals, a user-programmable feature
  - Alternate Clock modes allow on-the-fly switching to a lower clock speed for selective power reduction
- Fail-Safe Clock Monitor:
  - Detects clock failure and switches to on-chip, low-power RC Oscillator
- Ultra Low-Power Wake-up Pin Provides an External Trigger for Wake from Sleep
- 10,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- 100,000 Erase/Write Cycle Endurance Data EEPROM, Typical
- Flash and Data EEPROM Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its Own On-Chip RC Oscillator for Reliable Operation
- On-Chip Regulator for 5V Operation
- Selectable Windowed WDT Feature
- Selectable Oscillator Options including:
  - 4x Phase-Locked Loop (PLL)
- 8 MHz (FRC) Internal RC Oscillator:
  - HS/EC, High-Speed Crystal/Resonator Oscillator or External Clock
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) – via Two Pins
- In-Circuit Debugging
- Programmable High/Low-Voltage Detect (HLVD) module
- Programmable Brown-out Reset (BOR):
  - Software enable feature
  - Configurable shutdown in Sleep
  - Auto-configures power mode and sensitivity based on device operating speed
  - LPBOR available for re-arming of the POR

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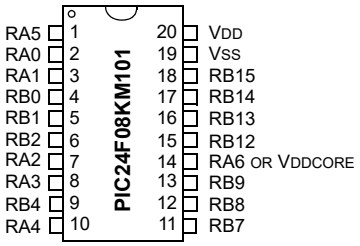
Pin Diagrams

20-Pin PDIP/SSOP/SOIC



Pin	Pin Features	
	PIC24F08KM101	PIC24FV08KM101
1	$\overline{\text{MCLR}}$/VPP/RA5	
2	PGEC2/CVREF+/VREF+/AN0/CN2/RA0	
3	PGED2/CVREF-/VREF-/AN1/CN3/RA1	
4	PGED1/AN2/CTCMP/ULPWU/C1IND/OC2A/CN4/RB0	
5	PGEC1/AN3/C1INC/CTED12/CN5/RB1	
6	AN4/U1RX/TCKIB/CTED13/CN6/RB2	
7	OSCI/CLKI/AN13/C1INB/CN30/RA2	
8	OSCO/CLKO/AN14/C1INA/CN29/RA3	
9	PGED3/SOSCI/AN15/CLCINA/CN1/RB4	
10	PGEC3/SOSCO/SCLKI/AN16/PWRLCLK/CLCINB/CN0/RA4	
11	AN19/U1TX/CTED1/INT0/CN23/RB7	AN19/U1TX/IC1/OC1A/CTED1/INT0/CN23/RB7
12	AN20/SCL1/$\overline{\text{U1CTS}}$/OC1B/CTED10/CN22/RB8	
13	AN21/SDA1/T1CK/$\overline{\text{U1RTS}}$/U1BCLK/IC2/CLC1O/CTED4/CN21/RB9	
14	IC1/OC1A/INT2/CN8/RA6	VCAP OR VDDCORE
15	AN12/HLVDIN/SCK1/OC1C/CTED2/CN14/RB12	AN12/HLVDIN/SCK1/OC1C/CTED2/INT2/CN14/RB12
16	AN11/SDO1/OCFB/OC1D/CTPLS/CN13/RB13	
17	CVREF/AN10/SDI1/C1OUT/OCFA/CTED5/INT1/CN12/RB14	
18	AN9/REFO/$\overline{\text{SS1}}$/TCKIA/CTED6/CN11/RB15	
19	VSS/AVSS	
20	VDD/AVDD	

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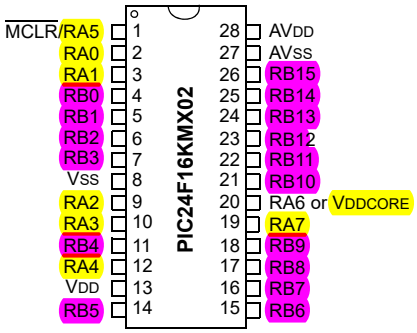
Pin Diagrams (Continued)

28-Pin SPDIP/SSOP/SOIC

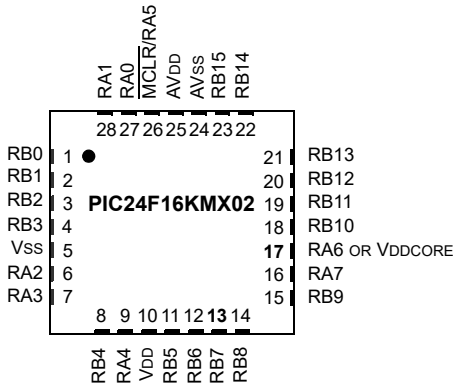


Pin	Pin Features	
	PIC24FXXKMX02	PIC24FVXXKMX02
1	MCLR/VPP/RA5	
2	CVREF+/VREF+/DAC1REF+/AN0/C3INC/CN2/RA0	
3	CVREF-/VREF-/AN1/CN3/RA1	CVREF-/VREF-/AN1/RA1
4	PGED1/AN2/CTCMP/ULPWU/C1IND/C2INB/C3IND/U2TX/CN4/RB0	
5	PGEC1/OA1INA/OA2INA/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1	
6	OA1INB/OA2INB/AN4/C1INB/C2IND/SDA2/U1RX/TCKIB/CTED13/CN6/RB2	
7	OA1OUT/AN5/C1INA/C2INC/SCL2/CN7/RB3	
8	VSS	
9	OSCI/CLKI/AN13/CN30/RA2	
10	OSCO/CLKO/AN14/CN29/RA3	
11	SOSCI/AN15/U2RTS/U2BCLK/CN1/RB4	
12	SOSCO/SCLKI/AN16/PWRLCLK/U2CTS/CN0/RA4	
13	VDD	
14	PGED3/AN17/ASDA1/SCK2/IC4/OC1E/CLCINA/CN27/RB5	
15	PGEC3/AN18/ASCL1/SDO2/IC5/OC1F/CLCINB/CN24/RB6	
16	AN19/U1TX/INT0/CN23/RB7	AN19/U1TX/C2OUT/OC1A/INT0/CN23/RB7
17	AN20/SCL1/U1CTS/C3OUT/OC1B/CTED10/CN22/RB8	
18	AN21/SDA1/T1CK/U1RTS/U1BCLK/IC2/OC4/CLC1O/CTED4/CN21/RB9	
19	SDI2/IC1/OC5/CLC2O/CTED3/CN9/RA7	
20	C2OUT/OC1A/CTED1/INT2/CN8/RA6	VCAP OR VDDCORE
21	PGED2/SDI1/OC3A/OC1C/CTED11/CN16/RB10	
22	PGEC2/SCK1/OC2A/CTED9/CN15/RB11	
23	DAC1OUT/AN12/HLVDIN/SS2/IC3/OC2B/CTED2/CN14/RB12	DAC1OUT/AN12/HLVDIN/SS2/IC3/OC2B/CTED2/INT2/CN14/RB12
24	OA1INC/OA2INC/AN11/SDO1/OCFB/OC3B/OC1D/CTPLS/CN13/RB13	
25	DAC2OUT/CVREF/OA1IND/OA2IND/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14	
26	DAC2REF+/OA2OUT/AN9/C3INA/REFO/SS1/TCKIA/CTED6/CN11/RB15	
27	VSS/AVSS	
28	VDD/AVDD	

Legend: Values in red indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

Pin Diagrams (Continued)

28-Pin QFN(1)



Pin	Pin Features	Pin Features
	PIC24FXXKMX02	PIC24FVXXKMX02
1	PGED1/AN2/CTCMP/ULPWU/C1IND/C2INB/C3IND/U2TX/CN4/RB0	
2	PGEC1/OA1INA/OA2INA/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1	
3	OA1INB/OA2INB/AN4/C1INB/C2IND/SDA2/U1RX/TCKIB/CTED13/CN6/RB2	
4	OA1OUT/AN5/C1INA/C2INC/SCL2/CN7/RB3	
5	VSS	
6	OSCI/CLKI/AN13/CN30/RA2	
7	OSCO/CLKO/AN14/CN29/RA3	
8	SOSCI/AN15/$\overline{\text{U2RTS}}$/U2BCLK/CN1/RB4	
9	SOSCO/SCLKI/AN16/PWRLCLK/$\overline{\text{U2CTS}}$/CN0/RA4	
10	VDD	
11	PGED3/AN17/ASDA1/SCK2/IC4/OC1E/CLCINA/CN27/RB5	
12	PGEC3/AN18/ASCL1/SDO2/IC5/OC1F/CLCINB/CN24/RB6	
13	AN19/U1TX/INT0/CN23/RB7	AN19/U1TX/C2OUT/OC1A/INT0/CN23/RB7
14	AN20/SCL1/$\overline{\text{U1CTS}}$/C3OUT/OC1B/CTED10/CN22/RB8	
15	AN21/SDA1/T1CK/$\overline{\text{U1RTS}}$/U1BCLK/IC2/OC4/CLC1O/CTED4/CN21/RB9	
16	SDI2/IC1/OC5/CLC2O/CTED3/CN9/RA7	
17	C2OUT/OC1A/CTED1/INT2/CN8/RA6	VDDCORE/VCAP
18	PGED2/SDI1/OC3A/OC1C/CTED11/CN16/RB10	
19	PGEC2/SCK1/OC2A/CTED9/CN15/RB11	
20	DAC1OUT/AN12/HLVDIN/$\overline{\text{SS2}}$/IC3/OC2B/CTED2/CN14/RB12	DAC1OUT/AN12/HLVDIN/$\overline{\text{SS2}}$/IC3/OC2B/CTED2/INT2/CN14/RB12
21	OA1INC/OA2INC/AN11/SDO1/OCFB/OC3B/OC1D/CTPLS/CN13/RB13	
22	DAC2OUT/CVREF/OA1IND/OA2IND/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14	
23	DAC2REF+/OA2OUT/AN9/C3INA/REFO/$\overline{\text{SS1}}$/TCKIA/CTED6/CN11/RB15	
24	AVSS	
25	AVDD	
26	$\overline{\text{MCLR}}$/VPP/RA5	
27	CVREF+/VREF+/DAC1REF+/AN0/C3INC/CN2/RA0	CVREF+/VREF+/DAC1REF+/AN0/C3INC/CTED1/CN2/RA0
28	CVREF-/VREF-/AN1/CN3/RA1	

Legend: Values in red indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

Note 1: Exposed pad on underside of device is connected to VSS.

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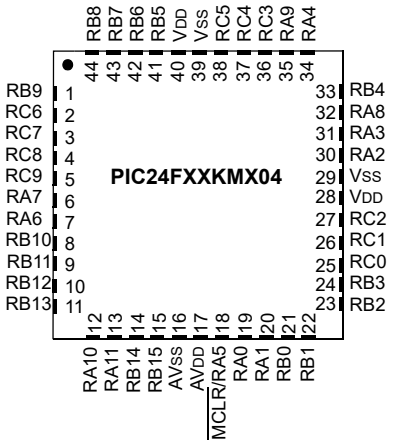
Pin Diagrams (Continued)

44-Pin TQFP/QFN(1)



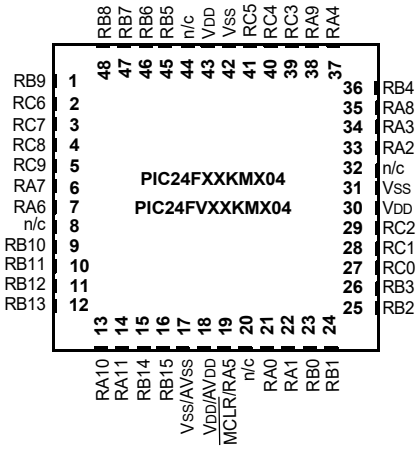
Pin	Pin Features	
	PIC24FXXKMX04	PIC24FVXXKMX04
1	AN21/SDA1/T1CK/$\overline{\text{U1RTS}}$/U1BCLK/IC2/OC4/CLC1O/CTED4/CN21/RB9	
2	U1RX/OC2C/CN18/RC6	
3	U1TX/OC2D/CN17/RC7	
4	OC2E/CN20/RC8	
5	IC4/OC2F/CTED7/CN19/RC9	
6	IC1/OC5/CLC2O/CTED3/CN9/RA7	
7	C2OUT/OC1A/CTED1/INT2/CN8/RA6	VCAP or VDDCORE
8	PGED2/SDI1/OC1C/CTED11/CN16/RB10	
9	PGEC2/SCK1/OC2A/CTED9/CN15/RB11	
10	DAC1OUT/AN12/HLVDIN/OC2B/CTED2/CN14/RB12	DAC1OUT/AN12/HLVDIN/OC2B/CTED2/INT2/CN14/RB12
11	OA1INC/OA2INC/AN11/SDO1/OC1D/CTPLS/CN13/RB13	
12	IC5/OC3A/CN35/RA10	
13	IC3/OC3B/CTED8/CN36/RA11	
14	DAC2OUT/CVREF/OA1IND/OA2IND/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14	
15	DAC2REF+/OA2OUT/AN9/C3INA/REFO/$\overline{\text{SS1}}$/TCKIA/CTED6/CN11/RB15	
16	AVSS	
17	AVDD	
18	$\overline{\text{MCLR}}$/VPP/RA5	
19	CVREF+/VREF+/DAC1REF+/AN0/C3INC/CN2/RA0	CVREF+/VREF+/DAC1REF+/AN0/C3INC/CTED1/CN2/RA0
20	CVREF-/VREF-/AN1/CN3/RA1	
21	PGED1/AN2/CTCMP/ULPWU/C1IND/C2INB/C3IND/U2TX/CN4/RB0	
22	PGEC1/OA1INA/OA2INA/AN3/C1INC/C2INA/U2RX/CTED12/CN5//RB1	
23	OA1INB/OA2INB/AN4/C1INB/C2IND/SDA2/TCKIB/CTED13/CN6/RB2	
24	OA1OUT/AN5/C1INA/C2INC/SCL2/CN7/RB3	
25	AN6/CN32/RC0	
26	AN7/CN31/RC1	
27	AN8/CN10/RC2	
28	VDD	
29	VSS	
30	OSCI/CLKI/AN13/CN30/RA2	
31	OSCO/CLKO/AN14/CN29/RA3	
32	OCFB/CN33/RA8	
33	SOSCI/AN15/$\overline{\text{U2RTS}}$/U2BCLK/CN1/RB4	
34	SOSCO/SCLKI/AN16/PWRLCLK/$\overline{\text{U2CTS}}$/CN0/RA4	
35	$\overline{\text{SS2}}$/CN34/RA9	
36	SDI2/CN28/RC3	
37	SDO2/CN25/RC4	
38	SCK2/CN26/RC5	
39	VSS	
40	VDD	
41	PGED3/AN17/ASDA1/OC1E/CLCINA/CN27/RB5	
42	PGEC3/AN18/ASCL1/OC1F/CLCINB/CN24/RB6	
43	AN19/INT0/CN23/RB7	AN19/C2OUT/OC1A/INT0/CN23/RB7
44	AN20/SCL1/$\overline{\text{U1CTS}}$/C3OUT/OC1B/CTED10/CN22/RB8	

Legend: Values in red indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

Note 1: Exposed pad on underside of device is connected to VSS.

Pin Diagrams (Continued)

48-Pin UQFN(1)



Pin	Pin Features	
	PIC24FXXKMX04	PIC24FVXXKMX04
1	AN21/SDA1/T1CK/U1RTS/U1BCLK/IC2/OC4/CLC1O/CTED4/CN21/RB9	
2	U1RX/OC2C/CN18/RC6	
3	U1TX/OC2D/CN17/RC7	
4	OC2/CN20/RC8	
5	IC4/OC2F/CTED7/CN19/RC9	
6	IC1/OC5/CLC2O/CTED3/CN9/RA7	
7	C2OUT/OC1A/CTED1/INT2/CN8/RA6	VDDCORE or VCAP
8	n/c	n/c
9	PGED2/SDI1/OC1C/CTED11/CN16/RB10	
10	PGEC2/SCK1/OC2A/CTED9/CN15/RB11	
11	DAC1OUT/AN12/HLVDIN/OC2B/CTED2/CN14/RB12	DAC1OUT/AN12/HLVDIN/OC2B/CTED2/INT2/CN14/RB12
12	OA1INC/OA2INC/AN11/SDO1/OC1D/CTPLS/CN13/RB13	
13	IC5/OC3A/CN35/RA10	
14	IC3/OC3B/CTED8/CN36/RA11	
15	DAC2OUT/CVREF/OA1IND/OA2IND/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14	
16	DAC2REF+/OA2OUT/AN9/C3INA/REFO/SS1/TCKIA/CTED6/CN11/RB15	
17	VSS/AVSS	
18	VDD/AVDD	
19	MCLR/VPP/RA5	
20	n/c	
21	CVREF+/VREF+/DAC1REF+/AN0/C3INC/CN2/RA0	CVREF+/VREF+/DAC1REF+/AN0/C3INC/CTED1/CN2/RA0
22	CVREF-/VREF-/AN1/CN3/RA1	
23	PGED1/AN2/CTCMP/ULPWU/C1IND/C2INB/C3IND/U2TX/CN4/RB0	
24	PGEC1/OA1INA/OA2INA/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1	
25	OA1INB/OA2INB/AN4/C1INB/C2IND/SDA2/TCKIB/CTED13/CN6/RB2	
26	OA1OUT/AN5/C1INA/C2INC/SCL2/CN7/RB3	
27	AN6/CN32/RC0	
28	AN7/CN31/RC1	
29	AN8/CN10/RC2	
30	VDD	
31	VSS	
32	n/c	
33	OSCI/AN13/CLKI/CN30/RA2	
34	OSCO/CLKO/AN14/CN29/RA3	
35	OCFB/CN33/RA8	
36	SOSCI/AN15/U2RTS/U2BCLK/CN1/RB4	
37	SOSCO/SCLKI/AN16/PWRLCLK/U2CTS/CN0/RA4	
38	SS2/CN34/RA9	
39	SDI2/CN28/RC3	
40	SDO2/CN25/RC4	
41	SCK2/CN26/RC5	
42	VSS	
43	VDD	
44	n/c	
45	PGED3/AN17/ASDA1/OC1E/CLCINA/CN27/RB5	
46	PGEC3/AN18/ASCL1/OC1F/CLCINB/CN24/RB6	
47	AN19/INT0/CN23/RB7	AN19/C2OUT/OC1A/INT0/CN23/RB7
48	AN20/SCL1/U1CTS/C3OUT/OC1B/CTED10/CN22/RB8	

Legend: Values in red indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

Note 1: Exposed pad on underside of device is connected to VSS.

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FV08KM101
- PIC24FV08KM102
- PIC24FV16KM102
- PIC24FV16KM104
- PIC24FV08KM202
- PIC24FV08KM204
- PIC24FV16KM202
- PIC24FV16KM204
- PIC24F08KM101
- PIC24F08KM102
- PIC24F16KM102
- PIC24F16KM104
- PIC24F08KM202
- PIC24F08KM204
- PIC24F16KM202
- PIC24F16KM204

The PIC24FV16KM204 family introduces many new analog features to the extreme low-power Microchip devices. This is a 16-bit microcontroller family with a broad peripheral feature set and enhanced computational performance. This family also offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but do not require the numerical processing power of a Digital Signal Processor (DSC).

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear Addressing of up to 16 Mbytes (program space) and 16 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32-bit by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as C
- Operational performance up to 16 MIPS

1.1.2 POWER-SAVING TECHNOLOGY

All of the devices in the PIC24FV16KM204 family incorporate a range of features that can significantly reduce power consumption during operation. Key features include:

- On-the-Fly Clock Switching, to allow the device clock to be changed under software control to the Timer1 source or the internal, low-power RC Oscillator during operation, allowing users to incorporate power-saving ideas into their software designs.
- Doze Mode Operation, when timing-sensitive applications, such as serial communications, require the uninterrupted operation of peripherals, the CPU clock speed can be selectively reduced, allowing incremental power savings without missing a beat.
- Instruction-Based Power-Saving Modes, to allow the microcontroller to suspend all operations or selectively shut down its core while leaving its peripherals active with a single instruction in software.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

The PIC24FV16KM204 family offers five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes using crystals or ceramic resonators.
- Two External Clock (EC) modes offering the option of a divide-by-2 clock output.
- Two Fast Internal Oscillators (FRCs), one with a nominal 8 MHz output and the other with a nominal 500 kHz output. These outputs can also be divided under software control to provide clock speed as low as 31 kHz or 2 kHz.
- A Phase-Locked Loop (PLL) frequency multiplier, available to the external oscillator modes and the 8 MHz FRC Oscillator, which allows clock speeds of up to 32 MHz.
- A separate internal RC Oscillator (LPRC) with a fixed 31 kHz output, which provides a low-power option for timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

The PIC24FV16KM204 family devices have two variants. The KM20X variant provides the full feature set of the device, while the KM10X offers a reduced peripheral set, allowing for the balance of features and cost (refer to Table 1-1). Both variants allow for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also helps in migrating to the next larger device. This is true when moving between devices with the same pin count, different die variants, or even moving from 20-pin or 28-pin devices to 44-pin/48-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple to the powerful and complex, yet still selecting a Microchip device.

1.2 Other Special Features

- Communications: The PIC24FV16KM204 family incorporates a range of serial communication peripherals to handle a range of application requirements. There is an MSSP module which implements both SPI and I^2C protocols, and supports both Master and Slave modes of operation for each. Devices also include one of two UARTs with built-in IrDA® encoders/decoders.
- Analog Features: Select members of the PIC24FV16KM204 family include two 8-bit Digital-to-Analog Converters (DACs) which offer support in Idle mode, and left and right justified input data, as well as up to two operational amplifiers with selectable power and speed modes.
- Real-Time Clock/Calendar (RTCC): This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- 12-Bit A/D Converter: This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and faster sampling speed. The 16-deep result buffer can be used either in Sleep, to reduce power, or in Active mode to improve throughput.
- Charge Time Measurement Unit (CTMU) Interface: The PIC24FV16KM204 family includes the new CTMU interface module, which can be used for capacitive touch sensing, proximity sensing, and also for precision time measurement and pulse generation. The CTMU can also be connected to the operational amplifiers to provide active guarding, which provides increased robustness in the presence of noise in capacitive touch applications.

1.3 Details on Individual Family Members

Devices in the PIC24FV16KM204 family are available in 20-pin, 28-pin, 44-pin and 48-pin packages. The general block diagram for all devices is shown in Figure 1-1.

Members of the PIC24FV16KM204 family are available as both standard and high-voltage devices. High-voltage devices, designated with an “FV” in the part number (such as PIC24FV16KM204), accommodate an operating V_{DD} range of 2.0V to 5.5V and have an on-board voltage regulator that powers the core. Peripherals operate at V_{DD}.

Standard devices, designated by “F” (such as PIC24F16KM204), function over a lower V_{DD} range of 1.8V to 3.6V. These parts do not have an internal regulator, and both the core and peripherals operate directly from V_{DD}.

The PIC24FV16KM204 family may be thought of as two different device groups, both offering slightly different sets of features. These differ from each other in multiple ways:

- The size of the Flash program memory
- The number of external analog channels available
- The number of Digital-to-Analog Converters
- The number of operational amplifiers
- The number of analog comparators
- The presence of a Real-Time Clock and Calendar (RTCC)
- The number and type of CCP modules (i.e., MCCP vs. SCCP)
- The number of serial communication modules (both MSSPs and UARTs)
- The number of Configurable Logic Cell (CLC) modules

The general differences between the different sub-families are shown in Table 1-1 and Table 1-2.

A list of the pin features available on the PIC24FV16KM204 family devices, sorted by function, is provided in Table 1-5.

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TABLE 1-1: DEVICE FEATURES FOR THE PIC24F16KM204 FAMILY

Features	PIC24F16KM204	PIC24F08KM204	PIC24F16KM202	PIC24F08KM202
Operating Frequency	DC-32 MHz			
Program Memory (bytes)	16K	8K	16K	8K
Program Memory (instructions)	5632	2816	5632	2816
Data Memory (bytes)	2048			
Data EEPROM Memory (bytes)	512			
Interrupt Sources (soft vectors/NMI traps)	40 (36/4)			
Voltage Range	1.8-3.6V			
I/O Ports	PORTA[11:0] PORTB[15:0] PORTC[9:0]		PORTA[7:0] PORTB[15:0]	
Total I/O Pins	38		24	
Timers	11 (One 16-bit timer, five MCCPs/SCCPs with up to two 16/32 timers each)			
Capture/Compare/PWM modules MCCP SCCP	 3 2			
Serial Communications MSSP UART	 2 2			
Input Change Notification Interrupt	37		23	
12-Bit Analog-to-Digital Module (input channels)	22	22	19	19
Analog Comparators	3			
8-Bit Digital-to-Analog Converters	2			
Operational Amplifiers	2			
Charge Time Measurement Unit (CTMU)	Yes			
Real-Time Clock and Calendar (RTCC)	Yes			
Configurable Logic Cell (CLC)	2			
Resets (and delays)	POR, BOR, `RESET` Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, `REPEAT` Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	44-Pin QFN/TQFP, 48-Pin UQFN		28-Pin SPDIP/SSOP/SOIC/QFN	

TABLE 1-2: DEVICE FEATURES FOR THE PIC24F16KM104 FAMILY

Features	PIC24F16KM104	PIC24F16KM102	PIC24F08KM102	PIC24F08KM101
Operating Frequency	DC-32 MHz			
Program Memory (bytes)	16K	16K	8K	8K
Program Memory (instructions)	5632	5632	2816	2816
Data Memory (bytes)	1024			
Data EEPROM Memory (bytes)	512			
Interrupt Sources (soft vectors/NMI traps)	25 (21/4)			
Voltage Range	1.8-3.6V			
I/O Ports	PORTA[11:0] PORTB[15:0] PORTC[9:0]	PORTA[7:0] PORTB[15:0]		PORTA[6:0] PORTB[15:12,9:7,4,2:0]
Total I/O Pins	38	24		18
Timers	5 (One 16-bit timer, two MCCPs/SCCPs with up to two 16/32 timers each)			
Capture/Compare/PWM modules MCCP SCCP	 1 1			
Serial Communications MSSP UART	 1 1			
Input Change Notification Interrupt	37	23		17
12-Bit Analog-to-Digital Module (input channels)	22	19		16
Analog Comparators	1			
8-Bit Digital-to-Analog Converters	—			
Operational Amplifiers	—			
Charge Time Measurement Unit (CTMU)	Yes			
Real-Time Clock and Calendar (RTCC)	—			
Configurable Logic Cell (CLC)	1			
Resets (and delays)	POR, BOR, `RESET` Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, `REPEAT` Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	44-Pin QFN/TQFP, 48-Pin UQFN	28-Pin SPDIP/SSOP/SOIC/QFN		20-Pin SOIC/SSOP/PDIP

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TABLE 1-3: DEVICE FEATURES FOR THE PIC24FV16KM204 FAMILY

Features	PIC24FV16KM204	PIC24FV08KM204	PIC24FV16KM202	PIC24FV08KM202
Operating Frequency	DC-32 MHz			
Program Memory (bytes)	16K	8K	16K	8K
Program Memory (instructions)	5632	2816	5632	2816
Data Memory (bytes)	2048			
Data EEPROM Memory (bytes)	512			
Interrupt Sources (soft vectors/NMI traps)	40 (36/4)			
Voltage Range	2.0-5.5V			
I/O Ports	PORTA[11:7,5:0] PORTB[15:0] PORTC[9:0]		PORTA[7,5:0] PORTB[15:0]	
Total I/O Pins	37		23	
Timers	11 (One 16-bit timer, five MCCPs/SCCPs with up to two 16/32 timers each)			
Capture/Compare/PWM modules MCCP SCCP	 3 2			
Serial Communications MSSP UART	 2 2			
Input Change Notification Interrupt	36		22	
12-Bit Analog-to-Digital Module (input channels)	22		19	
Analog Comparators	3			
8-Bit Digital-to-Analog Converters	2			
Operational Amplifiers	2			
Charge Time Measurement Unit (CTMU)	Yes			
Real-Time Clock and Calendar (RTCC)	Yes			
Configurable Logic Cell (CLC)	2			
Resets (and delays)	POR, BOR, `RESET` Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, `REPEAT` Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	44-Pin QFN/TQFP, 48-Pin UQFN		28-Pin SPDIP/SSOP/SOIC/QFN	

TABLE 1-4: DEVICE FEATURES FOR THE PIC24FV16KM104 FAMILY

Features	PIC24FV16KM104	PIC24FV16KM102	PIC24FV08KM102	PIC24FV08KM101
Operating Frequency	DC-32 MHz			
Program Memory (bytes)	16K	16K	8K	8K
Program Memory (instructions)	5632	5632	2816	2816
Data Memory (bytes)	1024			
Data EEPROM Memory (bytes)	512			
Interrupt Sources (soft vectors/NMI traps)	25 (21/4)			
Voltage Range	2.0-5.5V			
I/O Ports	PORTA[11:7,5:0] PORTB[15:0] PORTC[9:0]	PORTA[7,5:0] PORTB[15:0]		PORTA[5:0] PORTB[15:12,9:7,4,2:0]
Total I/O Pins	37	23		17
Timers	5 (One 16-bit timer, two MCCPs/SCCPs with up to two 16/32 timers each)			
Capture/Compare/PWM modules MCCP SCCP	 1 1			
Serial Communications MSSP UART	 1 1			
Input Change Notification Interrupt	36	22		16
12-Bit Analog-to-Digital Module (input channels)	22	19		16
Analog Comparators	1			
8-Bit Digital-to-Analog Converters	—			
Operational Amplifiers	—			
Charge Time Measurement Unit (CTMU)	Yes			
Real-Time Clock and Calendar (RTCC)	—			
Configurable Logic Cell (CLC)	1			
Resets (and delays)	POR, BOR, `RESET` Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, `REPEAT` Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	44-Pin QFN/TQFP, 48-Pin UQFN	28-Pin SPDIP/SSOP/SOIC/QFN		20-Pin SOIC/SSOP/PDIP

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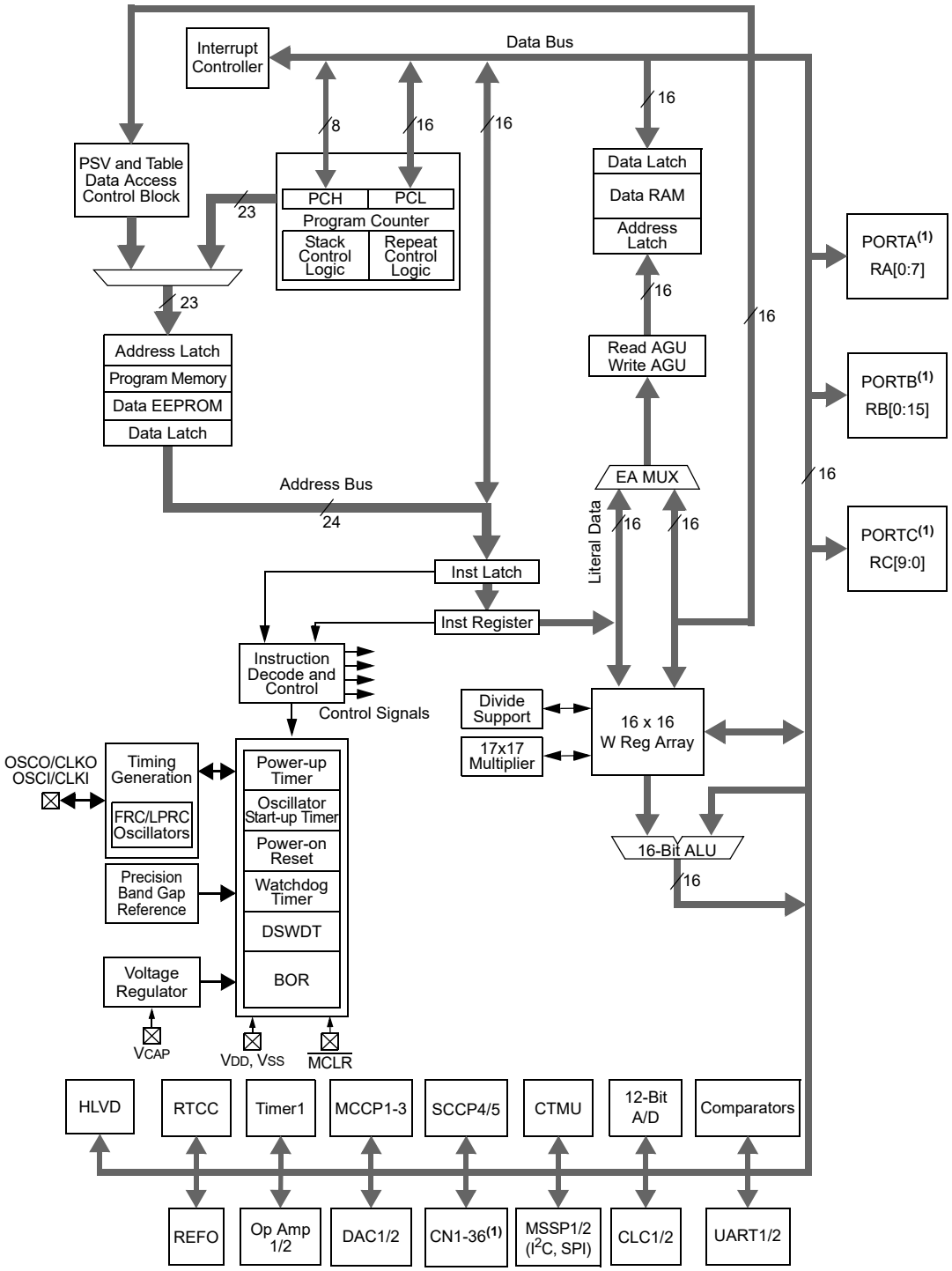
FIGURE 1-1: PIC24FXXXXX FAMILY GENERAL BLOCK DIAGRAMS



Note 1: All pins or features are not implemented on all device pinout configurations. See Table 1-5 for I/O port pin descriptions.

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
AN0	2	2	27	19	21	2	2	27	19	21	I	ANA	A/D Analog Inputs
AN1	3	3	28	20	22	3	3	28	20	22	I	ANA	A/D Analog Inputs
AN2	4	4	1	21	23	4	4	1	21	23	I	ANA	A/D Analog Inputs
AN3	5	5	2	22	24	5	5	2	22	24	I	ANA	A/D Analog Inputs
AN4	6	6	3	23	25	6	6	3	23	25	I	ANA	A/D Analog Inputs
AN5	—	7	4	24	26	—	7	4	24	26	I	ANA	A/D Analog Inputs
AN6	—	—	—	25	27	—	—	—	25	27	I	ANA	A/D Analog Inputs
AN7	—	—	—	26	28	—	—	—	26	28	I	ANA	A/D Analog Inputs
AN8	—	—	—	27	29	—	—	—	27	29	I	ANA	A/D Analog Inputs
AN9	18	26	23	15	16	18	26	23	15	16	I	ANA	A/D Analog Inputs
AN10	17	25	22	14	15	17	25	22	14	15	I	ANA	A/D Analog Inputs
AN11	16	24	21	11	12	16	24	21	11	12	I	ANA	A/D Analog Inputs
AN12	15	23	20	10	11	15	23	20	10	11	I	ANA	A/D Analog Inputs
AN13	7	9	6	30	33	7	9	6	30	33	I	ANA	A/D Analog Inputs
AN14	8	10	7	31	34	8	10	7	31	34	I	ANA	A/D Analog Inputs
AN15	9	11	8	33	36	9	11	8	33	36	I	ANA	A/D Analog Inputs
AN16	10	12	9	34	37	10	12	9	34	37	I	ANA	A/D Analog Inputs
AN17	—	14	11	41	45	—	14	11	41	45	I	ANA	A/D Analog Inputs
AN18	—	15	12	42	46	—	15	12	42	46	I	ANA	A/D Analog Inputs
AN19	11	16	13	43	47	11	16	13	43	47	I	ANA	A/D Analog Inputs
AN20	12	17	14	44	48	12	17	14	44	48	I	ANA	A/D Analog Inputs
AN21	13	18	15	1	1	13	18	15	1	1	I	ANA	A/D Analog Inputs
ASCL1	—	15	12	42	46	—	15	12	42	46	I/O	I^2C	Alternate I2C1 Clock Input/Output
ASDA1	—	14	11	41	45	—	14	11	41	45	I/O	I^2C	Alternate I2C1 Data Input/Output
AVDD	20	28	25	17	18	20	28	25	17	18	P	—	A/D Supply Pins
AVSS	19	27	24	16	17	19	27	24	16	17	P	—	A/D Supply Pins
C1INA	8	7	4	24	26	8	7	4	24	26	I	ANA	Comparator 1 Input A (+)
C1INB	7	6	3	23	25	7	6	3	23	25	I	ANA	Comparator 1 Input B (-)
C1INC	5	5	2	22	24	5	5	2	22	24	I	ANA	Comparator 1 Input C (+)
C1IND	4	4	1	21	23	4	4	1	21	23	I	ANA	Comparator 1 Input D (-)

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C = I^2C/SMBus input buffer

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TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
C1OUT	17	25	22	14	15	17	25	22	14	15	O	—	Comparator 1 Output
C2INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Comparator 2 Input A (+)
C2INB	—	4	1	21	23	—	4	1	21	23	I	ANA	Comparator 2 Input B (-)
C2INC	—	7	4	24	26	—	7	4	24	26	I	ANA	Comparator 2 Input C (+)
C2IND	—	6	3	23	25	—	6	3	23	25	I	ANA	Comparator 2 Input D (-)
C2OUT	—	20	17	7	7	—	16	13	43	47	O	—	Comparator 2 Output
C3INA	—	26	23	15	16	—	26	23	15	16	I	ANA	Comparator 3 Input A (+)
C3INB	—	25	22	14	15	—	25	22	14	15	I	ANA	Comparator 3 Input B (-)
C3INC	—	2	27	19	21	—	2	27	19	21	I	ANA	Comparator 3 Input C (+)
C3IND	—	4	1	21	23	—	4	1	21	23	I	ANA	Comparator 3 Input D (-)
C3OUT	—	17	14	44	48	—	17	14	44	48	O	—	Comparator 3 Output
CLC1O	13	18	15	1	1	13	18	15	1	1	O	—	CLC1 Output
CLC2O	—	19	16	6	6	—	19	16	6	6	O	—	CLC2 Output
CLCINA	9	14	11	41	45	9	14	11	41	45	I	ST	CLC External Input A
CLCINB	10	15	12	42	46	10	15	12	42	46	I	ST	CLC External Input B
CLKI	7	9	6	30	33	7	9	6	30	33	I	ANA	Primary Clock Input
CLKO	8	10	7	31	34	8	10	7	31	34	O	—	System Clock Output
CN0	10	12	9	34	37	10	12	9	34	37	I	ST	Interrupt-on-Change Inputs
CN1	9	11	8	33	36	9	11	8	33	36	I	ST	Interrupt-on-Change Inputs
CN2	2	2	27	19	21	2	2	27	19	21	I	ST	Interrupt-on-Change Inputs
CN3	3	3	28	20	22	3	3	28	20	22	I	ST	Interrupt-on-Change Inputs
CN4	4	4	1	21	23	4	4	1	21	23	I	ST	Interrupt-on-Change Inputs
CN5	5	5	2	22	24	5	5	2	22	24	I	ST	Interrupt-on-Change Inputs
CN6	6	6	3	23	25	6	6	3	23	25	I	ST	Interrupt-on-Change Inputs
CN7	—	7	4	24	26	—	7	4	24	26	I	ST	Interrupt-on-Change Inputs
CN8	14	20	17	7	7	—	—	—	—	—	I	ST	Interrupt-on-Change Inputs
CN9	—	19	16	6	6	—	19	16	6	6	I	ST	Interrupt-on-Change Inputs
CN10	—	—	—	27	29	—	—	—	27	29	I	ST	Interrupt-on-Change Inputs
CN11	18	26	23	15	16	18	26	23	15	16	I	ST	Interrupt-on-Change Inputs
CN12	17	25	22	14	15	17	25	22	14	15	I	ST	Interrupt-on-Change Inputs

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C = I^2C/SMBus input buffer

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TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CN13	16	24	21	11	12	16	24	21	11	12	I	ST	Interrupt-on-Change Inputs
CN14	15	23	20	10	11	15	23	20	10	11	I	ST	Interrupt-on-Change Inputs
CN15	—	22	19	9	10	—	22	19	9	10	I	ST	Interrupt-on-Change Inputs
CN16	—	21	18	8	9	—	21	18	8	9	I	ST	Interrupt-on-Change Inputs
CN17	—	—	—	3	3	—	—	—	3	3	I	ST	Interrupt-on-Change Inputs
CN18	—	—	—	2	2	—	—	—	2	2	I	ST	Interrupt-on-Change Inputs
CN19	—	—	—	5	5	—	—	—	5	5	I	ST	Interrupt-on-Change Inputs
CN20	—	—	—	4	4	—	—	—	4	4	I	ST	Interrupt-on-Change Inputs
CN21	13	18	15	1	1	13	18	15	1	1	I	ST	Interrupt-on-Change Inputs
CN22	12	17	14	44	48	12	17	14	44	48	I	ST	Interrupt-on-Change Inputs
CN23	11	16	13	43	47	11	16	13	43	47	I	ST	Interrupt-on-Change Inputs
CN24	—	15	12	42	46	—	15	12	42	46	I	ST	Interrupt-on-Change Inputs
CN25	—	—	—	37	40	—	—	—	37	40	I	ST	Interrupt-on-Change Inputs
CN26	—	—	—	38	41	—	—	—	38	41	I	ST	Interrupt-on-Change Inputs
CN27	—	14	11	41	45	—	14	11	41	45	I	ST	Interrupt-on-Change Inputs
CN28	—	—	—	36	39	—	—	—	36	39	I	ST	Interrupt-on-Change Inputs
CN29	8	10	7	31	34	8	10	7	31	34	I	ST	Interrupt-on-Change Inputs
CN30	7	9	6	30	33	7	9	6	30	33	I	ST	Interrupt-on-Change Inputs
CN31	—	—	—	26	28	—	—	—	26	28	I	ST	Interrupt-on-Change Inputs
CN32	—	—	—	25	27	—	—	—	25	27	I	ST	Interrupt-on-Change Inputs
CN33	—	—	—	32	35	—	—	—	32	35	I	ST	Interrupt-on-Change Inputs
CN34	—	—	—	35	38	—	—	—	35	38	I	ST	Interrupt-on-Change Inputs
CN35	—	—	—	12	13	—	—	—	12	13	I	ST	Interrupt-on-Change Inputs
CN36	—	—	—	13	14	—	—	—	13	14	I	ST	Interrupt-on-Change Inputs
CTCMP	4	4	1	21	23	4	4	1	21	23	I	ANA	CTMU Comparator Input

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C = I^2C/SMBus input buffer

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TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CTED1	11	20	17	7	7	11	2	27	19	21	I	ST	CTMU Trigger Edge Inputs
CTED2	15	23	20	10	11	15	23	20	10	11	I	ST	CTMU Trigger Edge Inputs
CTED3	—	19	16	6	6	—	19	16	6	6	I	ST	CTMU Trigger Edge Inputs
CTED4	13	18	15	1	1	13	18	15	1	1	I	ST	CTMU Trigger Edge Inputs
CTED5	17	25	22	14	15	17	25	22	14	15	I	ST	CTMU Trigger Edge Inputs
CTED6	18	26	23	15	16	18	26	23	15	16	I	ST	CTMU Trigger Edge Inputs
CTED7	—	—	—	5	5	—	—	—	5	5	I	ST	CTMU Trigger Edge Inputs
CTED8	—	—	—	13	14	—	—	—	13	14	I	ST	CTMU Trigger Edge Inputs
CTED9	—	22	19	9	10	—	22	19	9	10	I	ST	CTMU Trigger Edge Inputs
CTED10	12	17	14	44	48	12	17	14	44	48	I	ST	CTMU Trigger Edge Inputs
CTED11	—	21	18	8	9	—	21	18	8	9	I	ST	CTMU Trigger Edge Inputs
CTED12	5	5	2	22	24	5	5	2	22	24	I	ST	CTMU Trigger Edge Inputs
CTED13	6	6	3	23	25	6	6	3	23	25	I	ST	CTMU Trigger Edge Inputs
CTPLS	16	24	21	11	12	16	24	21	11	12	O	—	CTMU Pulse Output
CVREF	17	25	22	14	15	17	25	22	14	15	O	ANA	Comparator Voltage Reference Output
CVREF+	2	2	27	19	21	2	2	27	19	21	I	ANA	Comparator Voltage Reference Positive Input
CVREF-	3	3	28	20	22	3	3	28	20	22	I	ANA	Comparator Voltage Reference Negative Input
DAC1OUT	—	23	20	10	11	—	23	20	10	11	O	ANA	DAC1 Output
DAC1REF+	—	2	27	19	21	—	2	27	19	21	I	ANA	DAC1 Positive Voltage Reference Input
DAC2OUT	—	25	22	14	15	—	25	22	14	15	O	ANA	DAC2 Output
DAC2REF+	—	26	23	15	16	—	26	23	15	16	I	ANA	DAC2 Positive Voltage Reference Input
HLVDIN	15	23	20	10	11	15	23	20	10	11	I	ANA	External High/Low-Voltage Detect Input
IC1	14	19	16	6	6	11	19	16	6	6	I	ST	MCCP1 Input Capture Input
IC2	13	18	15	1	1	13	18	15	1	1	I	ST	MCCP2 Input Capture Input
IC3	—	23	20	13	14	—	23	20	13	14	I	ST	MCCP3 Input Capture Input
IC4	—	14	11	5	5	—	14	11	5	5	I	ST	SCCP4 Input Capture Input
IC5	—	15	12	12	13	—	15	12	12	13	I	ST	SCCP5 Input Capture Input
INT0	11	16	13	43	47	11	16	13	43	47	I	ST	External Interrupt 0 Input
INT1	17	25	22	14	15	17	25	22	14	15	I	ST	External Interrupt 1 Input
INT2	14	20	17	7	7	15	23	20	10	11	I	ST	External Interrupt 2 Input

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	Pin Number					Pin Number							
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$\overline{\text{MCLR}}$	1	1	26	18	19	1	1	26	18	19	I	ST	Master Clear (Device Reset) Input (active-low)
OA1INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 1 Input A
OA1INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 1 Input B
OA1INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 1 Input C
OA1IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 1 Input D
OA1OUT	—	7	4	24	26	—	7	4	24	26	O	ANA	Op Amp 1 Analog Output
OA2INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 2 Input A
OA2INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 2 Input B
OA2INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 2 Input C
OA2IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 2 Input D
OA2OUT	—	26	23	15	16	—	26	23	15	16	O	ANA	Op Amp 2 Analog Output
OC1A	14	20	17	7	7	11	16	13	43	47	O	—	MCCP1 Output Compare A
OC1B	12	17	14	44	48	12	17	14	44	48	O	—	MCCP1 Output Compare B
OC1C	15	21	18	8	9	15	21	18	8	9	O	—	MCCP1 Output Compare C
OC1D	16	24	21	11	12	16	24	21	11	12	O	—	MCCP1 Output Compare D
OC1E	—	14	11	41	45	—	14	11	41	45	O	—	MCCP1 Output Compare E
OC1F	—	15	12	42	46	—	15	12	42	46	O	—	MCCP1 Output Compare F
OC2A	4	22	19	9	10	4	22	19	9	10	O	—	MCCP2 Output Compare A
OC2B	—	23	20	10	11	—	23	20	10	11	O	—	MCCP2 Output Compare B
OC2C	—	—	—	2	2	—	—	—	2	2	O	—	MCCP2 Output Compare C
OC2D	—	—	—	3	3	—	—	—	3	3	O	—	MCCP2 Output Compare D
OC2E	—	—	—	4	4	—	—	—	4	4	O	—	MCCP2 Output Compare E
OC2F	—	—	—	5	5	—	—	—	5	5	O	—	MCCP2 Output Compare F
OC3A	—	21	18	12	13	—	21	18	12	13	O	—	MCCP3 Output Compare A
OC3B	—	24	21	13	14	—	24	21	13	14	O	—	MCCP3 Output Compare B
OC4	—	18	15	1	1	—	18	15	1	1	O	—	SCCP4 Output Compare
OC5	—	19	16	6	6	—	19	16	6	6	O	—	SCCP5 Output Compare
OCFA	17	25	22	14	15	17	25	22	14	15	I	ST	MCCP/SCCP Output Compare Fault Input A
OCFB	16	24	21	32	35	16	24	21	32	35	I	ST	MCCP/SCCP Output Compare Fault Input B

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	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
OSCI	7	9	6	30	33	7	9	6	30	33	I	ANA	Primary Oscillator Input
OSCO	8	10	7	31	34	8	10	7	31	34	O	ANA	Primary Oscillator Output
PGEC1	5	5	2	22	24	5	5	2	22	24	I/O	ST	ICSP™ Clock 1
PGED1	4	4	1	21	23	4	4	1	21	23	I/O	ST	ICSP Data 1
PGEC2	2	22	19	9	10	2	22	19	9	10	I/O	ST	ICSP Clock 2
PGED2	3	21	18	8	9	3	21	18	8	9	I/O	ST	ICSP Data 2
PGEC3	10	15	12	42	46	10	15	12	42	46	I/O	ST	ICSP Clock 3
PGED3	9	14	11	41	45	9	14	11	41	45	I/O	ST	ICSP Data 3
PWRLCLK	10	12	9	34	37	10	12	9	34	37	I	ST	RTCC Power Line Clock Input
RA0	2	2	27	19	21	2	2	27	19	21	I/O	ST	PORTA Pins
RA1	3	3	28	20	22	3	3	28	20	22	I/O	ST	PORTA Pins
RA2	7	9	6	30	33	7	9	6	30	33	I/O	ST	PORTA Pins
RA3	8	10	7	31	34	8	10	7	31	34	I/O	ST	PORTA Pins
RA4	10	12	9	34	37	10	12	9	34	37	I/O	ST	PORTA Pins
RA5	1	1	26	18	19	1	1	26	18	19	I/O	ST	PORTA Pins
RA6	14	20	17	7	7	—	—	—	—	—	I/O	ST	PORTA Pins
RA7	—	19	16	6	6	—	19	16	6	6	I/O	ST	PORTA Pins
RA8	—	—	—	32	35	—	—	—	32	35	I/O	ST	PORTA Pins
RA9	—	—	—	35	38	—	—	—	35	38	I/O	ST	PORTA Pins
RA10	—	—	—	12	13	—	—	—	12	13	I/O	ST	PORTA Pins
RA11	—	—	—	13	14	—	—	—	13	14	I/O	ST	PORTA Pins
RB0	4	4	1	21	23	4	4	1	21	23	I/O	ST	PORTB Pins
RB1	5	5	2	22	24	5	5	2	22	24	I/O	ST	PORTB Pins
RB2	6	6	3	23	25	6	6	3	23	25	I/O	ST	PORTB Pins
RB3	—	7	4	24	26	—	7	4	24	26	I/O	ST	PORTB Pins
RB4	9	11	8	33	36	9	11	8	33	36	I/O	ST	PORTB Pins
RB5	—	14	11	41	45	—	14	11	41	45	I/O	ST	PORTB Pins
RB6	—	15	12	42	46	—	15	12	42	46	I/O	ST	PORTB Pins
RB7	11	16	13	43	47	11	16	13	43	47	I/O	ST	PORTB Pins
RB8	12	17	14	44	48	12	17	14	44	48	I/O	ST	PORTB Pins

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C = I^2C/SMBus input buffer

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TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
RB9	13	18	15	1	1	13	18	15	1	1	I/O	ST	PORTB Pins
RB10	—	21	18	8	9	—	21	18	8	9	I/O	ST	PORTB Pins
RB11	—	22	19	9	10	—	22	19	9	10	I/O	ST	PORTB Pins
RB12	15	23	20	10	11	15	23	20	10	11	I/O	ST	PORTB Pins
RB13	16	24	21	11	12	16	24	21	11	12	I/O	ST	PORTB Pins
RB14	17	25	22	14	15	17	25	22	14	15	I/O	ST	PORTB Pins
RB15	18	26	23	15	16	18	26	23	15	16	I/O	ST	PORTB Pins
RC0	—	—	—	25	27	—	—	—	25	27	I/O	ST	PORTC Pins
RC1	—	—	—	26	28	—	—	—	26	28	I/O	ST	PORTC Pins
RC2	—	—	—	27	29	—	—	—	27	29	I/O	ST	PORTC Pins
RC3	—	—	—	36	39	—	—	—	36	39	I/O	ST	PORTC Pins
RC4	—	—	—	37	40	—	—	—	37	40	I/O	ST	PORTC Pins
RC5	—	—	—	38	41	—	—	—	38	41	I/O	ST	PORTC Pins
RC6	—	—	—	2	2	—	—	—	2	2	I/O	ST	PORTC Pins
RC7	—	—	—	3	3	—	—	—	3	3	I/O	ST	PORTC Pins
RC8	—	—	—	4	4	—	—	—	4	4	I/O	ST	PORTC Pins
RC9	—	—	—	5	5	—	—	—	5	5	I/O	ST	PORTC Pins
REFO	18	26	23	15	16	18	26	23	15	16	O	—	Reference Clock Output
RTCC	—	25	22	14	15	—	25	22	14	15	O	—	Real-Time Clock/Calendar Output
SCK1	15	22	19	9	10	15	22	19	9	10	I/O	ST	MSSP1 SPI Clock
SDI1	17	21	18	8	9	17	21	18	8	9	I	ST	MSSP1 SPI Data Input
SDO1	16	24	21	11	12	16	24	21	11	12	O	—	MSSP1 SPI Data Output
$\overline{SS1}$	18	26	23	15	16	18	26	23	15	16	I	ST	MSSP1 SPI Slave Select Input
SCK2	—	14	11	38	41	—	14	11	38	41	I/O	ST	MSSP2 SPI Clock
SDI2	—	19	16	36	39	—	19	16	36	39	I	ST	MSSP2 SPI Data Input
SDO2	—	15	12	37	40	—	15	12	37	40	O	—	MSSP2 SPI Data Output
$\overline{SS2}$	—	23	20	35	38	—	23	20	35	38	I	ST	MSSP2 SPI Slave Select Input

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C = I^2C/SMBus input buffer

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TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
SCL1	12	17	14	44	48	12	17	14	44	48	I/O	I2C	MSSP1 I^2C Clock
SDA1	13	18	15	1	1	13	18	15	1	1	I/O	I2C	MSSP1 I^2C Data
SCL2	—	7	4	24	26	—	7	4	24	26	I/O	I2C	MSSP2 I^2C Clock
SDA2	—	6	3	23	25	—	6	3	23	25	I/O	I2C	MSSP2 I^2C Data
SCLKI	10	12	9	34	37	10	12	9	34	37	I	ST	Secondary Clock Digital Input
SOSCI	9	11	8	33	36	9	11	8	33	36	I	ANA	Secondary Oscillator Input
SOSCO	10	12	9	34	37	10	12	9	34	37	I	ANA	Secondary Oscillator Output
T1CK	13	18	15	1	1	13	18	15	1	1	I	ST	Timer1 Digital Input Cock
TCKIA	18	26	23	15	16	18	26	23	15	16	I	ST	MCCP/SCCP Time Base Clock Input A
TCKIB	6	6	3	23	25	6	6	3	23	25	I	ST	MCCP/SCCP Time Base Clock Input B
$\overline{\text{U1CTS}}$	12	17	14	44	48	12	17	14	44	48	I	ST	UART1 Clear-to-Send Input
$\overline{\text{U1RTS}}$	13	18	15	1	1	13	18	15	1	1	O	—	UART1 Request-to-Send Output
U1BCLK	13	18	15	1	1	13	18	15	1	1	O	—	UART1 16x Baud Rate Clock Output
U1RX	6	6	3	2	2	6	6	3	2	2	I	ST	UART1 Receive
U1TX	11	16	13	3	3	11	16	13	3	3	O	—	UART1 Transmit
$\overline{\text{U2CTS}}$	—	12	9	34	37	—	12	9	34	37	I	ST	UART2 Clear-to-Send Input
$\overline{\text{U2RTS}}$	—	11	8	33	36	—	11	8	33	36	O	—	UART2 Request-to-Send Output
U2BCLK	13	18	15	1	1	13	18	15	1	1	O	—	UART2 16x Baud Rate Clock Output
U2RX	—	5	2	22	24	—	5	2	22	24	I	ST	UART2 Receive
U2TX	—	4	1	21	23	—	4	1	21	23	O	—	UART2 Transmit
ULPWU	4	4	1	21	23	4	4	1	21	23	I	ANA	Ultra Low-Power Wake-up Input
V_{CAP}	—	—	—	—	—	14	20	17	7	7	P	—	Regulator External Filter Capacitor Connection
V_{DD}	20	28	25	17,28,28	18,30,30	20	28	25	17,28,28	18,30,30	P	—	Device Positive Supply Voltage
V_{DDCORE}	—	—	—	—	—	14	20	17	7	7	P	—	Microcontroller Core Supply Voltage
V_{PP}	1	1	26	18	19	1	1	26	18	19	P	—	High-Voltage Programming Pin
V_{REF+}	2	2	27	19	21	2	2	27	19	21	I	ANA	A/D Reference Voltage Positive Input
V_{REF-}	3	3	28	20	22	3	3	28	20	22	I	ANA	A/D Reference Voltage Negative Input
V_{SS}	19	27	24	16,29,29	17,31,31	19	27	24	16,29,29	17,31,31	P	—	Device Ground Return Voltage

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C = I^2C/SMBus input buffer

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NOTES:

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2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24FV16KM204 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Power Supply Pins"**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used
  (see **Section 2.2 "Power Supply Pins"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pins
  (see **Section 2.4 "Voltage Regulator Pin (VCAP)"**)

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

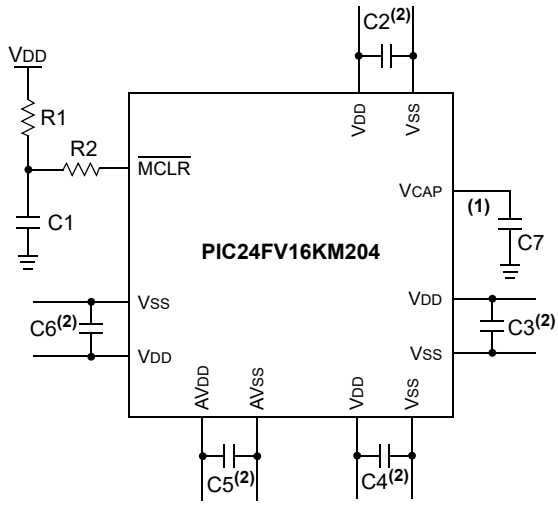
Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

Note:	The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 µF, 20V ceramic

C7: 10 µF, 16V tantalum or ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

Note 1: See **Section 2.4 "Voltage Regulator Pin (VCAP)"** for an explanation of VCAP pin connections.

2: The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 µF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 µF in parallel with 0.001 µF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

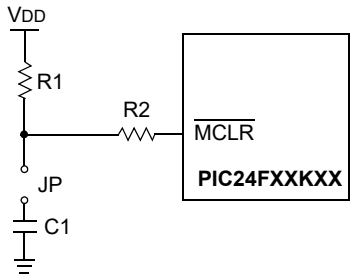
2.3 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



Note 1: R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{\text{MCLR}}$ pin VIH and VIL specifications are met.

2: R2 ≤ 470Ω will limit any current flowing into $\overline{\text{MCLR}}$ from the external capacitor, C, in the event of $\overline{\text{MCLR}}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{\text{MCLR}}$ pin VIH and VIL specifications are met.

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2.4 Voltage Regulator Pin (VCAP)

Note: This section applies only to PIC24FV16KM devices with an on-chip voltage regulator.

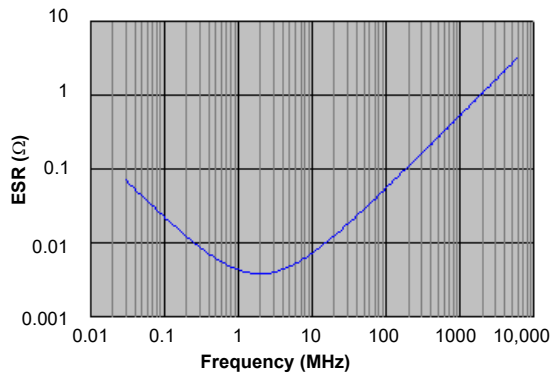
Some of the PIC24FV16KM devices have an internal voltage regulator. These devices have the voltage regulator output brought out on the VCAP pin. On the PIC24F K devices with regulators, a low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the voltage regulator output. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 27.0 "Electrical Characteristics"** for additional information.

Refer to **Section 27.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to +125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to +85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

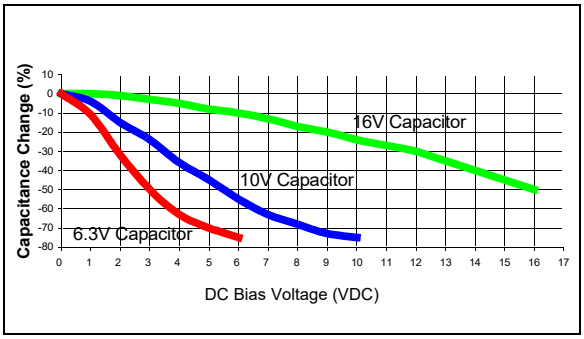
Typical low-cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 3.3V or 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pins, Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 26.0 "Development Support"**.

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2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to for **Section 9.0 "Oscillator Configuration"**details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-5. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins and other signals, in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

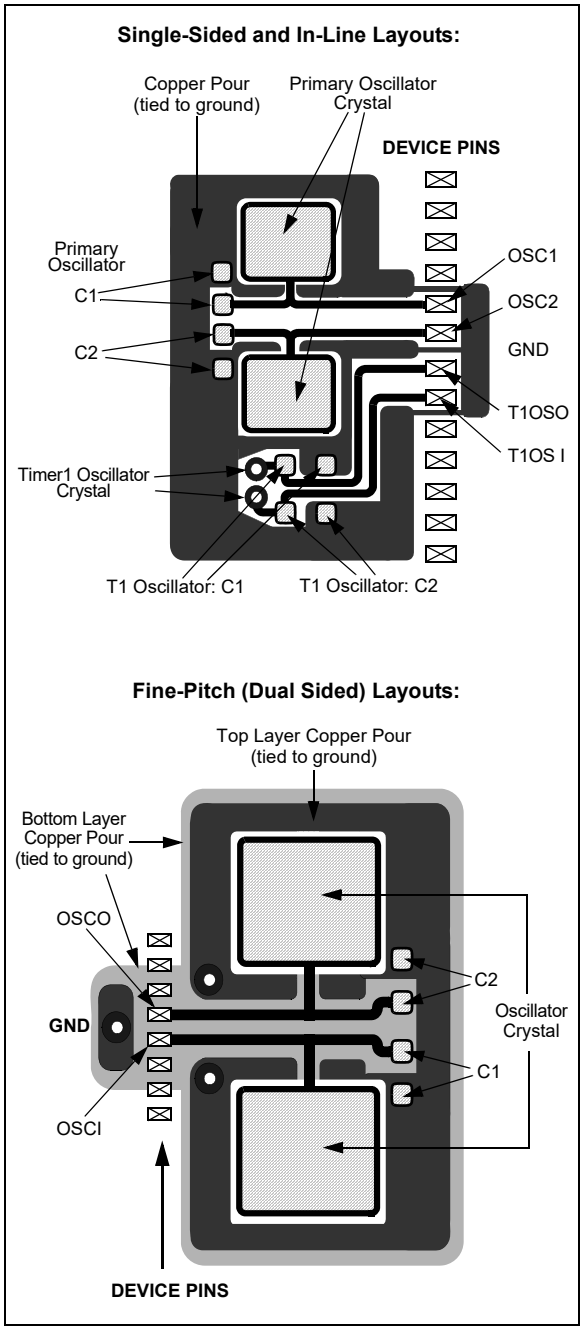
For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- *AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- *AN849, "Basic PICmicro® Oscillator Design"*
- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*

2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a Logic Low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output to logic low.

FIGURE 2-5: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



NOTES:

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3.0 CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to **"CPU"** (www.microchip.com/DS39703) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `REPEAT` instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into program space at any 16K word boundary of either program memory or data EEPROM memory, defined by the 8-bit Program Space Visibility Page Address (PSVPAG) register. The program to Data Space mapping feature lets any instruction access program space as if it were Data Space.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs.

The core supports Inherent (no operand), Relative, Literal, Memory Direct and three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a Working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (i.e., A + B = C) to be executed in a single cycle.

A high-speed, 17-bit by 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit by 16-bit or 8-bit by 8-bit integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the `REPEAT` instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to eight sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is illustrated in Figure 3-1.

3.1 Programmer's Model

Figure 3-2 displays the programmer's model for the PIC24F. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions.

Table 3-1 provides a description of each register. All registers associated with the programmer's model are memory mapped.

FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM

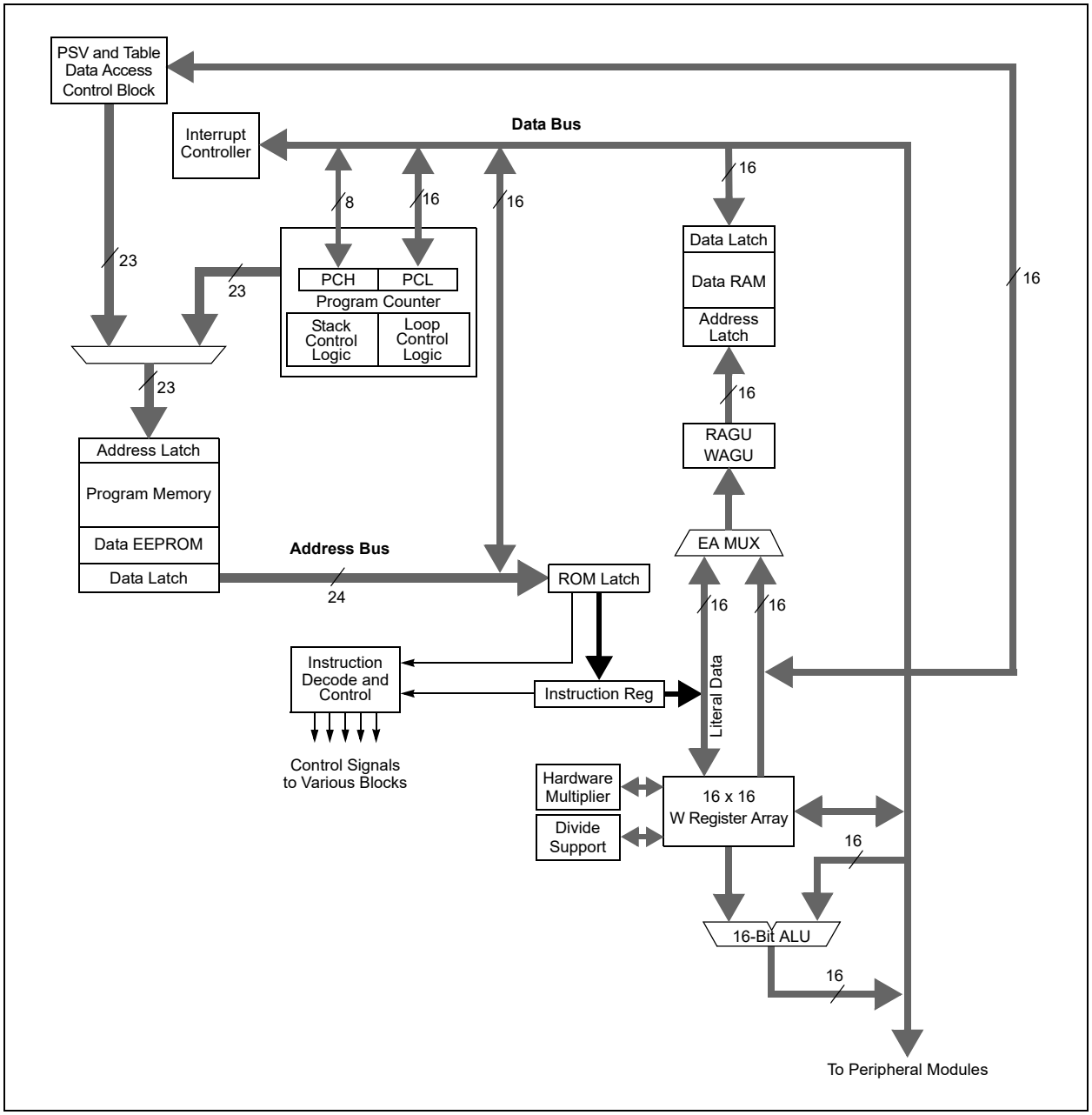

TABLE 3-1: CPU CORE REGISTERS

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
PSVPAG	Program Space Visibility Page Address Register
RCOUNT	`REPEAT` Loop Counter Register
CORCON	CPU Control Register

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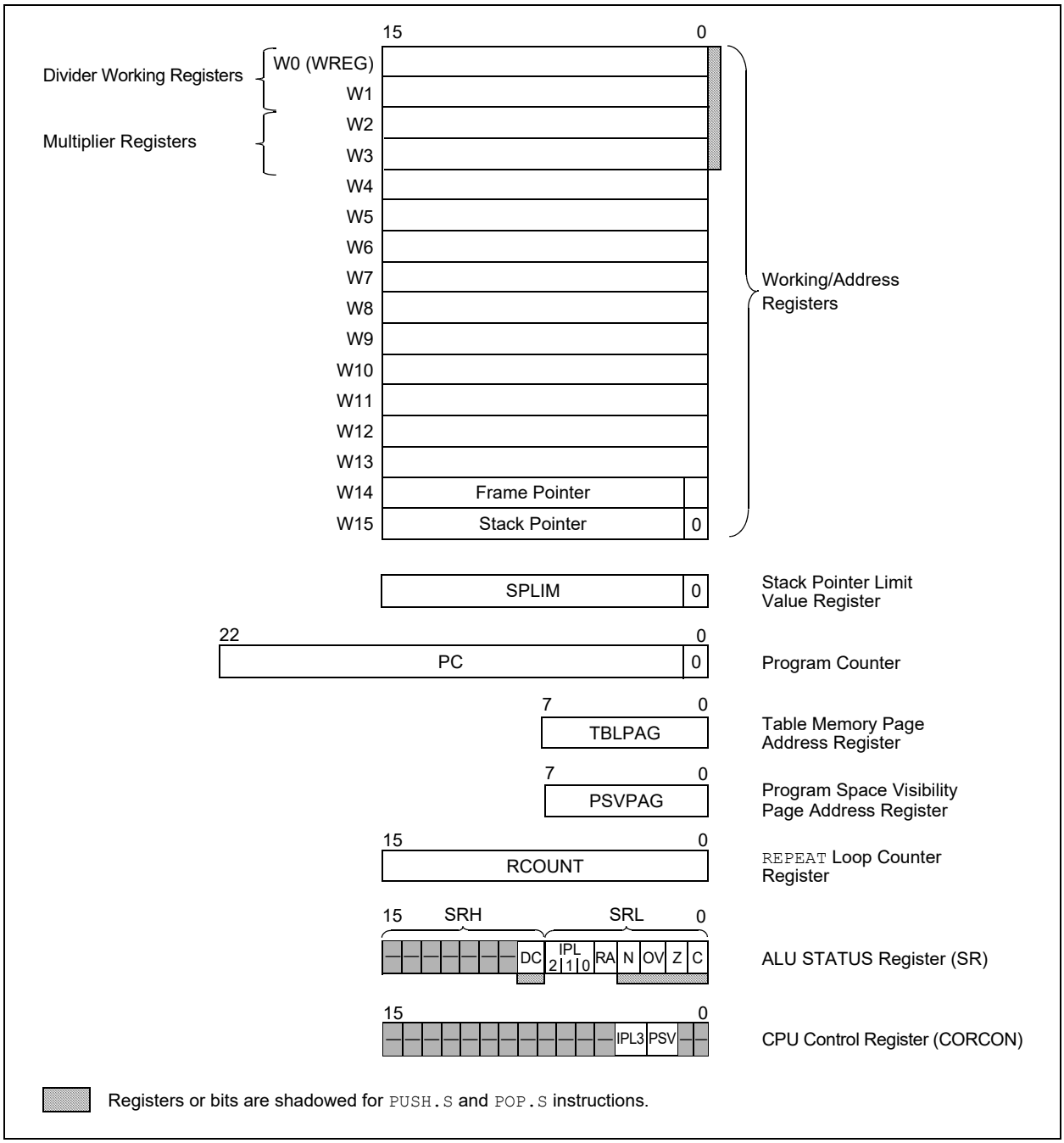
FIGURE 3-2: PROGRAMMER'S MODEL



3.2 CPU Control Registers

REGISTER 3-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	HSC/R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

HSC/R/W-0(1)	HSC/R/W-0(1)	HSC/R/W-0(1)	HSC/R-0	HSC/R/W-0	HSC/R/W-0	HSC/R/W-0	HSC/R/W-0
IPL2(2)	IPL1(2)	IPL0(2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8 **DC:** ALU Half Carry/Borrow bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th or 8th low-order bit of the result has occurred

bit 7-5 **IPL[2:0]:** CPU Interrupt Priority Level Status bits(1,2)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** ALU Negative bit
1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** ALU Overflow bit
1 = Overflow occurred for signed (two’s complement) arithmetic in this arithmetic operation
0 = No overflow has occurred

bit 1 **Z:** ALU Zero bit
1 = An operation, which effects the Z bit, has set it at some time in the past
0 = The most recent operation, which effects the Z bit, has cleared it (i.e., a non-zero result)

bit 0 **C:** ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the Most Significant bit (MSb) of the result occurred
0 = No carry-out from the Most Significant bit (MSb) of the result occurred

Note 1: The IPLx Status bits are read-only when NSTDIS (INTCON1[15]) = 1.
2: The IPL[2:0] Status bits are concatenated with the IPL3 bit (CORCON[3]) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

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REGISTER 3-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	HSC/R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3[1]	PSV	—	—
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit[1]
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
1 = Program space is visible in Data Space
0 = Program space is not visible in Data Space

bit 1-0 **Unimplemented:** Read as ‘0’

Note 1: User interrupts are disabled when IPL3 = 1.

3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware division for 16-bit divisor.

3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.3.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

1. 32-bit signed/16-bit signed divide
2. 32-bit unsigned/16-bit unsigned divide
3. 16-bit signed/16-bit signed divide
4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. Sixteen-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn), and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.3.3 MULTIBIT SHIFT SUPPORT

The PIC24F ALU supports both single bit and single-cycle, multibit arithmetic and logic shifts. Multibit shifts are implemented using a shifter block, capable of performing up to a 15-bit arithmetic right shift, or up to a 15-bit left shift, in a single cycle. All multibit shift instructions only support Register Direct Addressing for both the operand source and result destination.

A full summary of instructions that use the shift operation is provided in Table 3-2.

TABLE 3-2: INSTRUCTIONS THAT USE THE SINGLE AND MULTIBIT SHIFT OPERATION

Instruction	Description
`ASR`	Arithmetic shift right source register by one or more bits.
`SL`	Shift left source register by one or more bits.
`LSR`	Logical shift right source register by one or more bits.

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4.0 MEMORY ORGANIZATION

As with Harvard architecture devices, the PIC24F microcontrollers feature separate program and data memory space and busing. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

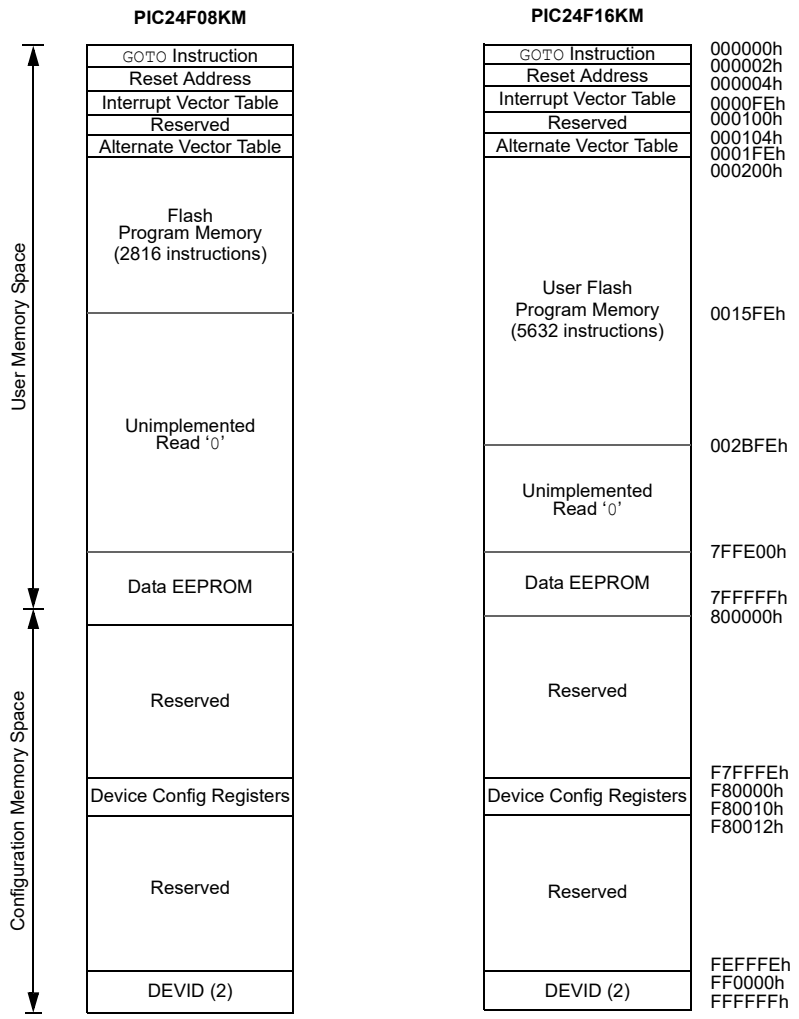
4.1 Program Address Space

The program address memory space of the PIC24F devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from a table operation or Data Space remapping, as described in **Section 4.3 "Interfacing Program and Data Memory Spaces"**.

The user access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of `TBLRD/TBLWT` operations, which use TBLPAG[7] to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for the PIC24FV16KM204 family of devices are displayed in Figure 4-1.

FIGURE 4-1: PROGRAM SPACE MEMORY MAP FOR PIC24FXXXXX FAMILY DEVICES



Note: Memory areas are not displayed to scale.

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with Data Memory Space Addressing and makes it possible to access data in the program memory space.

4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 00000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user at 000000h with the actual address for the start of code at 000002h.

PIC24F devices also have two Interrupt Vector Tables, located from 000004h to 0000FFh, and 000104h to 0001FFh. These vector tables allow each of the many device interrupt sources to be handled by separate ISRs. **Section 8.1 "Interrupt Vector Table (IVT)"** discusses the Interrupt Vector Tables in more detail.

4.1.3 DATA EEPROM

In the PIC24FV16KM204 family, the data EEPROM is mapped to the top of the user program memory space, starting at address, 7FFE00, and expanding up to address, 7FFFFF.

The data EEPROM is organized as 16-bit wide memory and 256 words deep. This memory is accessed using Table Read and Write operations similar to the user code memory.

4.1.4 DEVICE CONFIGURATION WORDS

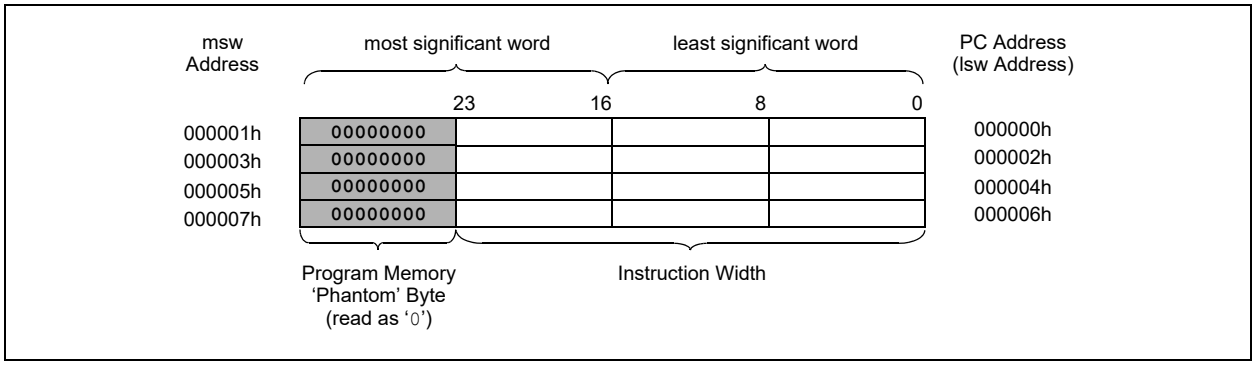
Table 4-1 provides the addresses of the device Configuration Words for the PIC24FV16KM204 family. Their location in the memory map is displayed in Figure 4-1.

Refer to **Section 25.1 "Configuration Bits"** for more information on device Configuration Words.

TABLE 4-1: DEVICE CONFIGURATION WORDS FOR PIC24FXXXXX FAMILY DEVICES

Configuration Word	Configuration Word Addresses
FBS	F80000
FGS	F80004
FOSCSEL	F80006
FOSC	F80008
FWDT	F8000A
FPOR	F8000C
FICD	F8000E

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION



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4.2 Data Address Space

The PIC24F core has a separate, 16-bit wide data memory space, addressable as a single linear range. The Data Space is accessed using two Address Generation Units (AGUs), one each for read and write operations. The Data Space memory map is displayed in Figure 4-3.

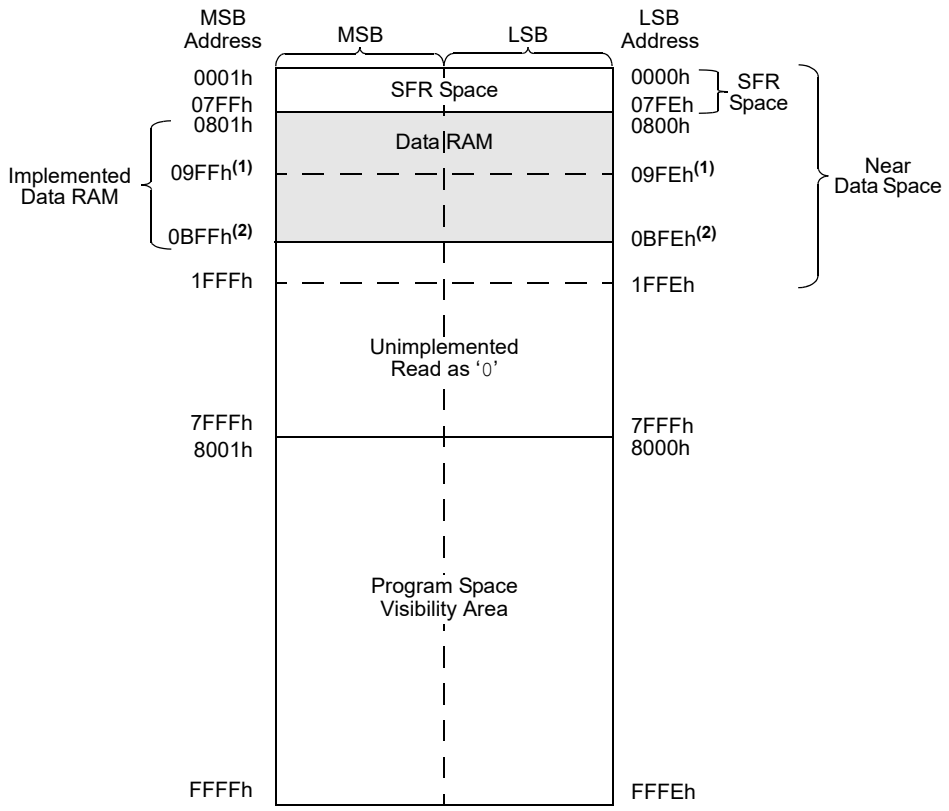
All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This gives a Data Space address range of 64 Kbytes or 32K words. The lower half of the data memory space (that is, when EA[15] = 0) is used for implemented memory addresses, while the upper half (EA[15] = 1) is reserved for the Program Space Visibility (PSV) area (see **Section 4.3.3 "Reading Data from Program Memory Using Program Space Visibility"**).

Depending on the particular device, PIC24FV16KM family devices implement either 512 or 1024 words of data memory. Should an EA point to a location outside of this area, an all zero word or byte will be returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data are aligned in data memory and registers as 16-bit words, but all the Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

FIGURE 4-3: DATA SPACE MEMORY MAP FOR PIC24FXXXXX FAMILY DEVICES(3)



Note 1: Upper data memory boundary for PIC24FXXKM10X devices.
2: Upper data memory boundary for PIC24FXXKM20X devices.
3: Data memory areas are not shown to scale.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® devices and improve Data Space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all EA calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, the data memory and the registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register, which matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed, but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (`SE`) instruction is provided to allow the users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (`ZE`) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

4.2.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the Data Space is addressable indirectly. Additionally, the whole Data Space is addressable using `MOV` instructions, which support Memory Direct Addressing (MDA) with a 16-bit address field. For PIC24FV16KM204 family devices, the entire implemented data memory lies in Near Data Space (NDS).

4.2.4 SFR SPACE

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by that module. Much of the SFR space contains unused addresses; these are read as '`0`'. The SFR space, where the SFRs are actually implemented, is provided in Table 4-2. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR. A complete listing of implemented SFRs, including their addresses, is provided in Table 4-3 through Table 4-26.

TABLE 4-2: IMPLEMENTED REGIONS OF SFR DATA SPACE

	SFR Space Address							
	xx00	**xx20**	**xx40**	**xx60**	**xx80**	**xxA0**	**xxC0**	**xxE0**
000h	Core			ICN	Interrupts			—
100h	Timers	CLC	MCCP/SCCP					
200h	MSSP	UART	Op Amp	DAC	—	—	I/O	
300h	A/D/CMTU				—	—	—	—
400h	—	—	—	—	—	—	—	ANSEL
500h	—	—	—	—	—	—	—	—
600h	—	RTCC/Comp	—	Band Gap	—			
700h	—	—	System/ HLVD	NVM/PMD	—	—	—	—

Legend: — = No implemented SFRs in this block.

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TABLE 4-3: CPU CORE REGISTERS MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
WREG0	0h	WREG0																0000
WREG1	2h	WREG1																0000
WREG2	4h	WREG2																0000
WREG3	6h	WREG3																0000
WREG4	8h	WREG4																0000
WREG5	Ah	WREG5																0000
WREG6	Ch	WREG6																0000
WREG7	Eh	WREG7																0000
WREG8	10h	WREG8																0000
WREG9	12h	WREG9																0000
WREG10	14h	WREG10																0000
WREG11	16h	WREG11																0000
WREG12	18h	WREG12																0000
WREG13	1Ah	WREG13																0000
WREG14	1Ch	WREG14																0000
WREG15	1Eh	WREG15																0800
SPLIM	20h	SPLIM Register																xxxx
PCL	2Eh	PCL Register																0000
PCH	30h	—	—	—	—	—	—	—	—	PCH[7:0]								0000
TBLPAG	32h	—	—	—	—	—	—	—	—	TBLPAG[7:0]								0000
PSVPAG	34h	—	—	—	—	—	—	—	—	PSVPAG[7:0]								0000
RCOUNT	36h	RCOUNT Register																xxxx
SR	42h	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000
CORCON	44h	—	—	—	—	—	—	—	—	—	—	—	—	IPL3	PSV	—	—	0000
DISICNT	52h	—	—	DISICNT[13:0]														xxxx

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

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TABLE 4-4: ICN REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNPD1	56h	CN15PDE(1,2)	CN14PDE	CN13PDE	CN12PDE	CN11PDE	CN10PDE(2)	CN9PDE(1,2)	—	CN7PDE(1,2)	CN6PDE	CN5PDE	CN4PDE	CN3PDE	CN2PDE	CN1PDE	CN0PDE	0000
CNPD2	58h	CN31PDE(2)	CN30PDE	CN29PDE	CN28PDE(2)	CN27PDE(1,2)	CN26PDE(2)	CN25PDE(2)	CN24PDE(1,2)	CN23PDE	CN22PDE	CN21PDE	CN20PDE(2)	CN19PDE(2)	CN18PDE(2)	CN17PDE(2)	CN16PDE(1,2)	0000
CNPD3	5Ah	—	—	—	—	—	—	—	—	—	—	—	CN36PDE(2)	CN35PDE(2)	CN34PDE(2)	CN33PDE(2)	CN32PDE(2)	0000
CNEN1	62h	CN15IE(1,2)	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE(2)	CN9IE(1,2)	—	CN7IE(1,2)	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	64h	CN31IE(2)	CN30IE	CN29IE	CN28IE(2)	CN27IE(1,2)	CN26IE(2)	CN25IE(2)	CN24IE(1,2)	CN23IE	CN22IE	CN21IE	CN20IE(2)	CN19IE(2)	CN18IE(2)	CN17IE(2)	CN16IE(1,2)	0000
CNEN3	66h	—	—	—	—	—	—	—	—	—	—	—	CN36IE(2)	CN35IE(2)	CN34IE(2)	CN33IE(2)	CN32IE(2)	0000
CNPU1	6Eh	CN15PUE(1,2)	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE(2)	CN9PUE(1,2)	—	CN7PUE(1,2)	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	70h	CN31PUE(2)	CN30PUE	CN29PUE	CN28PUE(2)	CN27PUE(1,2)	CN26PUE(2)	CN25PUE(2)	CN24PUE(1,2)	CN23PUE	CN22PUE	CN21PUE	CN20PUE(2)	CN19PUE(2)	CN18PUE(2)	CN17PUE(2)	CN16PUE(1,2)	0000
CNPU3	72h	—	—	—	—	—	—	—	—	—	—	—	CN36PUE(2)	CN35PUE(2)	CN34PUE(2)	CN33PUE(2)	CN32PUE(2)	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are available only on 28-pin devices

2: These bits are available only on 44-pin devices

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TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	80h	NSTDIS	—	—	—	—	—	—	—	—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	82h	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	84h	NVMIF	—	AD1IF	U1TXIF	U1RXIF	—	—	CCT2IF	CCT1IF	CCP4IF	CCP3IF	—	T1IF	CCP2IF	CCP1IF	INT0IF	0000
IFS1	86h	U2TXIF	U2RXIF	INT2IF	CCT4IF	CCT3IF	—	—	—	—	CCP5IF	—	INT1IF	CNIF	CMIF	BCL1IF	SSP1IF	0000
IFS2	88h	—	—	—	—	—	—	CCT5IF	—	—	—	—	—	—	—	—	—	0000
IFS3	8Ah	—	RTCIF	—	—	—	—	—	—	—	—	—	—	—	BCL2IF	SSP2IF	—	0000
IFS4	8Ch	DAC2IF	DAC1IF	CTMUIF	—	—	—	—	HLVDIF	—	—	—	—	—	U2ERIF	U1ERIF	—	0000
IFS5	8Eh	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIF	0000
IFS6	90h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLC2IF	CLC1IF	0000
IEC0	94h	NVMIE	—	AD1IE	U1TXIE	U1RXIE	—	—	CCT2IE	CCT1IE	CCP4IE	CCP3IE	—	T1IE	CCP2IE	CCP1IE	INT0IE	0000
IEC1	96h	U2TXIE	U2RXIE	INT2IE	CCT4IE	CCT3IE	—	—	—	—	CCP5IE	—	INT1IE	CNIE	CMIE	BCL1IE	SSP1IE	0000
IEC2	98h	—	—	—	—	—	—	CCT5IE	—	—	—	—	—	—	—	—	—	0000
IEC3	9Ah	—	RTCIE	—	—	—	—	—	—	—	—	—	—	—	BCL2IE	SSP2IE	—	0000
IEC4	9Ch	DAC2IE	DAC1IE	CTMUIE	—	—	—	—	HLVDIE	—	—	—	—	—	U2ERIE	U1ERIE	—	0000
IEC5	9Eh	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIE	0000
IEC6	A0h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLC2IE	CLC1IE	0000
IPC0	A4h	—	T1IP2	T1IP1	T1IP0	—	CCP2IP2	CCP2IP1	CCP2IP0	—	CCP1IP2	CCP1IP1	CCP1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	A6h	—	CCT1IP2	CCT1IP1	CCT1IP0	—	CCP4IP2	CCP4IP1	CCP4IP0	—	CCP3IP2	CCP3IP1	CCP3IP0	—	—	—	—	4440
IPC2	A8h	—	U1RXIP2	U1RXIP1	U1RXIP0	—	—	—	—	—	—	—	—	—	CCT2IP2	CCT2IP1	CCT2IP0	4004
IPC3	AAh	—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4044
IPC4	ACh	—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0	—	BCL1IP2	BCL1IP1	BCL1IP0	—	SSP1IP2	SSP1IP1	SSP1IP0	4444
IPC5	AEh	—	—	—	—	—	CCP5IP2	CCP5IP1	CCP5IP0	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0404
IPC6	B0h	—	CCT3IP2	CCT3IP1	CCT3IP0	—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC7	B2h	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	CCT4IP2	CCT4IP1	CCT4IP0	4444
IPC10	B8h	—	—	—	—	—	—	—	—	—	CCT5IP2	CCT5IP1	CCT5IP0	—	—	—	—	0040
IPC12	BCh	—	—	—	—	—	BCL2IP2	BCL2IP1	BCL2IP0	—	SSP2IP2	SSP2IP1	SSP2IP0	—	—	—	—	0440
IPC15	C2h	—	—	—	—	—	RTCIP2	RTCIP1	RTCIP0	—	—	—	—	—	—	—	—	0400
IPC16	C4h	—	—	—	—	—	U2ERIP2	U2ERIP1	U2ERIP0	—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—	0440
IPC18	C8h	—	—	—	—	—	—	—	—	—	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0	0004
IPC19	CAh	—	DAC2IP2	DAC2IP1	DAC2IP0	—	DAC1IP2	DAC1IP1	DAC1IP0	—	CTMUIP2	CTMUIP1	CTMUIP0	—	—	—	—	4440
IPC20	CCh	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIP2	ULPWUIP1	ULPWUIP0	0004
IPC24	D4h	—	—	—	—	—	—	—	—	—	CLC2IP2	CLC2IP1	CLC2IP0	—	CLC1IP2	CLC1IP1	CLC1IP0	0044
INTTREG	E0h	CPUIRQ	—	VHOLD	—	ILR3	ILR2	ILR1	ILR0	—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

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TABLE 4-6: TIMER1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	100h	Timer1 Register																xxxx
PR1	102h	Timer1 Period Register																FFFF
T1CON	104h	TON	—	TSIDL	—	—	—	TECS1	TECS0	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-7: CLC1-2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CLC1CONL	122h	LCEN	—	—	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE2	MODE1	MODE0	0000
CLC1CONH	124h	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
CLC1SEL	126h	—	DS42	DS41	DS40	—	DS32	DS31	DS30	—	DS22	DS21	DS20	—	DS12	DS11	DS10	0000
CLC1GLSL	12Ah	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
CLC1GLSH	12Ch	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
CLC2CONL(1)	12Eh	LCEN	—	—	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE2	MODE1	MODE0	0000
CLC2CONH(1)	130h	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
CLC2SEL(1)	132h	—	DS42	DS41	DS40	—	DS32	DS31	DS30	—	DS22	DS21	DS20	—	DS12	DS11	DS10	0000
CLC2GLSL(1)	136h	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
CLC2GLSH(1)	138h	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

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TABLE 4-8: MCCP1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP1CON1L	140h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP1CON1H	142h	OPSSRC	RTRGEN	—	—	OPS3	OPS2	OPS1	OPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP1CON2L	144h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP1CON2H	146h	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0	0100
CCP1CON3L	148h	—	—	—	—	—	—	—	—	—		DT[5:0]						0000
CCP1CON3H	14Ah	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2	OUTM1	OUTM0	—	—	POLACE	POLBDF	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0	0000
CCP1STATL	14Ch	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP1TMRL	150h	MCCP1 Time Base Register Low Word																0000
CCP1TMRH	152h	MCCP1 Time Base Register High Word																0000
CCP1PRL	154h	MCCP1 Time Base Period Register Low Word																FFFF
CCP1PRH	156h	MCCP1 Time Base Period Register High Word																FFFF
CCP1RAL	158h	Output Compare 1 Data Word A																0000
CCP1RBL	15Ch	Output Compare 1 Data Word B																0000
CCP1BUFL	160h	Input Capture 1 Data Buffer Low Word																0000
CCP1BUFH	162h	Input Capture 1 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

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TABLE 4-9: MCCP2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP2CON1L	164h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP2CON1H	166h	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP2CON2L	168h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP2CON2H	16Ah	OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICSEL2	ICSEL1	ICSEL0	0100
CCP2CON3L	16Ch	—	—	—	—	—	—	—	—	—		DT[5:0]						0000
CCP2CON3H	16Eh	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2(1)	OUTM1(1)	OUTM0(1)	—	—	POLACE	POLBDF(1)	PSSACE1	PSSACE0	PSSBDF1(1)	PSSBDF0(1)	0000
CCP2STATL	170h	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP2TMRL	174h	MCCP2 Time Base Register Low Word																0000
CCP2TMRH	176h	MCCP2 Time Base Register High Word																0000
CCP2PRL	178h	MCCP2 Time Base Period Register Low Word																FFFF
CCP2PRH	17Ah	MCCP2 Time Base Period Register High Word																FFFF
CCP2RAL	17Ch	Output Compare 2 Data Word A																0000
CCP2RBL	180h	Output Compare 2 Data Word B																0000
CCP2BUFL	184h	Input Capture 2 Data Buffer Low Word																0000
CCP2BUFH	186h	Input Capture 2 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are available only on PIC24F(V)16KM2XX devices.

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TABLE 4-10: MCCP3 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP3CON1L(1)	188h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP3CON1H(1)	18Ah	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP3CON2L(1)	18Ch	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP3CON2H(1)	18Eh	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0	0100
CCP3CON3L(1)	190h	—	—	—	—	—	—	—	—	—	—	DT[5:0]						0000
CCP3CON3H(1)	192h	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2	OUTM1	OUTM0	—	—	POLACE	POLBDF	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0	0000
CCP3STAT(1)	194h	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP3TMRL(1)	198h	MCCP3 Time Base Register Low Word																0000
CCP3TMRH(1)	19Ah	MCCP3 Time Base Register High Word																0000
CCP3PRL(1)	19Ch	MCCP3 Time Base Period Register Low Word																FFFF
CCP3PRH(1)	19Eh	MCCP3 Time Base Period Register High Word																FFFF
CCP3RAL(1)	1A0h	Output Compare 3 Data Word A																0000
CCP3RBL(1)	1A4h	Output Compare 3 Data Word B																0000
CCP3BUFL(1)	1A8h	Input Capture 3 Data Buffer Low Word																0000
CCP3BUFH(1)	1AAh	Input Capture 3 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

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TABLE 4-11: SCCP4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP4CON1L(1)	1ACh	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP4CON1H(1)	1AEh	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP4CON2L(1)	1B0h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP4CON2H(1)	1B2h	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICSEL2	ICSEL1	ICSEL0	0100
CCP4CON3H(1)	1B6h	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	—	—	—	—	—	POLACE	—	PSSACE1	PSSACE0	—	—	0000
CCP4STATL(1)	1B8h	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP4TMRL(1)	1BCh	SCCP4 Time Base Register Low Word																0000
CCP4TMRH(1)	1BEh	SCCP4 Time Base Register High Word																0000
CCP4PRL(1)	1C0h	SCCP4 Time Base Period Register Low Word																FFFF
CCP4PRH(1)	1C2h	SCCP4 Time Base Period Register High Word																FFFF
CCP4RAL(1)	1C4h	Output Compare 4 Data Word A																0000
CCP4RBL(1)	1C8h	Output Compare 4 Data Word B																0000
CCP4BUFL(1)	1CCh	Input Capture 4 Data Buffer Low Word																0000
CCP4BUFH(1)	1CEh	Input Capture 4 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

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TABLE 4-12: SCCP5 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP5CON1L(1)	1D0h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP5CON1H(1)	1D2h	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP5CON2L(1)	1D4h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP5CON2H(1)	1D6h	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICSEL2	ICSEL1	ICSEL0	0100
CCP5CON3H(1)	1DAh	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	—	—	—	—	—	POLACE	—	PSSACE1	PSSACE0	—	—	0000
CCP5STATL(1)	1DCh	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP5TMRL(1)	1E0h	SCCP5 Time Base Register Low Word																0000
CCP5TMRH(1)	1E2h	SCCP5 Time Base Register High Word																0000
CCP5PRL(1)	1E4h	SCCP5 Time Base Period Register Low Word																FFFF
CCP5PRH(1)	1E6h	SCCP5 Time Base Period Register High Word																FFFF
CCP5RAL(1)	1E8h	Output Compare 5 Data Word A																0000
CCP5RBL(1)	1ECh	Output Compare 5 Data Word B																0000
CCP5BUFL(1)	1F0h	Input Capture 5 Data Buffer Low Word																0000
CCP5BUFH(1)	1F2h	Input Capture 5 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

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TABLE 4-13: MSSP1 (I^2C/SPI) REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SSP1BUF	200h	—	—	—	—	—	—	—	—	MSSP1 Receive Buffer/Transmit Register								00xx
SSP1CON1	202h	—	—	—	—	—	—	—	—	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000
SSP1CON2	204h	—	—	—	—	—	—	—	—	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
SSP1CON3	206h	—	—	—	—	—	—	—	—	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
SSP1STAT	208h	—	—	—	—	—	—	—	—	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000
SSP1ADD	20Ah	—	—	—	—	—	—	—	—	MSSP1 Address Register in I^2C Slave Mode MSSP1 Baud Rate Reload Register in I^2C Master Mode								0000
SSP1MSK	20Ch	—	—	—	—	—	—	—	—	MSK[7:0]								00FF

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-14: MSSP2 (I^2C/SPI) REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SSP2BUF(1)	210h	—	—	—	—	—	—	—	—	MSSP2 Receive Buffer/Transmit Register								00xx
SSP2CON1(1)	212h	—	—	—	—	—	—	—	—	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000
SSP2CON2(1)	214h	—	—	—	—	—	—	—	—	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
SSP2CON3(1)	216h	—	—	—	—	—	—	—	—	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
SSP2STAT(1)	218h	—	—	—	—	—	—	—	—	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000
SSP2ADD(1)	21Ah	—	—	—	—	—	—	—	—	MSSP2 Address Register in I^2C Slave Mode MSSP2 Baud Rate Reload Register in I^2C Master Mode								0000
SSP2MSK(1)	21Ch	—	—	—	—	—	—	—	—	MSK[7:0]								00FF

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

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TABLE 4-15: UART1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	220h	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	222h	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	224h	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	226h	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	228h	Baud Rate Generator Prescaler																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-16: UART2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U2MODE(1)	230h	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA(1)	232h	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG(1)	234h	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG(1)	236h	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG(1)	238h	Baud Rate Generator Prescaler																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

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TABLE 4-17: OP AMP 1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
AMP1CON(1)	24Ah	AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—	SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: This registers are available only on PIC24F(V)16KM2XX devices.

TABLE 4-18: OP AMP 2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
AMP2CON(1)	24Ch	AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—	SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: This registers are available only on PIC24F(V)16KM2XX devices.

TABLE 4-19: DAC1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DAC1CON(1)	274h	DACEN	—	DACSIDL	DACSLP	DACFM	—	SRDIS	DACTRIG	DACOE	DACTSEL4	DACTSEL3	DACTSEL2	DACTSEL1	DACTSEL0	DACREF1	DACREF0	0000
DAC1DAT(1)	276h	DACDAT[15:0](2)																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These registers are available only on PIC24F(V)16KM1XX devices.
2: The 8-bit result format depends on the value of the DACFM control bit.

TABLE 4-20: DAC2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DAC2CON(1)	278h	DACEN	—	DACSIDL	DACSLP	DACFM	—	SRDIS	DACTRIG	DACOE	DACTSEL4	DACTSEL3	DACTSEL2	DACTSEL1	DACTSEL0	DACREF1	DACREF0	0000
DAC2DAT(1)	27Ah	DACDAT[15:0](2)																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These registers are available only on PIC24F(V)16KM2XX devices.
2: The 8-bit result format depends on the value of the DACFM control bit.

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TABLE 4-21: PORTA REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11(4,5)	Bit 10(4,5)	Bit 9(4,5)	Bit 8(4,5)	Bit 7(4)	Bit 6(3)	Bit 5(2)	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	2C0h	—	—	—	—	TRISA[11:6]						—	TRISA[4:0]					0FDF(1)
PORTA	2C2h	—	—	—	—	RA[11:0]												xxxx
LATA	2C4h	—	—	—	—	LATA[11:6]						—	LATA[4:0]					xxxx
ODCA	2C6h	—	—	—	—	ODA[11:6]						—	ODA[4:0]					0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: Reset value depends on the device type; the PIC24F16KM204 value is shown.
2: These bits are only available when MCLRE (FPOR[7]) = 0.
3: These bits are not implemented in FV devices.
4: These bits are not implemented in 20-pin devices.
5: These bits are not implemented in 28-pin devices.

TABLE 4-22: PORTB REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11(2)	Bit 10(2)	Bit 9	Bit 8	Bit 7	Bit 6(2)	Bit 5(2)	Bit 4	Bit 3(2)	Bit 2	Bit 1	Bit 0	All Resets
TRISB	2C8h	TRISB[15:0]																FFFF(1)
PORTB	2CAh	RB[15:0]																xxxx
LATB	2CCh	LATB[15:0]																xxxx
ODCB	2CEh	ODB[15:0]																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: Reset value depends on the device type; the PIC24F16KM204 value is shown.
2: These bits are not implemented in 20-pin devices.

TABLE 4-23: PORTC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9(2,3)	Bit 8(2,3)	Bit 7(2,3)	Bit 6(2,3)	Bit 5(2,3)	Bit 4(2,3)	Bit 3(2,3)	Bit 2(2,3)	Bit 1(2,3)	Bit 0(2,3)	All Resets
TRISC	2D0h	—	—	—	—	—	—	TRISC[9:0]										03FF(1)
PORTC	2D2h	—	—	—	—	—	—	RC[9:0]										xxxx
LATTC	2D4h	—	—	—	—	—	—	LATC[9:0]										xxxx
ODCC	2D6h	—	—	—	—	—	—	ODC[9:0]										0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: Reset value depends on the device type; the PIC24F16KM204 value is shown.
2: These bits are not implemented in 20-pin devices.
3: These bits are not implemented in 28-pin devices.

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TABLE 4-24: PAD CONFIGURATION REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PADCFG1	2FCh	—	—	—	—	SDO2DIS(1)	SCK2DIS(1)	SDO1DIS	SCK1DIS	—	—	—	—	—	—	—	—	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These bits are not available on the PIC24F(V)08KM101 device, read as '0'.

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TABLE 4-25: A/D REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	300h	A/D Data Buffer 0/Threshold for Channel 0/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF1	302h	A/D Data Buffer 1/Threshold for Channel 1/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF2	304h	A/D Data Buffer 2/Threshold for Channel 2/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF3	306h	A/D Data Buffer 3/Threshold for Channel 3/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF4	308h	A/D Data Buffer 4/Threshold for Channel 4/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF5	30Ah	A/D Data Buffer 5/Threshold for Channel 5/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF6	30Ch	A/D Data Buffer 6/Threshold for Channel 6/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF7	30Eh	A/D Data Buffer 7/Threshold for Channel 7/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF8	310h	A/D Data Buffer 8/Threshold for Channel 8/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF9	312h	A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF10	314h	A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF11	316h	A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 11 & 23 in Window Compare																xxxx
ADC1BUF12	318h	A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF13	31Ah	A/D Data Buffer 13/Threshold for Channel 13/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF14	31Ch	A/D Data Buffer 14/Threshold for Channel 14/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF15	31Eh	A/D Data Buffer 15/Threshold for Channel 15/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF16	320h	A/D Data Buffer 16/Threshold for Channel 16/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF17	322h	A/D Data Buffer 17/Threshold for Channel 17/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF18	324h	A/D Data Buffer 18/Threshold for Channel 18/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF19	326h	A/D Data Buffer 19/Threshold for Channel 19/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF20	328h	A/D Data Buffer 20/Threshold for Channel 20/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF21	32Ah	A/D Data Buffer 21/Threshold for Channel 21/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF22	32Ch	A/D Data Buffer 22/Threshold for Channel 22/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF23	32Eh	A/D Data Buffer 23/Threshold for Channel 23/Threshold for Channel 11 & 23 in Window Compare																xxxx
AD1CON1	340h	ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE	0000
AD1CON2	342h	PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	344h	ADRC	EXTSAM	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	348h	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	34Eh	—	CSS30	CSS29	CSS28	CSS27	CSS26	—	—	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18(1)	CSS17(1)	CSS16	0000
AD1CSSL	350h	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8(1,2)	CSS7(1,2)	CSS6(1,2)	CSS5(1)	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON5	354h	ASEN	LPEN	CTMREQ	BGREQ	r	—	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
AD1CHITH	356h	—	—	—	—	—	—	—	—	CHH23	CHH22	CHH21	CHH20	CHH19	CHH18(1)	CHH17(1)	CHH16	0000
AD1CHITL	358h	CHH15	CHH14	CHH13	CHH12	CHH11	CHH10	CHH9	CHH8(1,2)	CHH7(1,2)	CHH6(1,2)	CHH5(1)	CHH4	CHH3	CHH2	CHH1	CHH0	0000
AD1CTMENH	360h	—	—	—	—	—	—	—	—	CTMEN23	CTMEN22	CTMEN21	CTMEN20	CTMEN19	CTMEN18(1)	CTMEN17(1)	CTMEN16	0000
AD1CTMENL	362h	CTMEN15	CTMEN14	CTMEN13	CTMEN12	CTMEN11	CTMEN10	CTMEN9	CTMEN8(1,2)	CTMEN7(1,2)	CTMEN6(1,2)	CTMEN5(1)	CTMEN4	CTMEN3	CTMEN2	CTMEN1	CTMEN0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are not implemented in 20-pin devices.

2: These bits are not implemented in 28-pin devices.

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TABLE 4-26: CTMU REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1L	35Ah	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	0000
CTMUCON1H	35Ch	EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—	0000
CTMUCON2L	35Eh	—	—	—	—	—	—	—	—	—	—	—	IRSTEN	—	DISCHS2	DISCHS1	DISCHS0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-27: ANSEL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ANSA	4E0h	—	—	—	—	—	—	—	—	—	—	—	ANSA4(2)	ANSA3	ANSA2	ANSA1	ANSA0	001F(1)
ANSB	4E2h	ANSB15	ANSB14	ANSB13	ANSB12	—	—	ANSB9	ANSB8	ANSB7	ANSB6(2)	ANSB5(2)	ANSB4	ANSB3(2)	ANSB2	ANSB1	ANSB0	F3FF(1)
ANSC	4E4h	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC2(2,3)	ANSC1(2,3)	ANSC0(2,3)	0007(1)

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: Reset value depends on the device type; the PIC24F16KM204 value is shown.
2: These bits are not implemented in 20-pin devices.
3: These bits are not implemented in 28-pin devices.

TABLE 4-28: REAL-TIME CLOCK AND CALENDAR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	620h	Alarm Value High Register Window Based on APTR[1:0]																xxxx
ALCFGRPT	622h	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000(1)
RTCVAL	624h	RTCC Value High Register Window Based on RTCPTR[1:0]																xxxx
RCFGCAL	626h	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	0000(1)
RTCPWC	628h	PWCEN	PWCPOL	PWCCPRE	PWCSPRE	RTCCLK1	RTCCLK0	RTCOUT1	RTCOUT0	—	—	—	—	—	—	—	—	0000(1)

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: Values are reset only on a VDD POR event.

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TABLE 4-29: COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	630h	CMIDL	—	—	—		C3EVT(1)	C2EVT(1)	C1EVT	—	—	—	—	—	C3OUT(1)	C2OUT(1)	C1OUT	0000
CVRCON	632h	—	—	—	—	—	—	—	—	CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0	0000
CM1CON	634h	CON	COE	CPOL	CLPWR	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF1	CREF0	—	CCH1	CCH0	0000
CM2CON(1)	636h	CON	COE	CPOL	CLPWR	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF1(1)	CREF0	—	CCH1	CCH0	0000
CM3CON(1)	638h	CON	COE	CPOL	CLPWR	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF1(1)	CREF0	—	CCH1	CCH0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These registers and bits are available only on PIC24F(V)16KM2XX devices.

TABLE 4-30: BAND GAP BUFFER CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
BUFCON0	670h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUFREF[1:0]		0001

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

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TABLE 4-31: CLOCK CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	740h	TRAPR	IOPUWR	SBOREN	RETEN	—	—	CM	PMSLP	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	(Note 1)
OSCCON	742h	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	—	LOCK	—	CF	SOSCDRV	SOSCEN	OSWEN	(Note 2)
CLKDIV	744h	ROI	DOZE2	DOZE1	DOZE0	DOZEN	RCDIV2	RCDIV1	RCDIV0	—	—	—	—	—	—	—	—	0100
OSCTUN	748h	—	—	—	—	—	—	—	—	—	—	TUN[5:0]						0000
REFOCON	74Eh	ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000
HLVDCON	756h	HLVDEN	—	HLSIDL	—	—	—	—	—	VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: RCON register Reset values are dependent on the type of Reset.
2: OSCCON register Reset values are dependent on Configuration fuses and by type of Reset.

TABLE 4-32: NVM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	760h	WR	WREN	WRERR	PGMONLY	—	—	—	—	—	ERASE	NVMOP5	NVMOP4	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMKEY	766h	—	—	—	—	—	—	—	—	NVMKEY[7:0]								0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-33: ULTRA LOW-POWER WAKE-UP REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ULPWCON	768h	ULPEN	—	ULPSIDL	—	—	—	—	ULPSINK	—	—	—	—	—	—	—	—	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-34: PMD REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	770h	—	—	—	—	T1MD	—	—	—	SSP1MD	U2MD(1)	U1MD	—	—	—	—	ADCMD	0000
PMD2	772h	—	—	—	—	—	—	—	—	—	—	—	CCP5MD(1)	CCP4MD(1)	CCP3MD(1)	CCP2MD	CCP1MD	0000
PMD3	774h	—	—	—	—	—	CMPMD	RTCCMD	—	—	DAC1MD(1)	—	—	—	—	SSP2MD(1)	—	0000
PMD4	776h	—	—	—	—	—	—	—	—	—	ULPWUMD	—	—	REFOMD	CTMUMD	HLVDMD	—	0000
PMD6	77Ah	—	—	—	—	—	—	—	—	—	—	AMP1MD(1)	DAC2MD(1)	AMP2MD(1)	—	—	—	0000
PMD8	77Eh	—	—	—	—	—	—	—	—	—	—	—	—	CLC2MD(1)	CLC1MD	—	—	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These bits are available only on PIC24F(V)16KM2XX devices.

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4.2.5 SOFTWARE STACK

In addition to its use as a Working register, the W15 register in PIC24F devices is also used as a Software Stack Pointer. The pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as depicted in Figure 4-4.

For a PC push during any `CALL` instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

> **Note:** A PC push during exception processing will concatenate the SRL register to the MSB of the PC prior to the push.

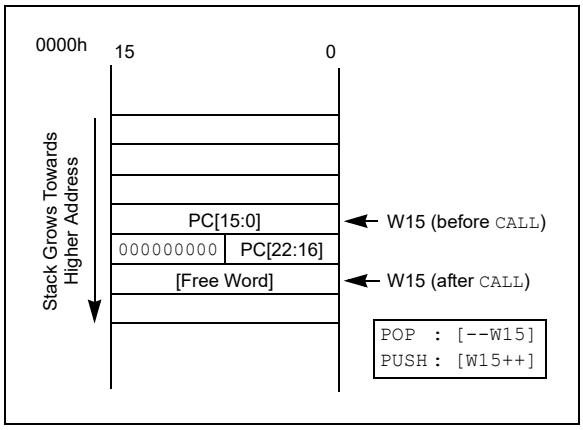
The Stack Pointer Limit Value (SPLIM) register, associated with the Stack Pointer, sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM[0] is forced to '`0`' as all stack operations must be word-aligned. Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal, and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation.

Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address, 0DF6 in RAM, initialize the SPLIM with the value, 0DF4.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0800h. This prevents the stack from interfering with the Special Function Register (SFR) space.

> **Note:** A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-4: `CALL` STACK FRAME



4.3 Interfacing Program and Data Memory Spaces

The PIC24F architecture uses a 24-bit wide program space and 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use these data successfully, they must be accessed in a way that preserves the alignment of information in both spaces.

Apart from the normal execution, the PIC24F architecture provides two methods by which the program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the Data Space, PSV

Table instructions allow an application to read or write small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look ups from a large table of static data. It can only access the least significant word (lsw) of the program word.

4.3.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Memory Page Address register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the Most Significant bit (MSb) of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG[7] = `0`) or the configuration memory (TBLPAG[7] = `1`).

For remapping operations, the 8-bit Program Space Visibility Page Address register (PSVPAG) is used to define a 16K word page in the program space. When the MSb of the EA is '`1`', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike the table operations, this limits remapping operations strictly to the user memory area.

See Table 4-35 and Figure 4-5 to know how the program EA is created for table operations and remapping accesses from the data EA. Here, P[23:0] refers to a program space word, whereas D[15:0] refers to a Data Space word.

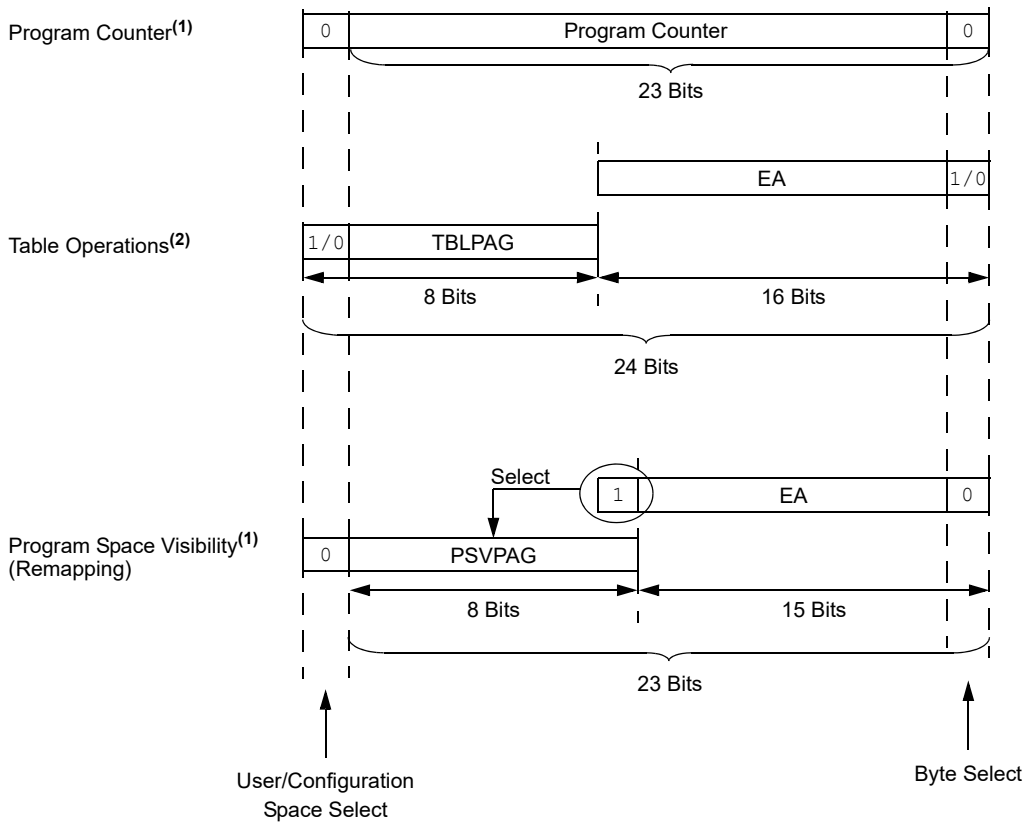
TABLE 4-35: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		[23]	[22:16]	[15]	[14:1]	[0]
Instruction Access (Code Execution)	User	0	PC[22:1]			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG[7:0]		Data EA[15:0]		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG[7:0]		Data EA[15:0]		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	PSVPAG[7:0](2)		Data EA[14:0](1)	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

Note 1: Data EA[15] is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG[0].

2: PSVPAG can have only two values ('00' to access program memory and FF to access data EEPROM) on the PIC24F16KM family.

FIGURE 4-5: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The LSb of program space addresses is always fixed as '0' in order to maintain word alignment of data in the program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

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4.3.2 DATA ACCESS FROM PROGRAM MEMORY AND DATA EEPROM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program memory without going through Data Space. It also offers a direct method of reading or writing a word of any address within data EEPROM memory. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

> **Note:** The TBLRDH and TBLWTH instructions are not used while accessing data EEPROM memory.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit, word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P[15:0]) to a data address (D[15:0]).

   In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P[23:16]) to a data address. Note that D[15:8], the 'phantom' byte, will always be '0'.

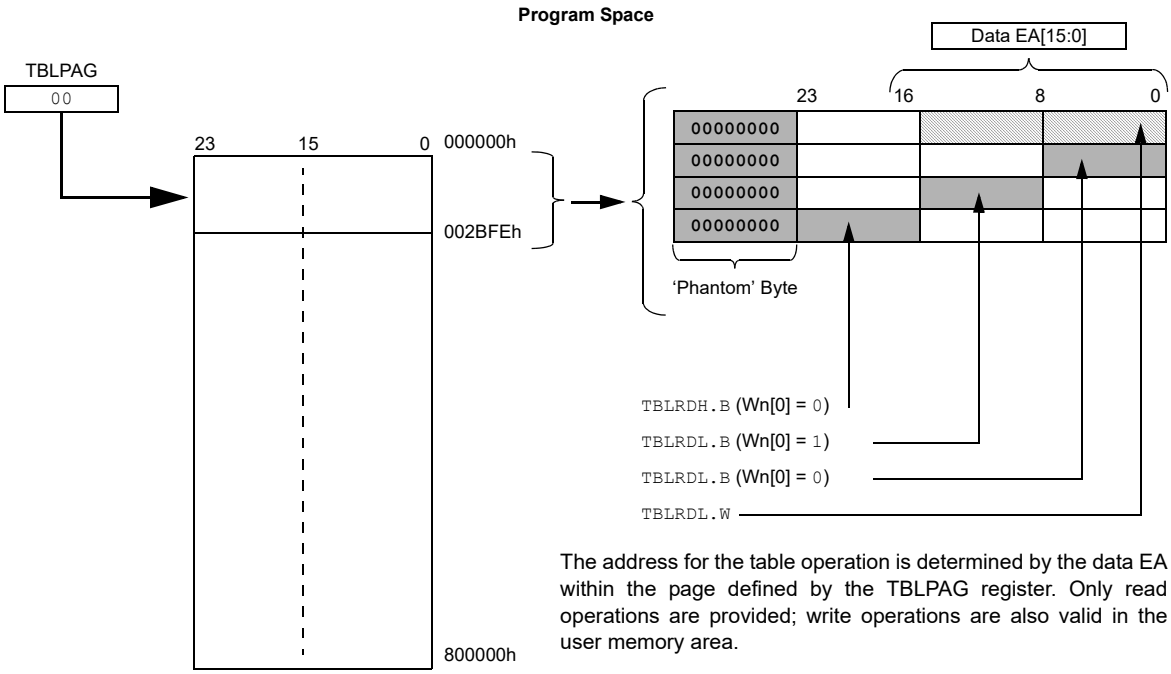
   In Byte mode, it maps the upper or lower byte of the program word to D[7:0] of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG[7] = 0, the table page is located in the user memory space. When TBLPAG[7] = 1, the page is located in configuration space.

> **Note:** Only Table Read operations will execute in the configuration memory space, and only then, in implemented areas, such as the Device ID. Table Write operations are not allowed.

FIGURE 4-6: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



4.3.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of Data Space may optionally be mapped into a 16K word page of the program space. This provides transparent access of stored constant data from the Data Space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the Data Space occurs if the MSb of the Data Space, EA, is '1' and PSV is enabled by setting the PSV bit in the CPU Control (CORCON[2]) register. The location of the program memory space to be mapped into the Data Space is determined by the Program Space Visibility Page Address register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits.

By incrementing the PC by two for each program memory word, the lower 15 bits of Data Space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads from this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each Data Space address, 8000h and higher, maps directly into a corresponding program memory address (see Figure 4-7), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space locations used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

> **Note:** PSV access is temporarily disabled during Table Reads/Writes.

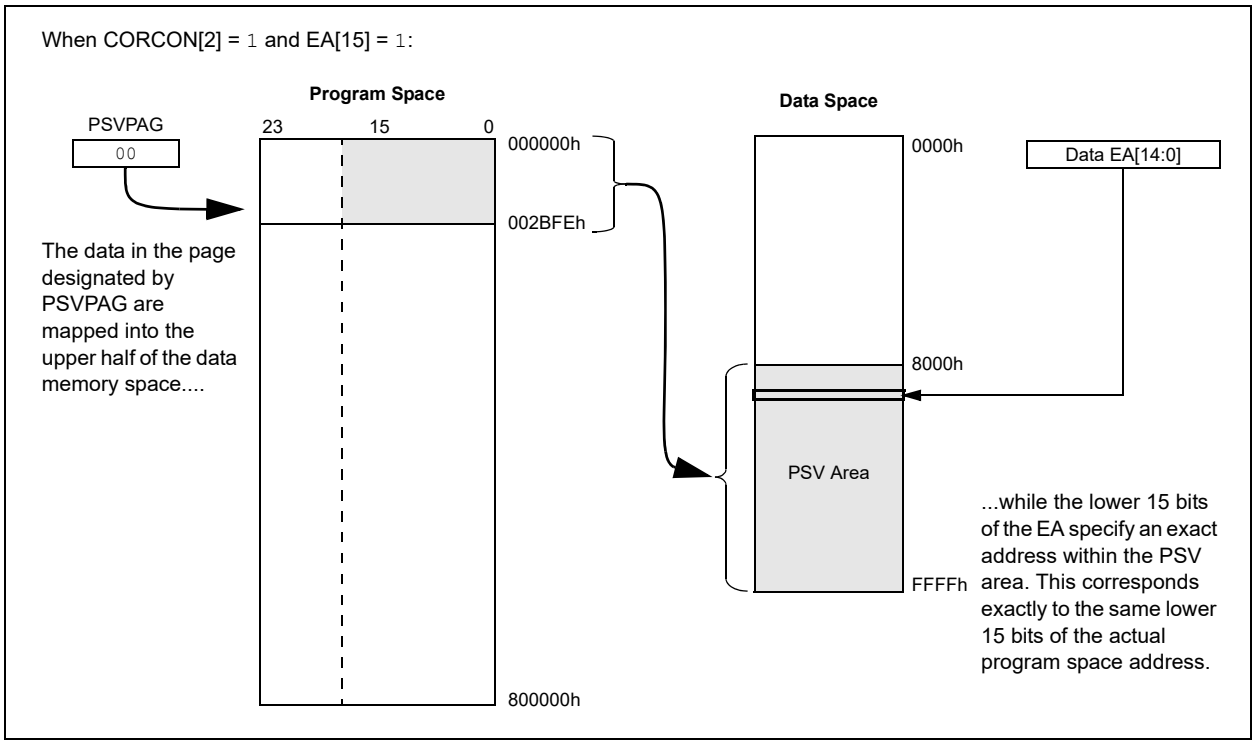
For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions will require one instruction cycle in addition to the specified execution time. All other instructions will require two instruction cycles in addition to the specified execution time.

For operations that use PSV, which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data, using PSV, to execute in a single cycle.

FIGURE 4-7: PROGRAM SPACE VISIBILITY OPERATION



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5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Flash programming, refer to **"PIC24F Flash Program Memory"** (www.microchip.com/DS30009715) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The PIC24FV16KM204 family of devices contains internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable when operating with VDD over 1.8V.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24FXXXXX device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (which are named PGECx and PGEDx, respectively), and three other lines for power (VDD), ground (VSS) and Master Clear/Program Mode Entry Voltage (MCLR/VPP). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or custom firmware to be programmed.

Run-Time Self-Programming (RTSP) is accomplished using `TBLRD` (Table Read) and `TBLWT` (Table Write) instructions. With RTSP, the user may write program memory data in blocks of 32 instructions (96 bytes) at a time, and erase program memory in blocks of 32, 64 and 128 instructions (96,192 and 384 bytes) at a time.

The NVMOP[1:0] (NVMCON[1:0]) bits decide the erase block size.

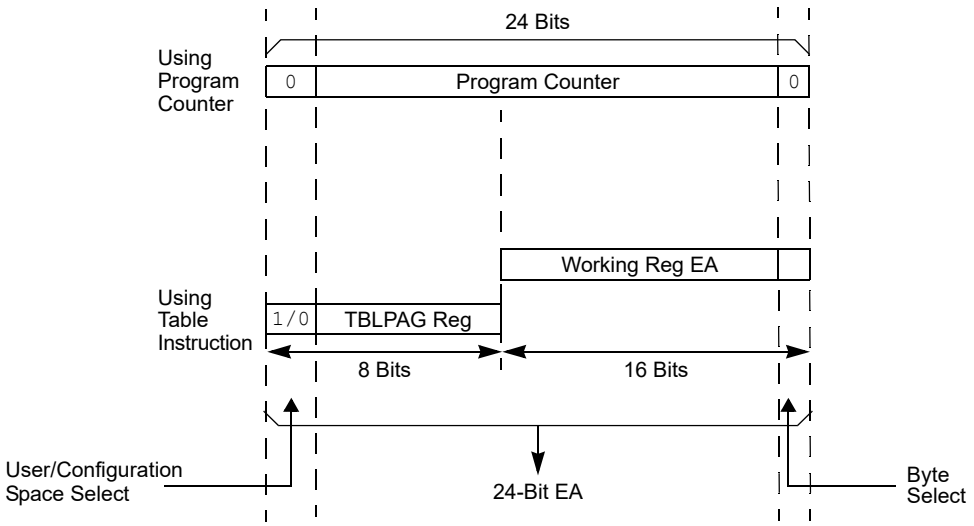
5.1 Table Instructions and Flash Programming

Regardless of the method used, Flash memory programming is done with the Table Read and Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG[7:0] bits and the Effective Address (EA) from a W register, specified in the table instruction, as depicted in Figure 5-1.

The `TBLRDL` and the `TBLWTL` instructions are used to read or write to bits[15:0] of program memory. `TBLRDL` and `TBLWTL` can access program memory in both Word and Byte modes.

The `TBLRDH` and `TBLWTH` instructions are used to read or write to bits[23:16] of program memory. `TBLRDH` and `TBLWTH` can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



5.2 RTSP Operation

The PIC24F Flash program memory array is organized into rows of 32 instructions or 96 bytes. RTSP allows the user to erase blocks of one row, two rows and four rows (32, 64 and 128 instructions) at a time, and to program one row at a time. It is also possible to program single words.

The 1-row (96 bytes), 2-row (192 bytes) and 4-row (384 bytes) erase blocks, and single row write block (96 bytes) are edge-aligned, from the beginning of program memory.

When data are written to program memory using `TBLWT` instructions, the data are not written directly to memory. Instead, data written using Table Writes are stored in holding latches until the programming sequence is executed.

Any number of `TBLWT` instructions can be executed and a write will be successfully performed. However, 32 `TBLWT` instructions are required to write the full row of memory.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of `TBLWT` instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register.

Data can be loaded in any order and the holding registers can be written to multiple times before performing a write operation. Subsequent writes, however, will wipe out any previous writes.

Note:	Writing to a location multiple times, without erasing it, is not recommended.

All of the Table Write operations are single-word writes (two instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

5.3 Enhanced In-Circuit Serial Programming

Enhanced ICSP uses an on-board bootloader, known as the Program Executive (PE), to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

5.4 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls the blocks that need to be erased, which memory type is to be programmed and when the programming cycle starts.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register. Refer to **Section 5.5 “Programming Operations”** for further details.

5.5 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. During a programming or erase operation, the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON[15]) starts the operation and the WR bit is automatically cleared when the operation is finished.

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REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

HC/R/SO-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	PGMONLY(4)	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ERASE	NVMOP5(1)	NVMOP4(1)	NVMOP3(1)	NVMOP2(1)	NVMOP1(1)	NVMOP0(1)
bit 7							bit 0

Legend:	SO = Settable Only bit	HC = Hardware Clearable bit	
-n = Value at POR	‘1’ = Bit is set	R = Readable bit	W = Writable bit
‘0’ = Bit is cleared	x = Bit is unknown	U = Unimplemented bit, read as ‘0’	

bit 15 **WR:** Write Control bit
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit
- 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **PGMONLY:** Program Only Enable bit(4)

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6 **ERASE:** Erase/Program Enable bit
- 1 = Performs the erase operation specified by the NVMOP[5:0] bits on the next WR command
- 0 = Performs the program operation specified by the NVMOP[5:0] bits on the next WR command

bit 5-0 **NVMOP[5:0]:** Programming Operation Command Byte bits(1)

Erase Operations (when ERASE bit is ‘1’):
- 1010xx = Erases entire boot block (including code-protected boot block)(2)
- 1001xx = Erases entire memory (including boot block, configuration block, general block)(2)
- 011010 = Erases four rows of Flash memory(3)
- 011001 = Erases two rows of Flash memory(3)
- 011000 = Erases one row of Flash memory(3)
- 0101xx = Erases entire configuration block (except code protection bits)
- 0100xx = Erases entire data EEPROM(4)
- 0011xx = Erases entire general memory block programming operations
- 0001xx = Writes one row of Flash memory (when ERASE bit is ‘0’)(3)

Note 1: All other combinations of NVMOP[5:0] are no operation.
2: Available in ICSP™ mode only. Refer to the device programming specification.
3: The address in the Table Pointer decides which rows will be erased.
4: This bit is used only while accessing data EEPROM.

5.5.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of Flash program memory at a time by erasing the programmable row. The general process is:

1. Read a row of program memory (32 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase a row (see Example 5-1):
   a) Set the NVMOPx bits (NVMCON[5:0]) to '011000' to configure for row erase. Set the ERASE (NVMCON[6]) and WREN (NVMCON[14]) bits.
   b) Write the starting address of the block to be erased into the TBLPAG and W registers.
   c) Write 55h to NVMKEY.
   d) Write AAh to NVMKEY.
   e) Set the WR bit (NVMCON[15]). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Write the first 32 instructions from data RAM into the program memory buffers (see Example 5-1).
5. Write the program block to Flash memory:
   a) Set the NVMOPx bits to '000100' to configure for row programming. Clear the ERASE bit and set the WREN bit.
   b) Write 55h to NVMKEY.
   c) Write AAh to NVMKEY.
   d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs, as displayed in Example 5-5.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY ROW – ASSEMBLY LANGUAGE CODE

```
; Set up NVMCON for row erase operation
        MOV     #0x4058, W0                 ;
        MOV     W0, NVMCON                  ; Initialize NVMCON
; Init pointer to row to be ERASED
        MOV     #tblpage(PROG_ADDR), W0     ;
        MOV     W0, TBLPAG                  ; Initialize PM Page Boundary SFR
        MOV     #tbloffset(PROG_ADDR), W0   ; Initialize in-page EA[15:0] pointer
        TBLWTL  W0, [W0]                    ; Set base address of erase block
        DISI    #5                          ; Block all interrupts
                                              for next 5 instructions
        MOV     #0x55, W0
        MOV     W0, NVMKEY                  ; Write the 55 key
        MOV     #0xAA, W1                   ;
        MOV     W1, NVMKEY                  ; Write the AA key
        BSET    NVMCON, #WR                 ; Start the erase sequence
        NOP                                 ; Insert two NOPs after the erase
        NOP                                 ; command is asserted
```

EXAMPLE 5-2: ERASING A PROGRAM MEMORY ROW – 'C' LANGUAGE CODE

```
// C example using MPLAB C30

int __attribute__ ((space(auto_psv))) progAddr = 0x1234;     // Variable located in Pgm Memory, declared as a
                                                             // global variable
    unsigned int offset;

//Set up pointer to the first memory location to be written

    TBLPAG = __builtin_tblpage(&progAddr);                   // Initialize PM Page Boundary SFR
    offset = __builtin_tbloffset(&progAddr);                 // Initialize lower word of address

    __builtin_tblwtl(offset, 0x0000);                        // Set base address of erase block
                                                             // with dummy latch write

    NVMCON = 0x4058;                                         // Initialize NVMCON

    asm("DISI #5");                                          // Block all interrupts for next 5 instructions
    __builtin_write_NVM();                                   // C30 function to perform unlock
                                                             // sequence and set WR
```


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EXAMPLE 5-3: LOADING THE WRITE BUFFERS – ASSEMBLY LANGUAGE CODE

```
; Set up NVMCON for row programming operations
        MOV     #0x4004, W0                 ;
        MOV     W0, NVMCON                  ; Initialize NVMCON
; Set up a pointer to the first program memory location to be written
; program memory selected, and writes enabled
        MOV     #0x0000, W0                 ;
        MOV     W0, TBLPAG                  ; Initialize PM Page Boundary SFR
        MOV     #0x1500, W0                 ; An example program memory address
; Perform the TBLWT instructions to write the latches
; 0th_program_word
        MOV     #LOW_WORD_0, W2             ;
        MOV     #HIGH_BYTE_0, W3            ;
        TBLWTL  W2, [W0]                    ; Write PM low word into program latch
        TBLWTH  W3, [W0++]                  ; Write PM high byte into program latch
; 1st_program_word
        MOV     #LOW_WORD_1, W2             ;
        MOV     #HIGH_BYTE_1, W3            ;
        TBLWTL  W2, [W0]                    ; Write PM low word into program latch
        TBLWTH  W3, [W0++]                  ; Write PM high byte into program latch
; 2nd_program_word
        MOV     #LOW_WORD_2, W2             ;
        MOV     #HIGH_BYTE_2, W3            ;
        TBLWTL  W2, [W0]                    ; Write PM low word into program latch
        TBLWTH  W3, [W0++]                  ; Write PM high byte into program latch
        •
        •
        •
; 32nd_program_word
        MOV     #LOW_WORD_31, W2            ;
        MOV     #HIGH_BYTE_31, W3           ;
        TBLWTL  W2, [W0]                    ; Write PM low word into program latch
        TBLWTH  W3, [W0]                    ; Write PM high byte into program latch
```

EXAMPLE 5-4: LOADING THE WRITE BUFFERS – 'C' LANGUAGE CODE

```
// C example using MPLAB C30

   #define  NUM_INSTRUCTION_PER_ROW 64
int __attribute__ ((space(auto_psv))) progAddr = 0x1234      // Variable located in Pgm Memory
   unsigned int offset;
   unsigned int i;
   unsigned int progData[2*NUM_INSTRUCTION_PER_ROW];         // Buffer of data to write

   //Set up NVMCON for row programming
   NVMCON = 0x4004;                                          // Initialize NVMCON

   //Set up pointer to the first memory location to be written
   TBLPAG = __builtin_tblpage(&progAddr);                    // Initialize PM Page Boundary SFR
   offset = __builtin_tbloffset(&progAddr);                  // Initialize lower word of address

   //Perform TBLWT instructions to write necessary number of latches
   for(i=0; i < 2*NUM_INSTRUCTION_PER_ROW; i++)
   {
       __builtin_tblwtl(offset, progData[i++]);              // Write to address low word
       __builtin_tblwth(offset, progData[i]);                // Write to upper byte
       offset = offset + 2;                                  // Increment address
   }
```

EXAMPLE 5-5: INITIATING A PROGRAMMING SEQUENCE – ASSEMBLY LANGUAGE CODE

```
        DISI    #5                      ; Block all interrupts
                                          for next 5 instructions
        MOV     #0x55, W0
        MOV     W0, NVMKEY              ; Write the 55 key
        MOV     #0xAA, W1               ;
        MOV     W1, NVMKEY              ; Write the AA key
        BSET    NVMCON, #WR             ; Start the erase sequence
        NOP                             ; 2 NOPs required after setting WR
        NOP                             ;
        BTSC    NVMCON, #15             ; Wait for the sequence to be completed
        BRA     $-2                     ;
```

EXAMPLE 5-6: INITIATING A PROGRAMMING SEQUENCE – 'C' LANGUAGE CODE

```
// C example using MPLAB C30

asm("DISI #5");               // Block all interrupts for next 5 instructions

__builtin_write_NVM();        // Perform unlock sequence and set WR
```


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6.0 DATA EEPROM MEMORY

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on data EEPROM, refer to **"Data EEPROM"** (www.microchip.com/DS39720) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The data EEPROM memory is a Nonvolatile Memory (NVM), separate from the program and volatile data RAM. Data EEPROM memory is based on the same Flash technology as program memory, and is optimized for both long retention and a higher number of erase/write cycles.

The data EEPROM is mapped to the top of the user program memory space, with the top address at program memory address, 7FFE00h to 7FFFFFh. The size of the data EEPROM is 256 words in PIC24FXXXXX devices.

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable during normal operation over the entire VDD range.

Unlike the Flash program memory, normal program execution is not stopped during a data EEPROM program or erase operation.

The data EEPROM programming operations are controlled using the three NVM Control registers:

- NVMCON: Nonvolatile Memory Control Register
- NVMKEY: Nonvolatile Memory Key Register
- NVMADR: Nonvolatile Memory Address Register

6.1 NVMCON Register

The NVMCON register (Register 6-1) is also the primary control register for data EEPROM program/erase operations. The upper byte contains the control bits used to start the program or erase cycle and the flag bit to indicate if the operation was successfully performed. The lower byte of NVMCOM configures the type of NVM operation that will be performed.

6.2 NVMKEY Register

The NVMKEY is a write-only register that is used to prevent accidental writes or erasures of data EEPROM locations.

To start any programming or erase sequence, the following instructions must be executed first, in the exact order provided:

1. Write 55h to NVMKEY.
2. Write AAh to NVMKEY.

After this sequence, a write will be allowed to the NVMCON register for one instruction cycle. In most cases, the user will simply need to set the WR bit in the NVMCON register to start the program or erase cycle. Interrupts should be disabled during the unlock sequence.

The MPLAB® C30 C compiler provides a defined library procedure (`builtin_write_NVM`) to perform the unlock sequence. Example 6-1 illustrates how the unlock sequence can be performed with in-line assembly.

EXAMPLE 6-1: DATA EEPROM UNLOCK SEQUENCE

```
//Disable Interrupts For 5 instructions
asm volatile   ("disi #5");
//Issue Unlock Sequence
asm volatile   ("mov #0x55, W0     \n"
               "mov W0, NVMKEY     \n"
               "mov #0xAA, W1      \n"
               "mov W1, NVMKEY     \n");
// Perform Write/Erase operations
asm volatile   ("bset NVMCON, #WR  \n"
               "nop                \n"
               "nop                \n");
```

REGISTER 6-1: NVMCON: NONVOLATILE MEMORY CONTROL REGISTER

HC/R/SO-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	PGMONLY	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ERASE	NVMOP5	NVMOP4	NVMOP3	NVMOP2	NVMOP1	NVMOP0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	U = Unimplemented bit, read as ‘0’	
R = Readable bit	W = Writable bit	S = Settable Only bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit (program or erase)
`1` = Initiates a data EEPROM erase or write cycle (can be set, but not cleared in software)
`0` = Write cycle is complete (cleared automatically by hardware)

bit 14 **WREN:** Write Enable bit (erase or program)
`1` = Enables an erase or program operation
`0` = No operation allowed (device clears this bit on completion of the write/erase operation)

bit 13 **WRERR:** Flash Error Flag bit
`1` = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ or WDT Reset during programming operation)
`0` = The write operation completed successfully

bit 12 **PGMONLY:** Program Only Enable bit
`1` = Write operation is executed without erasing target address(es) first
`0` = Automatic erase-before-write
Write operations are preceded automatically by an erase of the target address(es).

bit 11-7 **Unimplemented:** Read as ‘`0`’

bit 6 **ERASE:** Erase Operation Select bit
`1` = Performs an erase operation when WR is set
`0` = Performs a write operation when WR is set

bit 5-0 **NVMOP[5:0]:** Programming Operation Command Byte bits
Erase Operations (when ERASE bit is ‘`1`’):
`011010` = Erases eight words
`011001` = Erases four words
`011000` = Erases one word
`0100xx` = Erases entire data EEPROM
Programming Operations (when ERASE bit is ‘`0`’):
`0001xx` = Writes one word

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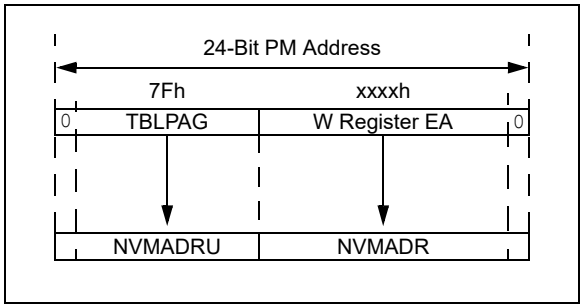
6.3 NVM Address Register

As with Flash program memory, the NVM Address registers, NVMADRU and NVMADR, form the 24-bit Effective Address (EA) of the selected row or word for data EEPROM operations. The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA. These registers are not mapped into the Special Function Register (SFR) space; instead, they directly capture the EA[23:0] of the last Table Write instruction that has been executed and select the data EEPROM row to erase. Figure 6-1 depicts the program memory EA that is formed for programming and erase operations.

Like program memory operations, the Least Significant bit (LSb) of NVMADR is restricted to even addresses. This is because any given address in the data EEPROM space consists of only the lower word of the program memory width; the upper word, including the uppermost “phantom byte”, are unavailable. This means that the LSb of a data EEPROM address will always be ‘0’.

Similarly, the Most Significant bit (MSb) of NVMADRU is always ‘0’, since all addresses lie in the user program space.

FIGURE 6-1: DATA EEPROM ADDRESSING WITH TBLPAG AND NVM ADDRESS REGISTERS



6.4 Data EEPROM Operations

The EEPROM block is accessed using Table Read and Write operations, similar to those used for program memory. The `TBLWTH` and `TBLRDH` instructions are not required for data EEPROM operations since the memory is only 16 bits wide (data on the lower address are valid only). The following programming operations can be performed on the data EEPROM:

- Erase one, four or eight words
- Bulk erase the entire data EEPROM
- Write one word
- Read one word

Note 1: Unexpected results will be obtained if the user attempts to read the EEPROM while a programming or erase operation is underway.

2: The XC16 C compiler includes library procedures to automatically perform the Table Read and Table Write operations, manage the Table Pointer and write buffers, and unlock and initiate memory write sequences. This eliminates the need to create assembler macros or time critical routines in C for each application.

The library procedures are used in the code examples detailed in the following sections. General descriptions of each process are provided for users who are not using the XC16 compiler libraries.

6.4.1 ERASE DATA EEPROM

The data EEPROM can be fully erased, or can be partially erased, at three different sizes: one word, four words or eight words. The bits, NVMOP[1:0] (NVMCON[1:0]), decide the number of words to be erased. To erase partially from the data EEPROM, the following sequence must be followed:

1. Configure NVMCON to erase the required number of words: one, four or eight.
2. Load TBLPAG and WREG with the EEPROM address to be erased.
3. Clear the NVMIF status bit and enable the NVM interrupt (optional).
4. Write the key sequence to NVMKEY.
5. Set the WR bit to begin the erase cycle.
6. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical erase sequence is provided in Example 6-2. This example shows how to do a one-word erase. Similarly, a four-word erase and an eight-word erase can be done. This example uses C library procedures to manage the Table Pointer (`builtin_tblpage` and `builtin_tbloffset`) and the Erase Page Pointer (`builtin_tblwtl`). The memory unlock sequence (`builtin_write_NVM`) also sets the WR bit to initiate the operation and returns control when complete.

EXAMPLE 6-2: SINGLE-WORD ERASE

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
/*-----------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the erase
-----------------------------------------------------------------------------------------
*/
    unsigned int offset;

    // Set up NVMCON to erase one word of data EEPROM
    NVMCON = 0x4058;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);             // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);           // Initizlize lower word of address
    __builtin_tblwtl(offset, 0);                     // Write EEPROM data to write latch

    asm volatile ("disi #5");                        // Disable Interrupts For 5 Instructions
    __builtin_write_NVM();                           // Issue Unlock Sequence & Start Write Cycle
    while(NVMCONbits.WR==1);                         // Optional: Poll WR bit to wait for
                                                     // write sequence to complete
```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6.4.1.1 Data EEPROM Bulk Erase

To erase the entire data EEPROM (bulk erase), the address registers do not need to be configured because this operation affects the entire data EEPROM. The following sequence helps in performing a bulk erase:

1. Configure NVMCON to Bulk Erase mode.
2. Clear the NVMIF status bit and enable the NVM interrupt (optional).
3. Write the key sequence to NVMKEY.
4. Set the WR bit to begin the erase cycle.
5. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical bulk erase sequence is provided in Example 6-3.

6.4.2 SINGLE-WORD WRITE

To write a single word in the data EEPROM, the following sequence must be followed:

1. Erase one data EEPROM word (as mentioned in the previous section) if the PGMONLY bit (NVMCON[12]) is set to '1'.
2. Write the data word into the data EEPROM latch.
3. Program the data word into the EEPROM:
   - Configure the NVMCON register to program one EEPROM word (NVMCON[5:0] = 0001xx).
   - Clear the NVMIF status bit and enable the NVM interrupt (optional).
   - Write the key sequence to NVMKEY.
   - Set the WR bit to begin the erase cycle.
   - Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).
   - To get cleared, wait until NVMIF is set.

A typical single-word write sequence is provided in Example 6-4.

EXAMPLE 6-3: DATA EEPROM BULK ERASE

```
    // Set up NVMCON to bulk erase the data EEPROM
    NVMCON = 0x4050;

    // Disable Interrupts For 5 Instructions
    asm volatile ("disi #5");

    // Issue Unlock Sequence and Start Erase Cycle
    __builtin_write_NVM();
```

EXAMPLE 6-4: SINGLE-WORD WRITE TO DATA EEPROM

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
   int newData;                                        // New data to write to EEPROM
/*-----------------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the write
-----------------------------------------------------------------------------------------------
*/
   unsigned int offset;

   // Set up NVMCON to erase one word of data EEPROM
   NVMCON = 0x4004;

   // Set up a pointer to the EEPROM location to be erased
   TBLPAG = __builtin_tblpage(&eeData);                // Initialize EE Data page pointer
   offset = __builtin_tbloffset(&eeData);              // Initizlize lower word of address
   __builtin_tblwtl(offset, newData);                  // Write EEPROM data to write latch

   asm volatile ("disi #5");                           // Disable Interrupts For 5 Instructions
   __builtin_write_NVM();                              // Issue Unlock Sequence & Start Write Cycle
   while(NVMCONbits.WR==1);                            // Optional: Poll WR bit to wait for
                                                       // write sequence to complete
```

6.4.3 READING THE DATA EEPROM

To read a word from data EEPROM, the Table Read instruction is used. Since the EEPROM array is only 16 bits wide, only the `TBLRDL` instruction is needed. The read operation is performed by loading TBLPAG and WREG with the address of the EEPROM location, followed by a `TBLRDL` instruction.

A typical read sequence, using the Table Pointer management (`builtin_tblpage` and `builtin_tbloffset`) and Table Read (`builtin_tblrdl`) procedures from the C30 compiler library, is provided in Example 6-5.

Program Space Visibility (PSV) can also be used to read locations in the data EEPROM.

EXAMPLE 6-5: READING THE DATA EEPROM USING THE `TBLRD` COMMAND

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
int data;                                                // Data read from EEPROM
/*-----------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the read
-----------------------------------------------------------------------------------------
*/
    unsigned int offset;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);                 // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);               // Initizlize lower word of address
    data = __builtin_tblrdl(offset);                     // Write EEPROM data to write latch
```


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7.0 RESETS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Resets, refer to **"Reset with Programmable Brown-out Reset"** (www.microchip.com/DS39728) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Pin Reset
- SWR: `RESET` Instruction
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- LPBOR: Low-Power BOR
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 7-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on Power-on Reset (POR) and unchanged by all other Resets.

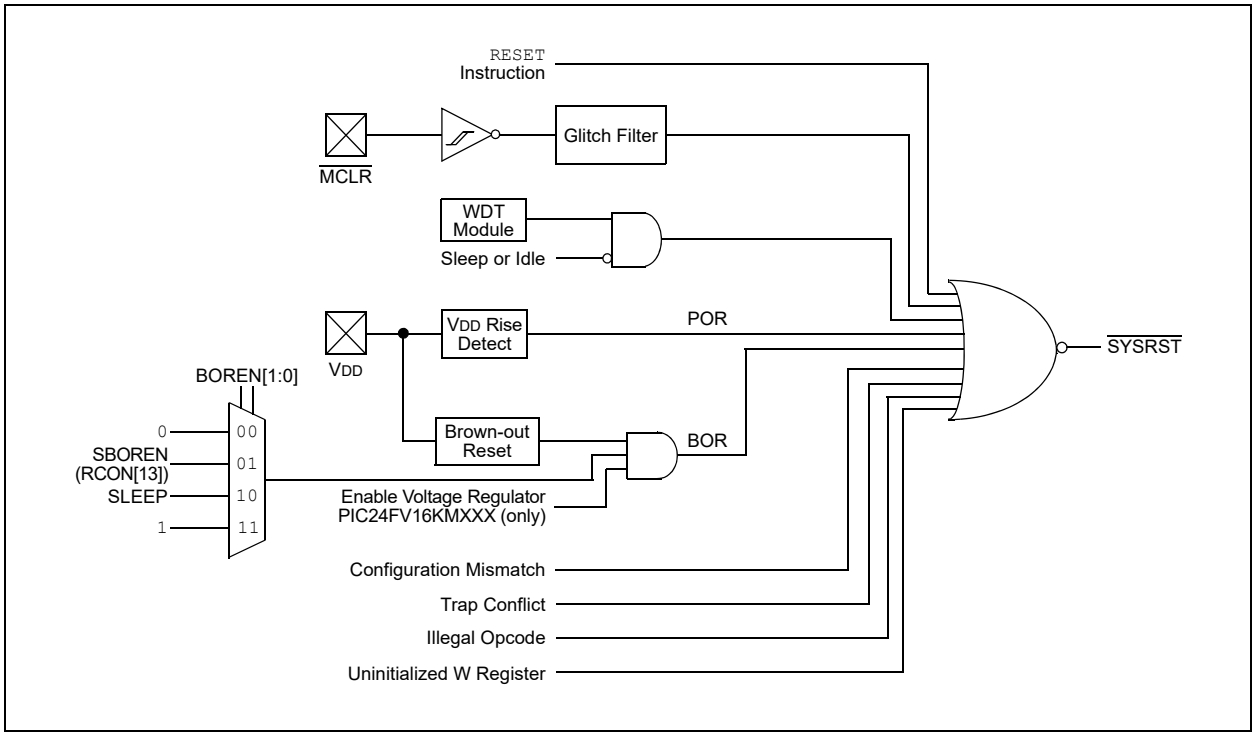
Note: Refer to the specific peripheral or **Section 3.0 "CPU"** of this data sheet for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A Power-on Reset will clear all bits except for the BOR and POR bits (RCON[1:0]) which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

FIGURE 7-1: RESET SYSTEM BLOCK DIAGRAM



REGISTER 7-1: RCON: RESET CONTROL REGISTER[1]

HS/R/W-0	HS/R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	SBOREN	RETEN[3]	—	—	CM	PMSLP
bit 15							bit 8

HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-1	HS/R/W-1
EXTR	SWR	SWDTEN[2]	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W Reset has not occurred

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12 **RETEN:** Retention Sleep Mode bit[3]
1 = Regulated voltage supply provided by the Retention Regulator (RETREG) during Sleep
0 = Regulated voltage supply provided by the main Voltage Regulator (VREG) during Sleep

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9 **CM:** Configuration Word Mismatch Reset Flag bit
1 = A Configuration Word Mismatch Reset has occurred
0 = A Configuration Word Mismatch Reset has not occurred

bit 8 **PMSLP:** Program Memory Power During Sleep bit
1 = Program memory bias voltage remains powered during Sleep
0 = Program memory bias voltage is powered down during Sleep and the voltage regulator enters Standby mode

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit[2]
1 = WDT is enabled
0 = WDT is disabled

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN[1:0] Configuration bits are ‘11’ (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.

3: This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

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REGISTER 7-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred (the BOR is also set after a POR)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN[1:0] Configuration bits are '11' (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.

3: This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON[15])	Trap Conflict Event	POR
IOPUWR (RCON[14])	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON[9])	Configuration Mismatch Reset	POR
EXTR (RCON[7])	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON[6])	RESET Instruction	POR
WDTO (RCON[4])	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON[3])	PWRSAV #SLEEP Instruction	POR
IDLE (RCON[2])	PWRSAV #IDLE Instruction	POR
BOR (RCON[1])	POR, BOR	—
POR (RCON[0])	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

7.1 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 7-2. If clock switching is disabled, the system clock source is always selected according to the Oscillator Configuration bits. For more information, see **Section 9.0 "Oscillator Configuration"**.

TABLE 7-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant
POR	FNOSC[2:0] Configuration bits (FOSCSEL[2:0])
BOR	
$\overline{\text{MCLR}}$	COSC[2:0] Control bits (OSCCON[14:12])
WDTO	
SWR	

7.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 7-3. Note that the System Reset signal, $\overline{\text{SYSRST}}$, is released after the POR and PWRT delay times expire.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable $\overline{\text{SYSRST}}$ delay times.

The FSCM delay determines the time at which the FSCM begins to monitor the system clock source after the $\overline{\text{SYSRST}}$ signal is released.

TABLE 7-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR(6)	EC	TPOR + TPWRT	—	1, 2
	FRC, FRCDIV	TPOR + TPWRT	TFRC	1, 2, 3
	LPRC	TPOR + TPWRT	TLPRC	1, 2, 3
	ECPLL	TPOR + TPWRT	TLOCK	1, 2, 4
	FRCPLL	TPOR + TPWRT	TFRC + TLOCK	1, 2, 3, 4
	XT, HS, SOSC	TPOR+ TPWRT	TOST	1, 2, 5
	XTPLL, HSPLL	TPOR + TPWRT	TOST + TLOCK	1, 2, 4, 5
BOR	EC	TPWRT	—	2
	FRC, FRCDIV	TPWRT	TFRC	2, 3
	LPRC	TPWRT	TLPRC	2, 3
	ECPLL	TPWRT	TLOCK	2, 4
	FRCPLL	TPWRT	TFRC + TLOCK	2, 3, 4
	XT, HS, SOSC	TPWRT	TOST	2, 5
	XTPLL, HSPLL	TPWRT	TFRC + TLOCK	2, 3, 4
All Others	Any Clock	—	—	None

Note 1: TPOR = Power-on Reset delay.

2: TPWRT = 64 ms nominal if the Power-up Timer is enabled; otherwise, it is zero.

3: TFRC and TLPRC = RC Oscillator start-up times.

4: TLOCK = PLL Lock time.

5: TOST = Oscillator Start-up Timer (OST). A 10-bit counter waits 1024 oscillator periods before releasing the oscillator clock to the system.

6: If Two-Speed Start-up is enabled, regardless of the Primary Oscillator selected, the device starts with FRC, and in such cases, FRC start-up time is valid.

Note: For detailed operating frequency and timing specifications, see **Section 27.0 "Electrical Characteristics"**.

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7.2.1 POR AND LONG OSCILLATOR START-UP TIMES

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer (OST) has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

7.2.2 FAIL-SAFE CLOCK MONITOR (FSCM) AND DEVICE RESETS

If the FSCM is enabled, it will begin to monitor the system clock source when $\overline{\text{SYSRST}}$ is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC Oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine (TSR).

7.3 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the FNOSCx bits in the Flash Configuration Word (FOSCSEL[2:0]); see Table 7-2. The RCFGCAL and NVMCON registers are only affected by a POR.

7.4 Brown-out Reset (BOR)

The PIC24FXXXXX family devices implement a BOR circuit, which provides the user several configuration and power-saving options. The BOR is controlled by the BORV[1:0] and BOREN[1:0] Configuration bits (FPOR[6:5,1:0]). There are a total of four BOR configurations, which are provided in Table 7-3.

The BOR threshold is set by the BORV[1:0] bits. If BOR is enabled (any values of BOREN[1:0], except '00'), any drop of V_{DD} below the set threshold point will reset the device. The chip will remain in BOR until V_{DD} rises above the threshold.

If the Power-up Timer is enabled, it will be invoked after V_{DD} rises above the threshold. Then, it will keep the chip in Reset for an additional time delay, T_{PWRT}, if V_{DD} drops below the threshold while the Power-up Timer is running. The chip goes back into a BOR and the Power-up Timer will be initialized. Once V_{DD} rises above the threshold, the Power-up Timer will execute the additional time delay.

BOR and the Power-up Timer (PWRT) are independently configured. Enabling the Brown-out Reset does not automatically enable the PWRT.

7.4.1 LOW-POWER BOR (LPBOR)

The Low-Power BOR is an alternate setting for the BOR, designed to consume minimal power. In LPBOR mode, BORV[1:0] (FPOR[6:5]) = 00. The BOR trip point is approximately 2.0V. Due to the low current consumption, the accuracy of the LPBOR mode can vary.

Unlike the other BOR modes, LPBOR mode will not cause a device Reset when V_{DD} drops below the trip point. Instead, it re-arms the POR circuit to ensure that the device will reset properly in the event that V_{DD} continues to drop below the minimum operating voltage.

The device will continue to execute code when V_{DD} is below the level of the LPBOR trip point. A device that requires falling edge BOR protection to prevent code from improperly executing should use one of the other BOR voltage settings.

7.4.2 SOFTWARE ENABLED BOR

When BOREN[1:0] = 01, the BOR can be enabled or disabled by the user in software. This is done with the control bit, SBOREN (RCON[13]). Setting SBOREN enables the BOR to function as previously described. Clearing the SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise, it is read as '0'.

Placing BOR under software control gives the user the additional flexibility of tailoring the application to its environment without having to reprogram the device to change the BOR configuration. It also allows the user to tailor the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

Note:	Even when the BOR is under software control, the Brown-out Reset voltage level is still set by the BORV[1:0] Configuration bits; it can not be changed in software.

7.4.3 DETECTING BOR

When BOR is enabled, the BOR bit (RCON[1]) is always reset to '1' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR and BOR bits are reset to '0' in the software immediately after any POR event. If the BOR bit is '1' while POR is '0', it can be reliably assumed that a BOR event has occurred.

7.4.4 DISABLING BOR IN SLEEP MODE

When BOREN[1:0] = 10, BOR remains under hardware control and operates as previously described. However, whenever the device enters Sleep mode, BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

Note:	BOR levels differ depending on device type; PIC24FV16KM204 devices are at different levels than those of PIC24F16KM204 devices. See **Section 27.0 "Electrical Characteristics"** for BOR voltage levels.

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8.0 INTERRUPT CONTROLLER

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Interrupt Controller, refer to **"Interrupts"** (www.microchip.com/DS70000600) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The PIC24F interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the CPU. It has the following features:

- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with up to 118 Vectors
- Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Alternate Interrupt Vector Table (AIVT) for Debug Support
- Fixed Interrupt Entry and Return Latencies

8.1 Interrupt Vector Table (IVT)

The IVT is shown in Figure 8-1. The IVT resides in the program memory, starting at location, 000004h. The IVT contains 126 vectors, consisting of eight non-maskable trap vectors, plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with Vector 0 will take priority over interrupts at any other vector address.

PIC24FV16KM204 family devices implement non-maskable traps and unique interrupts; these are summarized in Table 8-1.

8.1.1 ALTERNATE INTERRUPT VECTOR TABLE (AIVT)

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 8-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2[15]). If the ALTIVT bit is set, all interrupt and exception processes will use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports emulation and debugging efforts by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

8.2 Reset Sequence

A device Reset is not a true exception, because the interrupt controller is not involved in the Reset process. The PIC24F devices clear their registers in response to a Reset, which forces the Program Counter (PC) to zero. The microcontroller then begins program execution at location, 000000h. The user programs a `GOTO` instruction at the Reset address, which redirects the program execution to the appropriate start-up routine.

Note:	Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLE

Decreasing Natural Order Priority

Reset – GOTO Instruction	000000h	
Reset – GOTO Address	000002h	
Reserved	000004h	
Oscillator Fail Trap Vector		
Address Error Trap Vector		
Stack Error Trap Vector		
Math Error Trap Vector		
Reserved		
Reserved		
Reserved		
Interrupt Vector 0	000014h	Interrupt Vector Table (IVT)
Interrupt Vector 1		
—		
—		
—		
Interrupt Vector 52	00007Ch	
Interrupt Vector 53	00007Eh	
Interrupt Vector 54	000080h	
—		
—		
—		
Interrupt Vector 116	0000FCh	
Interrupt Vector 117	0000FEh	
Reserved	000100h	
Reserved	000102h	
Reserved		
Oscillator Fail Trap Vector		
Address Error Trap Vector		
Stack Error Trap Vector		
Math Error Trap Vector		
Reserved		
Reserved		Alternate Interrupt Vector Table (AIVT)
Reserved		
Interrupt Vector 0	000114h	
Interrupt Vector 1		
—		
—		
—		
Interrupt Vector 52	00017Ch	
Interrupt Vector 53	00017Eh	
Interrupt Vector 54	000180h	
—		
—		
—		
Interrupt Vector 116		
Interrupt Vector 117	0001FEh	
Start of Code	000200h	

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TABLE 8-1: TRAP VECTOR DETAILS

Vector Number	IVT Address	AIVT Address	Trap Source
0	000004h	000104h	Reserved
1	000006h	000106h	Oscillator Failure
2	000008h	000108h	Address Error
3	00000Ah	00010Ah	Stack Error
4	00000Ch	00010Ch	Math Error
5	00000Eh	00010Eh	Reserved
6	000010h	000110h	Reserved
7	000012h	000112h	Reserved

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS

Interrupt Source	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT Address	AIVT Address	Interrupt Bit Locations		
						Flag	Enable	Priority
INT0 – External Interrupt 0	__INT0Interrupt	8	0	000014h	000114h	IFS0[0]	IEC0[0]	IPC0[2:0]
MCCP1 – Capture/Compare 1	__CCP1Interrupt	9	1	000016h	000116h	IFS0[1]	IEC0[1]	IPC0[6:4]
MCCP2 – Capture/Compare 2	__CCP2Interrupt	10	2	000018h	000118h	IFS0[2]	IEC0[2]	IPC0[10:8]
TMR1 – Timer1	__T1Interrupt	11	3	00001Ah	00011Ah	IFS0[3]	IEC0[3]	IPC0[14:12]
MCCP3 – Capture/Compare 3	__CCP3Interrupt	13	5	00001Eh	00011Eh	IFS0[5]	IEC0[5]	IPC1[6:4]
SCCP4 – Capture/Compare 4	__CCP4Interrupt	14	6	000020h	000120h	IFS0[6]	IEC0[6]	IPC1[10:8]
MCCP1 – Time Base 1	__CCT1Interrupt	15	7	000022h	000122h	IFS0[7]	IEC0[7]	IPC1[14:12]
MCCP2 – Time Base 2	__CCT2Interrupt	16	8	000024h	000124h	IFS0[8]	IEC0[8]	IPC2[2:0]
UART1RX – UART1 Receiver	__U1RXInterrupt	19	11	00002Ah	00012Ah	IFS0[11]	IEC0[11]	IPC2[14:12]
UART1TX – UART1 Transmitter	__U1TXInterrupt	20	12	00002Ch	00012Ch	IFS0[12]	IEC0[12]	IPC3[2:0]
ADC1 – ADC1 Convert Done	__ADC1Interrupt	21	13	00002Eh	00012Eh	IFS0[13]	IEC0[13]	IPC3[6:4]
NVM – NVM Write Complete	__NVMInterrupt	23	15	000032h	000132h	IFS0[15]	IEC0[15]	IPC3[14:12]
MSSP1 – I^2C/SPI Interrupt 1	__MSSP1Interrupt	24	16	000034h	000134h	IFS1[0]	IEC1[0]	IPC4[2:0]
MSSP1 – Bus Collision Interrupt 1	__MSSP1BCInterrupt	25	17	000036h	000136h	IFS1[1]	IEC1[1]	IPC4[6:4]
Comparator Interrupt	__CompInterrupt	26	18	000038h	000138h	IFS1[2]	IEC1[2]	IPC4[10:8]
ICN – Input Change Notification	__CNInterrupt	27	19	00003Ah	00013Ah	IFS1[3]	IEC1[3]	IPC4[14:12]
INT1 – External Interrupt 1	__INT1Interrupt	28	20	00003Ch	00013Ch	IFS1[4]	IEC1[4]	IPC5[2:0]
SCCP5 – Capture/Compare 5	__CCP5Interrupt	30	22	000040h	000140h	IFS1[6]	IEC1[6]	IPC5[10:8]
MCCP3 – Time Base 3	__CCT3Interrupt	35	27	00004Ah	00014Ah	IFS1[11]	IEC1[11]	IPC6[14:12]
SCCP4 – Time Base 4	__CCT4Interrupt	36	28	00004Ch	00014Ch	IFS1[12]	IEC1[12]	IPC7[2:0]
INT2 – External Interrupt 2	__INT2Interrupt	37	29	00004Eh	00014Eh	IFS1[13]	IEC1[13]	IPC7[6:4]
UART2RX – UART2 Receiver	__U2RXInterrupt	38	30	000050h	000150h	IFS1[14]	IEC1[14]	IPC7[10:8]
UART2TX – UART2 Transmitter	__U2TXInterrupt	39	31	000052h	000152h	IFS1[15]	IEC1[15]	IPC7[14:12]
SCCP5 – Time Base 5	__CCT5Interrupt	49	41	000066h	000166h	IFS2[9]	IEC2[9]	IPC10[6:4]
MSSP2 – I^2C/SPI Interrupt 2	__MSSP2Interrupt	57	49	000076h	000176h	IFS3[1]	IEC3[1]	IPC12[6:4]
MSSP2 – Bus Collision Interrupt 2	__MSSP2BCInterrupt	58	50	000078h	000178h	IFS3[2]	IEC3[2]	IPC12[10:8]
RTCC – Real-Time Clock/Calendar	__RTCCInterrupt	70	62	000090h	000190h	IFS3[14]	IEC3[14]	IPC15[10:8]
U1Err – UART1 Error	__U1ErrInterrupt	73	65	000096h	000196h	IFS4[1]	IEC4[1]	IPC16[6:4]
U2Err – UART2 Error	__U2ErrInterrupt	74	66	000098h	000198h	IFS4[2]	IEC4[2]	IPC16[10:8]
HLVD – High/Low-Voltage Detect	__HLVDInterrupt	80	72	0000A4h	0001A4h	IFS4[8]	IEC4[8]	IPC18[2:0]
CTMU	__CTMUInterrupt	85	77	0000AEh	0001AEh	IFS4[13]	IEC4[13]	IPC19[6:4]
DAC1 – Buffer Update 1	__DAC1Interrupt	86	78	0000B0h	0001B0h	IFS4[14]	IEC4[14]	IPC19[10:8]
DAC2 – Buffer Update 2	__DAC2Interrupt	87	79	0000B2h	0001B2h	IFS4[15]	IEC4[15]	IPC19[14:12]
ULPWU – Ultra Low-Power Wake-up	__ULPWUInterrupt	88	80	0000B4h	0001B4h	IFS5[0]	IEC5[0]	IPC20[2:0]
CLC1	__CLC1Interrupt	104	96	0000D4h	0001D4h	IFS6[0]	IEC6[0]	IPC24[2:0]
CLC2	__CLC2Interrupt	105	97	0000D6h	0001D6h	IFS6[1]	IEC6[1]	IPC24[6:4]

8.3 Interrupt Control and Status Registers

The PIC24FV16KM204 family of devices implements a total of 33 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFS0 through IFS6
- IEC0 through IEC6
- IPC0 through IPC7, IPC10, IPC12, IPC15, IPC16, IPC18 through IPC20 and IPC24
- INTTREG

Global Interrupt Enable (GIE) control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the AIVT.

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals, or external signal, and is cleared via software.

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM[6:0]) and the Interrupt Level (ILR[3:0]) bit fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence. For example, the INT0 (External Interrupt 0) is depicted as having a vector number and a natural order priority of 0. The INT0IF status bit is found in IFS0[0], the INT0IE enable bit in IEC0[0] and the INT0IP[2:0] priority bits are in the first position of IPC0 (IPC0[2:0]).

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. The ALU STATUS Register (SR) contains the IPL[2:0] bits (SR[7:5]). These indicate the current CPU Interrupt Priority Level. The user may change the current CPU Interrupt Priority Level by writing to the IPLx bits.

The CORCON register contains the IPL3 bit, which together with IPL[2:0], also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that the trap events cannot be masked by the user's software.

All Interrupt registers are described in Register 8-3 through Register 8-35, in the following sections.

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REGISTER 8-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	HSC/R-0
—	—	—	—	—	—	—	DC(1)
bit 15							bit 8

HSC/R/W-0	HSC/R/W-0	HSC/R/W-0	HSC/R-0	HSC/R/W-0	HSC/R/W-0	HSC/R/W-0	HSC/R/W-0
IPL2(2,3)	IPL1(2,3)	IPL0(2,3)	RA(1)	N(1)	OV(1)	Z(1)	C(1)
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 7-5 **IPL[2:0]:** CPU Interrupt Priority Level Status bits(2,3)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

Note 1: See Register 3-1 for the description of these bits, which are not dedicated to interrupt control functions.

2: The IPL[2:0] bits are concatenated with the IPL3 bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the Interrupt Priority Level if IPL3 = 1.

3: The IPLx Status bits are read-only when NSTDIS (INTCON1[15]) = 1.

Note: Bit 8 and bits 4 through 0 are described in **Section 3.0 “CPU”**.

REGISTER 8-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	HSC/R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3[2]	PSV[1]	—	—
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit[2]
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 1-0 **Unimplemented:** Read as ‘0’

Note 1: See Register 3-2 for the description of this bit, which is not dedicated to interrupt control functions.
2: The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.

Note: Bit 2 is described in **Section 3.0 “CPU”**.

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REGISTER 8-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
NSTDIS	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	U-0
—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14-5 **Unimplemented:** Read as ‘0’

bit 4 **MATHERR:** Arithmetic Error Trap Status bit
1 = Overflow trap has occurred
0 = Overflow trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	HSC/R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table (AIVT)
0 = Uses standard (default) Interrupt Vector Table (IVT)

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

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REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

HS/R/W-0	U-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	U-0	U-0	HS/R/W-0
NVMIF	—	AD1IF	U1TXIF	U1RXIF	—	—	CCT2IF
bit 15							bit 8

HS/R/W-0	HS/R/W-0	HS/R/W-0	U-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0
CCT1IF	CCP4IF	CCP3IF	—	T1IF	CCP2IF	CCP1IF	INT0IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NVMIF:** NVM Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **AD1IF:** A/D Conversion Complete Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **U1TXIF:** UART1 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **U1RXIF:** UART1 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **CCT2IF:** Capture/Compare 2 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **CCT1IF:** Capture/Compare 1 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **CCP4IF:** Capture/Compare 4 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **CCP3IF:** Capture/Compare 3 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **T1IF:** Timer1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **CCP2IF:** Capture/Compare 2 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **CCP1IF:** Capture/Compare 1 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	U-0	U-0	U-0
U2TXIF	U2RXIF	INT2IF	CCT4IF	CCT3IF	—	—	—
bit 15							bit 8

U-0	HS/R/W-0	U-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0	HS/R/W-0
—	CCP5IF	—	INT1IF	CNIF	CMIF	BCL1IF	SSP1IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIF:** UART2 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **U2RXIF:** UART2 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **INT2IF:** External Interrupt 2 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **CCT4IF:** Capture/Compare 4 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **CCT3IF:** Capture/Compare 3 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10-7 **Unimplemented:** Read as ‘0’

bit 6 **CCP5IF:** Capture/Compare 5 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CNIF:** Input Change Notification Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **CMIF:** Comparator Interrupt Flag Status Bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **BCL1IF:** MSSP1 I^2C Bus Collision Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **SI2C1IF:** MSSP1 SPI/I^2C Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

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REGISTER 8-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	HS/R/W-0	U-0
—	—	—	—	—	—	CCT5IF	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9 **CCT5IF:** Capture/Compare 5 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8-0 **Unimplemented:** Read as ‘0’

REGISTER 8-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3

U-0	HS/R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	RTCIF	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	HS/R/W-0	HS/R/W-0	U-0
—	—	—	—	—	BCL2IF	SSP2IF	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **RTCIF:** Real-Time Clock and Calendar Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **BCL2IF:** MSSP2 I^2C Bus Collision Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **SSP2IF:** MSSP2 SPI/I^2C Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 8-9: IFS4: INTERRUPT FLAG STATUS REGISTER 4

HS/R/W-0	HS/R/W-0	HS/R/W-0	U-0	U-0	U-0	U-0	R/W-0, HS
DAC2IF	DAC1IF	CTMUIF	—	—	—	—	HLVDIF
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	HS/R/W-0	HS/R/W-0	U-0
—	—	—	—	—	U2ERIF	U1ERIF	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DAC2IF:** Digital-to-Analog Converter 2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **DAC1IF:** Digital-to-Analog Converter 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **CTMUIF:** CTMU Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **HLVDIF:** High/Low-Voltage Detect Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **U2ERIF:** UART2 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **U1ERIF:** UART1 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **Unimplemented:** Read as ‘0’

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REGISTER 8-10: IFS5: INTERRUPT FLAG STATUS REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	HS/R/W-0
—	—	—	—	—	—	—	ULPWUIF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **ULPWUIF:** Ultra Low-Power Wake-up Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-11: IFS6: INTERRUPT FLAG STATUS REGISTER 6

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	HS/R/W-0	HS/R/W-0
—	—	—	—	—	—	CLC2IF	CLC1IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1 **CLC2IF:** Configurable Logic Cell 2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **CLC1IF:** Configurable Logic Cell 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-12: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
NVMIE	—	AD1IE	U1TXIE	U1RXIE	—	—	CCT2IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CCT1IE	CCP4IE	CCP3IE	—	T1IE	CCP2IE	CCP1IE	INT0IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NVMIE:** NVM Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **AD1IE:** A/D Conversion Complete Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **U1RXIE:** UART1 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **CCT2IE:** Capture/Compare 2 Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **CCT1IE:** Capture/Compare 1 Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **CCP4IE:** Capture/Compare 4 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **CCP3IE:** Capture/Compare 3 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **T1IE:** Timer1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CCP2IE:** Capture/Compare 2 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **CCP1IE:** Capture/Compare 1 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **INT0IE:** External Interrupt 0 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

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REGISTER 8-13: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
U2TXIE	U2RXIE	INT2IE	CCT4IE	CCT3IE	—	—	—
bit 15							bit 8

U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CCP5IE	—	INT1IE	CNIE	CMIE	BCL1IE	SSP1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIE:** UART2 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **U2RXIE:** UART2 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **CCT4IE:** Capture/Compare 4 Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **CCT3IE:** Capture/Compare 3 Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10-7 **Unimplemented:** Read as ‘0’

bit 6 **CCP5IE:** Capture/Compare 5 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **CNIE:** Input Change Notification Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CMIE:** Comparator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **BCL1IE:** MSSP1 I^2C Bus Collision Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SSP1IE:** MSSP1 SPI/I^2C Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-14: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	CCT5IE	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9 **CCT5IE:** Capture/Compare 5 Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8-0 **Unimplemented:** Read as ‘0’

REGISTER 8-15: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	RTCIE	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	BCL2IE	SSP2IE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **RTCIE:** Real-Time Clock and Calendar Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **BCL2IE:** MSSP2 I^2C Bus Collision Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **SSP2IE:** MSSP2 SPI/I^2C Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as ‘0’

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REGISTER 8-16: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
DAC2IE	DAC1IE	CTMUIE	—	—	—	—	HLVDIE
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	U2ERIE	U1ERIE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DAC2IE:** Digital-to-Analog Converter 2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **DAC1IE:** Digital-to-Analog Converter 1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **U2ERIE:** UART2 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U1ERIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 8-17: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ULPWUIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **ULPWUIE:** Ultra Low-Power Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-18: IEC6: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CLC2IE	CLC1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1 **CLC2IE:** Configurable Logic Cell 2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **CLC1IE:** Configurable Logic Cell 1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

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REGISTER 8-19: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T1IP2	T1IP1	T1IP0	—	CCP2IP2	CCP2IP1	CCP2IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCP1IP2	CCP1IP1	CCP1IP0	—	INT0IP2	INT0IP1	INT0IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T1IP[2:0]:** Timer1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP2IP[2:0]:** Capture/Compare 2 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **CCP1IP[2:0]:** Capture/Compare 1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT0IP[2:0]:** External Interrupt 0 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-20: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCT1IP2	CCT1IP1	CCT1IP0	—	CCP4IP2	CCP4IP1	CCP4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CCP3IP2	CCP3IP1	CCP3IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CCT1IP[2:0]:** Capture/Compare 1 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP4IP[2:0]:** Capture/Compare 4 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **CCP3IP[2:0]:** Capture/Compare 3 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

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REGISTER 8-21: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1RXIP2	U1RXIP1	U1RXIP0	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	CCT2IP2	CCT2IP1	CCT2IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U1RXIP[2:0]:** UART1 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-3 **Unimplemented:** Read as ‘0’

bit 2-0 **CCT2IP[2:0]:** Capture/Compare 2 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-22: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **NVMIP[2:0]:** NVM Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP[2:0]:** A/D Conversion Complete Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP[2:0]:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

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REGISTER 8-23: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	BCL1IP2	BCL1IP1	BCL1IP0	—	SSP1IP2	SSP1IP1	SSP1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP[2:0]:** Input Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CMIP[2:0]:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **BCL1IP[2:0]:** MSSP1 I^2C Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SSP1IP[2:0]:** MSSP1 SPI/I^2C Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-24: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	CCP5IP2	CCP5IP1	CCP5IP0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP5IP[2:0]:** Capture/Compare 5 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT1IP[2:0]:** External Interrupt 1 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

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REGISTER 8-25: IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CCT3IP2	CCT3IP1	CCT3IP0	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CCT3IP[2:0]:** Capture/Compare 3 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-0 **Unimplemented:** Read as ‘0’

REGISTER 8-26: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	INT2IP2	INT2IP1	INT2IP0	—	CCT4IP2	CCT4IP1	CCT4IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U2TXIP[2:0]:** UART2 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U2RXIP[2:0]:** UART2 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **INT2IP[2:0]:** External Interrupt 2 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **CCT4IP[2:0]:** Capture/Compare 4 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

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REGISTER 8-27: IPC10: INTERRUPT PRIORITY CONTROL REGISTER 10

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CCT5IP2	CCT5IP1	CCT5IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CCT5IP[2:0]:** Capture/Compare 5 Timer Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 8-28: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	BCL2IP2	BCL2IP1	BCL2IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	SSP2IP2	SSP2IP1	SSP2IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **BCL2IP[2:0]:** MSSP2 I^2C Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SSP2IP[2:0]:** MSSP2 SPI/I^2C Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

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REGISTER 8-29: IPC15: INTERRUPT PRIORITY CONTROL REGISTER 15

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	RTCIP2	RTCIP1	RTCIP0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **RTCIP[2:0]:** Real-Time Clock and Calendar Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 8-30: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	U2ERIP2	U2ERIP1	U2ERIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **U2ERIP[2:0]:** UART2 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **U1ERIP[2:0]:** UART1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

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REGISTER 8-31: IPC18: INTERRUPT PRIORITY CONTROL REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **HLVDIP[2:0]:** High/Low-Voltage Detect Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

REGISTER 8-32: IPC19: INTERRUPT PRIORITY CONTROL REGISTER 19

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	DAC2IP2	DAC2IP1	DAC2IP0	—	DAC1IP2	DAC1IP1	DAC1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CTMUIP2	CTMUIP1	CTMUIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **DAC2IP[2:0]:** Digital-to-Analog Converter 2 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **DAC1IP[2:0]:** Digital-to-Analog Converter 1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **CTMUIP[2:0]:** CTMU Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

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REGISTER 8-33: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	ULPWUIP2	ULPWUIP1	ULPWUIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ULPWUIP[2:0]:** Ultra Low-Power Wake-up Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-34: IPC24: INTERRUPT PRIORITY CONTROL REGISTER 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CLC2IP2	CLC2IP1	CLC2IP0	—	CLC1IP2	CLC1IP1	CLC1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CLC2IP[2:0]:** CLC2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **CLC1IP[2:0]:** CLC1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-35: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

R-0	U-0	R/W-0	U-0	R-0	R-0	R-0	R-0
CPUIRQ	—	VHOLD	—	ILR3	ILR2	ILR1	ILR0
bit 15							bit 8

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM[6:0]						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CPUIRQ:** Interrupt Request from Interrupt Controller CPU bit

`1` = An interrupt request has occurred but has not yet been Acknowledged by the CPU (this will happen when the CPU priority is higher than the interrupt priority)

`0` = No interrupt request is left unacknowledged

bit 14 **Unimplemented:** Read as ‘`0`’

bit 13 **VHOLD:** Vector Hold bit

Allows Vector Number Capture and Changes which Interrupt is Stored in the VECNUM[6:0] bits:

`1` = VECNUM[6:0] will contain the value of the highest priority pending interrupt, instead of the current interrupt

`0` = VECNUM[6:0] will contain the value of the last Acknowledged interrupt (last interrupt that has occurred with higher priority than the CPU, even if other interrupts are pending)

bit 12 **Unimplemented:** Read as ‘`0`’

bit 11-8 **ILR[3:0]:** New CPU Interrupt Priority Level bits

`1111` = CPU Interrupt Priority Level is 15

•
•
•

`0001` = CPU Interrupt Priority Level is 1

`0000` = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as ‘`0`’

bit 6-0 **VECNUM[6:0]:** Vector Number of Pending Interrupt bits

`0111111` = Interrupt vector pending is Number 135

•
•
•

`0000001` = Interrupt vector pending is Number 9

`0000000` = Interrupt vector pending is Number 8

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8.4 Interrupt Setup Procedures

8.4.1 INITIALIZATION

To configure an interrupt source:

1. Set the NSTDIS control bit (INTCON1[15]) if nested interrupts are not desired.
2. Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources may be programmed to the same non-zero value.

Note:	At a device Reset, the IPCx registers are initialized, such that all user interrupt sources are assigned to Priority Level 4.

3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

8.4.2 INTERRUPT SERVICE ROUTINE

The method that is used to declare an ISR (Interrupt Service Routine) and initialize the IVT with the correct vector address depends on the programming language (i.e., C or assembly), and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of the interrupt that the ISR handles. Otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a `RETFIE` instruction to unstack the saved PC value, SRL value and old CPU priority level.

8.4.3 TRAP SERVICE ROUTINE (TSR)

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

8.4.4 INTERRUPT DISABLE

All user interrupts can be disabled using the following procedure:

1. Push the current SR value onto the software stack using the `PUSH` instruction.
2. Force the CPU to Priority Level 7 by inclusive ORing the value, 0Eh, with SRL.

To enable user interrupts, the `POP` instruction may be used to restore the previous SR value.

Only user interrupts with a priority level of 7 or less can be disabled. Trap sources (Levels 8-15) cannot be disabled.

The `DISI` instruction provides a convenient way to disable interrupts of Priority Levels 1-6 for a fixed period. Level 7 interrupt sources are not disabled by the `DISI` instruction.

NOTES:

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9.0 OSCILLATOR CONFIGURATION

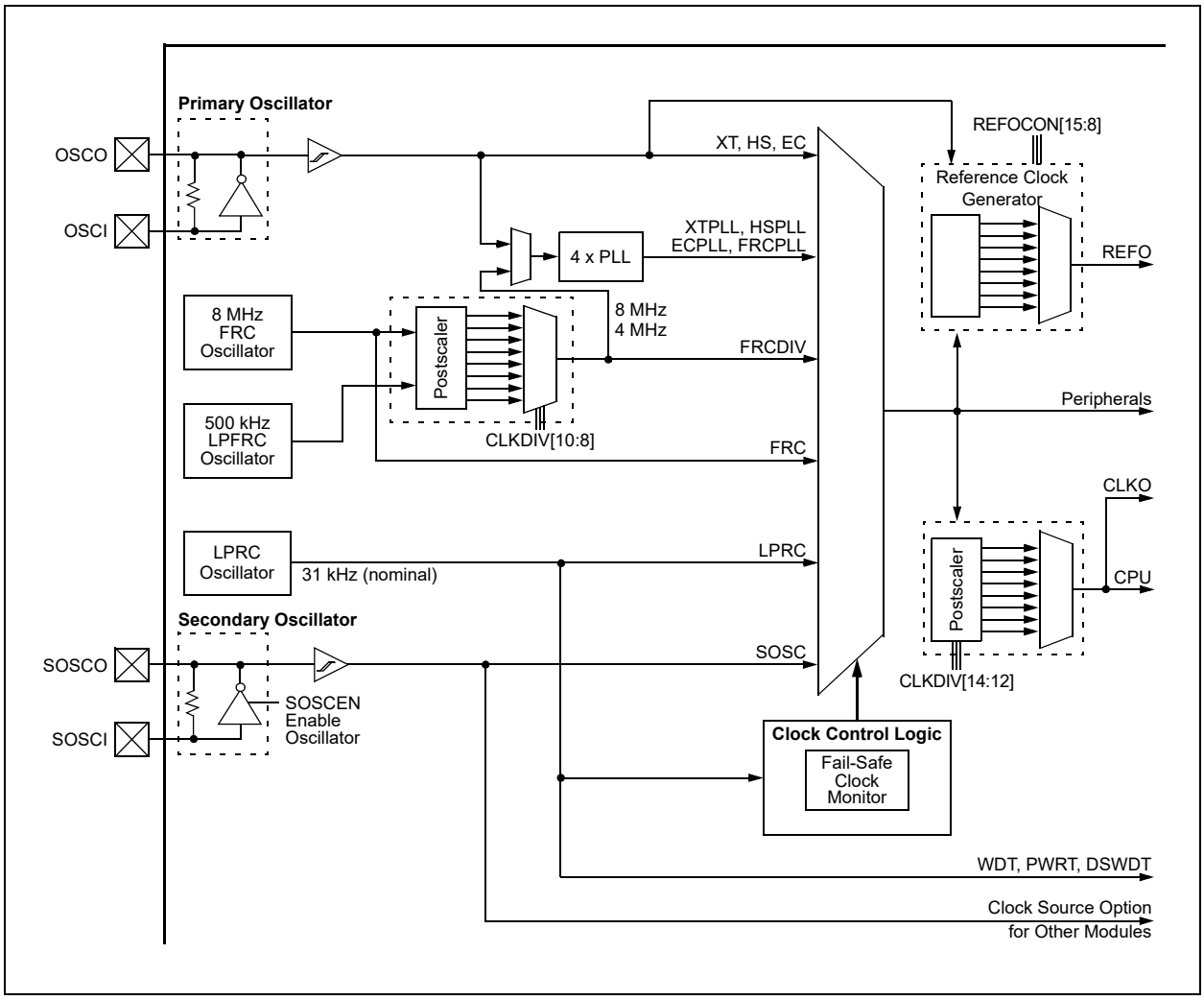
Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on oscillator configuration, refer to **"Oscillator with 500 kHz Low-Power FRC"** (www.microchip.com/DS39726) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The oscillator system for the PIC24FV16KM204 family of devices has the following features:

- A total of five external and internal oscillator options as clock sources, providing 11 different clock modes.
- On-chip 4x Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources.
- Software-controllable switching between various clock sources.
- Software-controllable postscaler for selective clocking of CPU for system power savings.
- System frequency range declaration bits for External Clock (EC) mode. When using an EC source, the current consumption is reduced by setting the declaration bits to the expected frequency range.
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown.

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: PIC24FXXXXX FAMILY CLOCK DIAGRAM



9.1 CPU Clocking Scheme

The system clock source can be provided by one of four sources:

- Primary Oscillator (POSC) on the OSCI and OSCO pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins

  The PIC24FXXXXX family devices consist of two types of secondary oscillator:

  - High-Power Secondary Oscillator
  - Low-Power Secondary Oscillator

  These can be selected by using the SOSCSEL (FOSC[5]) bit.
- Fast Internal RC (FRC) Oscillator:
  - 8 MHz FRC Oscillator
  - 500 kHz Lower Power FRC Oscillator
- Low-Power Internal RC (LPRC) Oscillator with two modes:
  - High-Power/High-Accuracy mode
  - Low-Power/Low-Accuracy mode

The Primary Oscillator and 8 MHz FRC sources have the option of using the internal 4x PLL. The frequency of the FRC clock source can optionally be reduced by the programmable clock divider. The selected clock source generates the processor and peripheral clock sources.

The processor clock source is divided by two to produce the internal instruction cycle clock, FCY. In this document, the instruction cycle clock is also denoted by FOSC/2. The internal instruction cycle clock, FOSC/2, can be provided on the OSCO I/O pin for some operating modes of the Primary Oscillator.

9.2 Initial Configuration on POR

The oscillator source (and operating mode) that is used at a device Power-on Reset (POR) event is selected using Configuration bit settings. The Oscillator Configuration bit settings are located in the Configuration registers in the program memory (for more information, see **Section 25.1 “Configuration Bits”**). The Primary Oscillator Configuration bits, POSCMOD[1:0] (FOSC[1:0]), and the Initial Oscillator Select Configuration bits, FNOSC[2:0] (FOSCSEL[2:0]), select the oscillator source that is used at a POR. The FRC Primary Oscillator with Postscaler (FRCDIV) is the default (unprogrammed) selection. The Secondary Oscillator, or one of the internal oscillators, may be chosen by programming these bit locations. The EC mode Frequency Range Configuration bits, POSCFREQ[1:0] (FOSC[4:3]), optimize power consumption when running in EC mode. The default configuration is “frequency range is greater than 8 MHz”.

The Configuration bits allow users to choose between the various clock modes, as shown in Table 9-1.

9.2.1 CLOCK SWITCHING MODE CONFIGURATION BITS

The FCKSM[1:0] Configuration bits (FOSC[7:6]) are used jointly to configure device clock switching and the FSCM. Clock switching is enabled only when FCKSM1 is programmed (‘0’). The FSCM is enabled only when FCKSM[1:0] are both programmed (‘00’).

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMOD[1:0]	FNOSC[2:0]	Notes
8 MHz FRC Oscillator with Postscaler (FRCDIV)	Internal	11	111	1, 2
500 kHz FRC Oscillator with Postscaler (LPFRCDIV)	Internal	11	110	1
Low-Power RC Oscillator (LPRC)	Internal	11	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	00	100	1
Primary Oscillator (HS) with PLL Module (HSPLL)	Primary	10	011	
Primary Oscillator (EC) with PLL Module (ECPLL)	Primary	00	011	
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	
8 MHz FRC Oscillator with PLL Module (FRCPLL)	Internal	11	001	1
8 MHz FRC Oscillator (FRC)	Internal	11	000	1

Note 1: The OSCO pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

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9.3 Control Registers

The operation of the oscillator is controlled by three Special Function Registers (SFRs):

- OSCCON
- CLKDIV
- OSCTUN

The OSCCON register (Register 9-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources.

The Clock Divider register (Register 9-2) controls the features associated with Doze mode, as well as the postscaler for the FRC Oscillator.

The FRC Oscillator Tune register (Register 9-3) allows the user to fine-tune the FRC Oscillator over a range of approximately ±5.25%. Each bit increment or decrement changes the factory calibrated frequency of the FRC Oscillator by a fixed amount.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	HSC/R-0	HSC/R-0	HSC/R-0	U-0	R/W-x(1)	R/W-x(1)	R/W-x(1)
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15							bit 8

HSC/R/SO-0	U-0	HSC/R-0(2)	U-0	HS/R/CO-0	R/W-0(3)	R/W-0	R/W-0
CLKLOCK	—	LOCK	—	CF	SOSCDRV	SOSCEN	OSWEN
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
HS = Hardware Settable bit	CO = Clearable Only bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC[2:0]:** Current Oscillator Selection bits
- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC[2:0]:** New Oscillator Selection bits(1)
- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

Note 1: Reset values for these bits are determined by the FNOSCx Configuration bits.

2: This bit also resets to ‘0’ during any valid clock switch or whenever a non-PLL Clock mode is selected.

3: When SOSC is selected to run from a digital clock input rather than an external crystal (SOSCSRC = 0), this bit has no effect.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
If FSCM is Enabled (FCKSM1 = 1):
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
If FSCM is Disabled (FCKSM1 = 0):
Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **Unimplemented:** Read as '0'

bit 5 **LOCK:** PLL Lock Status bit(2)
1 = PLL module is in lock or PLL module start-up timer is satisfied
0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **SOSCDRV**: Secondary Oscillator Drive Strength bit(3)
1 = High-power SOSC circuit is selected
0 = Low/high-power select is done via the SOSCSRC Configuration bit

bit 1 **SOSCEN:** 32 kHz Secondary Oscillator (SOSC) Enable bit
1 = Enables the Secondary Oscillator
0 = Disables the Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Initiates an oscillator switch to the clock source specified by the NOSC[2:0] bits
0 = Oscillator switch is complete

Note 1: Reset values for these bits are determined by the FNOSCx Configuration bits.
2: This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
3: When SOSC is selected to run from a digital clock input rather than an external crystal (SOSCSRC = 0), this bit has no effect.

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REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
ROI	DOZE2	DOZE1	DOZE0	DOZEN(1)	RCDIV2	RCDIV1	RCDIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts clear the DOZEN bit, and reset the CPU and peripheral clock ratio to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE[2:0]:** CPU and Peripheral Clock Ratio Select bits
111 = 1:128
110 = 1:64
101 = 1:32
100 = 1:16
011 = 1:8
010 = 1:4
001 = 1:2
000 = 1:1

bit 11 **DOZEN:** Doze Enable bit(1)
1 = DOZE[2:0] bits specify the CPU and peripheral clock ratio
0 = CPU and peripheral clock ratio are set to 1:1

bit 10-8 **RCDIV[2:0]:** FRC Postscaler Select bits
When COSC[2:0] (OSCCON[14:12]) = 111:
111 = 31.25 kHz (divide-by-256)
110 = 125 kHz (divide-by-64)
101 = 250 kHz (divide-by-32)
100 = 500 kHz (divide-by-16)
011 = 1 MHz (divide-by-8)
010 = 2 MHz (divide-by-4)
001 = 4 MHz (divide-by-2) – default
000 = 8 MHz (divide-by-1)
When COSC[2:0] (OSCCON[14:12]) = 110:
111 = 1.95 kHz (divide-by-256)
110 = 7.81 kHz (divide-by-64)
101 = 15.62 kHz (divide-by-32)
100 = 31.25 kHz (divide-by-16)
011 = 62.5 kHz (divide-by-8)
010 = 125 kHz (divide-by-4)
001 = 250 kHz (divide-by-2) – default
000 = 500 kHz (divide-by-1)

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.

REGISTER 9-3: OSCTUN: FRC OSCILLATOR TUNE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN[5:0][1]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN[5:0]:** FRC Oscillator Tuning bits[1]

011111 = Maximum frequency deviation
011110
•
•
•
000001
000000 = Center frequency, oscillator is running at factory calibrated frequency
111111
•
•
•
100001
100000 = Minimum frequency deviation

Note 1: Increments or decrements of TUN[5:0] may not change the FRC frequency in equal steps over the FRC tuning range and may not be monotonic.

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9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMODx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to '0'. (Refer to **Section 25.0 "Special Features"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and FSCM function are disabled; this is the default setting.

The NOSCx control bits (OSCCON[10:8]) do not control the clock selection when clock switching is disabled. However, the COSCx bits (OSCCON[14:12]) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON[0]) has no effect when clock switching is disabled; it is held at '0' at all times.

9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSCx bits (OSCCON[14:12]) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSCx bits (OSCCON[10:8]) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically, as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON[5]) and CF (OSCCON[3]) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for ten clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT, FSCM or RTCC with LPRC as a clock source is enabled) or SOSC (if SOSCEN remains enabled).

Note 1: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: An unlock sequence must be performed before a write to OSCCON is allowed.

The following code sequence for a clock switch is recommended:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON[15:8], in two back-to-back instructions.
3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON[7:0], in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1 and Example 9-2.

EXAMPLE 9-1: ASSEMBLY CODE SEQUENCE FOR CLOCK SWITCHING

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV         #OSCCONH, w1
MOV         #0x78, w2
MOV         #0x9A, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Set new oscillator selection
MOV.b       WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV         #OSCCONL, w1
MOV         #0x46, w2
MOV         #0x57, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Start oscillator switch operation
BSET        OSCCON,#0
```

EXAMPLE 9-2: BASIC 'C' CODE SEQUENCE FOR CLOCK SWITCHING

```
//Use compiler built-in function to write
new clock setting
__builtin_write_OSCCONH(0x01); //0x01
switches to FRCPLL

//Use compiler built-in function to set the
OSWEN bit.
__builtin_write_OSCCONL(OSCCONL | 0x01);

//Optional: Wait for clock switch sequence
to complete
while(OSCCONbits.OSWEN == 1);
```

9.5 Reference Clock Output

In addition to the CLKO output (FOSC/2) available in certain oscillator modes, the device clock in the PIC24FXXXXX family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCON register (Register 9-4). Setting the ROEN bit (REFOCON[15]) makes the clock signal available on the REFO pin. The RODIV[3:0] bits (REFOCON[11:8]) enable the selection of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON[13:12]) control the availability of the reference output during Sleep mode. The ROSEL bit determines if the oscillator on OSC1 and OSC2, or the current system clock source, is used for the reference clock output. The ROSSLP bit determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSSLP and ROSEL bits must be set. The device clock must also be configured for one of the primary modes (EC, HS or XT); otherwise, if the ROSEL bit is not also set, the oscillator on OSC1 and OSC2 will be powered down when the device enters Sleep mode. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

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REGISTER 9-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Oscillator Output Enable bit
1 = Reference Oscillator is enabled on the REFO pin
0 = Reference Oscillator is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **ROSSLP:** Reference Oscillator Output Stop in Sleep bit
1 = Reference Oscillator continues to run in Sleep
0 = Reference Oscillator is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Primary Oscillator is used as the base clock(1)
0 = System clock is used as the base clock; base clock reflects any clock switching of the device

bit 11-8 **RODIV[3:0]:** Reference Oscillator Divisor Select bits
1111 = Base clock value divided by 32,768
1110 = Base clock value divided by 16,384
1101 = Base clock value divided by 8,192
1100 = Base clock value divided by 4,096
1011 = Base clock value divided by 2,048
1010 = Base clock value divided by 1,024
1001 = Base clock value divided by 512
1000 = Base clock value divided by 256
0111 = Base clock value divided by 128
0110 = Base clock value divided by 64
0101 = Base clock value divided by 32
0100 = Base clock value divided by 16
0011 = Base clock value divided by 8
0010 = Base clock value divided by 4
0001 = Base clock value divided by 2
0000 = Base clock value

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: The crystal oscillator must be enabled using the FOSC[2:0] bits; the crystal maintains the operation in Sleep mode.

NOTES:

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10.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Power-Saving Features with VBAT"** (www.microchip.com/30622) in the *"dsPIC33/PIC24F Family Reference Manual"*.

This FRM describes some features which are not implemented in this device. Sections related to the VBAT pin and Deep Sleep do not apply to the PIC24FV16KM204 family.

The PIC24FV16KM204 family of devices provides the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. All PIC24F devices manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption, while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits. The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

PIC24F devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution; Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation.

The 'C' syntax of the `PWRSAV` instruction is shown in Example 10-1.

Note: `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

10.2.1 SLEEP MODE

Sleep mode includes these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be reduced to a minimum provided that no I/O pin is sourcing current.
- The I/O pin directions and states are frozen.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT or RTCC with LPRC as the clock source is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items, such as the Input Change Notification on the I/O ports or peripherals that use an External Clock input. Any peripheral that requires the system clock source for its operation will be disabled in Sleep mode.

The device will wake-up from Sleep mode on any of these events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

On wake-up from Sleep, the processor will restart with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: 'C' POWER-SAVING ENTRY

```
Sleep();                //Put the device into Sleep mode
Idle();                 //Put the device into Idle mode
```

10.2.2 IDLE MODE

Idle mode includes these features:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.6 "Selective Peripheral Module Control"**).
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the `PWRSAV` instruction or the first instruction in the ISR.

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAV` instruction will be held off until entry into Sleep or Idle mode has completed. The device will then wake-up from Sleep or Idle mode.

10.2.3.1 Power-on Resets (PORs)

V_{DD} voltage is monitored to produce PORs. When a true POR occurs, the entire device is reset.

10.3 Ultra Low-Power Wake-up

The Ultra Low-Power Wake-up (ULPWU) on pin, RB0, allows a slow falling voltage to generate an interrupt without excess current consumption.

To use this feature:

1. Charge the capacitor on RB0 by configuring the RB0 pin to an output and setting it to '`1`'.
2. Stop charging the capacitor by configuring RB0 as an input.
3. Discharge the capacitor by setting the ULPEN and ULPSINK bits in the ULPWCON register.
4. Configure Sleep mode.
5. Enter Sleep mode.

When the voltage on RB0 drops below V_{IL}, the device wakes up and executes the next instruction.

This feature provides a low-power technique for periodically waking up the device from Sleep mode.

The time-out is dependent on the discharge time of the RC circuit on RB0.

When the ULPWU module wakes the device from Sleep mode, the ULPWUIF bit (IFS5[0]) is set. Software can check this bit upon wake-up to determine the wake-up source.

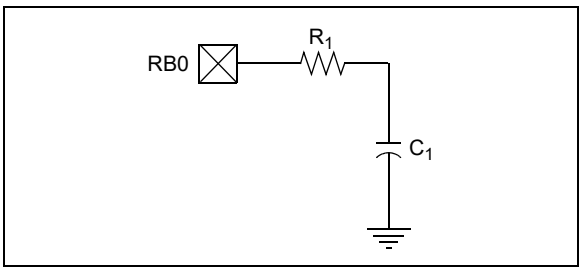
See Example 10-2 for initializing the ULPWU module.

EXAMPLE 10-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION

```
//*******************************
// 1. Charge the capacitor on RB0
//*******************************
    TRISBbits.TRISB0 = 0;
    LATBbits.LATB0 = 1;
    for(i = 0; i < 10000; i++) Nop();
//*****************************
//2. Stop Charging the capacitor
//   on RB0
//*****************************
    TRISBbits.TRISB0 = 1;
//*****************************
//3. Enable ULPWU Interrupt
//*****************************
IFS5bits.ULPWUIF = 0;
IEC5bits.ULPWUIE = 1;
IPC21bits.ULPWUIP = 0x7;
//*****************************
//4. Enable the Ultra Low Power
//   Wakeup module and allow
//   capacitor discharge
//*****************************
    ULPWCONbits.ULPEN = 1;
    ULPWCONbit.ULPSINK = 1;
//*****************************
//5. Enter Sleep Mode
//*****************************
    Sleep();
//for sleep, execution will
//resume here
```

A series resistor, between RB0 and the external capacitor provides overcurrent protection for the AN2/ULPWU/RB0 pin and enables software calibration of the time-out (see Figure 10-1).

FIGURE 10-1: SERIES RESISTOR



A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired delay in Sleep. This technique compensates for the affects of temperature, voltage and component accuracy. The peripheral can also be configured as a simple, programmable Low-Voltage Detect (LVD) or temperature sensor.

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REGISTER 10-1: ULPWCON: ULPWU CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
ULPEN	—	ULPSIDL	—	—	—	—	ULPSINK
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ULPEN:** ULPWU Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **ULPSIDL:** ULPWU Stop in Idle Select bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **ULPSINK:** ULPWU Current Sink Enable bit
1 = Current sink is enabled
0 = Current sink is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

10.4 Voltage Regulator-Based Power-Saving Features

The PIC24FV16KM204 family series devices have a voltage regulator that has the ability to alter functionality to provide power savings. The on-chip regulator is made up of two basic modules: the Voltage Regulator (VREG) and the Retention Regulator (RETREG). With the combination of VREG and RETREG, the following power modes are available:

10.4.1 RUN MODE

In Run mode, the main VREG is providing a regulated voltage with enough current to supply a device running at full speed and the device is not in Sleep mode. The RETREG may or may not be running, but is unused.

10.4.2 SLEEP MODE

In Sleep mode, the device is in Sleep and the main VREG is providing a regulated voltage to the core. By default, in Sleep mode, the regulator enters a Low-Power Standby state which consumes reduced quiescent current. The PMSLP bit (RCON[8]) controls the regulator state in Sleep mode. If the PMSLP bit is set, the program Flash memory will stay powered on during Sleep mode and the regulator will stay in its full-power mode.

10.4.3 RETENTION REGULATOR

The Retention Regulator, sometimes referred to as the low-voltage regulator, is designed to provide power to the core at a lower voltage than the standard voltage regulator, while consuming significantly lower quiescent current. Refer to **Section 27.0 "Electrical Characteristics"** for the voltage output range of the RETREG. This regulator is only used in Sleep mode, and has limited output current to maintain the RAM and provide power for limited peripherals, such as the WDT, while the device is in Sleep. It is controlled by the RETCFG Configuration bit (FPOR[2]) and in firmware by the RETEN bit (RCON[12]). RETCFG must be programmed (= 0) and the RETEN bit must be set (= 1) for the Retention Regulator to be enabled.

10.4.4 RETENTION SLEEP MODE

In Retention Sleep mode, the device is in Sleep and all regulated voltage is provided solely by the RETREG, while the main VREG is disabled. Consequently, this mode provides the lowest Sleep power consumption, but has a trade-off of a longer wake-up time. The low-voltage Sleep wake-up time is longer than Sleep mode due to the extra time required to re-enable the VREG and raise the V_{DDCORE} supply rail back to normal regulated levels.

> **Note:** The PIC24F16KM204 family devices do not have any internal voltage regulation, and therefore, do not support Retention Sleep mode.

TABLE 10-1: VOLTAGE REGULATION CONFIGURATION SETTINGS FOR PIC24FXXXXX FAMILY DEVICES

RETCFG Bit (FPOR[2])	RETEN Bit (RCON[12]	PMSLP Bit (RCON[8])	Power Mode During Sleep	Description
0	0	1	Sleep	VREG mode (normal) is unchanged during Sleep. RETREG is unused.
0	0	0	Sleep (Standby)	VREG goes to Low-Power Standby mode during Sleep. RETREG is unused.
0	1	0	Retention Sleep	VREG is off during Sleep. RETREG is enabled and provides Sleep voltage regulation.
1	x	1	Sleep	VREG mode (normal) is unchanged during Sleep. RETREG is disabled at all times.
1	x	0	Sleep (Standby)	VREG goes to Low-Power Standby mode during Sleep. RETREG is disabled at all times.

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10.5 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV[11]). The ratio between peripheral and core clock speed is determined by the DOZE[2:0] bits (CLKDIV[14:12]). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default.

It is also possible to use Doze mode to selectively reduce power consumption in event driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption. Meanwhile, the CPU Idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV[15]). By default, interrupt events have no effect on Doze mode operation.

10.6 Selective Peripheral Module Control

Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume power. There may be cases where the application needs what these modes do not provide: the allocation of power resources to CPU processing with minimal power consumption from the peripherals.

PIC24F devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- The Peripheral Enable bit, generically named, “XXXEN”, located in the module’s main control SFR.
- The Peripheral Module Disable (PMD) bit, generically named, “XXXMD”, located in one of the PMDx Control registers.

Both bits have similar functions in enabling or disabling its associated module. Setting the PMDx bits for a module, disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect, and read values will be invalid. Many peripheral modules have a corresponding PMDx bit.

In contrast, disabling a module by clearing its XXXEN bit, disables its functionality, but leaves its registers available to be read and written to. Power consumption is reduced, but not by as much as when the PMDx bits are used. Most peripheral modules have an enable bit; exceptions include capture, compare and RTCC.

To achieve more selective power savings, peripheral modules can also be selectively disabled when the device enters Idle mode. This is done through the control bit of the generic name format, “XXXIDL”. By default, all modules that can operate during Idle mode will do so. Using the disable on Idle feature disables the module while in Idle mode, allowing further reduction of power consumption during Idle mode, enhancing power savings for extremely critical power applications.

NOTES:

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11.0 I/O PORTS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the I/O ports, refer to **"I/O Ports with Peripheral Pin Select (PPS)"** (www.microchip.com/DS30009711) in the *"dsPIC33/PIC24F Family Reference Manual"*. Note that the PIC24FV16KM204 family devices do not support Peripheral Pin Select features.

All of the device pins (except VDD and VSS) are shared between the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

A Parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

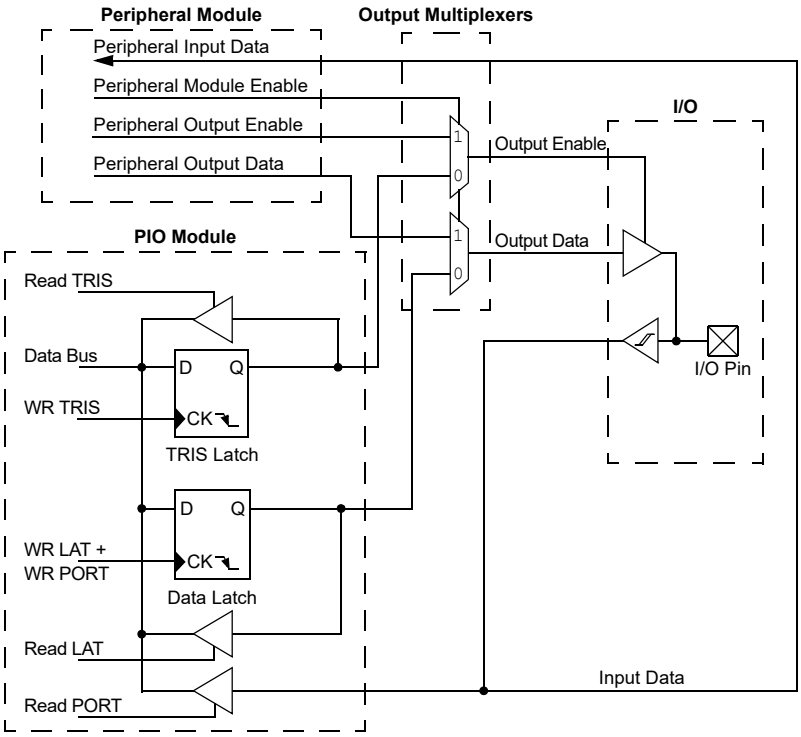
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the Data Direction register bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Data Latch register (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins; writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The maximum open-drain voltage allowed is the same as the maximum VIH specification.

11.2 Configuring Analog Port Pins

The use of the ANSx and TRISx registers controls the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRISx bit set (input). If the TRISx bit is cleared (output), the digital output level (VOH or VOL) will be converted.

When reading the PORTx register, all pins configured as analog input channels will read as cleared (a low level). Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

11.2.1 ANALOG SELECTION REGISTER

I/O pins with shared analog functionality, such as A/D inputs and comparator inputs, must have their digital inputs shut off when analog functionality is used. Note that analog functionality includes an analog voltage being applied to the pin externally.

To allow for analog control, the ANSx registers are provided. There is one ANSx register for each port (ANSA, ANSB and ANSC). Within each ANSx register, there is a bit for each pin that shares analog functionality with the digital I/O functionality.

If a particular pin does not have an analog function, that bit is unimplemented. See Register 11-1 to Register 11-3 for implementation.

REGISTER 11-1: ANSA: PORTA ANALOG SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	ANSA[4:0](1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **ANSA[4:0]:** Analog Select Control bits(1)
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

Note 1: The ANSA4 bit is not available on 20-pin devices.

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REGISTER 11-2: ANSB: PORTB ANALOG SELECTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	U-0	R/W-1	R/W-1
ANSB[15:12]				—	—	ANSB[9:8]	
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSB[7:0][(1)]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **ANSB[15:12]:** Analog Select Control bits
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9-0 **ANSB[9:0]:** Analog Select Control bits[(1)]
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

Note 1: The ANSB[6:5,3] bits are not available on 20-pin devices.

REGISTER 11-3: ANSC: PORTC ANALOG SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
—	—	—	—	—	ANSC[2:0][(1)]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ANSC[2:0]:** Analog Select Control bits[(1)]
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

Note 1: These bits are not implemented in 20-pin and 28-pin devices.

11.2.2 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation, and a read operation of the same port. Typically, this instruction would be a NOP.

11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows the PIC24FXXXXX family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States, even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 37 external signals (CN0 through CN36) that may be selected (enabled) for generating an interrupt request on a Change-of-State.

There are six control registers associated with the CN module. The CNEN1 and CNEN3 registers contain the interrupt enable control bits for each of the CNx input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CNx pin also has a weak pull-up/pull-down connected to it. The pull-ups act as a current source that is connected to the pin. The pull-downs act as a current sink to eliminate the need for external resistors when push button or keypad devices are connected.

On any pin, only the pull-up resistor or the pull-down resistor should be enabled, but not both of them. If the push button or the keypad is connected to V_{DD}, enable the pull-down, or if they are connected to V_{SS}, enable the pull-up resistors. The pull-ups are enabled separately using the CNPU1 and CNPU3 registers, which contain the control bits for each of the CNx pins.

Setting any of the control bits enables the weak pull-ups for the corresponding pins. The pull-downs are enabled separately using the CNPD1 and CNPD3 registers, which contain the control bits for each of the CNx pins. Setting any of the control bits enables the weak pull-downs for the corresponding pins.

When the internal pull-up is selected, the pin uses V_{DD} as the pull-up source voltage. When the internal pull-down is selected, the pins are pulled down to V_{SS} by an internal resistor. Make sure that there is no external pull-up source/pull-down sink when the internal pull-ups/pull-downs are enabled.

Note: Pull-ups and pull-downs on Change Notification (CN) pins should always be disabled whenever the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0;          //Configure PORTB[15:8] as inputs and PORTB[7:0] as outputs
MOV   W0, TRISB;
NOP;                       //Delay 1 cycle
BTSS  PORTB, #13;          //Next Instruction

Equivalent 'C' Code
TRISB = 0xFF00;            //Configure PORTB[15:8] as inputs and PORTB[7:0] as outputs
NOP();                     //Delay 1 cycle
if(PORTBbits.RB13 == 1)    // execute following code if PORTB pin 13 is set.
{
}
```


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12.0 TIMER1

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on timers, refer to **"Timers"** (www.microchip.com/DS39704) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The Timer1 module is a 16-bit timer which operates as a free-running, interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

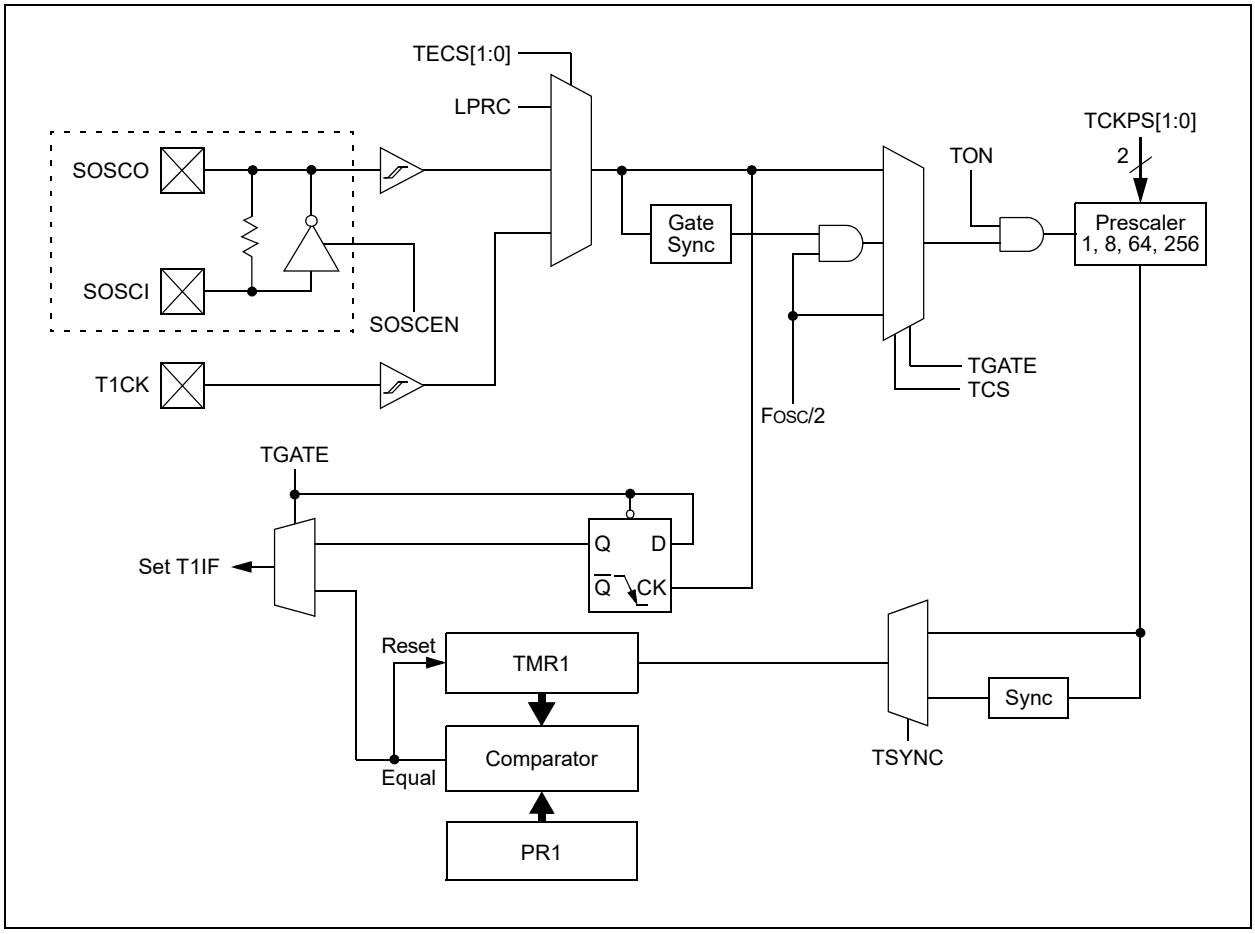
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation During CPU Idle and Sleep modes
- Interrupt on 16-Bit Period Register Match or Falling Edge of External Gate Signal

Figure 12-1 illustrates a block diagram of the 16-bit Timer1 module.

To configure Timer1 for operation:

1. Set the TON bit (= 1).
2. Select the timer prescaler ratio using the TCKPS[1:0] bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Set or clear the TSYNC bit to configure synchronous or asynchronous operation.
5. Load the timer period value into the PR1 register.
6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP[2:0], to set the interrupt priority.

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	—	TSIDL	—	—	—	TECS1[(1)]	TECS0[(1)]
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9-8 **TECS[1:0]:** Timer1 Extended Clock Select bits[(1)]
11 = Reserved; do not use
10 = Timer1 uses the LPRC as the clock source
01 = Timer1 uses the External Clock (EC) from T1CK
00 = Timer1 uses the Secondary Oscillator (SOSC) as the clock source

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS[1:0]:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronizes External Clock input
0 = Does not synchronize External Clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit
1 = Timer1 clock source is selected by TECS[1:0]
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as ‘0’

Note 1: The TECSx bits are valid only when TCS = 1.

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13.0 CAPTURE/COMPARE/PWM/ TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the MCCP/SCCP modules, refer to **"Capture/Compare/PWM/ Timer (MCCP and SCCP)"** (www.microchip.com/DS30003035) in the *"dsPIC33/PIC24F Family Reference Manual"*.

PIC24FV16KM204 family devices include several Capture/Compare/PWM/Timer base modules, which provide the functionality of three different peripherals of earlier PIC24F devices. The module can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

The module is provided in two different forms, distinguished by the number of PWM outputs that the module can generate. Single output modules (SCCPs) provide only one PWM output. Multiple output modules (MCCPs) can provide up to six outputs and an extended range of power control features, depending on the pin count of the particular device. All other features of the modules are identical.

The SCCP and MCCP modules can be operated only in one of the three major modes at any time. The other modes are not available unless the module is reconfigured for the new mode.

A conceptual block diagram for the module is shown in Figure 13-1. All three modes share a time base generator and a common Timer register pair (CCPxTMRH/L); other shared hardware components are added as a particular mode requires.

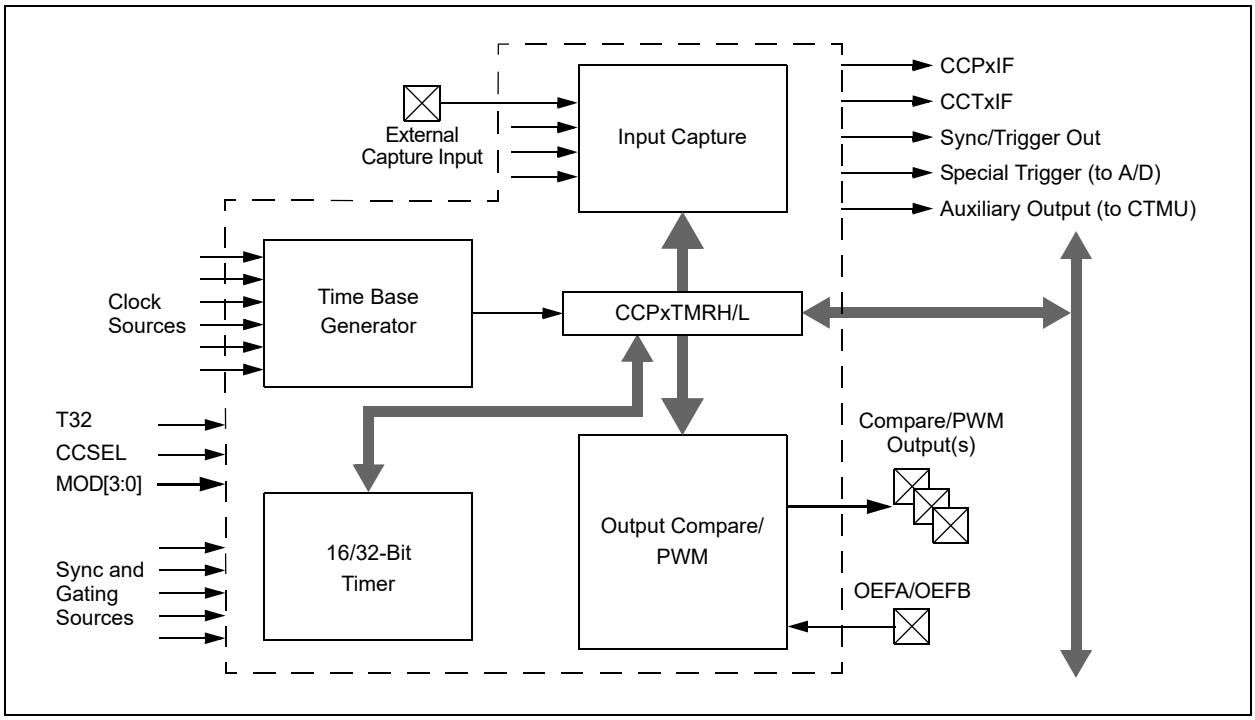
Each module has a total of seven control and status registers:

- CCPxCON1L (Register 13-1)
- CCPxCON1H (Register 13-2)
- CCPxCON2L (Register 13-3)
- CCPxCON2H (Register 13-4)
- CCPxCON3L (Register 13-5)
- CCPxCON3H (Register 13-6)
- CCPxSTATL (Register 13-7)

Each module also includes eight buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMRH/CCPxTMRL (Timer High/Low Counters)
- CCPxPRH/CCPxPRL (Timer Period High/Low)
- CCPxRA (Primary Output Compare Data Buffer)
- CCPxRB (Secondary Output Compare Data Buffer)
- CCPxBUFH/CCPxBUFL (Input Capture High/Low Buffers)

FIGURE 13-1: MCCPx/SCCPx CONCEPTUAL BLOCK DIAGRAM



13.1 Time Base Generator

The Timer Clock Generator (TCG) generates a clock for the module's internal time base, using one of the clock signals already available on the microcontroller. This is used as the time reference for the module in its three major modes. The internal time base is shown in Figure 13-2.

There are eight inputs available to the clock generator, which are selected using the CLKSEL[2:0] bits (CCPxCON1L[10:8]). Available sources include the FRC and LPRC, the Secondary Oscillator, and the TCLKI External Clock inputs. The system clock is the default source (CLKSEL[2:0] = 000). On PIC24FV16KM204 family devices, clock sources to the MCCPx module must be synchronized with the system clock; as a result, when clock sources are selected, clock input timing restrictions or module operating restrictions may exist. Table 13-1 describes which time base sources are valid for the various operating modes.

TABLE 13-1: VALID TIMER OPTIONS FOR MCCPx/SCCPx MODES

CLKSEL [2:0](1)	Timer		Input Capture	Output Compare
	Sync(2)	Async(3)		
111	X	—	—	—
110	X	—	—	—
101	X	—	—	—
011	X	—	—	—
010	X	—	—	—
001	X	—	—	—
000(4)	—	X	X	X

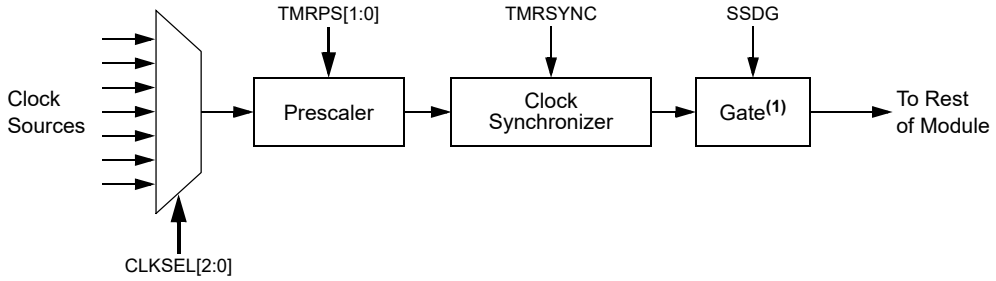
Note 1: See Register 13-1 for the description of the time base sources.

2: Synchronous Operation: TMRSYNC (CCPxCON1L[11]) = 1 and TRIGEN (CCPxCON1H[7]) = 0.

3: Asynchronous Operation: (TMRSYNC = 0) or Triggered mode (TRIGEN = 1).

4: When CLKSEL[2:0] = 000, the TMRSYNC bit must be cleared.

FIGURE 13-2: TIMER CLOCK GENERATOR



Note 1: Gating available in Timer modes only.

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13.2 General Purpose Timer

Timer mode is selected when CCSEL = 0 and MOD[3:0] = 0000. The timer can function as a 32-bit timer or a dual 16-bit timer, depending on the setting of the T32 bit (Table 13-2).

TABLE 13-2: TIMER OPERATION MODE

T32 (CCPxCON1L[5])	Operating Mode
0	Dual Timer Mode (16-bit)
1	Timer Mode (32-bit)

Dual 16-Bit Timer mode provides a simple timer function with two independent 16-bit timer/counters. The primary timer uses CCPxTMRL and CCPxPRL. Only the primary timer can interact with other modules on the device. It generates the MCCPx Sync out signals for use by other MCCP modules. It can also use the SYNC[4:0] bits signal generated by other modules.

The secondary timer uses CCPxTMRH and CCPxPRH. It is intended to be used only as a periodic interrupt source for scheduling CPU events. It does not generate an Output Sync/Trigger signal like the primary time base.

The 32-Bit Timer mode uses the CCPxTMRL and CCPxTMRH registers, together, as a single 32-bit timer. When CCPxTMRL overflows, CCPxTMRH increments by one. This mode provides a simple timer function when it is important to track long time periods. Note that the T32 bit (CCPxCON1L[5]) should be set before the CCPxTMRL or CCPxPRH registers are written to initialize the 32-bit timer.

13.2.1 SYNC AND TRIGGER OPERATION

In both 16-bit and 32-bit modes, the timer can also function in either Synchronization (“Sync”) or Trigger operation. Both use the SYNC[4:0] bits (CCPxCON1H[4:0]) to determine the input signal source. The difference is how that signal affects the timer.

In Sync operation, the timer Reset or clear occurs when the input selected by SYNC[4:0] is asserted. The timer immediately begins to count again from zero unless it is held for some other reason. Sync operation is used whenever the TRIGEN bit (CCPxCON1H[7]) is cleared. SYNC[4:0] can have any value except ‘11111’.

In Trigger operation, the timer is held in Reset until the input selected by SYNC[4:0] is asserted; when it occurs, the timer starts counting. Trigger operation is used whenever the TRIGEN bit is set. In Trigger mode, the timer will continue running after a Trigger event as long as the CCPTRIG bit (CCPxSTATL[7]) is set. To clear CCPTRIG, the TRCLR bit (CCPxSTATL[5]) must be set to clear the Trigger event, reset the timer and hold it at zero until another Trigger event occurs. On PIC24FV16KM204 family devices, Trigger operation can only be used when the system clock is the time base source (CLKSEL[2:0] = 000).

FIGURE 13-3: DUAL 16-BIT TIMER MODE

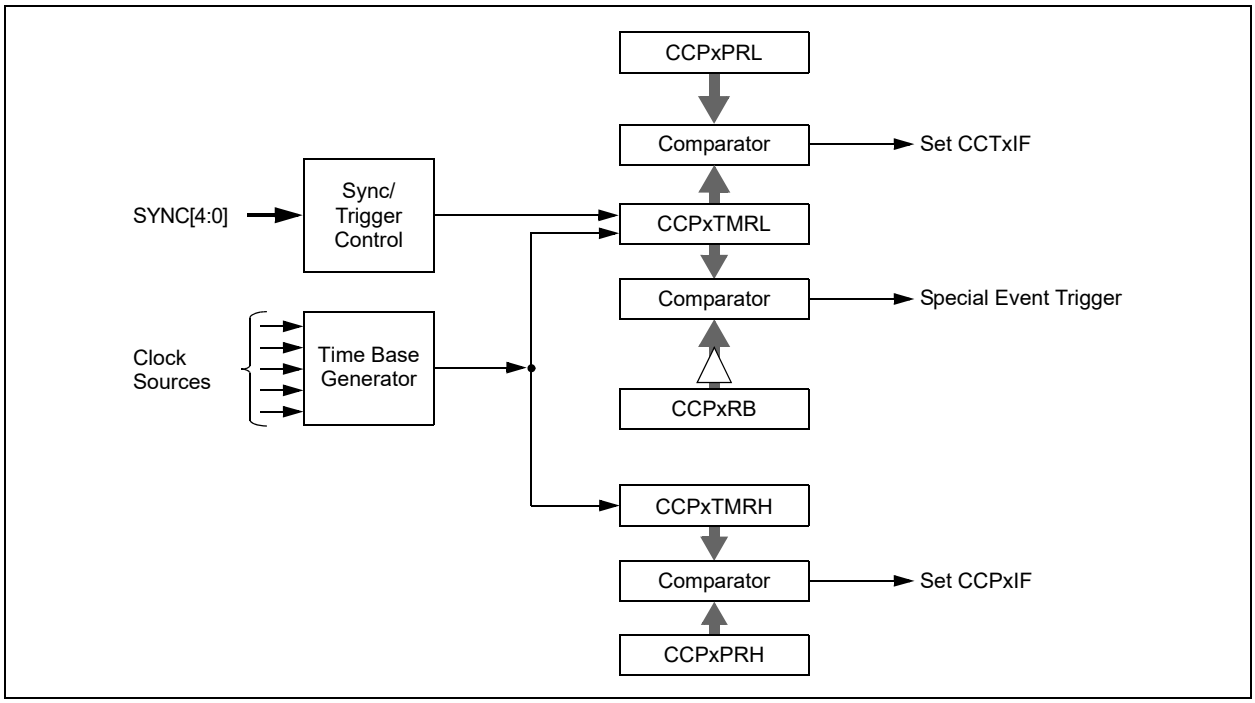
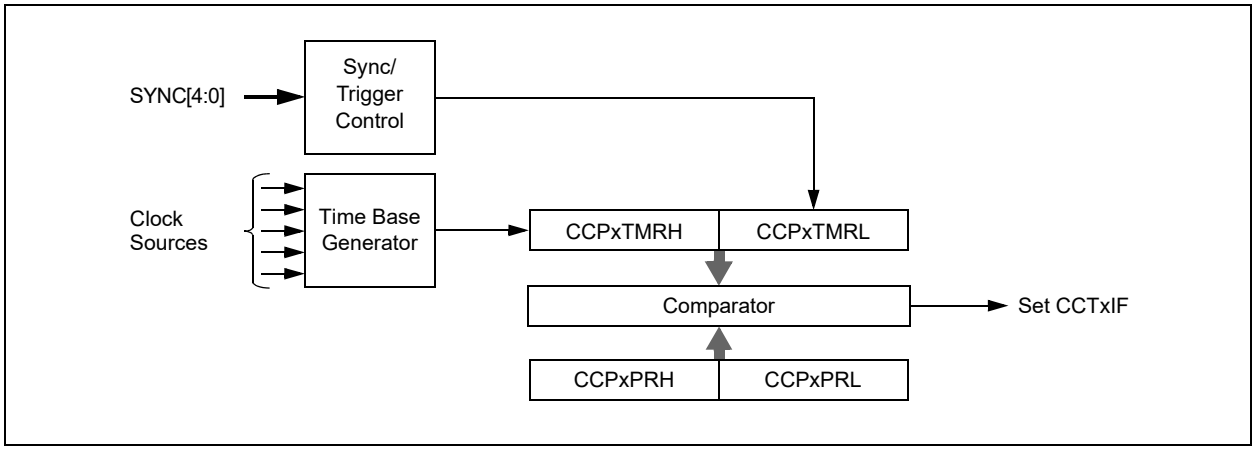


FIGURE 13-4: 32-BIT TIMER MODE



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13.3 Output Compare Mode

Output Compare mode compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The Output Compare x module on compare match events has the ability to generate a single output transition or a train of output pulses. Like most PIC® MCU peripherals, the Output Compare x module can also generate interrupts on a compare match event.

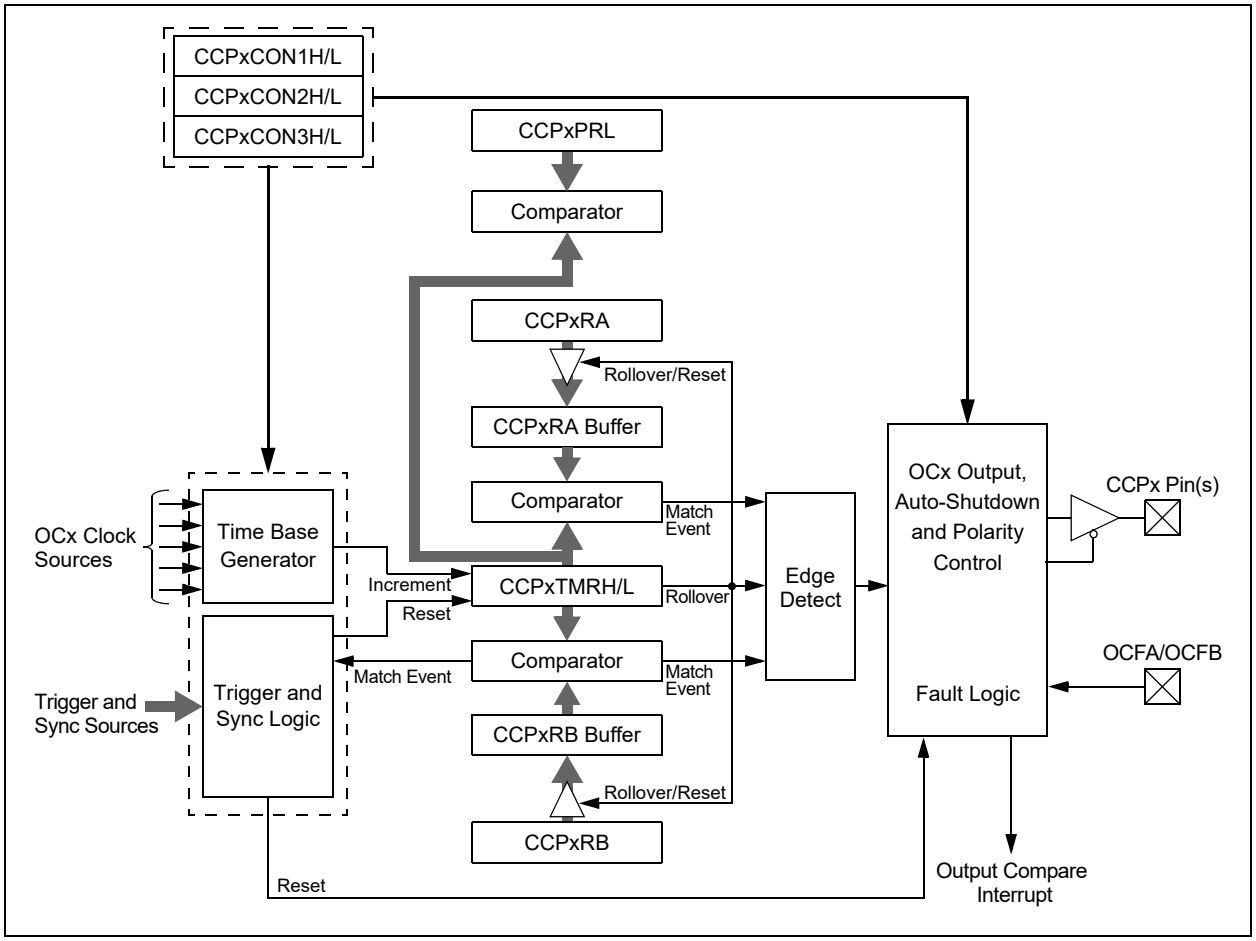
Table 13-3 shows the various modes available in Output Compare modes.

TABLE 13-3: OUTPUT COMPARE/PWM MODES

MOD[3:0] (CCPxCON1L[3:0])	T32 (CCPxCON1L[5])	Operating Mode	
0001	0	Output High on Compare (16-bit)	Single Edge Mode
0001	1	Output High on Compare (32-bit)	
0010	0	Output Low on Compare (16-bit)	
0010	1	Output Low on Compare (32-bit)	
0011	0	Output Toggle on Compare (16-bit)	
0011	1	Output Toggle on Compare (32-bit)	
0100	0	Dual Edge Compare (16-bit)	Dual Edge Mode
0101	0	Dual Edge Compare (16-bit buffered)	PWM Mode
0110	0	Center-Aligned Pulse (16-bit buffered)	Center PWM(1)
0111	0	Variable Frequency Pulse (16-bit)	
0111	1	Variable Frequency Pulse (32-bit)	

Note 1: Center-Aligned PWM mode is disabled on SCCP. Please use MCCP instead.

FIGURE 13-5: OUTPUT COMPARE x BLOCK DIAGRAM



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13.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal Trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 13-6 depicts a simplified block diagram of Input Capture mode.

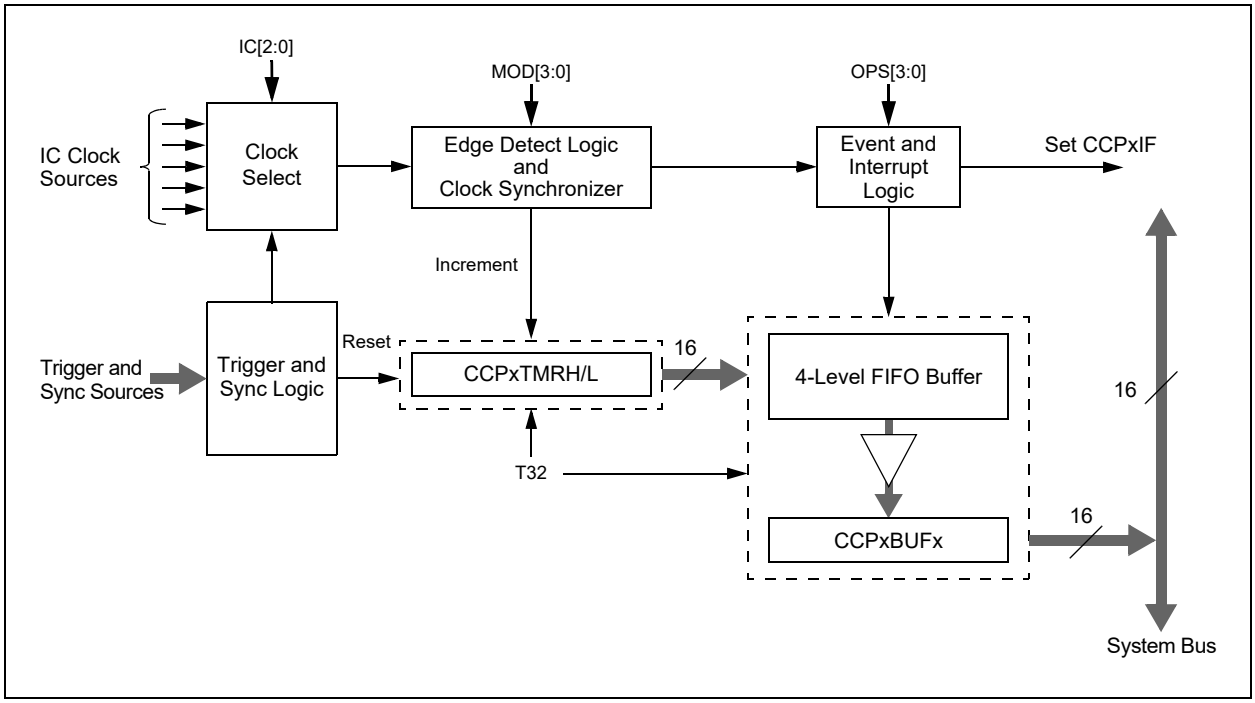
Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L register.

To use Input Capture mode, the CCSEL bit (CCPxCON1L[4]) must be set. The T32 and the MOD[3:0] bits are used to select the proper Capture mode, as shown in Table 13-4.

TABLE 13-4: INPUT CAPTURE MODES

MOD[3:0] (CCPxCON1L[3:0])	T32 (CCPxCON1L[5])	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)
0011	0	Every Rise/Fall (16-bit capture)
0011	1	Every Rise/Fall (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

FIGURE 13-6: INPUT CAPTURE x BLOCK DIAGRAM



13.5 Auxiliary Output

The MCCPx and SCCPx modules have an auxiliary (secondary) output that provides other peripherals access to internal module signals. The auxiliary output is intended to connect to other MCCP or SCCP modules, or other digital peripherals, to provide these types of functions:

- Time Base Synchronization
- Peripheral Trigger and Clock Inputs
- Signal Gating

The type of output signal is selected using the AUXOUT[1:0] control bits (CCPxCON2H[4:3]). The type of output signal is also dependent on the module operating mode.

On the PIC24FV16KM204 family of devices, only the CTMU discharge trigger has access to the auxiliary output signal.

TABLE 13-5: AUXILIARY OUTPUT

AUXOUT[1:0]	CCSEL	MOD[3:0]	Comments	Signal Description
00	x	xxxx	Auxiliary output disabled	No Output
01	0	0000	Time Base modes	Time Base Period Reset or Rollover
10				Special Event Trigger Output
11				No Output
01	0	0001 through 1111	Output Compare modes	Time Base Period Reset or Rollover
10				Output Compare Event Signal
11				Output Compare Signal
01	1	xxxx	Input Capture modes	Time Base Period Reset or Rollover
10				Reflects the Value of the ICDIS bit
11				Input Capture Event Signal

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REGISTER 13-1: CCPxCON1L: CCPx CONTROL 1 LOW REGISTERS

R/W-0	U-0	R/W-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
CCPON	—	CCPSIDL	—	TMRSYNC	CLKSEL2(1)	CLKSEL1(1)	CLKSEL0(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CCPON:** CCPx Module Enable bit
1 = Module is enabled with an operating mode specified by the MOD[3:0] control bits
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CCPSIDL:** CCPx Stop in Idle Mode Bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **Reserved:** Maintain as ‘0’

bit 11 **TMRSYNC:** Time Base Clock Synchronization bit
1 = Asynchronous module time base clock is selected and synchronized to the internal system clocks (CLKSEL[2:0] ≠ 000)
0 = Synchronous module time base clock is selected and does not require synchronization (CLKSEL[2:0] = 000)

bit 10-8 **CLKSEL[2:0]:** CCPx Time Base Clock Select bits(1)
111 = External TCKIA input
110 = External TCKIB input
101 = CLC1
100 = Reserved
011 = LPRC (31 kHz source)
010 = Secondary Oscillator
001 = Reserved
000 = Peripheral clock (TCY)

bit 7-6 **TMRPS[1:0]:** Time Base Prescale Select bits
11 = 1:64 Prescaler
10 = 1:16 Prescaler
01 = 1:4 Prescaler
00 = 1:1 Prescaler

bit 5 **T32:** 32-Bit Time Base Select bit
1 = Uses 32-bit time base for timer, single edge output compare or input capture function
0 = Uses 16-bit time base for timer, single edge output compare or input capture function

bit 4 **CCSEL:** Capture/Compare Mode Select bit
1 = Input Capture peripheral
0 = Output Compare/PWM/Timer peripheral (exact function is selected by the MOD[3:0] bits)

Note 1: Clock options are limited in some operating modes. See Table 13-1 for restrictions.

REGISTER 13-1: CCPxCON1L: CCPx CONTROL 1 LOW REGISTERS (CONTINUED)

bit 3-0 **MOD[3:0]:** CCPx Mode Select bits

For CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)

For CCSEL = 0 (Output Compare/Timer modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS[2:0]
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode
0110 = Center-Aligned Pulse Compare mode, buffered
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode, output functions are disabled

Note 1: Clock options are limited in some operating modes. See Table 13-1 for restrictions.

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REGISTER 13-2: CCPxCON1H: CCPx CONTROL 1 HIGH REGISTERS

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
OPSSRC(1)	RTRGEN(2)	—	—	OPS3(3)	OPS2(3)	OPS1(3)	OPS0(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGEN(4)	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **OPSSRC:** Output Postscaler Source Select bit(1)
- 1 = Output postscaler scales module Trigger output events
- 0 = Output postscaler scales time base interrupt events

bit 14 **RTRGEN:** Retrigger Enable bit(2)
- 1 = Time base can be retriggered when TRIGEN bit = 1
- 0 = Time base may not be retriggered when TRIGEN bit = 1

bit 13-12 **Unimplemented:** Read as ‘0’

bit 11-8 **OPS3[3:0]:** CCPx Interrupt Output Postscale Select bits(3)
- 1111 = Interrupt every 16th time base period match
- 1110 = Interrupt every 15th time base period match
- . . .
- 0100 = Interrupt every 5th time base period match
- 0011 = Interrupt every 4th time base period match or 4th input capture event
- 0010 = Interrupt every 3rd time base period match or 3rd input capture event
- 0001 = Interrupt every 2nd time base period match or 2nd input capture event
- 0000 = Interrupt after each time base period match or input capture event

bit 7 **TRIGEN:** CCPx Trigger Enable bit(4)
- 1 = Trigger operation of time base is enabled
- 0 = Trigger operation of time base is disabled

bit 6 **ONESHOT:** One-Shot Mode Enable bit
- 1 = One-Shot Trigger mode is enabled; Trigger duration is set by OSCNT[2:0]
- 0 = One-Shot Trigger mode is disabled

bit 5 **ALTSYNC:** CCPx Clock Select bits
- 1 = An alternate signal is used as the module synchronization output signal
- 0 = The module synchronization output signal is the Time Base Reset/rollover event

bit 4-0 **SYNC[4:0]:** CCPx Synchronization Source Select bits
See Table 13-6 for the definition of inputs.

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Output postscale settings from 1:5 to 1:16 (0100-1111) will result in a FIFO buffer overflow for Input Capture modes.
4: Clock source options are limited when Trigger operation is enabled; refer to Table 13-1.

TABLE 13-6: SYNCHRONIZATION SOURCES

SYNC[4:0]	Synchronization Source
00000	None; Timer with Rollover on CCPxPR Match or FFFFh
00001	MCCP1 or SCCP1 Sync Output
00010	MCCP2 or SCCP2 Sync Output
00011	MCCP3 or SCCP3 Sync Output
00100	MCCP4 or SCCP4 Sync Output
00101	MCCP5 or SCCP5 Sync Output
00110 to 01010	Unused
01011	Timer1 Sync Output(1)
01100 to 01111	Unused
10000	CLC1 Output(1)
10001	CLC2 Output(1)
10010 to 11010	Unused
11011	A/D(1)
11110	Unused
11111	None; Timer with Auto-Rollover (FFFFh → 0000h)

Note 1: These sources are only available when the source module is being used in a Synchronous mode.

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REGISTER 13-3: CCPxCON2L: CCPx CONTROL 2 LOW REGISTERS

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
PWMRSEN	ASDGM	—	SSDG	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASDG[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
- 1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
- 0 = ASEVT bit must be cleared in software to resume PWM activity on output pins

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
- 1 = Waits until the next Time Base Reset or rollover for shutdown to occur
- 0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as ‘0’

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
- 1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
- 0 = Normal module operation

bit 11-8 **Unimplemented:** Read as ‘0’

bit 7-0 **ASDG[7:0]:** CCPx Auto-Shutdown/Gating Source Enable bits
- 1 = ASDGx Source n is enabled (see Table 13-7 for auto-shutdown/gating sources)
- 0 = ASDGx Source n is disabled

TABLE 13-7: AUTO-SHUTDOWN AND GATING SOURCES

ASDG[7:0] Bits	Auto-Shutdown/Gating Source
0	Comparator 1 Output
1	Comparator 2 Output
2	Comparator 3 Output
3	SCCP4 Output Compare
4	SCCP5 Output Compare
5	CLC1 Output
6	OCFA Fault Input
7	OCFB Fault Input

REGISTER 13-4: CCPxCON2H: CCPx CONTROL 2 HIGH REGISTERS

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **OENSYNC:** Output Enable Synchronization bit
- 1 = Update by output enable bits occurs on the next Time Base Reset or rollover
- 0 = Update by output enable bits occurs immediately

bit 14 **Unimplemented:** Read as ‘0’

bit 13-8 **OC[F:A]EN:** Output Enable/Steering Control bits(1)
- 1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
- 0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 7-6 **ICGSM[1:0]:** Input Capture Gating Source Mode Control bits
- 11 = Reserved
- 10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
- 01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
- 00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 5 **Unimplemented:** Read as ‘0’

bit 4-3 **AUXOUT[1:0]:** Auxiliary Output Signal on Event Selection bits
- 11 = Input capture or output compare event; no signal in Timer mode
- 10 = Signal output is defined by module operating mode (see Table 13-5)
- 01 = Time base rollover event (all modes)
- 00 = Disabled

bit 2-0 **ICS[2:0]:** Input Capture Source Select bits
- 111 = Unused
- 110 = CLC2 output
- 101 = CLC1 output
- 100 = Unused
- 011 = Comparator 3 output
- 010 = Comparator 2 output
- 001 = Comparator 1 output
- 000 = Input Capture x (ICx) I/O pin

Note 1: OCFEN through OCBEN (bits[13:9]) are implemented in MCCPx modules only.

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REGISTER 13-5: CCPxCON3L: CCPx CONTROL 3 LOW REGISTERS (1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DT[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DT[5:0]:** CCPx Dead-Time Select bits
111111 = Inserts 63 dead-time delay periods between complementary output signals
111110 = Inserts 62 dead-time delay periods between complementary output signals
. . .
000010 = Inserts 2 dead-time delay periods between complementary output signals
000001 = Inserts 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: This register is implemented in MCCPx modules only.

REGISTER 13-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2(1)	OUTM1(1)	OUTM0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	POLBDF(1)	PSSACE1	PSSACE0	PSSBDF1(1)	PSSBDF0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** CCPx Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT[2:0]:** One-Shot Event Count bits
111 = Extends one-shot event by 7 time base periods (8 time base periods total)
110 = Extends one-shot event by 6 time base periods (7 time base periods total)
101 = Extends one-shot event by 5 time base periods (6 time base periods total)
100 = Extends one-shot event by 4 time base periods (5 time base periods total)
011 = Extends one-shot event by 3 time base periods (4 time base periods total)
010 = Extends one-shot event by 2 time base periods (3 time base periods total)
001 = Extends one-shot event by 1 time base period (2 time base periods total)
000 = Does not extend one-shot Trigger event

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **OUTM[2:0]:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 4 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit(1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 3-2 **PSSACE[1:0]:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are tri-stated when a shutdown event occurs

bit 1-0 **PSSBDF[1:0]:** PWMx Output Pins, OCxB, OCxD, and OCxF, Shutdown State Control bits(1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a High-Impedance state when a shutdown event occurs

Note 1: These bits are implemented in MCCPx modules only.

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REGISTER 13-7: CCPxSTATL: CCPx STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	W1-0	W1-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W1 = Write ‘1’ only	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **CCPTRIG:** CCPx Trigger Status bit
1 = Timer has been triggered and is running
0 = Timer has not been triggered and is held in Reset

bit 6 **TRSET:** CCPx Trigger Set Request bit
Write ‘1’ to this location to trigger the timer when TRIGEN = 1 (location always reads as ‘0’).

bit 5 **TRCLR:** CCPx Trigger Clear Request bit
Write ‘1’ to this location to cancel the timer Trigger when TRIGEN = 1 (location always reads as ‘0’).

bit 4 **ASEVT:** CCPx Auto-Shutdown Event Status/Control bit
1 = A shutdown event is in progress; CCPx outputs are in the Shutdown state
0 = CCPx outputs operate normally

bit 3 **SCEVT:** Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred

bit 2 **ICDIS:** Input Capture x Disable bit
1 = Event on Input Capture x pin (ICx) does not generate a capture event
0 = Event on Input Capture x pin will generate a capture event

bit 1 **ICOV:** Input Capture x Buffer Overflow Status bit
1 = The Input Capture x FIFO buffer has overflowed
0 = The Input Capture x FIFO buffer has not overflowed

bit 0 **ICBNE:** Input Capture x Buffer Status bit
1 = Input Capture x buffer has data available
0 = Input Capture x buffer is empty

NOTES:

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14.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on MSSP, refer to **"Master Synchronous Serial Port (MSSP)"** (www.microchip.com/DS30627) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The Master Synchronous Serial Port (MSSP) module is an 8-bit serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, Shift registers, display drivers, A/D Converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)
  - Full Master mode
  - Slave mode (with general address call)

The SPI interface supports these modes in hardware:

- Master mode
- Slave mode
- Daisy-Chaining Operation in Slave mode
- Synchronized Slave Operation

The I^2C interface supports the following modes in hardware:

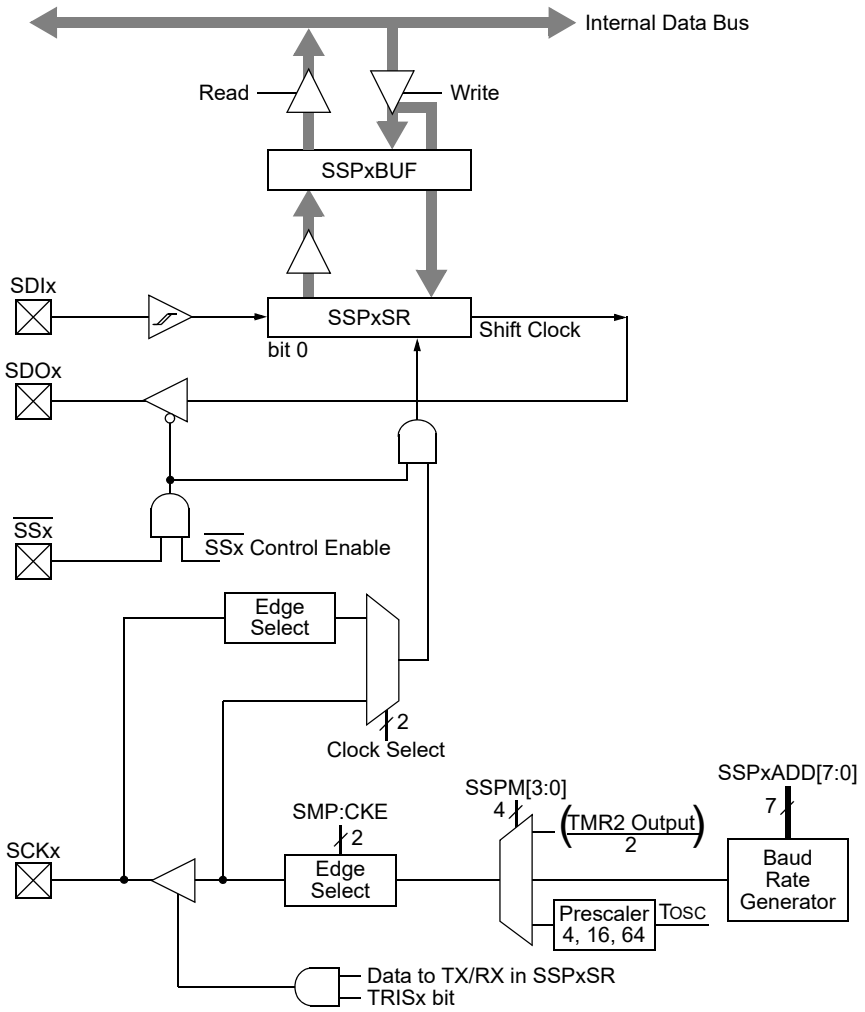
- Master mode
- Multi-Master mode
- Slave mode with 10-Bit and 7-Bit Addressing and Address Masking
- Byte NACKing
- Selectable Address and Data Hold, and Interrupt Masking

14.1 I/O Pin Configuration for SPI

In SPI Master mode, the MSSP module will assert control over any pins associated with the SDOx and SCKx outputs. This does not automatically disable other digital functions associated with the pin and may result in the module driving the digital I/O port inputs. To prevent this, the MSSP module outputs must be disconnected from their output pins while the module is in SPI Master mode. While disabling the module temporarily may be an option, it may not be a practical solution in all applications.

The SDOx and SCKx outputs for the module can be selectively disabled by using the SDOxDIS and SCKxDIS bits in the PADCFG1 register (Register 14-10). Setting the bit disconnects the corresponding output for a particular module from its assigned pin.

FIGURE 14-1: MSSPx BLOCK DIAGRAM (SPI MODE)



Note: Refer to the device data sheet for pin multiplexing.

FIGURE 14-2: SPI MASTER/SLAVE CONNECTION

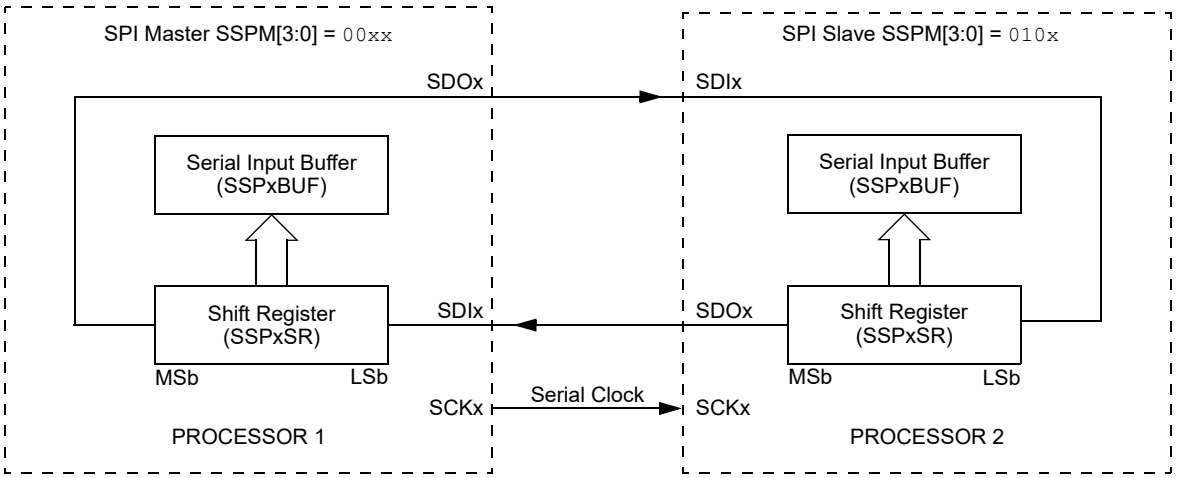


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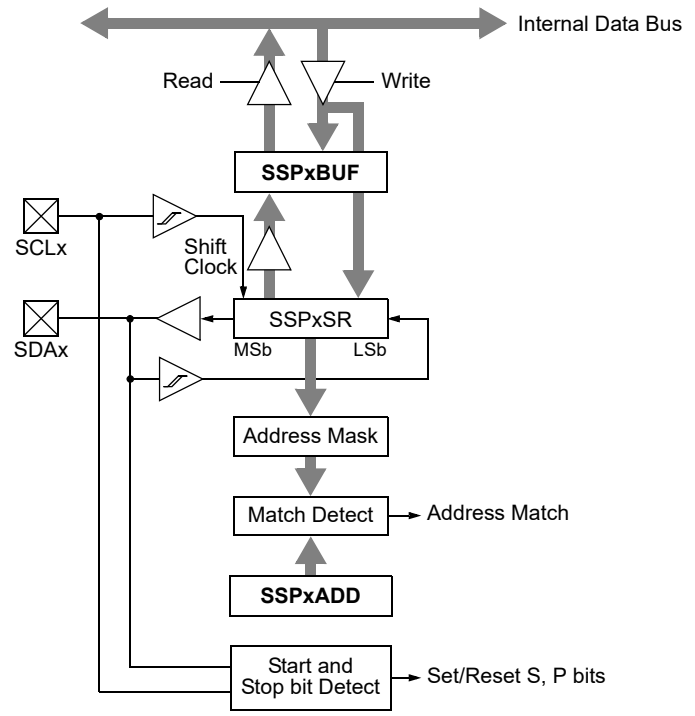
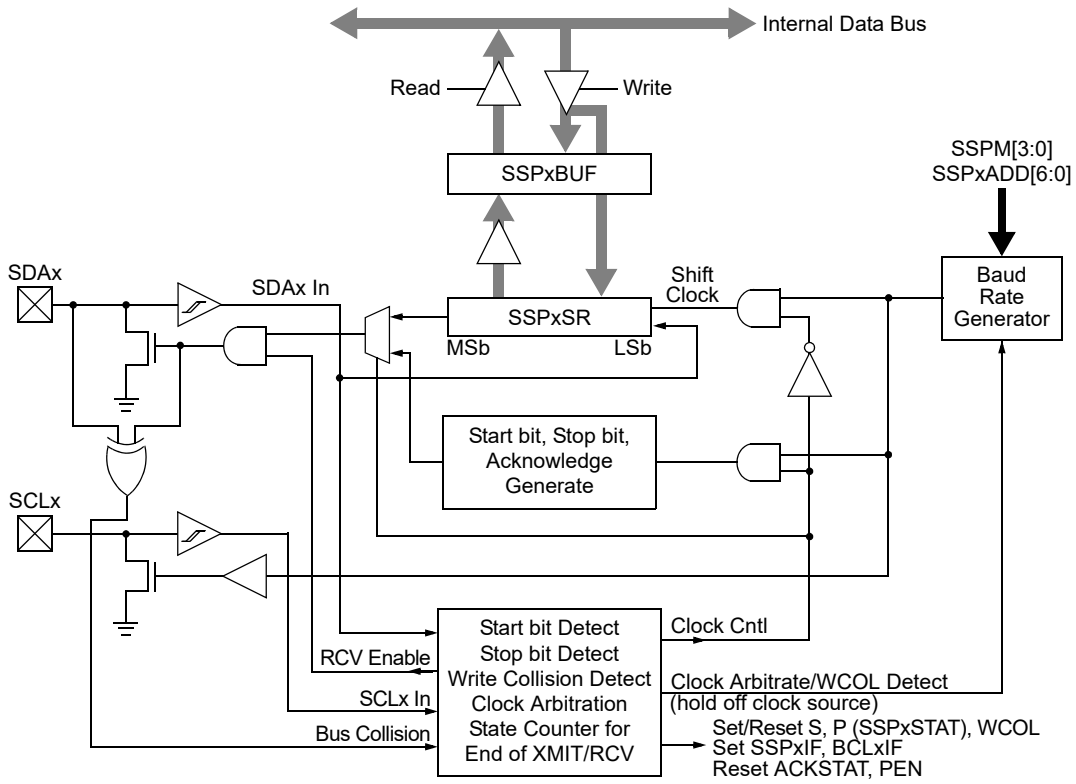
FIGURE 14-3: MSSPx BLOCK DIAGRAM (I^2C MODE)



Note: Only port I/O names are shown in this diagram. Refer to the text for a full list of multiplexed functions.

FIGURE 14-4: MSSPx BLOCK DIAGRAM (I^2C MASTER MODE)



REGISTER 14-1: SSPxSTAT: MSSPx STATUS REGISTER (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE(1)	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **SMP:** Sample bit
SPI Master mode:
1 = Input data are sampled at the end of data output time
0 = Input data are sampled at the middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE:** SPI Clock Select bit(1)
1 = Transmit occurs on transition from active to Idle Clock state
0 = Transmit occurs on transition from Idle to Active Clock state

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit
Used in I^2C mode only.

bit 4 **P:** Stop bit
Used in I^2C mode only. This bit is cleared when the MSSPx module is disabled; SSPEN bit is cleared.

bit 3 **S:** Start bit
Used in I^2C mode only.

bit 2 **R/$\overline{W}$:** Read/$\overline{\text{Write}}$ Information bit
Used in I^2C mode only.

bit 1 **UA:** Update Address bit
Used in I^2C mode only.

bit 0 **BF:** Buffer Full Status bit
1 = Receive is complete, SSPxBUF is full
0 = Receive is not complete, SSPxBUF is empty

Note 1: Polarity of clock state is set by the CKP bit (SSPxCON1[4]).

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REGISTER 14-2: SSPxSTAT: MSSPx STATUS REGISTER (I^2C MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P(1)	S(1)	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **SMP:** Slew Rate Control bit
In Master or Slave mode:
1 = Slew rate control is disabled for Standard Speed mode (100 kHz and 1 MHz)
0 = Slew rate control is enabled for High-Speed mode (400 kHz)

bit 6 **CKE:** SMBus Select bit
In Master or Slave mode:
1 = Enables SMBus-specific inputs
0 = Disables SMBus-specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit
In Master mode:
Reserved.
In Slave mode:
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit(1)
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

bit 3 **S:** Start bit(1)
1 = Indicates that a Start bit has been detected last
0 = Start bit was not detected last

bit 2 **R/$\overline{W}$:** Read/$\overline{\text{Write}}$ Information bit
In Slave mode:(2)
1 = Read
0 = Write
In Master mode:(3)
1 = Transmit is in progress
0 = Transmit is not in progress

bit 1 **UA:** Update Address bit (10-Bit Slave mode only)
1 = Indicates that the user needs to update the address in the SSPxADD register
0 = Address does not need to be updated

Note 1: This bit is cleared on Reset and when SSPEN is cleared.
2: This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{\text{ACK}}$ bit.
3: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSPx is in Active mode.

REGISTER 14-2: SSPxSTAT: MSSPx STATUS REGISTER (I^2C MODE) (CONTINUED)

bit 0 **BF:** Buffer Full Status bit

In Transmit mode:
1 = Transmit is in progress, SSPxBUF is full
0 = Transmit is complete, SSPxBUF is empty

In Receive mode:
1 = SSPxBUF is full (does not include the $\overline{ACK}$ and Stop bits)
0 = SSPxBUF is empty (does not include the $\overline{ACK}$ and Stop bits)

Note 1: This bit is cleared on Reset and when SSPEN is cleared.

2: This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{ACK}$ bit.

3: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSPx is in Active mode.

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REGISTER 14-3: SSPxCON1: MSSPx CONTROL REGISTER 1 (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV(1)	SSPEN(2)	CKP	SSPM3(3)	SSPM2(3)	SSPM1(3)	SSPM0(3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **WCOL:** Write Collision Detect bit
1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6 **SSPOV:** Master Synchronous Serial Port Receive Overflow Indicator bit(1)
SPI Slave mode:
1 = A new byte is received while the SSPxBUF register is still holding the previous data. In case of overflow, the data in SSPxSR are lost. Overflow can only occur in Slave mode. The user must read the SSPxBUF, even if only transmitting data, to avoid setting overflow (must be cleared in software).
0 = No overflow

bit 5 **SSPEN:** Master Synchronous Serial Port Enable bit(2)
1 = Enables the serial port and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables the serial port and configures these pins as I/O port pins

bit 4 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level

bit 3-0 **SSPM[3:0]:** Master Synchronous Serial Port Mode Select bits(3)
1010 = SPI Master mode, Clock = FOSC/(2 * ([SSPxADD] + 1))
0101 = SPI Slave mode, Clock = SCKx pin; $\overline{SSx}$ pin control is disabled, $\overline{SSx}$ can be used as an I/O pin
0100 = SPI Slave mode, Clock = SCKx pin; $\overline{SSx}$ pin control is enabled
0011 = Reserved
0010 = SPI Master mode, Clock = FOSC/32
0001 = SPI Master mode, Clock = FOSC/8
0000 = SPI Master mode, Clock = FOSC/2

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.
2: When enabled, these pins must be properly configured as inputs or outputs.
3: Bit combinations not specifically listed here are either reserved or implemented in I^2C mode only.

REGISTER 14-4: SSPxCON1: MSSPx CONTROL REGISTER 1 (I^2C MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN(1)	CKP	SSPM3(2)	SSPM2(2)	SSPM1(2)	SSPM0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **WCOL:** Write Collision Detect bit

In Master Transmit mode:
1 = A write to the SSPxBUF register was attempted while the I^2C conditions were not valid for a transmission to be started (must be cleared in software)
0 = No collision

In Slave Transmit mode:
1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

In Receive mode (Master or Slave modes):
This is a “don’t care” bit.

bit 6 **SSPOV:** Master Synchronous Serial Port Receive Overflow Indicator bit

In Receive mode:
1 = A byte is received while the SSPxBUF register is still holding the previous byte (must be cleared in software)
0 = No overflow

In Transmit mode:
This is a “don’t care” bit in Transmit mode.

bit 5 **SSPEN:** Master Synchronous Serial Port Enable bit(1)

1 = Enables the serial port and configures the SDAx and SCLx pins as the serial port pins
0 = Disables the serial port and configures these pins as I/O port pins

bit 4 **CKP:** SCLx Release Control bit

In Slave mode:
1 = Releases clock
0 = Holds clock low (clock stretch), used to ensure data setup time

In Master mode:
Unused in this mode.

bit 3-0 **SSPM[3:0]:** Master Synchronous Serial Port Mode Select bits(2)

1111 = I^2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I^2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1011 = I^2C Firmware Controlled Master mode (Slave Idle)
1000 = I^2C Master mode, Clock = FOSC/(2 * ([SSPxADD] + 1))(3)
0111 = I^2C Slave mode, 10-bit address
0110 = I^2C Slave mode, 7-bit address

Note 1: When enabled, the SDAx and SCLx pins must be configured as inputs.
2: Bit combinations not specifically listed here are either reserved or implemented in SPI mode only.
3: SSPxADD values of 0, 1 or 2 are not supported when the Baud Rate Generator is used with I^2C mode.

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REGISTER 14-5: SSPxCON2: MSSPx CONTROL REGISTER 2 (I^2C MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ACKDT(1)	ACKEN(2)	RCEN(2)	PEN(2)	RSEN(2)	SEN(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **GCEN:** General Call Enable bit (Slave mode only)
1 = Enables interrupt when a general call address (0000h) is received in the SSPxSR
0 = General call address is disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (Master Transmit mode only)
1 = Acknowledge was not received from Slave
0 = Acknowledge was received from Slave

bit 5 **ACKDT:** Acknowledge Data bit (Master Receive mode only)(1)
1 = No Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (Master mode only)(2)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; automatically cleared by hardware
0 = Acknowledge sequence is Idle

bit 3 **RCEN:** Receive Enable bit (Master Receive mode only)(2)
1 = Enables Receive mode for I^2C
0 = Receive is Idle

bit 2 **PEN:** Stop Condition Enable bit (Master mode only)(2)
1 = Initiates Stop condition on SDAx and SCLx pins; automatically cleared by hardware
0 = Stop condition is Idle

bit 1 **RSEN:** Repeated Start Condition Enable bit (Master mode only)(2)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; automatically cleared by hardware
0 = Repeated Start condition is Idle

bit 0 **SEN:** Start Condition Enable bit(2)
Master Mode:
1 = Initiates Start condition on SDAx and SCLx pins; automatically cleared by hardware
0 = Start condition is Idle
Slave Mode:
1 = Clock stretching is enabled for both Slave transmit and Slave receive (stretch is enabled)
0 = Clock stretching is disabled

Note 1: The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.

2: If the I^2C module is active, these bits may not be set (no spooling) and the SSPxBUF may not be written (or writes to the SSPxBUF are disabled).

REGISTER 14-6: SSPxCON3: MSSPx CONTROL REGISTER 3 (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACKTIM	PCIE	SCIE	BOEN(1)	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **ACKTIM:** Acknowledge Time Status bit (I^2C mode only)
Unused in SPI mode.

bit 6 **PCIE**: Stop Condition Interrupt Enable bit (I^2C mode only)
Unused in SPI mode.

bit 5 **SCIE**: Start Condition Interrupt Enable bit (I^2C mode only)
Unused in SPI mode.

bit 4 **BOEN:** Buffer Overwrite Enable bit(1)
In SPI Slave mode:
1 = SSPxBUF updates every time that a new data byte is shifted in, ignoring the BF bit
0 = If a new byte is received with the BF bit of the SSPxSTAT register already set, the SSPOV bit of the SSPxCON1 register is set and the buffer is not updated

bit 3 **SDAHT:** SDAx Hold Time Selection bit (I^2C mode only)
Unused in SPI mode.

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
Unused in SPI mode.

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
Unused in SPI mode.

bit 0 **DHEN:** Data Hold Enable bit (Slave mode only)
Unused in SPI mode.

Note 1: For Daisy-Chained SPI Operation: Allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPxBUF.

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REGISTER 14-7: SSPxCON3: MSSPx CONTROL REGISTER 3 (I^2C MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACKTIM(1)	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **ACKTIM:** Acknowledge Time Status bit(1)
1 = Indicates the I^2C bus is in an Acknowledge sequence, sets on the 8th falling edge of the SCLx clock
0 = Not an Acknowledge sequence, cleared on the 9th rising edge of the SCLx clock

bit 6 **PCIE**: Stop Condition Interrupt Enable bit
1 = Enables interrupt on detection of a Stop condition
0 = Stop detection interrupts are disabled(2)

bit 5 **SCIE**: Start Condition Interrupt Enable bit
1 = Enables interrupt on detection of a Start or Restart condition
0 = Start detection interrupts are disabled(2)

bit 4 **BOEN:** Buffer Overwrite Enable bit
I^2C Master mode:
This bit is ignored.
I^2C Slave mode:
1 = SSPxBUF is updated and an $\overline{ACK}$ is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0
0 = SSPxBUF is only updated when SSPOV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (Slave mode only)
1 = Enables Slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte; CKP bit of the SSPxCON1 register will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte; Slave hardware clears the CKP bit of the SSPxCON1 register and SCLx is held low
0 = Data holding is disabled

Note 1: This bit has no effect in Slave modes for which Start and Stop condition detection is explicitly listed as enabled.
2: The ACKTIM status bit is active only when the AHEN bit or DHEN bit is set.

REGISTER 14-8: SSPxADD: MSSPx SLAVE ADDRESS/BAUD RATE GENERATOR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADD[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **ADD[7:0]:** Slave Address/Baud Rate Generator Value bits

SPI Master and I^2C Master modes:
Reload value for the Baud Rate Generator. Clock period is (([SPxADD] + 1) * 2)/FOSC.

I^2C Slave modes:
Represents 7 or 8 bits of the Slave address, depending on the addressing mode used:

7-Bit mode: Address is ADD[7:1]; ADD[0] is ignored.

10-Bit LSb mode: ADD[7:0] are the Least Significant bits of the address.

10-Bit MSb mode: ADD[2:1] are the two Most Significant bits of the address; ADD[7:3] are always ‘11110’ as a specification requirement; ADD[0] is ignored.

REGISTER 14-9: SSPxMSK: I^2C SLAVE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
MSK[7:0](1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **MSK[7:0]:** Slave Address Mask Select bits(1)

1 = Masking of corresponding bit of SSPxADD is enabled
0 = Masking of corresponding bit of SSPxADD is disabled

Note 1: MSK0 is not used as a mask bit in 7-bit addressing.

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REGISTER 14-10: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SDO2DIS(1)	SCK2DIS(1)	SDO1DIS	SCK1DIS
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **SDO2DIS:** MSSP2 SDO2 Pin Disable bit(1)
1 = The SPI output data (SDO2) of MSSP2 to the pin are disabled
0 = The SPI output data (SDO2) of MSSP2 are output to the pin

bit 10 **SCK2DIS:** MSSP2 SCK2 Pin Disable bit(1)
1 = The SPI clock (SCK2) of MSSP2 to the pin is disabled
0 = The SPI clock (SCK2) of MSSP2 is output to the pin

bit 9 **SDO1DIS:** MSSP1 SDO1 Pin Disable bit
1 = The SPI output data (SDO1) of MSSP1 to the pin are disabled
0 = The SPI output data (SDO1) of MSSP1 are output to the pin

bit 8 **SCK1DIS:** MSSP1 SCK1 Pin Disable bit
1 = The SPI clock (SCK1) of MSSP1 to the pin is disabled
0 = The SPI clock (SCK1) of MSSP1 is output to the pin

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: These bits are implemented only on PIC24FXXKM20X devices.

NOTES:

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15.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Universal Asynchronous Receiver Transmitter, refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in this PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. This module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

The primary features of the UART module are:

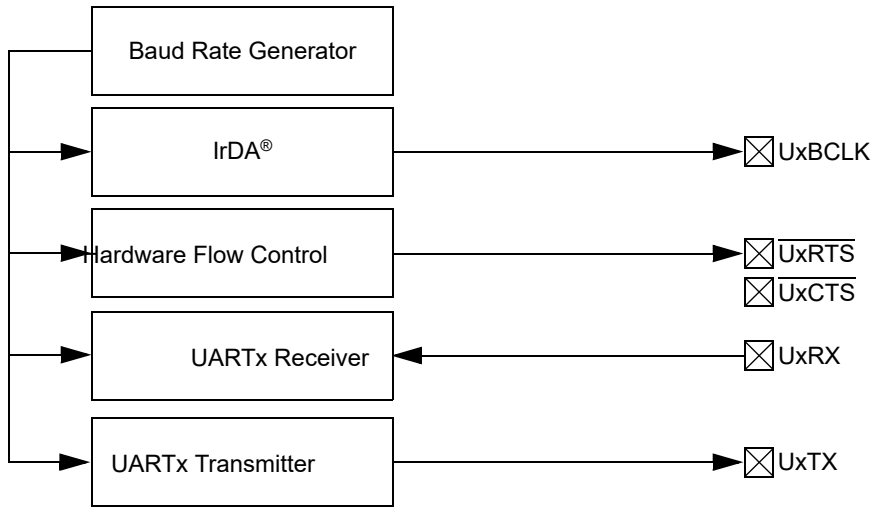
- Full-Duplex, 8-Bit or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator (IBRG) with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 15-1. The UARTx module consists of these important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

Note: Throughout this section, references to register and bit names that may be associated with a specific USART module are referred to generically by the use of 'x' in place of the specific module number. Thus, "UxSTA" might refer to the USART Status register for either USART1 or USART2.

FIGURE 15-1: UARTx MODULE SIMPLIFIED BLOCK DIAGRAM



15.1 UARTx Baud Rate Generator (BRG)

The UARTx module includes a dedicated 16-bit Baud Rate Generator (BRG). The UxBRG register controls the period of a free-running, 16-bit timer. Equation 15-1 provides the formula for computation of the baud rate with BRGH = 0.

EQUATION 15-1: UARTx BAUD RATE WITH BRGH = 0(1)

$$\text{Baud Rate} = \frac{F_{CY}}{16 \cdot (\text{UxBRG} + 1)}$$

$$\text{UxBRG} = \frac{F_{CY}}{16 \cdot \text{Baud Rate}} - 1$$

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.

Example 15-1 provides the calculation of the baud rate error for the following conditions:

- F_{CY} = 4 MHz
- Desired Baud Rate = 9600

The maximum baud rate (BRGH = 0) possible is $F_{CY}/16$ (for UxBRG = 0) and the minimum baud rate possible is $F_{CY}/(16 * 65536)$.

Equation 15-2 shows the formula for computation of the baud rate with BRGH = 1.

EQUATION 15-2: UARTx BAUD RATE WITH BRGH = 1(1)

$$\text{Baud Rate} = \frac{F_{CY}}{4 \cdot (\text{UxBRG} + 1)}$$

$$\text{UxBRG} = \frac{F_{CY}}{4 \cdot \text{Baud Rate}} - 1$$

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.

The maximum baud rate (BRGH = 1) possible is $F_{CY}/4$ (for UxBRG = 0) and the minimum baud rate possible is $F_{CY}/(4 * 65536)$.

Writing a new value to the UxBRG register causes the BRG timer to be reset (cleared). This ensures the BRG does not wait for a timer overflow before generating the new baud rate.

EXAMPLE 15-1: BAUD RATE ERROR CALCULATION (BRGH = 0)(1)

Desired Baud Rate = $F_{CY}/(16\ (\text{UxBRG} + 1))$

Solving for UxBRG value:

UxBRG = $((F_{CY}/\text{Desired Baud Rate})/16) - 1$
UxBRG = $((4000000/9600)/16) - 1$
UxBRG = 25

Calculated Baud Rate = $4000000/(16\ (25 + 1))$
= 9615

Error = $\frac{(\text{Calculated Baud Rate} - \text{Desired Baud Rate})}{\text{Desired Baud Rate}}$
= $(9615 - 9600)/9600$
= 0.16%

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.

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15.2 Transmitting in 8-Bit Data Mode

1. Set up the UARTx:
   a) Write the appropriate values for data, parity and Stop bits.
   b) Write the appropriate baud rate value to the UxBRG register.
   c) Set up transmit and receive interrupt enable and priority bits.
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write the data byte to the lower byte of the UxTXREG word. The value will be immediately transferred to the Transmit Shift Register (TSR) and the serial bit stream will start shifting out with the next rising edge of the baud clock.
5. Alternately, the data byte may be transferred while UTXEN = 0, and then, the user may set UTXEN. This will cause the serial bit stream to begin immediately, because the baud clock will start from a cleared state.
6. A transmit interrupt will be generated as per interrupt control bit, UTXISELx.

15.3 Transmitting in 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 15.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write UxTXREG as a 16-bit value only.
5. A word write to UxTXREG triggers the transfer of the 9-bit data to the TSR. The serial bit stream will start shifting out with the first rising edge of the baud clock.
6. A transmit interrupt will be generated as per the setting of control bit, UTXISELx.

15.4 Break and Sync Transmit Sequence

The following sequence will send a message frame header, made up of a Break, followed by an Auto-Baud Sync byte.

1. Configure the UARTx for the desired mode.
2. Set UTXEN and UTXBRK – this sets up the Break character.
3. Load the UxTXREG with a dummy character to initiate transmission (value is ignored).
4. Write '55h' to UxTXREG – loads the Sync character into the transmit FIFO.
5. After the Break has been sent, the UTXBRK bit is reset by hardware. The Sync character now transmits.

15.5 Receiving in 8-Bit or 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 15.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. A receive interrupt will be generated when one or more data characters have been received, as per interrupt control bit, URXISELx.
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read UxRXREG.

The act of reading the UxRXREG character will move the next character to the top of the receive FIFO, including a new set of PERR and FERR values.

15.6 Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Control Pins

UARTx Clear-to-Send ($\overline{\text{UxCTS}}$) and Request-to-Send ($\overline{\text{UxRTS}}$) are the two hardware controlled pins that are associated with the UARTx module. These two pins allow the UARTx to operate in Simplex and Flow Control modes. They are implemented to control the transmission and reception between the Data Terminal Equipment (DTE). The UEN[1:0] bits in the UxMODE register configure these pins.

15.7 Infrared Support

The UARTx module provides two types of infrared UARTx support: one is the IrDA clock output to support an external IrDA encoder and decoder device (legacy module support), and the other is the full implementation of the IrDA encoder and decoder.

As the IrDA modes require a 16x baud clock, they will only work when the BRGH bit (UxMODE[3]) is '0'.

15.7.1 EXTERNAL IrDA SUPPORT – IrDA CLOCK OUTPUT

To support external IrDA encoder and decoder devices, the UxBCLK pin (same as the $\overline{\text{UxRTS}}$ pin) can be configured to generate the 16x baud clock. When UEN[1:0] = 11, the UxBCLK pin will output the 16x baud clock if the UARTx module is enabled; it can be used to support the IrDA codec chip.

15.7.2 BUILT-IN IrDA ENCODER AND DECODER

The UARTx has full implementation of the IrDA encoder and decoder as part of the UARTx module. The built-in IrDA encoder and decoder functionality is enabled using the IREN bit (UxMODE[12]). When enabled (IREN = 1), the receive pin (UxRX) acts as the input from the infrared receiver. The transmit pin (UxTX) acts as the output to the infrared transmitter.

REGISTER 15-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0(2)	R/W-0(2)
UARTEN	—	USIDL	IREN(1)	RTSMD	—	UEN1	UEN0
bit 15							bit 8

HC/R/C-0	R/W-0	HC/R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UARTx Enable bit
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx, as defined by UEN[1:0]
- 0 = UARTx is disabled; all UARTx pins are controlled by port latches, UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when the device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(1)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **UEN[1:0]:** UARTx Enable bits(2)
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
- 1 = UARTx will continue to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
- 0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Enables Loopback mode
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
- 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
- 0 = Baud rate measurement is disabled or completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
- 1 = UxRX Idle state is ‘0’
- 0 = UxRX Idle state is ‘1’

Note 1: This feature is is only available for the 16x BRG mode (BRGH = 0).
2: The bit availability depends on the pin availability.

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REGISTER 15-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL[1:0]:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

Note 1: This feature is is only available for the 16x BRG mode (BRGH = 0).
2: The bit availability depends on the pin availability.

REGISTER 15-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	HC/R/W-0	R/W-0	HSC/R-0	HSC/R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	HSC/R-1	HSC/R-0	HSC/R-0	HS/R/C-0	HSC/R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
HS = Hardware Settable bit	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL[1:0]:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** IrDA® Encoder Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle ‘0’
- 0 = UxTX Idle ‘1’

If IREN = 1:
- 1 = UxTX Idle ‘1’
- 0 = UxTX Idle ‘0’

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve ‘0’ bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit
- 1 = Transmit is enabled; UxTX pin is controlled by UARTx
- 0 = Transmit is disabled; any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT register

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and the transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty; a transmission is in progress or queued

bit 7-6 **URXISEL[1:0]:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on an RSR transfer, making the receive buffer full (i.e., has four data characters)
- 10 = Interrupt is set on an RSR transfer, making the receive buffer 3/4 full (i.e., has three data characters)
- 0x = Interrupt is set when any character is received and transferred from the RSR to the receive buffer; receive buffer has one or more characters

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REGISTER 15-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed (clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the RSR to the Empty state)

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data; at least one more character can be read
0 = Receive buffer is empty

REGISTER 15-3: UxTXREG: UARTx TRANSMIT REGISTER

U-x	U-x	U-x	U-x	U-x	U-x	U-x	W-x
—	—	—	—	—	—	—	UTX8
bit 15							bit 8

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
UTX[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8 **UTX8:** Data of the Transmitted Character bit (in 9-bit mode)

bit 7-0 **UTX[7:0]:** Data of the Transmitted Character bits

REGISTER 15-4: UxRXREG: UARTx RECEIVE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	HSC/R-0
—	—	—	—	—	—	—	URX8
bit 15							bit 8

HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0	HSC/R-0
URX[7:0]							
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8 **URX8:** Data of the Received Character bit (in 9-bit mode)

bit 7-0 **URX[7:0]:** Data of the Received Character bits

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16.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to **"RTCC with External Power Control"** (www.microchip.com/DS39745) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The RTCC provides the user with a Real-Time Clock and Calendar (RTCC) function that can be calibrated.

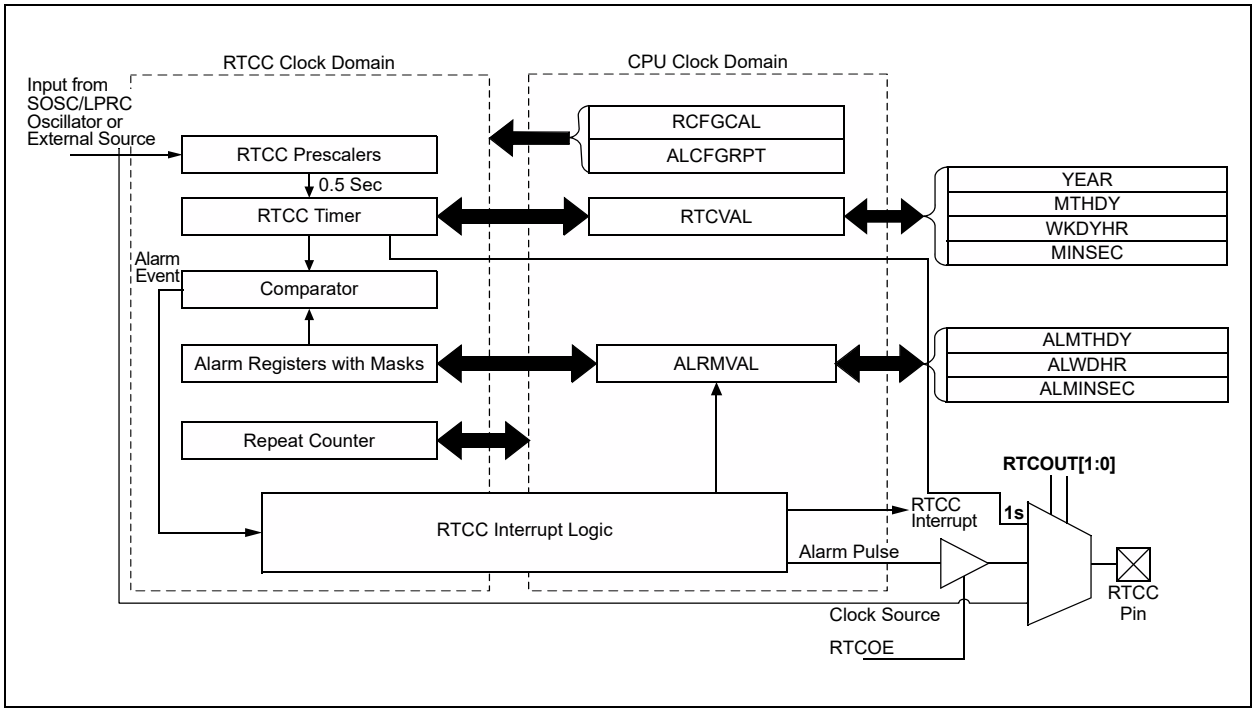
Key features of the RTCC module are:

- Operates in Sleep and Retention Sleep Modes
- Selectable Clock Source
- Provides Hours, Minutes and Seconds Using 24-Hour Format
- Visibility of One Half Second Period
- Provides Calendar – Weekday, Date, Month and Year
- Alarm-Configurable for Half a second, One Second, Ten Seconds, One Minute, Ten Minutes, One Hour, One Day, One Week, One Month or One Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat Chime
- Year 2000 to 2099 Leap Year Correction
- BCD Format for Smaller Software Overhead
- Optimized for Long-Term Battery Operation
- User Calibration of the 32.768 kHz Clock Crystal/32K INTRC Frequency with Periodic Auto-Adjust
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- Calibration to within ±2.64 Seconds Error per Month
- Calibrates Up to 260 ppm of Crystal Error
- Ability to Periodically Wake-up External Devices without CPU Intervention (External Power Control)
- Power Control Output for External Circuit Control
- Calibration takes Effect Every 15 Seconds
- Runs from Any One of the Following:
  - External Real-Time Clock of 32.768 kHz
  - Internal 31.25 kHz LPRC Clock
  - 50 Hz or 60 Hz External Input

16.1 RTCC Source Clock

The user can select between the SOSC crystal oscillator, LPRC internal oscillator or an external 50 Hz/60 Hz power line input as the clock reference for the RTCC module. This gives the user an option to trade off system cost, accuracy and power consumption, based on the overall system needs.

FIGURE 16-1: RTCC BLOCK DIAGRAM



16.2 RTCC Module Registers

The RTCC module registers are organized into three categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers

16.2.1 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding register pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTRx bits (RCFGCAL[9:8]) to select the desired Timer register pair (see Table 16-1).

By writing the RTCVALH byte, the RTCC Pointer value, the RTCPTR[1:0] bits decrement by one until they reach '00'. Once they reach '00', the MINUTES and SECONDS value will be accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 16-1: RTCVAL REGISTER MAPPING

RTCPTR[1:0]	RTCC Value Register Window	
	RTCVAL[15:8]	RTCVAL[7:0]
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTRx bits (ALCFGRPT[9:8]) to select the desired Alarm register pair (see Table 16-2).

By writing the ALRMVALH byte, the ALRMPTR[1:0] bits (Alarm Pointer value) decrement by one until they reach '00'. Once they reach '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL, until the pointer value is manually changed.

TABLE 16-2: ALRMVAL REGISTER MAPPING

ALRMPTR [1:0]	Alarm Value Register Window	
	ALRMVALH[15:8]	ALRMVALL[7:0]
00	ALRMMIN	ALRMSEC
01	ALRMWD	ALRMHR
10	ALRMMNTH	ALRMDAY
11	PWCSTAB	PWCSAMP

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL bytes, the ALRMPTR[1:0] value will be decremented. The same applies to the RTCVALH or RTCVALL bytes with the RTCPTR[1:0] being decremented.

Note: This only applies to read operations and not write operations.

16.2.2 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RCFGCAL[13]) must be set (see Example 16-1 and Example 16-2).

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL[13]) is kept clear at any other time. For the RTCWREN bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN. Therefore, it is recommended that code follow the procedure in Example 16-2.

16.2.3 SELECTING RTCC CLOCK SOURCE

There are four reference source clock options that can be selected for the RTCC using the RTCCLK[1:0] bits (RTCPWC[11:10]): 00 = Secondary Oscillator, 01 = LPRC, 10 = 50 Hz External Clock and 11 = 60 Hz External Clock.

EXAMPLE 16-1: SETTING THE RTCWREN BIT IN ASSEMBLY

```
push    w7              ; Store W7 and W8 values on the stack.
push    w8
disi    #5              ; Disable interrupts until sequence is complete.
mov     #0x55, w7       ; Write 0x55 unlock value to NVMKEY.
mov     w7, NVMKEY
mov     #0xAA, w8       ; Write 0xAA unlock value to NVMKEY.
mov     w8, NVMKEY
bset    RCFGCAL, #13    ; Set the RTCWREN bit.
pop     w8              ; Restore the original W register values from the stack.
pop     w7
```

EXAMPLE 16-2: SETTING THE RTCWREN BIT IN 'C'

```
//This builtin function executes implements the unlock sequence and sets
//the RTCWREN bit.
__builtin_write_RTCWEN();
```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16.2.4 RTCC CONTROL REGISTERS

REGISTER 16-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1)

R/W-0	U-0	R/W-0	HSC/R-0	HSC/R-0	R/W-0	R/W-0	R/W-0
RTCEN(2)	—	RTCWREN	RTCSYNC	HALFSEC(3)	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL[7:0]							
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit(2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
1 = RTCVALH and RTCVALL registers can be written to by the user
0 = RTCVALH and RTCVALL registers are locked out from being written to by the user

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading due to a rollover ripple resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = RTCVALH, RTCVALL or ALCFGRPT registers can be read without concern over a rollover ripple

bit 11 **HALFSEC:** Half Second Status bit(3)
1 = Second half period of a second
0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 9-8 **RTCPTR[1:0]:** RTCC Value Register Window Pointer bits
Points to the corresponding RTCC Value registers when reading the RTCVALH and RTCVALL registers. The RTCPTR[1:0] value decrements on every read or write of RTCVALH until it reaches ‘00’.

RTCVAL[15:8]:
00 = MINUTES
01 = WEEKDAY
10 = MONTH
11 = Reserved

RTCVAL[7:0]:
00 = SECONDS
01 = HOURS
10 = DAY
11 = YEAR

Note 1: The RCFGCAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only; it is cleared to ‘0’ on a write to the lower half of the MINSEC register.

REGISTER 16-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1) (CONTINUED)

bit 7-0 **CAL[7:0]:** RTC Drift Calibration bits

`01111111` = Maximum positive adjustment; adds 508 RTC clock pulses every one minute
•
•
•
`00000001` = Minimum positive adjustment; adds 4 RTC clock pulses every one minute
`00000000` = No adjustment
`11111111` = Minimum negative adjustment; subtracts 4 RTC clock pulses every one minute
•
•
•
`10000000` = Maximum negative adjustment; subtracts 512 RTC clock pulses every one minute

Note 1: The RCFGCAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = `1`.
3: This bit is read-only; it is cleared to ‘`0`’ on a write to the lower half of the MINSEC register.

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REGISTER 16-2: RTCPWC: RTCC CONFIGURATION REGISTER 2[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCEN	PWCPOL	PWCCPRE	PWCSPRE	RTCCLK1[2]	RTCCLK0[2]	RTCOUT1	RTCOUT0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWCEN:** Power Control Enable bit
1 = Power control is enabled
0 = Power control is disabled

bit 14 **PWCPOL:** Power Control Polarity bit
1 = Power control output is active-high
0 = Power control output is active-low

bit 13 **PWCCPRE:** Power Control/Stability Prescaler bits
1 = PWC stability window clock is divide-by-2 of source RTCC clock
0 = PWC stability window clock is divide-by-1 of source RTCC clock

bit 12 **PWCSPRE:** Power Control Sample Prescaler bits
1 = PWC sample window clock is divide-by-2 of source RTCC clock
0 = PWC sample window clock is divide-by-1 of source RTCC clock

bit 11-10 **RTCCLK[1:0]:** RTCC Clock Select bits[2]
Determines the source of the internal RTCC clock, which is used for all RTCC timer operations.
00 = External Secondary Oscillator (SOSC)
01 = Internal LPRC Oscillator
10 = External power line source – 50 Hz
11 = External power line source – 60 Hz

bit 9-8 **RTCOUT[1:0]:** RTCC Output Select bits
Determines the source of the RTCC pin output.
00 = RTCC alarm pulse
01 = RTCC seconds clock
10 = RTCC clock
11 = Power control

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: The RTCPWC register is only affected by a POR.
2: When a new value is written to these register bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

REGISTER 16-3: ALCFGRPT: ALARM CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit

`1` = Alarm is enabled (cleared automatically after an alarm event whenever ARPT[7:0] = `00h` and CHIME = `0`)
`0` = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

`1` = Chime is enabled; ARPT[7:0] bits are allowed to roll over from 00h to FFh
`0` = Chime is disabled; ARPT[7:0] bits stop once they reach 00h

bit 13-10 **AMASK[3:0]:** Alarm Mask Configuration bits

`0000` = Every half second
`0001` = Every second
`0010` = Every ten seconds
`0011` = Every minute
`0100` = Every ten minutes
`0101` = Every hour
`0110` = Once a day
`0111` = Once a week
`1000` = Once a month
`1001` = Once a year (except when configured for February 29th, once every 4 years)
`101x` = Reserved – do not use
`11xx` = Reserved – do not use

bit 9-8 **ALRMPTR[1:0]:** Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVALH and ALRMVALL registers. The ALRMPTR[1:0] value decrements on every read or write of ALRMVALH until it reaches ‘`00`’.

ALRMVAL[15:8]:
`00` = ALRMMIN
`01` = ALRMWD
`10` = ALRMMNTH
`11` = Unimplemented

ALRMVAL[7:0]:
`00` = ALRMSEC
`01` = ALRMHR
`10` = ALRMDAY
`11` = Unimplemented

bit 7-0 **ARPT[7:0]:** Alarm Repeat Counter Value bits

`11111111` = Alarm will repeat 255 more times
•
•
•
`00000000` = Alarm will not repeat

The counter decrements on any alarm event; it is prevented from rolling over from 00h to FFh unless CHIME = `1`.

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16.2.5 RTCVAL REGISTER MAPPINGS

REGISTER 16-4: YEAR: YEAR VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-4 **YRTEN[3:0]:** Binary Coded Decimal Value of Year’s Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE[3:0]:** Binary Coded Decimal Value of Year’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 16-5: MTHDY: MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month’s Tens Digit bit
Contains a value of ‘0’ or ‘1’.

bit 11-8 **MTHONE[3:0]:** Binary Coded Decimal Value of Month’s Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DAYTEN[1:0]:** Binary Coded Decimal Value of Day’s Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE[3:0]:** Binary Coded Decimal Value of Day’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 16-6: WKDYHR: WEEKDAY AND HOURS VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY[2:0]		
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **WDAY[2:0]:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **HRTEN[1:0]:** Binary Coded Decimal Value of Hour’s Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE[3:0]:** Binary Coded Decimal Value of Hour’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 16-7: MINSEC: MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **MINTEN[2:0]:** Binary Coded Decimal Value of Minute’s Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE[3:0]:** Binary Coded Decimal Value of Minute’s Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SECTEN[2:0]:** Binary Coded Decimal Value of Second’s Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE[3:0]:** Binary Coded Decimal Value of Second’s Ones Digit bits
Contains a value from 0 to 9.

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16.2.6 ALRMVAL REGISTER MAPPINGS

REGISTER 16-8: ALMTHDY: ALARM MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month’s Tens Digit bit
Contains a value of ‘0’ or ‘1’.

bit 11-8 **MTHONE[3:0]:** Binary Coded Decimal Value of Month’s Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DAYTEN[1:0]:** Binary Coded Decimal Value of Day’s Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE[3:0]:** Binary Coded Decimal Value of Day’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 16-9: ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY[2:0]		
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **WDAY[2:0]:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **HRTEN[1:0]:** Binary Coded Decimal Value of Hour’s Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE[3:0]:** Binary Coded Decimal Value of Hour’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 16-10: ALMINSEC: ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **MINTEN[2:0]:** Binary Coded Decimal Value of Minute’s Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE[3:0]:** Binary Coded Decimal Value of Minute’s Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SECTEN[2:0]:** Binary Coded Decimal Value of Second’s Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE[3:0]:** Binary Coded Decimal Value of Second’s Ones Digit bits
Contains a value from 0 to 9.

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REGISTER 16-11: RTCCSWT: RTCC CONTROL/SAMPLE WINDOW TIMER REGISTER(1)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PWCSTAB[7:0]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PWCSAMP[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **PWCSTAB[7:0]:** PWM Stability Window Timer bits

`11111111` = Stability window is 255 TPWCCLK clock periods

•

•

•

`00000000` = Stability window is 0 TPWCCLK clock periods

The sample window starts when the alarm event triggers. The stability window timer starts counting from every alarm event when PWCEN = `1`.

bit 7-0 **PWCSAMP[7:0]:** PWM Sample Window Timer bits

`11111111` = Sample window is always enabled, even when PWCEN = `0`

`11111110` = Sample window is 254 TPWCCLK clock periods

•

•

•

`00000000` = Sample window is 0 TPWCCLK clock periods

The sample window timer starts counting at the end of the stability window when PWCEN = `1`. If PWCSTAB[7:0] = `00000000`, the sample window timer starts counting from every alarm event when PWCEN = `1`.

Note 1: A write to this register is only allowed when RTCWREN = `1`.

16.3 Calibration

The real-time crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than three seconds per month. This is accomplished by finding the number of error clock pulses and storing the value into the lower half of the RCFGCAL register. The 8-bit signed value, loaded into the lower half of RCFGCAL, is multiplied by four and will be either added or subtracted from the RTCC timer, once every minute. Refer to the steps below for RTCC calibration:

1. Using another timer resource on the device, the user must find the error of the 32.768 kHz crystal.
2. Once the error is known, it must be converted to the number of error clock pulses per minute.
3. a) If the oscillator is faster than ideal (negative result from Step 2), the RCFGCAL register value must be negative. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

   b) If the oscillator is slower than ideal (positive result from Step 2), the RCFGCAL register value must be positive. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

EQUATION 16-1:

(Ideal Frequency† – Measured Frequency) * 60 = Clocks per Minute

† Ideal Frequency = 32,768 Hz

Writes to the lower half of the RCFGCAL register should only occur when the timer is turned off, or immediately after the rising edge of the seconds pulse, except when SECONDS = 00, 15, 30 or 45. This is due to the auto-adjust of the RTCC at 15 second intervals.

Note: It is up to the user to include, in the error value, the initial error of the crystal: drift due to temperature and drift due to crystal aging.

16.4 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (ALCFGRPT[15])
- One-time alarm and repeat alarm options are available

16.4.1 CONFIGURING THE ALARM

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to ALRMVAL should only take place when ALRMEN = `0`.

As shown in Figure 16-2, the interval selection of the alarm is configured through the AMASKx bits (ALCFGRPT[13:10]). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ARPT[7:0] bits (ALCFGRPT[7:0]). When the value of the ARPTx bits equals 00h and the CHIME bit (ALCFGRPT[14]) is cleared, the repeat function is disabled, and only a single alarm will occur. The alarm can be repeated up to 255 times by loading ARPT[7:0] with FFh.

After each alarm is issued, the value of the ARPTx bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off.

Indefinite repetition of the alarm can occur if the CHIME bit = `1`. Instead of the alarm being disabled when the value of the ARPTx bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

16.4.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. In addition, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a Trigger clock to other peripherals.

Note: Changing any of the registers, other than the RCFGCAL and ALCFGRPT registers, and the CHIME bit while the alarm is enabled (ALRMEN = `1`), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = `0`). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = `0`.

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FIGURE 16-2: ALARM MASK SETTINGS

Alarm Mask Setting (AMASK[3:0])	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 - Every half second 0001 - Every second						
0010 - Every 10 seconds						s
0011 - Every minute						s s
0100 - Every 10 minutes					m	s s
0101 - Every hour					m m	s s
0110 - Every day				h h	m m	s s
0111 - Every week	d			h h	m m	s s
1000 - Every month			d d	h h	m m	s s
1001 - Every year(1)		m m	d d	h h	m m	s s

Note 1: Annually, except when configured for February 29.

16.5 Power Control

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake from the current low-power mode (Sleep, Deep Sleep, etc.).

To enable this feature, the RTCC must be enabled (RTCEN = 1), the PWCEN register bit must be set and the RTCC pin must be driving the PWC control signal (RTCOE = 1 and RTCCLK[1:0] = 11).

The polarity of the PWC control signal may be chosen using the PWCPOL register bit. Active-low or active-high may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin. This setting is able to drive the GND pin(s) of the external device directly (with the appropriate external V_{DD} pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

NOTES:

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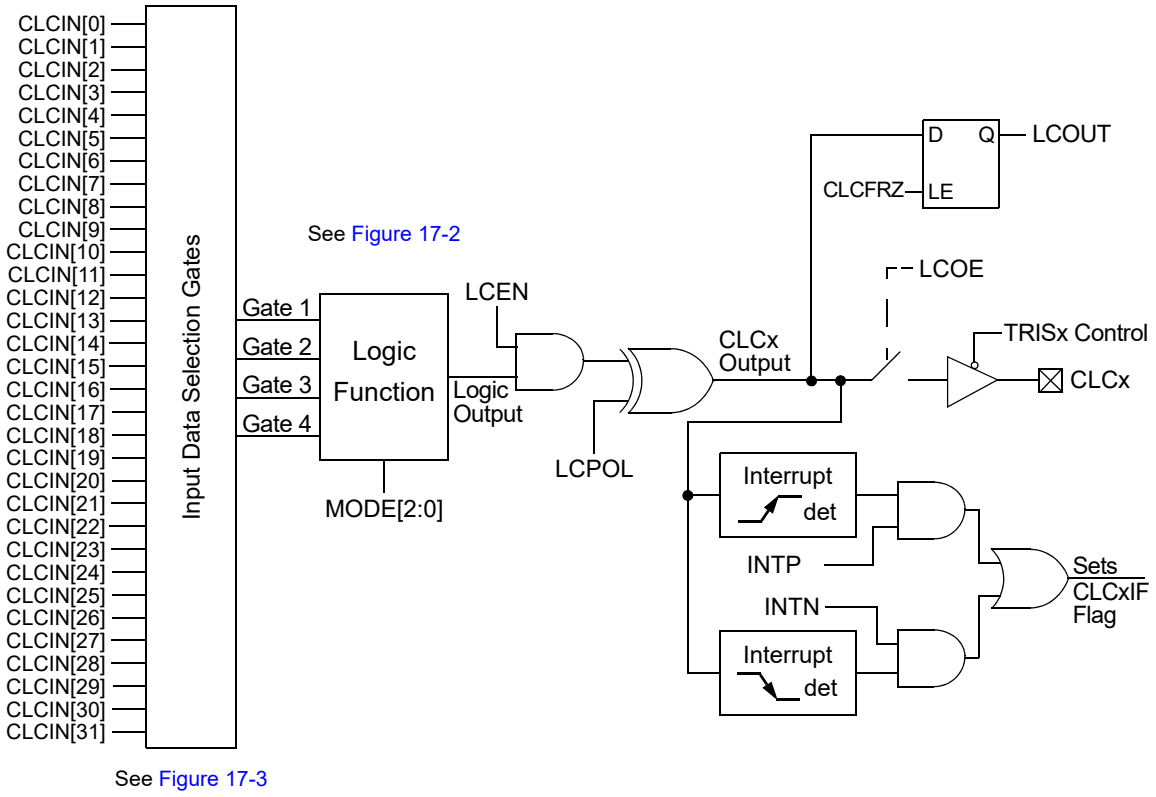
17.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator Voltage Reference, refer to **"Configurable Logic Cell (CLC)"** (www.microchip.com/DS70005298) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 17-1 shows an overview of the module. Figure 17-3 shows the details of the data source multiplexers and logic input gate connections.

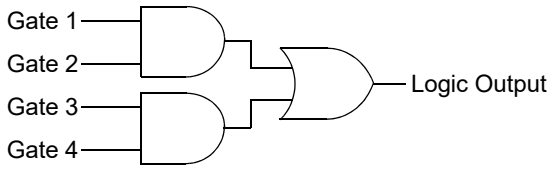
FIGURE 17-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCONL register.

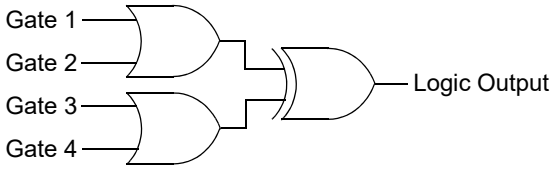
FIGURE 17-2: CLCx LOGIC FUNCTION COMBINATORIAL OPTIONS

AND – OR



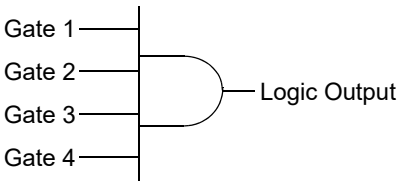
MODE[2:0] = 000

OR – XOR



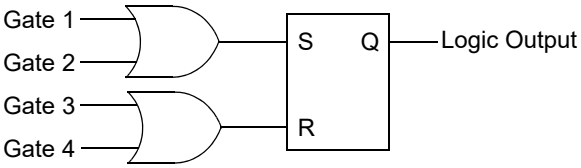
MODE[2:0] = 001

4-Input AND



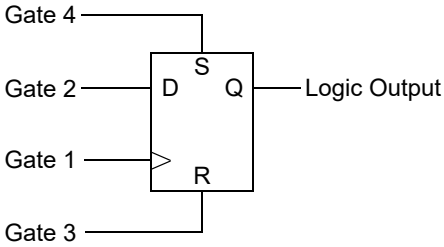
MODE[2:0] = 010

S-R Latch



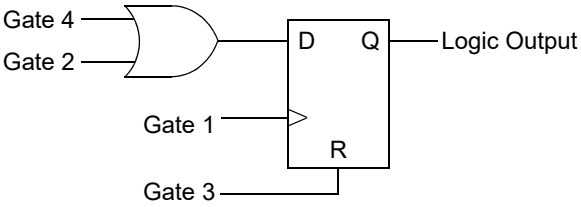
MODE[2:0] = 011

1-Input D Flip-Flop with S and R



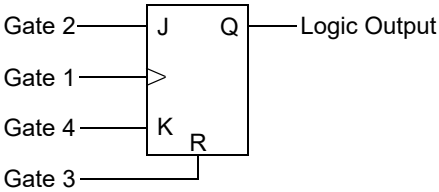
MODE[2:0] = 100

2-Input D Flip-Flop with R



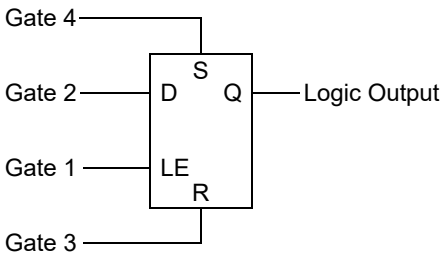
MODE[2:0] = 101

J-K Flip-Flop with R



MODE[2:0] = 110

1-Input Transparent Latch with S and R



MODE[2:0] = 111

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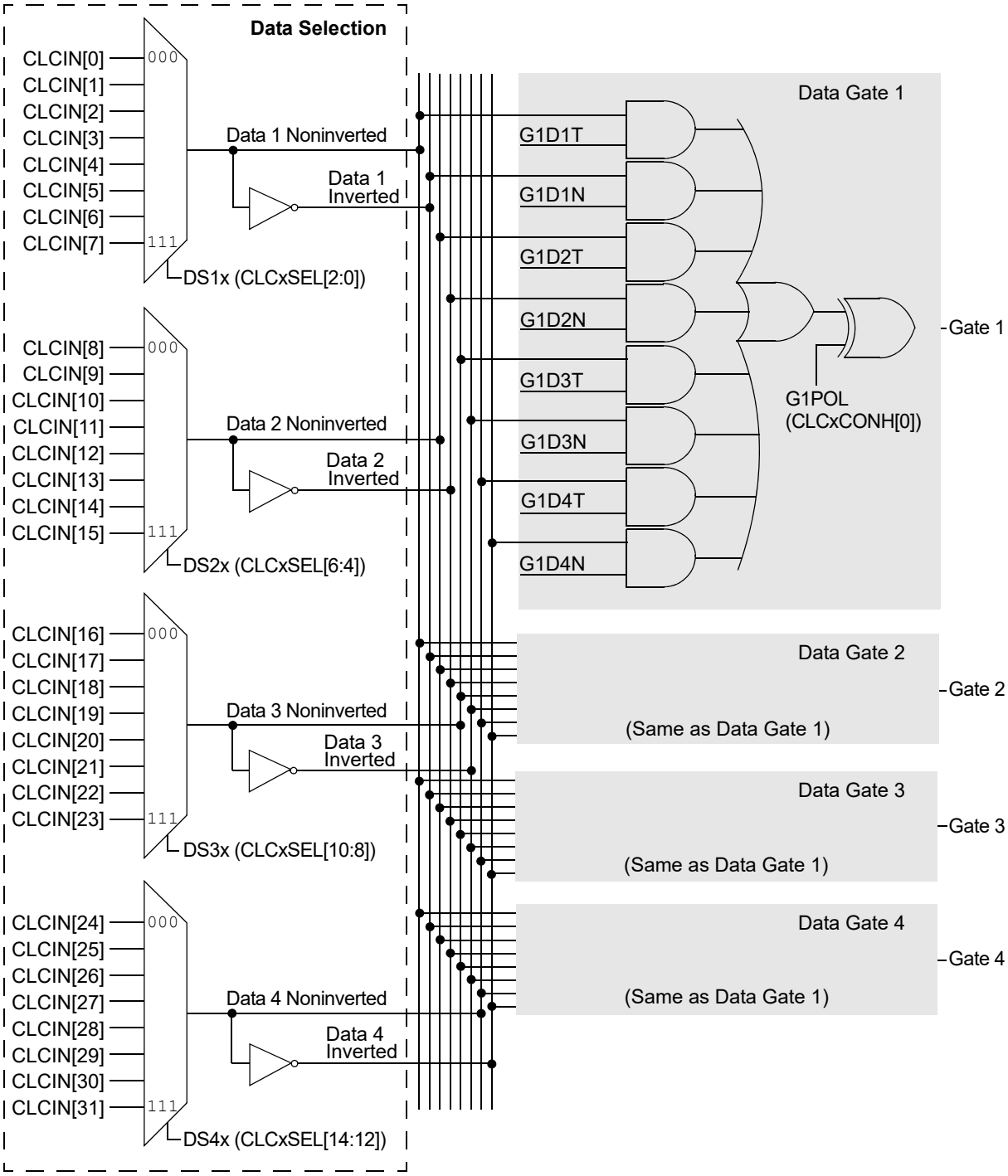
FIGURE 17-3: CLCx INPUT SOURCE SELECTION DIAGRAM



Note: All controls are undefined at power-up.

17.1 Control Registers

The CLCx module is controlled by the following registers:

- CLCxCONL
- CLCxCONH
- CLCxSEL
- CLCxGLSL
- CLCxGLSH

The CLCx Control registers (CLCxCONL and CLCxCONH) are used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Source Select register (CLCxSEL) allows the user to select up to four data input sources using the four data input selection multiplexers. Each multiplexer has a list of eight data sources available.

The CLCx Gate Logic Select registers (CLCxGLSL and CLCxGLSH) allow the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these eight signals are enabled, ORed together by the logic cell input gates.

REGISTER 17-1: CLCxCONL: CLCx CONTROL REGISTER (LOW)

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
LCEN	—	—	—	INTP	INTN	—	—
bit 15							bit 8

R-0	R-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
LCOE	LCOUT	LCPOL	—	—	MODE2	MODE1	MODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **LCEN:** CLCx Enable bit
1 = CLCx is enabled and mixing input signals
0 = CLCx is disabled and has logic zero outputs

bit 14-12 **Unimplemented:** Read as ‘0’

bit 11 **INTP:** CLCx Positive Edge Interrupt Enable bit
1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** CLCx Negative Edge Interrupt Enable bit
1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **LCOE:** CLCx Port Enable bit
1 = CLCx port pin output is enabled
0 = CLCx port pin output is disabled

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

bit 5 **LCPOL:** CLCx Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

bit 4-3 **Unimplemented:** Read as ‘0’

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REGISTER 17-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 **MODE[2:0]:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

REGISTER 17-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

REGISTER 17-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS42	DS41	DS40	—	DS32	DS31	DS30
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS22	DS21	DS20	—	DS12	DS11	DS10
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **DS4[2:0]:** Data Selection MUX 4 Signal Selection bits
111 = MCCP3 Compare Event Flag (CCP3IF)
110 = MCCP1 Compare Event Flag (CCP1IF)
101 = Digital logic low
100 = CTMU Trigger interrupt
For CLC1:
011 = SPI1 SDIx
010 = Comparator 3 output
001 = CLC2 output
000 = CLCINB I/O pin
For CLC2:
011 = SPI2 SDIx
010 = Comparator 3 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **DS3[2:0]:** Data Selection MUX 3 Signal Selection bits
111 = MCCP3 Compare Event Flag (CCP3IF)
110 = MCCP2 Compare Event Flag (CCP2IF)
101 = Digital logic low
For CLC1:
100 = UART1 RX
011 = SPI1 SDOx
010 = Comparator 2 output
001 = CLC1 output
000 = CLCINA I/O pin
For CLC2:
100 = UART2 RX
011 = SPI2 SDOx
010 = Comparator 2 output
001 = CLC2 output
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as ‘0’

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REGISTER 17-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 6-4 **DS2[2:0]:** Data Selection MUX 2 Signal Selection bits

111 = MCCP2 Compare Event Flag (CCP2IF)
110 = MCCP1 Compare Event Flag (CCP1IF)
101 = Digital logic low
100 = A/D end of conversion event

For CLC1:
011 = UART1 TX
010 = Comparator 1 output
001 = CLC2 output
000 = CLCINB I/O pin

For CLC2:
011 = UART2 TX
010 = Comparator 1 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1[2:0]:** Data Selection MUX 1 Signal Selection bits

111 = SCCP5 Compare Event Flag (CCP5IF)
110 = SCCP4 Compare Event Flag (CCP4IF)
101 = Digital logic low
100 = 8 MHz FRC clock source
011 = LPRC clock source
010 = SOSC clock source
001 = System clock (TCY)
000 = CLCINA I/O pin

REGISTER 17-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 2
0 = The Data Source 4 signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 2
0 = The Data Source 3 signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 2
0 = The Data Source 2 signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 2
0 = The Data Source 1 signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 1
0 = The Data Source 4 signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 1
0 = The Data Source 3 signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

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REGISTER 17-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 1
0 = The Data Source 2 signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 1
0 = The Data Source 1 signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

REGISTER 17-5: CLCxGLSH: CLCx GATE LOGIC INPUT SELECT HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **G4D4T:** Gate 4 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 4
0 = The Data Source 4 inverted signal is disabled for Gate 4

bit 14 **G4D4N:** Gate 4 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 4
0 = The Data Source 4 inverted signal is disabled for Gate 4

bit 13 **G4D3T:** Gate 4 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 4
0 = The Data Source 3 inverted signal is disabled for Gate 4

bit 12 **G4D3N:** Gate 4 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 4
0 = The Data Source 3 inverted signal is disabled for Gate 4

bit 11 **G4D2T:** Gate 4 Data Source 2 True Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 4
0 = The Data Source 2 inverted signal is disabled for Gate 4

bit 10 **G4D2N:** Gate 4 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 4
0 = The Data Source 2 inverted signal is disabled for Gate 4

bit 9 **G4D1T:** Gate 4 Data Source 1 True Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 4
0 = The Data Source 1 inverted signal is disabled for Gate 4

bit 8 **G4D1N:** Gate 4 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 4
0 = The Data Source 1 inverted signal is disabled for Gate 4

bit 7 **G3D4T:** Gate 3 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 3
0 = The Data Source 4 inverted signal is disabled for Gate 3

bit 6 **G3D4N:** Gate 3 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 3
0 = The Data Source 4 inverted signal is disabled for Gate 3

bit 5 **G3D3T:** Gate 3 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

bit 4 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

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REGISTER 17-5: CLCxGLSH: CLCx GATE LOGIC INPUT SELECT HIGH REGISTER (CONTINUED)

bit 3 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 3
0 = The Data Source 2 inverted signal is disabled for Gate 3

bit 2 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 3
0 = The Data Source 2 inverted signal is disabled for Gate 3

bit 1 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 3
0 = The Data Source 1 inverted signal is disabled for Gate 3

bit 0 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 3
0 = The Data Source 1 inverted signal is disabled for Gate 3

NOTES:

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18.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

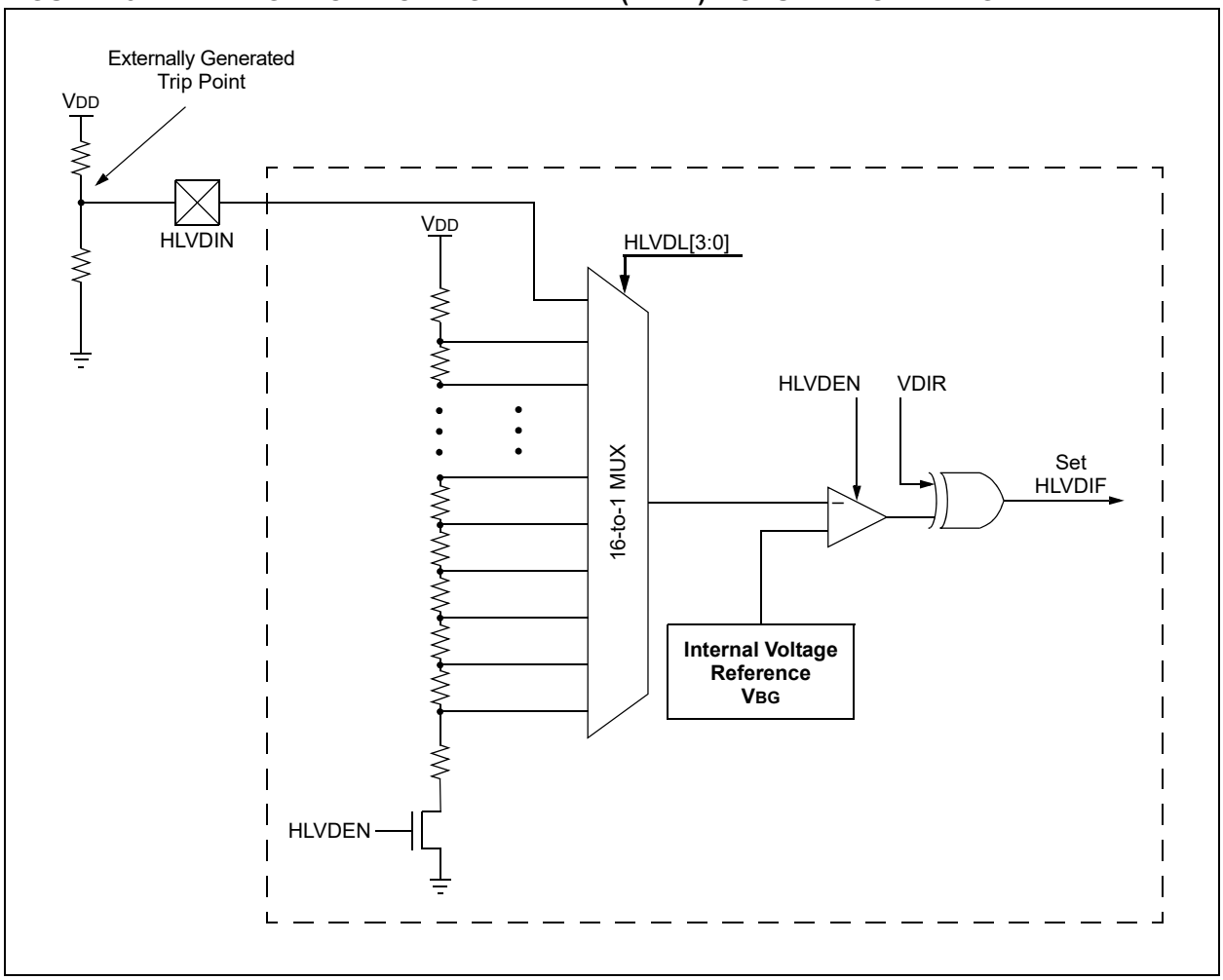
Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (www.microchip.com/DS39725) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The High/Low-Voltage Detect module (HLVD) is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 18-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 18-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



REGISTER 18-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit
1 = HLVD is enabled
0 = HLVD is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **Unimplemented:** Read as ‘0’

bit 7 **VDIR:** Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds trip point (HLVDL[3:0])
0 = Event occurs when voltage equals or falls below trip point (HLVDL[3:0])

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit
1 = Indicates that the band gap voltage is stable
0 = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Indicates that the internal reference voltage is stable and the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
0 = Indicates that the internal reference voltage is unstable and the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range, and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as ‘0’

bit 3-0 **HLVDL[3:0]:** High/Low-Voltage Detection Limit bits
1111 = External analog input is used (input comes from the HLVDIN pin)
1110 = Trip Point 1(1)
1101 = Trip Point 2(1)
1100 = Trip Point 3(1)
•
•
•
0000 = Trip Point 15(1)

Note 1: For the actual trip point, see **Section 27.0 “Electrical Characteristics”**.

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19.0 12-BIT A/D CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter with Threshold Detect, refer to **"12-Bit A/D Converter with Threshold Detect"** (www.microchip.com/DS39739) in the *"dsPIC33/PIC24F Family Reference Manual"*.

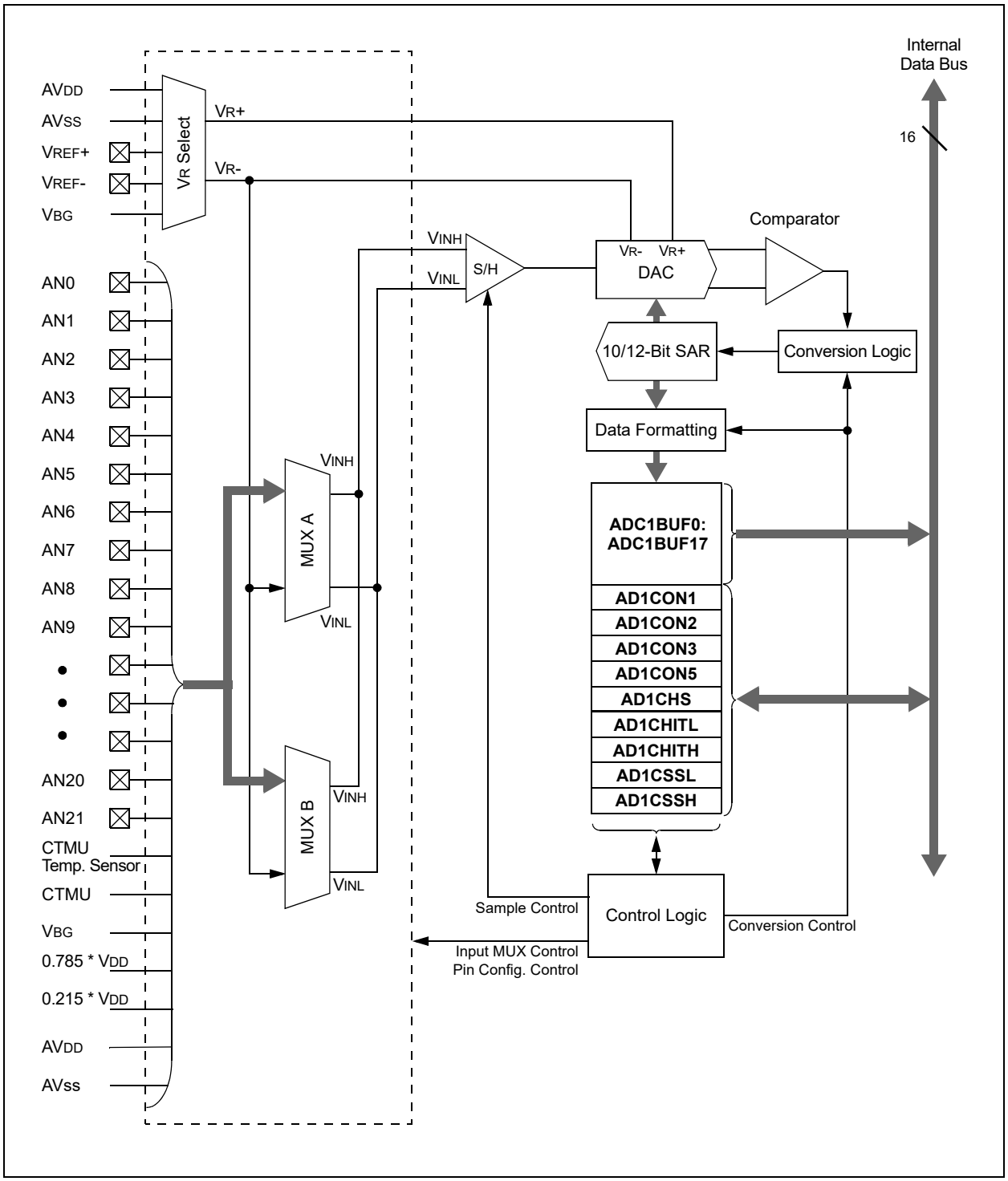
The PIC24F 12-bit A/D Converter has the following key features:

- Successive Approximation Register (SAR) Conversion
- Conversion Speeds of Up to 100 ksps
- Up to 32 Analog Input Channels (internal and external)
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H) Amplifier
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed-Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Operation During CPU Sleep and Idle modes

The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in some PIC24 devices. Both modules are Successive Approximation Register (SAR) converters at their cores, surrounded by a range of hardware features for flexible configuration. This version of the module extends functionality by providing 12-bit resolution, a wider range of automatic sampling options and tighter integration with other analog modules, such as the CTMU, and a configurable results buffer. There is a legacy 10-bit mode on this A/D to allow the option to run with lower resolution in order to obtain higher throughput. This module also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results.

A simplified block diagram for the module is illustrated in Figure 19-1.

FIGURE 19-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM



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To perform an A/D conversion:

1. Configure the A/D module:
   a) Configure the port pins as analog inputs and/or select band gap reference inputs (ANSx registers).
   b) Select the voltage reference source to match the expected range on the analog inputs (AD1CON2[15:13]).
   c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3[7:0]).
   d) Select the appropriate sample/conversion sequence (AD1CON1[7:4] and AD1CON3[12:8]).
   e) Configure the MODE12 bit to select A/D resolution (AD1CON1[10]).
   f) Select how conversion results are presented in the buffer (AD1CON1[9:8]).
   g) Select the interrupt rate (AD1CON2[6:2]).
   h) Turn on the A/D module (AD1CON1[15]).
2. Configure the A/D interrupt (if required):
   a) Clear the AD1IF bit.
   b) Select the A/D interrupt priority.

To perform an A/D sample and conversion using Threshold Detect scanning:

1. Configure the A/D module:
   a) Configure the port pins as analog inputs (ANSx registers).
   b) Select the voltage reference source to match the expected range on the analog inputs (AD1CON2[15:13]).
   c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3[7:0]).
   d) Select the appropriate sample/conversion sequence (AD1CON1[7:4] and AD1CON3[12:8]).
   e) Configure the MODE12 bit to select A/D resolution (AD1CON1[10]).
   f) Select how the conversion results are presented in the buffer (AD1CON1[9:8]).
   g) Select the interrupt rate (AD1CON2[6:2]).
2. Configure the threshold compare channels:
   a) Enable auto-scan; set the ASEN bit (AD1CON5[15]).
   b) Select the Compare mode, “Greater Than, Less Than or Windowed”; set the CMx bits (AD1CON5[1:0]).
   c) Select the threshold compare channels to be scanned (AD1CSSH, AD1CSSL).
   d) If the CTMU is required as a current source for a threshold compare channel, enable the corresponding CTMU channel (AD1CTMENH, AD1CTMENL).
   e) Write the threshold values into the corresponding ADC1BUFx registers.
   f) Turn on the A/D module (AD1CON1[15]).

Note: If performing an A/D sample and conversion, using Threshold Detect in Sleep Mode, the RC A/D clock source must be selected before entering into Sleep mode.

3. Configure the A/D interrupt (OPTIONAL):
   a) Clear the AD1IF bit.
   b) Select the A/D interrupt priority.

19.1 A/D Control Registers

The 12-bit A/D Converter module uses up to 43 registers for its operation. All registers are mapped in the data memory space.

19.1.1 CONTROL REGISTERS

Depending on the specific device, the module has up to eleven control and status registers:

- AD1CON1: A/D Control Register 1
- AD1CON2: A/D Control Register 2
- AD1CON3: A/D Control Register 3
- AD1CON5: A/D Control Register 5
- AD1CHS: A/D Sample Select Register
- AD1CHITH and AD1CHITL: A/D Scan Compare Hit Registers
- AD1CSSH and AD1CSSL: A/D Input Scan Select Registers
- AD1CTMENH and AD1CTMENL: CTMU Enable Registers

The AD1CON1, AD1CON2 and AD1CON3 registers (Register 19-1, Register 19-2 and Register 19-3) control the overall operation of the A/D module. This includes enabling the module, configuring the conversion clock and voltage reference sources, selecting the sampling and conversion Triggers, and manually controlling the sample/convert sequences. The AD1CON5 register (Register 19-4) specifically controls features of the Threshold Detect operation, including its function in power-saving modes.

The AD1CHS register (Register 19-5) selects the input channels to be connected to the S/H amplifier. It also allows the choice of input multiplexers and the selection of a reference source for differential sampling.

The AD1CHITH and AD1CHITL registers (Register 19-6 and Register 19-7) are semaphore registers used with Threshold Detect operations. The status of individual bits, or bit pairs in some cases, indicates if a match condition has occurred. AD1CHITL is always implemented, whereas AD1CHITH may not be implemented in devices with 16 or fewer channels.

The AD1CSSH/L registers (Register 19-8 and Register 19-9) select the channels to be included for sequential scanning.

The AD1CTMENH/L registers (Register 19-10 and Register 19-11) select the channel(s) to be used by the CTMU during conversions. Selecting a particular channel allows the A/D Converter to control the CTMU (particularly, its current source) and read its data through that channel. AD1CTMENL is always implemented, whereas AD1CTMENH may not be implemented in devices with 16 or fewer channels.

19.1.2 A/D RESULT BUFFERS

The module incorporates a multi-word, dual port buffer, called ADC1BUFx. Each of the locations is mapped into the data memory space and is separately addressable. The buffer locations are referred to as ADC1BUF0 through ADC1BUFx (x = up to 17).

The A/D result buffers are both readable and writable. When the module is active (AD1CON[15] = `1`), the buffers are read-only and store the results of A/D conversions. When the module is inactive (AD1CON[15] = `0`), the buffers are both readable and writable. In this state, writing to a buffer location programs a conversion threshold for Threshold Detect operations.

Buffer contents are not cleared when the module is deactivated with the ADON bit (AD1CON1[15]). Conversion results and any programmed threshold values are maintained when ADON is set or cleared.

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REGISTER 19-1: AD1CON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	HSC/R/W-0	HSC/R/C-0
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as ‘0’	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Operating Mode bit
`1` = A/D Converter is operating
`0` = A/D Converter is off

bit 14 **Unimplemented:** Read as ‘`0`’

bit 13 **ADSIDL:** A/D Stop in Idle Mode bit
`1` = Discontinues module operation when device enters Idle mode
`0` = Continues module operation in Idle mode

bit 12-11 **Unimplemented:** Read as ‘`0`’

bit 10 **MODE12:** 12-Bit A/D Operation Mode bit
`1` = 12-bit A/D operation
`0` = 10-bit A/D operation

bit 9-8 **FORM[1:0]:** Data Output Format bits (see the following formats)
`11` = Fractional result, signed, left justified
`10` = Absolute fractional result, unsigned, left justified
`01` = Decimal result, signed, right justified
`00` = Absolute decimal result, unsigned, right justified

bit 7-4 **SSRC[3:0]:** Sample Clock Source Select bits
`1111` = Reserved
•
•
•
`1101` = Reserved
`1100` = CLC2 event ends sampling and starts conversion
`1011` = SCCP4 Capture/Compare Event or Timer (CCP4IF/CCT4IF) ends sampling and starts conversion
`1010` = MCCP3 Capture/Compare Event or Timer (CCP3IF/CCT3IF) ends sampling and starts conversion
`1001` = MCCP2 Capture/Compare Event or Timer (CCP2IF/CCT2IF) ends sampling and starts conversion
`1000` = CLC1 event ends sampling and starts conversion
`0111` = Internal counter ends sampling and starts conversion (auto-convert)
`0110` = TMR1 Sleep mode Trigger event ends sampling and starts conversion(1)
`0101` = TMR1 event ends sampling and starts conversion
`0100` = CTMU event ends sampling and starts conversion
`0011` = SCCP5 Capture/Compare Event or Timer (CCP5IF/CCT5IF) ends sampling and starts conversion
`0010` = MCCP1 Capture/Compare Event or Timer (CCP1IF/CCT1IF) ends sampling and starts conversion
`0001` = INT0 event ends sampling and starts conversion
`0000` = Clearing the Sample bit ends sampling and starts conversion

Note 1: This version of the TMR1 Trigger allows A/D conversions to be triggered from TMR1 while the device is operating in Sleep mode. The SSRC[3:0] = `0101` option allows conversions to be triggered in Run or Idle modes only.

REGISTER 19-1: AD1CON1: A/D CONTROL REGISTER 1 (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when the SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit
1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion cycle has completed
0 = A/D conversion cycle has not started or is in progress

Note 1: This version of the TMR1 Trigger allows A/D conversions to be triggered from TMR1 while the device is operating in Sleep mode. The SSRC[3:0] = 0101 option allows conversions to be triggered in Run or Idle modes only.

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REGISTER 19-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0
PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS(1)	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM(1)	ALTS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **PVCFG[1:0]:** A/D Converter Positive Voltage Reference Configuration bits
11 = 4 * Internal V_{BG}(2)
10 = 2 * Internal V_{BG}(3)
01 = External V_{REF}+
00 = AV_{DD}

bit 13 **NVCFG0:** A/D Converter Negative Voltage Reference Configuration bit
1 = External V_{REF}-
0 = AV_{SS}

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **BUFREGEN:** A/D Buffer Register Enable bit
1 = Conversion result is loaded into a buffer location determined by the converted channel
0 = A/D result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ S/H Input for MUX A Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **BUFS:** A/D Buffer Fill Status bit(1)
1 = A/D is filling the upper half of the buffer; user should access data in the lower half
0 = A/D is filling the lower half of the buffer; user should access data in the upper half

bit 6-2 **SMPI[4:0]:** Interrupt Sample Rate Select bits
11111 = Interrupts at the completion of the conversion for each 32nd sample
11110 = Interrupts at the completion of the conversion for each 31st sample
•
•
•
00001 = Interrupts at the completion of the conversion for every other sample
00000 = Interrupts at the completion of the conversion for each sample

bit 1 **BUFM:** A/D Buffer Fill Mode Select bit(1)
1 = Starts filling the buffer at address, ADC1BUF0, on the first interrupt and ADC1BUF(x/2) on the next interrupt (Split Buffer mode)
0 = Starts filling the buffer at address, ADC1BUF0, and each sequential address on successive interrupts (FIFO mode)

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on the first sample and Sample B on the next sample
0 = Always uses channel input selects for Sample A

Note 1: This is only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.
2: PIC24FV16KMXXX devices only. Reference setting will not be within specification for V_{DD} below 4.5V.
3: Reference setting will not be within specification for V_{DD} below 2.3V.

REGISTER 19-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	EXTSAM	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS[7:0]							
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit
1 = RC clock
0 = Clock is derived from the system clock

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = A/D is still sampling after SAMP = 0
0 = A/D is finished sampling

bit 13 **Reserved:** Maintain as ‘0’

bit 12-8 **SAMC[4:0]:** Auto-Sample Time Select bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS[7:0]:** A/D Conversion Clock Select bits
11111111-01000000 = Reserved
00111111 = 64 * TCY = TAD
•
•
•
00000001 = 2 * TCY = TAD
00000000 = TCY = TAD

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REGISTER 19-4: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	r-0	U-0	R/W-0	R/W-0
ASEN[1]	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** A/D Auto-Scan Enable bit[1]
- 1 = Auto-scan is enabled
- 0 = Auto-scan is disabled

bit 14 **LPEN:** A/D Low-Power Enable bit
- 1 = Returns to Low-Power mode after scan
- 0 = Remains in Full-Power mode after scan

bit 13 **CTMREQ:** CTMU Request bit
- 1 = CTMU is enabled when the A/D is enabled and active
- 0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
- 1 = Band gap is enabled when the A/D is enabled and active
- 0 = Band gap is not enabled by the A/D

bit 11 **Reserved:** Maintain as ‘0’

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **ASINT[1:0]:** Auto-Scan (Threshold Detect) Interrupt Mode bits
- 11 = Interrupt after a Threshold Detect sequence has completed and a valid compare has occurred
- 10 = Interrupt after a valid compare has occurred
- 01 = Interrupt after a Threshold Detect sequence has completed
- 00 = No interrupt

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-2 **WM[1:0]:** A/D Write Mode bits
- 11 = Reserved
- 10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match, as defined by the CMx and ASINTx bits, occurs)
- 01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match, as defined by the CMx bits, occurs)
- 00 = Legacy operation (conversion data are saved to a location determined by the buffer register bits)

bit 1-0 **CM[1:0]:** A/D Compare Mode bits
- 11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
- 10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
- 01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
- 00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

Note 1: When using auto-scan with Threshold Detect (ASEN = 1), do not configure the sample clock source to Auto-Convert mode (SSRC[3:0] = 7). Any other available SSRC selection is valid. To use auto-convert as the sample clock source (SSRC[3:0] = 7), make sure ASEN is cleared.

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REGISTER 19-5: AD1CHS: A/D SAMPLE SELECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **CH0NB[2:0]:** Sample B Channel 0 Negative Input Select bits
`111` = AN6[1]
`110` = AN5[2]
`101` = AN4
`100` = AN3
`011` = AN2
`010` = AN1
`001` = AN0
`000` = AVSS

bit 12-8 **CH0SB[4:0]:** S/H Amplifier Positive Input Select for MUX B Multiplexer Setting bits
`11111` = Unimplemented, do not use
`11110` = AVDD[3]
`11101` = AVSS[3]
`11100` = Upper guardband rail (0.785 * VDD)
`11011` = Lower guardband rail (0.215 * VDD)
`11010` = Internal Band Gap Reference (VBG)[3]
`11000-11001` = Unimplemented, do not use
`10001` = No channels are connected, all inputs are floating (used for CTMU)
`10111` = No channels are connected, all inputs are floating (used for CTMU)
`10110` = No channels are connected, all inputs are floating (used for CTMU temperature sensor input); does not require the corresponding CTMEN22 (AD1CTMENH[6]) bit)
`10101` = Channel 0 positive input is AN21
`10100` = Channel 0 positive input is AN20
`10011` = Channel 0 positive input is AN19
`10010` = Channel 0 positive input is AN18[2]
`10001` = Channel 0 positive input is AN17[2]
•
•
•
`01001` = Channel 0 positive input is AN9
`01000` = Channel 0 positive input is AN8[1]
`00111` = Channel 0 positive input is AN7[1]
`00110` = Channel 0 positive input is AN6[1]
`00101` = Channel 0 positive input is AN5[2]
`00100` = Channel 0 positive input is AN4
`00011` = Channel 0 positive input is AN3
`00010` = Channel 0 positive input is AN2
`00001` = Channel 0 positive input is AN1
`00000` = Channel 0 positive input is AN0

Note 1: This is implemented on 44-pin devices only.
2: This is implemented on 28-pin and 44-pin devices only.
3: The band gap value used for this input is 2x or 4x the internal VBG, which is selected when PVCFG[1:0] = `1x`.

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REGISTER 19-5: AD1CHS: A/D SAMPLE SELECT REGISTER (CONTINUED)

bit 7-5 **CH0NA[2:0]:** Sample A Channel 0 Negative Input Select bits
The same definitions as for CHONB[2:0].

bit 4-0 **CH0SA[4:0]:** Sample A Channel 0 Positive Input Select bits
The same definitions as for CHONA[4:0].

Note 1: This is implemented on 44-pin devices only.
2: This is implemented on 28-pin and 44-pin devices only.
3: The band gap value used for this input is 2x or 4x the internal V_{BG}, which is selected when PVCFG[1:0] = `1x`.

REGISTER 19-6: AD1CHITH: A/D SCAN COMPARE HIT REGISTER (HIGH WORD)[1]

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH[23:16][2]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘`0`’.

bit 7-0 **CHH[23:16]:** A/D Compare Hit bits[2]
If CM[1:0] = `11`:
`1` = A/D Result Buffer x has been written with data or a match has occurred
`0` = A/D Result Buffer x has not been written with data
For All Other Values of CM[1:0]:
`1` = A match has occurred on A/D Result Channel x
`0` = No match has occurred on A/D Result Channel x

Note 1: Unimplemented channels are read as ‘`0`’.
2: The CHH[18:17] bits are not implemented in 20-pin devices.

REGISTER 19-7: AD1CHITL: A/D SCAN COMPARE HIT REGISTER (LOW WORD)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH[15:8](2,3)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH[7:0](2,3)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CHH[15:0]:** A/D Compare Hit bits(2,3)

If CM[1:0] = 11:

1 = A/D Result Buffer x has been written with data or a match has occurred

0 = A/D Result Buffer x has not been written with data

For All Other Values of CM[1:0]:

1 = A match has occurred on A/D Result Channel x

0 = No match has occurred on A/D Result Channel x

Note 1: Unimplemented channels are read as ‘0’.

2: The CHH[8:5] bits are not implemented in 20-pin devices.

3: The CHH[8:6] bits are not implemented in 28-pin devices.

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REGISTER 19-8: AD1CSSH: A/D INPUT SCAN SELECT REGISTER (HIGH WORD)(1)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	CSS[30:26]					—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS[23:16](2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-10 **CSS[30:26]:** A/D Input Scan Selection bits
1 = Includes the corresponding channel for input scan
0 = Skips the channel for input scan

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7-0 **CSS[23:16]:** A/D Input Scan Selection bits(2)
1 = Includes the corresponding channel for input scan
0 = Skips the channel for input scan

Note 1: Unimplemented channels are read as ‘0’. Do not select unimplemented channels for sampling as indeterminate results may be produced.

2: The CSS[18:17] bits are not implemented in 20-pin devices.

REGISTER 19-9: AD1CSSL: A/D INPUT SCAN SELECT REGISTER (LOW WORD)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS[15:8](2,3)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS[7:0](2,3)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CSS[15:0]:** A/D Input Scan Selection bits(2,3)
1 = Includes the corresponding ANx input for scan
0 = Skips the channel for input scan

Note 1: Unimplemented channels are read as ‘0’. Do not select unimplemented channels for sampling as indeterminate results may be produced.

2: The CSS[8:5] bits are not implemented in 20-pin devices.

3: The CSS[8:6] bits are not implemented in 28-pin devices.

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REGISTER 19-10: AD1CTMENH: CTMU ENABLE REGISTER (HIGH WORD)(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN[23:16](2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’.

bit 7-0 **CTMEN[23:16]:** CTMU Enabled During Conversion bits(2)
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

Note 1: Unimplemented channels are read as ‘0’.
2: The CTMEN[18:17] bits are not implemented in 20-pin devices.

REGISTER 19-11: AD1CTMENL: CTMU ENABLE REGISTER (LOW WORD)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN[15:8](2,3)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN[7:0](2,3)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CTMEN[15:0]:** CTMU Enabled During Conversion bits(2,3)
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

Note 1: Unimplemented channels are read as ‘0’.
2: The CTMEN[8:5] bits are not implemented in 20-pin devices.
3: The CTMEN[8:6] bits are not implemented in 28-pin devices.

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19.2 A/D Sampling Requirements

The analog input model of the 12-bit A/D Converter is shown in Figure 19-2. The total sampling time for the A/D is a function of the holding capacitor charge time.

For the A/D Converter to meet its specified accuracy, the Charge Holding Capacitor (CHOLD) must be allowed to fully charge to the voltage level on the analog input pin. The Source Impedance (RS), the Interconnect Impedance (RIC) and the Internal Sampling Switch Impedance (RSS) combine to directly affect the time required to charge CHOLD. The combined impedance of the analog sources must, therefore, be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the A/D Converter, the maximum recommended source impedance, RS, is 2.5 kΩ. After the analog input channel is selected (changed), this sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a Discharged state prior to each sample operation.

At least 1 TAD time period should be allowed between conversions for the sample time. For more details, see **Section 27.0 "Electrical Characteristics"**.

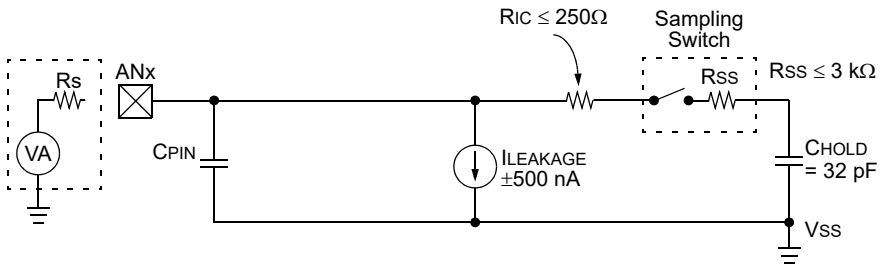
EQUATION 19-1: A/D CONVERSION CLOCK PERIOD

$$T_{AD} = T_{CY}\,(ADCS + 1)$$

$$ADCS = \frac{T_{AD}}{T_{CY}} - 1$$

Note: Based on TCY = 2/FOSC; Doze mode and PLL are disabled.

FIGURE 19-2: 12-BIT A/D CONVERTER ANALOG INPUT MODEL



Legend:
- CPIN = Input Capacitance
- VT = Threshold Voltage
- ILEAKAGE = Leakage Current at the Pin Due to Various Junctions
- RIC = Interconnect Resistance
- RSS = Sampling Switch Resistance
- CHOLD = Sample-and-Hold Capacitance (from DAC)

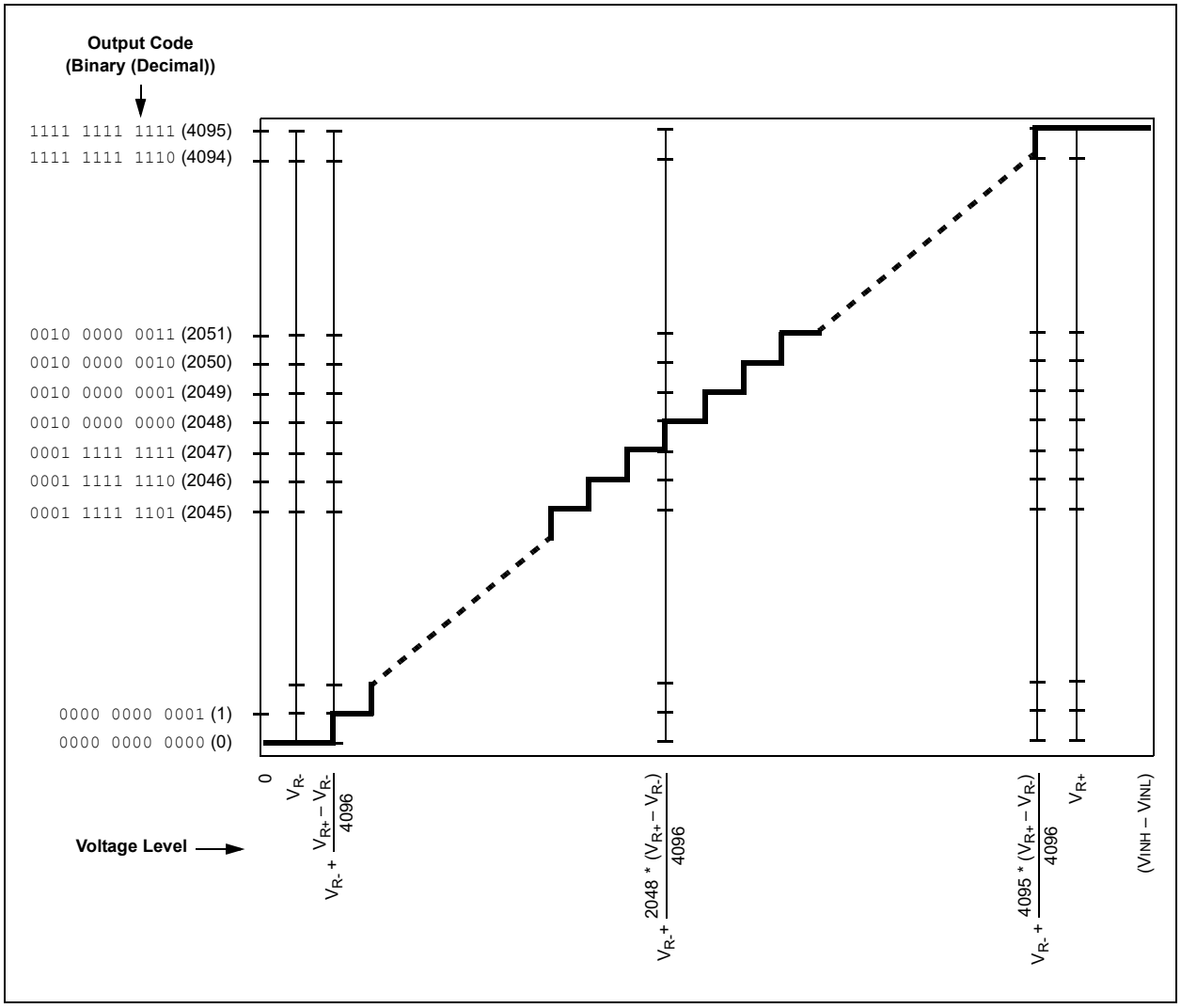
Note: The CPIN value depends on the device package and is not tested. The effect of CPIN is negligible if Rs ≤ 5 kΩ.

19.3 Transfer Function

The transfer functions of the A/D Converter in 12-bit resolution are shown in Figure 19-3. The difference of the input voltages ($V_{INH} - V_{INL}$) is compared to the reference ((V_{R+}) – (V_{R-})).

- The first code transition occurs when the input voltage is ((V_{R+}) – (V_{R-}))/4096 or 1.0 LSb.
- The '0000 0000 0001' code is centered at V_{R-} + (1.5 * ((V_{R+}) – (V_{R-}))/4096).
- The '0010 0000 0000' code is centered at V_{REFL} + (2048.5 * ((V_{R+}) – (V_{R-}))/4096).
- An input voltage less than V_{R-} + (((V_{R-}) – (V_{R-}))/4096) converts as '0000 0000 0000'.
- An input voltage greater than (V_{R-}) + (4095 ((V_{R+}) – (V_{R-}))/4096) converts as '1111 1111 1111'.

FIGURE 19-3: 12-BIT A/D TRANSFER FUNCTION



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19.4 Buffer Data Formats

The A/D conversions are fully differential 12-bit values when MODE12 = 1 (AD1CON1[10]) and 10-bit values when MODE12 = 0. When absolute fractional or absolute integer formats are used, the results are 12 or 10 bits wide, respectively. When signed decimal formatting is used, the conversion also includes a Sign bit, making 12-bit conversions 13 bits wide and 10-bit conversions 11 bits wide. The signed decimal format yields 12-bit and 10-bit values, respectively. The Sign bit (bit 12 or bit 10) is sign-extended to fill the buffer. The FORM[1:0] bits (AD1CON1[9:8]) select the format. Figure 19-4 and Figure 19-5 show the data output formats that can be selected. Table 19-1 through Table 19-4 show the numerical equivalents for the various conversion result codes.

FIGURE 19-4: A/D OUTPUT DATA FORMATS (12-BIT)

RAM Contents:					d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Read to Bus:																
Integer	0	0	0	0	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Signed Integer	s0	s0	s0	s0	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Fractional (1.15)	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0	0
Signed Fractional (1.15)	s0	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0

TABLE 19-1: NUMERICAL EQUIVALENTS OF VARIOUS RESULT CODES: 12-BIT INTEGER FORMATS

VIN/VREF	12-Bit Differential Output Code (13-bit result)	16-Bit Integer Format/ Equivalent Decimal Value		16-Bit Signed Integer Format/ Equivalent Decimal Value	
+4095/4096	0 1111 1111 1111	0000 1111 1111 1111	+4095	0000 1111 1111 1111	+4095
+4094/4096	0 1111 1111 1110	0000 1111 1111 1110	+4094	0000 1111 1111 1110	+4094
• • •					
+1/4096	0 1000 0000 0001	0000 0000 0000 0001	+1	0000 0000 0000 0001	+1
0/4096	0 0000 0000 0000	0000 0000 0000 0000	0	0000 0000 0000 0000	0
-1/4096	1 0111 1111 1111	0000 0000 0000 0000	0	1111 1111 1111 1111	-1
• • •					
-4095/4096	1 0000 0000 0001	0000 0000 0000 0000	0	1111 0000 0000 0001	-4095
-4096/4096	1 0000 0000 0000	0000 0000 0000 0000	0	1111 0000 0000 0000	-4096

TABLE 19-2: NUMERICAL EQUIVALENTS OF VARIOUS RESULT CODES: 12-BIT FRACTIONAL FORMATS

VIN/VREF	12-Bit Output Code	16-Bit Fractional Format/ Equivalent Decimal Value		16-Bit Signed Fractional Format/ Equivalent Decimal Value	
+4095/4096	0 1111 1111 1111	1111 1111 1111 0000	0.999	0111 1111 1111 1000	0.999
+4094/4096	0 1111 1111 1110	1111 1111 1110 0000	0.998	0111 1111 1110 1000	0.998
• • •					
+1/4096	0 0000 0000 0001	0000 0000 0001 0000	0.001	0000 0000 0000 1000	0.001
0/4096	0 0000 0000 0000	0000 0000 0000 0000	0.000	0000 0000 0000 0000	0.000
-1/4096	1 0111 1111 1111	0000 0000 0000 0000	0.000	1111 1111 1111 1000	-0.001
• • •					
-4095/4096	1 0000 0000 0001	0000 0000 0000 0000	0.000	1000 0000 0000 1000	-0.999
-4096/4096	1 0000 0000 0000	0000 0000 0000 0000	0.000	1000 0000 0000 0000	-1.000

FIGURE 19-5: A/D OUTPUT DATA FORMATS (10-BIT)

RAM Contents:							d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Read to Bus:																
Integer	0	0	0	0	0	0	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Signed Integer	s0	s0	s0	s0	s0	s0	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Fractional (1.15)	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0	0	0	0
Signed Fractional (1.15)	s0	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0	0	0

TABLE 19-3: NUMERICAL EQUIVALENTS OF VARIOUS RESULT CODES: 10-BIT INTEGER FORMATS

VIN/VREF	10-Bit Differential Output Code (11-bit result)	16-Bit Integer Format/ Equivalent Decimal Value		16-Bit Signed Integer Format/ Equivalent Decimal Value	
+1023/1024	011 1111 1111	0000 0011 1111 1111	1023	0000 0001 1111 1111	1023
+1022/1024	011 1111 1110	0000 0011 1111 1110	1022	0000 0001 1111 1110	1022
• • •					
+1/1024	000 0000 0001	0000 0000 0000 0001	1	0000 0000 0000 0001	1
0/1024	000 0000 0000	0000 0000 0000 0000	0	0000 0000 0000 0000	0
-1/1024	101 1111 1111	0000 0000 0000 0000	0	1111 1111 1111 1111	-1
• • •					
-1023/1024	100 0000 0001	0000 0000 0000 0000	0	1111 1110 0000 0001	-1023
-1024/1024	100 0000 0000	0000 0000 0000 0000	0	1111 1110 0000 0000	-1024

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TABLE 19-4: NUMERICAL EQUIVALENTS OF VARIOUS RESULT CODES: 10-BIT FRACTIONAL FORMATS

VIN/VREF	10-Bit Differential Output Code (11-bit result)	16-Bit Fractional Format/ Equivalent Decimal Value		16-Bit Signed Fractional Format/ Equivalent Decimal Value	
+1023/1024	011 1111 1111	1111 1111 1100 0000	0.999	0111 1111 1110 0000	0.999
+1022/1024	011 1111 1110	1111 1111 1000 0000	0.998	0111 1111 1000 0000	0.998
•••					
+1/1024	000 0000 0001	0000 0000 0100 0000	0.001	0000 0000 0010 0000	0.001
0/1024	000 0000 0000	0000 0000 0000 0000	0.000	0000 0000 0000 0000	0.000
-1/1024	101 1111 1111	0000 0000 0000 0000	0.000	1111 1111 1110 0000	-0.001
•••					
-1023/1024	100 0000 0001	0000 0000 0000 0000	0.000	1000 0000 0010 0000	-0.999
-1024/1024	100 0000 0000	0000 0000 0000 0000	0.000	1000 0000 0000 0000	-1.000

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NOTES:

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20.0 8-BIT DIGITAL-TO-ANALOG CONVERTER (DAC)

PIC24FV16KM204 family devices include two 8-bit Digital-to-Analog Converters (DACs) for generating analog outputs from digital data. A simplified block diagram for a single DAC is shown in Figure 20-1. Both of the DACs are identical.

The DAC generates an analog output voltage based on the digital input code, according to the formula:

$$V_{DAC} = \frac{V_{DACREF} \times DACxDAT}{256}$$

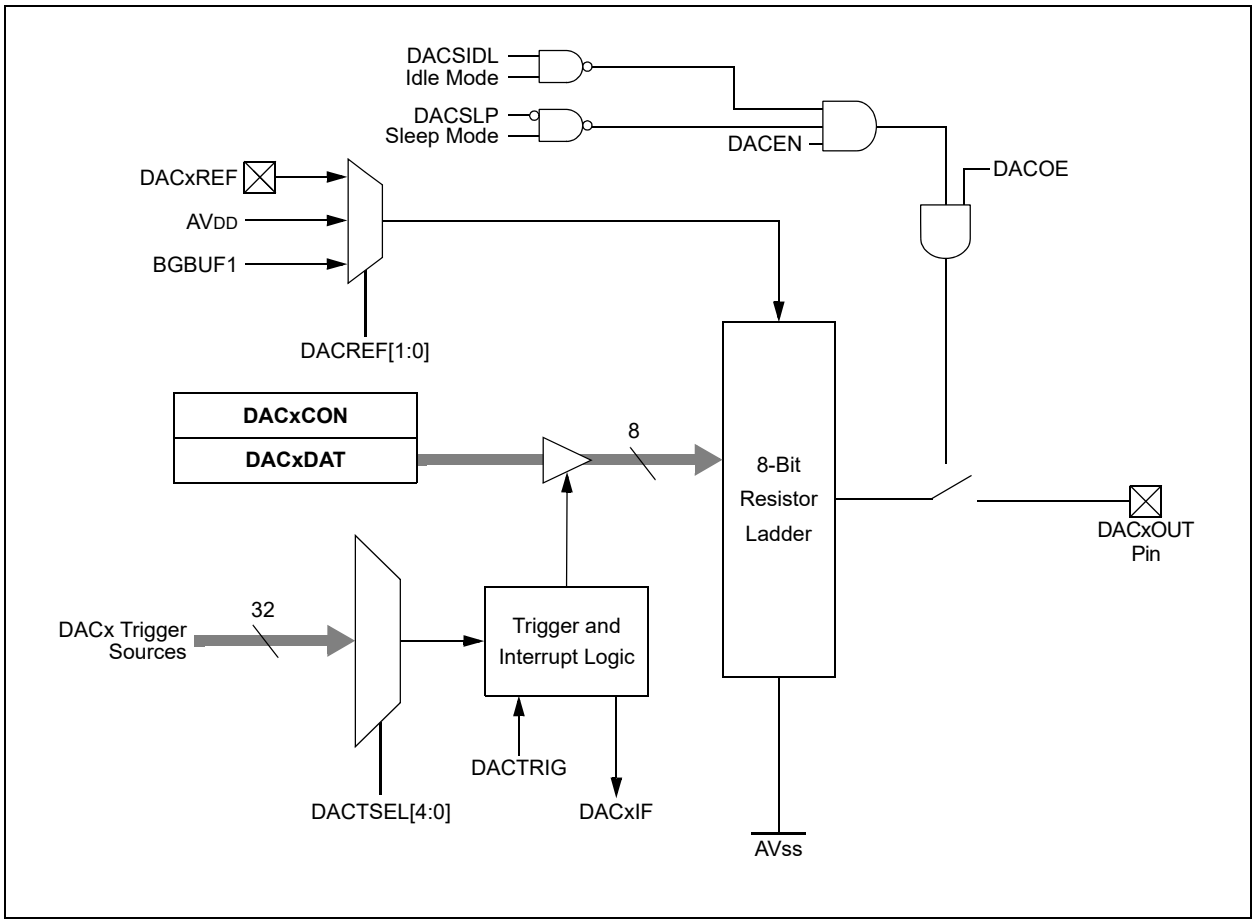
where V_{DAC} is the analog output voltage and V_{DACREF} is the reference voltage selected by DACREF[1:0].

Each DAC includes these features:

- Precision 8-Bit Resistor Ladder for High Accuracy
- Fast Settling Time, Supporting 1 Msps Effective Sampling Rates
- Three User-Selectable Voltage Reference Options
- Multiple Conversion Trigger Options, Plus a Manual Convert-on-Write Option
- Left and Right Justified Input Data Options
- User-Selectable Sleep and Idle Mode Operation

When using the DAC, it is recommended to set the ANSx and TRISx bits for the DACx output pin to configure it as an analog output. See **Section 11.2 "Configuring Analog Port Pins"** for more information.

FIGURE 20-1: SINGLE DACx SIMPLIFIED BLOCK DIAGRAM



REGISTER 20-1: DACxCON: DACx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
DACEN	—	DACSIDL	DACSLP	DACFM	—	SRDIS	DACTRIG
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACOE	DACTSEL4	DACTSEL3	DACTSEL2	DACTSEL1	DACTSEL0	DACREF1	DACREF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DACEN:** DACx Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **DACSIDL:** DACx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **DACSLP:** DACx Enable Peripheral During Sleep bit
1 = DACx continues to output the most recent value of DACxDAT during Sleep mode
0 = DACx is powered down in Sleep mode; DACxOUT pin is controlled by the TRISx and LATx bits

bit 11 **DACFM:** DACx Data Format Select bit
1 = Data are left justified (data stored in DACxDAT[15:8])
0 = Data are right justified (data stored in DACxDAT[7:0])

bit 10 **Unimplemented:** Read as ‘0’

bit 9 **SRDIS:** Soft Reset Disable bit
1 = DACxCON and DACxDAT SFRs reset only on a POR or BOR Reset
0 = DACxCON and DACxDAT SFRs reset on any type of device Reset

bit 8 **DACTRIG:** DACx Trigger Input Enable bit
1 = Analog output value updates when the selected (by DACTSEL[4:0]) event occurs
0 = Analog output value updates as soon as DACxDAT is written (DAC Trigger is ignored)

bit 7 **DACOE:** DACx Output Enable bit
1 = DACx output pin is enabled and driven on the DACxOUT pin
0 = DACx output pin is disabled, DACx output is available internally to other peripherals only

Note 1: BGBUF1 voltage is configured by BUFREF[1:0] (BUFCON0[1:0]).

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REGISTER 20-1: DACxCON: DACx CONTROL REGISTER (CONTINUED)

bit 6-2 **DACTSEL[4:0]:** DACx Trigger Source Select bits
11101-11111 = Unused
11100 = CTMU
11011 = A/D
11010 = Comparator 3
11001 = Comparator 2
11000 = Comparator 1
10011 to 10111 = Unused
10010 = CLC2 output
10001 = CLC1 output
01100 to 10000 = Unused
01011 = Timer1 Sync output
01010 = External Interrupt 2
01001 = External Interrupt 1
01000 = External Interrupt 0
0011x = Unused
00101 = MCCP5 or SCCP5 Sync output
00100 = MCCP4 or SCCP4 Sync output
00011 = MCCP3 or SCCP3 Sync output
00010 = MCCP2 or SCCP2 Sync output
00001 = MCCP1 or SCCP1 Sync output
00000 = Unused

bit 1-0 **DACREF[1:0]:** DACx Reference Source Select bits
11 = Internal Band Gap Buffer 1 (BGBUF1)(1)
10 = AV_{DD}
01 = DV_{REF+}
00 = Reference is not connected (lowest power but no DAC functionality)

Note 1: BGBUF1 voltage is configured by BUFREF[1:0] (BUFCON0[1:0]).

REGISTER 20-2: BUFCON0: INTERNAL VOLTAGE REFERENCE CONTROL REGISTER 0

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-1
—	—	—	—	—	—	BUFREF[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1-0 **BUFREF[1:0]:** Internal Voltage Reference Select bits
- 11 = Reference output is set at 4 * BGBUF1[(1)]
- 10 = Reference output is set at 2 * BGBUF1[(2)]
- 01 = Reference output is set at BGBUF1
- 00 = Reserved, do not use

Note 1: Available only on PIC24FV16KMXXX devices. The reference may not be within specifications for VDD below specified levels; see Table 27-15 for minimum VDD limits.

2: The reference may not be within specifications for VDD below specified levels; see Table 27-15 for minimum VDD limits.

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21.0 DUAL OPERATIONAL AMPLIFIER MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Operational Amplifier (Op Amp)"** (www.microchip.com/DS30505) in the *"dsPIC33/PIC24F Family Reference Manual"*. Device-specific information in this data sheet supersedes the information in the *"dsPIC33/PIC24F Family Reference Manual"*.

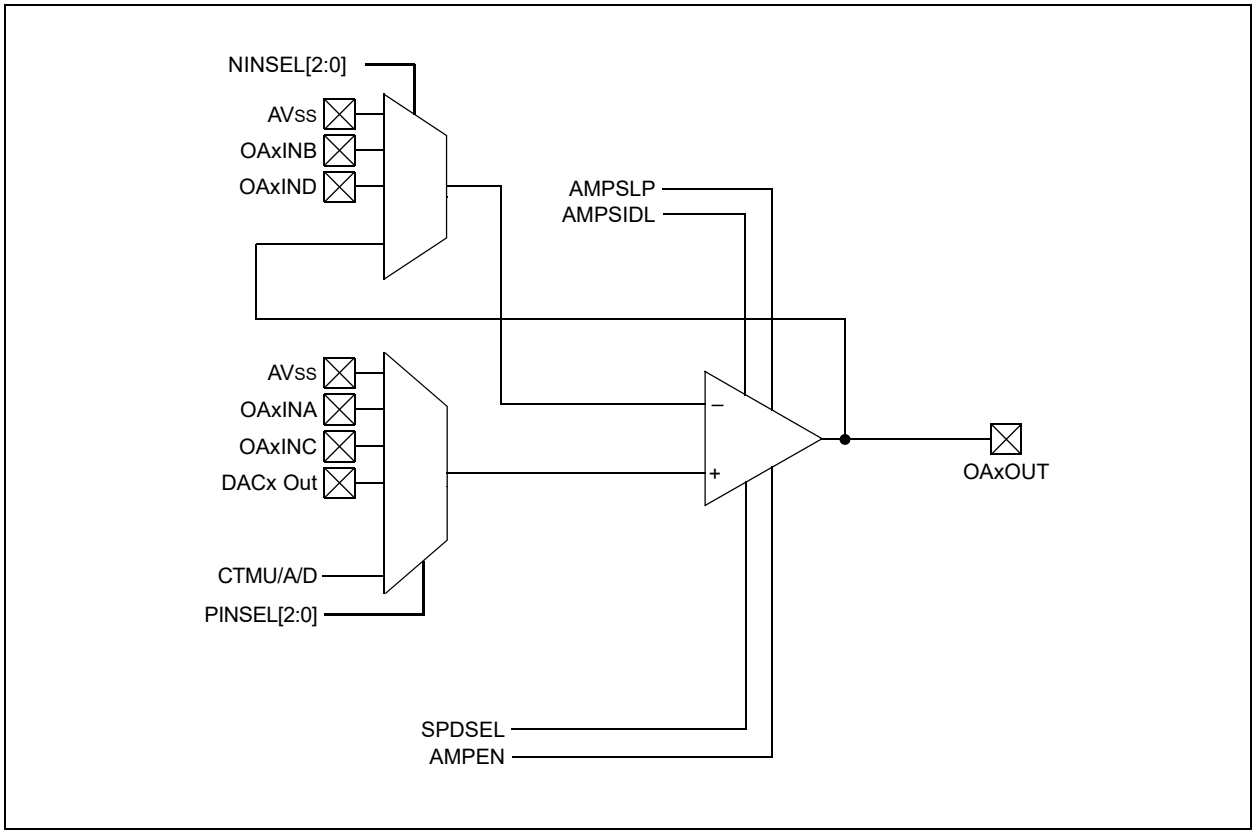
PIC24FV16KM204 family devices include two operational amplifiers to complement the microcontroller's other analog features. They may be used to provide analog signal conditioning, either as stand-alone devices or in addition to other analog peripherals.

The two op amps are functionally identical; the block diagram for a single amplifier is shown in Figure 21-1. Each op amp has these features:

- Internal Unity Gain Buffer Option
- Multiple Input Options Each on the Inverting and Noninverting Amplifier Inputs
- Rail-to-Rail Input and Output Capabilities
- User-Selectable Option for Regular or Low-Power Operation
- User-Selectable Operation in Idle and Sleep Modes

When using the op amps, it is recommended to set the ANSx and TRISx bits of both the input and output pins to configure them as analog pins. See **Section 11.2 "Configuring Analog Port Pins"** for more information.

FIGURE 21-1: SINGLE OPERATIONAL AMPLIFIER BLOCK DIAGRAM



REGISTER 21-1: AMPxCON: OP AMP x CONTROL REGISTER[1]

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **AMPEN:** Op Amp x Control Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **AMPSIDL:** Op Amp x Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **AMPSLP:** Op Amp x Peripheral Enabled in Sleep Mode bit
1 = Continues module operation when device enters Sleep mode
0 = Discontinues module operation in Sleep mode

bit 11-8 **Unimplemented:** Read as ‘0’

bit 7 **SPDSEL:** Op Amp x Power/Speed Select bit
1 = Higher power and bandwidth (faster response time)
0 = Lower power and bandwidth (slower response time)

bit 6 **Unimplemented:** Read as ‘0’

bit 5-3 **NINSEL[2:0]:** Negative Op Amp Input Select bits
111 = Reserved; do not use
110 = Reserved; do not use
101 = Op amp negative input is connected to the op amp output (voltage follower)
100 = Reserved; do not use
011 = Reserved; do not use
010 = Op amp negative input is connected to the OAxIND pin
001 = Op amp negative input is connected to the OAxINB pin
000 = Op amp negative input is connected to AVSS

bit 2-0 **PINSEL[2:0]:** Positive Op Amp Input Select bits
111 = Op amp positive input is connected to the output of the A/D input multiplexer
110 = Reserved; do not use
101 = Op amp positive input is connected to the DAC1 output for OA1 (DAC2 output for OA2)
100 = Reserved; do not use
011 = Reserved; do not use
010 = Op amp positive input is connected to the OAxINC pin
001 = Op amp positive input is connected to the OAxINA pin
000 = Op amp positive input is connected to AVSS

Note 1: This register is available only on PIC24F(V)16KM2XX devices.

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22.0 COMPARATOR MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator module, refer to **"Scalable Comparator Module"** (www.microchip.com/DS39734) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of four external analog inputs, as well as a voltage reference input from either the Internal Band Gap Buffer 1 (BGBUF1) or the comparator voltage reference generator.

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 22-1. Diagrams of the possible individual comparator configurations are shown in Figure 22-2.

Each comparator has its own control register, CMxCON (Register 22-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 22-2).

FIGURE 22-1: COMPARATOR x MODULE BLOCK DIAGRAM

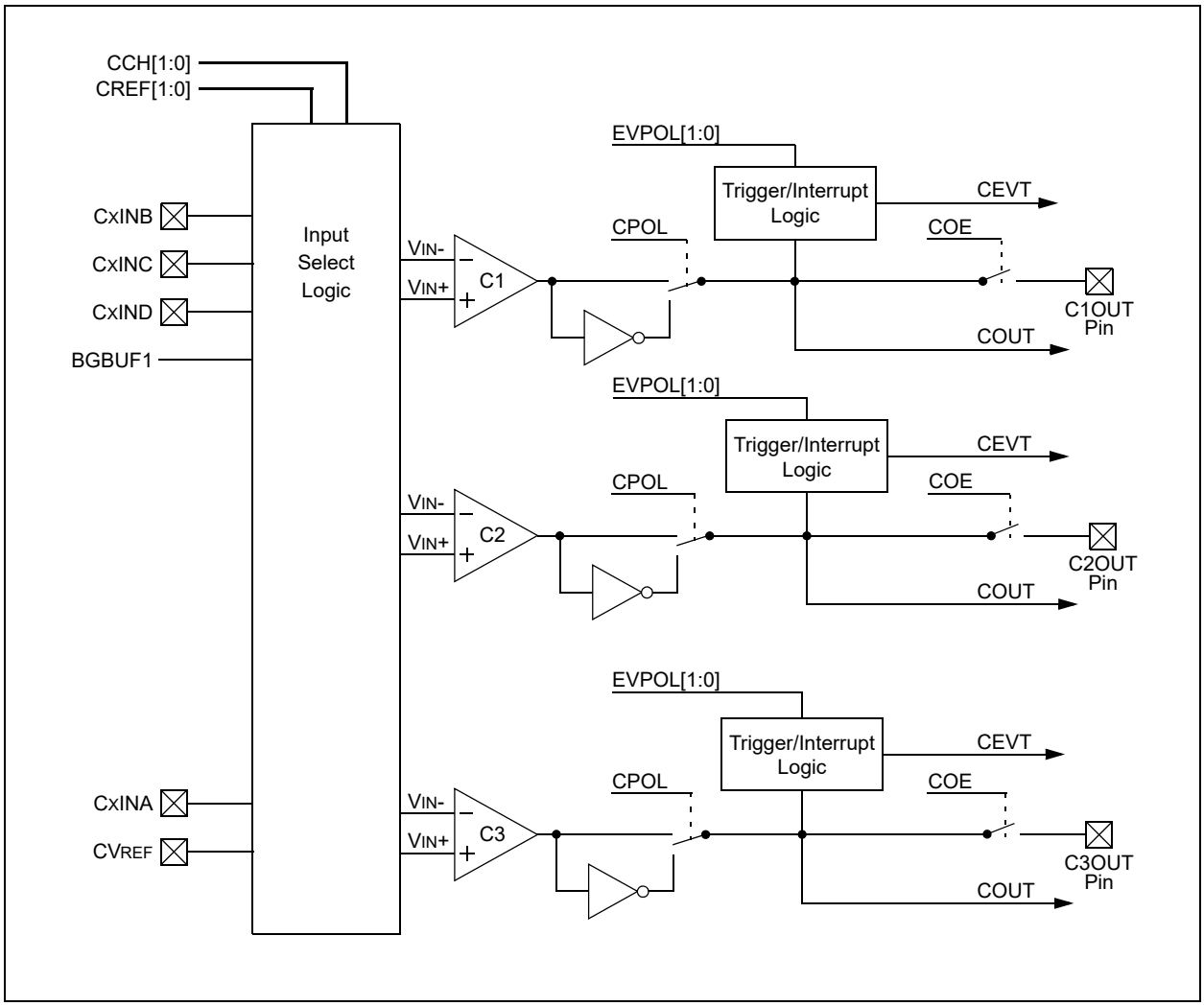
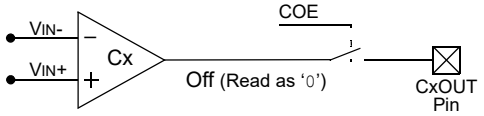
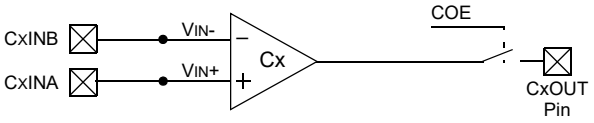


FIGURE 22-2: INDIVIDUAL COMPARATOR CONFIGURATIONS

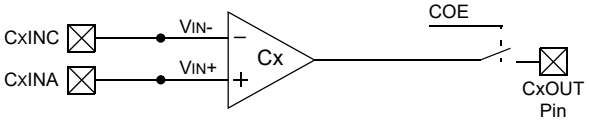
Comparator Off
CON = 0, CREF[1:0] = xx, CCH[1:0] = xx



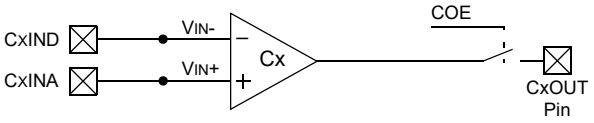
Comparator CxINB > CxINA Compare
CON = 1, CREF[1:0] = 00, CCH[1:0] = 00



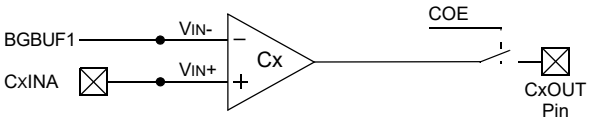
Comparator CxINC > CxINA Compare
CON = 1, CREF[1:0] = 00, CCH[1:0] = 01



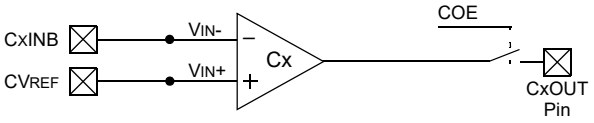
Comparator CxIND > CxINA Compare
CON = 1, CREF[1:0] = 00, CCH[1:0] = 10



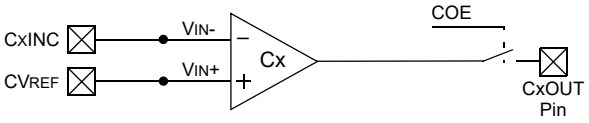
Comparator BGBUF1 > CxINA Compare
CON = 1, CREF[1:0] = 00, CCH[1:0] = 11



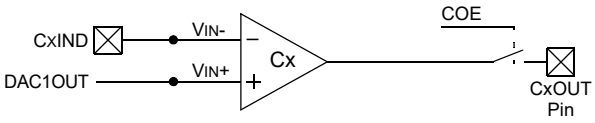
Comparator CxINB > CVREF Compare
CON = 1, CREF[1:0] = 01, CCH[1:0] = 00



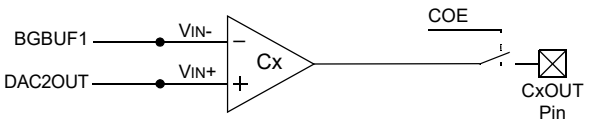
Comparator CxINC > CVREF Compare
CON = 1, CREF[1:0] = 01, CCH[1:0] = 01



Comparator CxIND > DAC1OUT Compare
CON = 1, CREF[1:0] = 10, CCH[1:0] = 10



Comparator BGBUF1 > DAC2OUT Compare
CON = 1, CREF[1:0] = 11, CCH[1:0] = 11



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REGISTER 22-1: CMxCON: COMPARATOR x CONTROL REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	CLPWR	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1[2]	EVPOL0[2]	CREF1	CREF0	—	—	CCH1	CCH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Comparator x Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator x Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator x Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12 **CLPWR:** Comparator x Low-Power Mode Select bit
1 = Comparator operates in Low-Power mode
0 = Comparator does not operate in Low-Power mode

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9 **CEVT:** Comparator x Event bit
1 = Comparator event, defined by EVPOL[1:0], has occurred; subsequent Triggers and interrupts are disabled until the bit is cleared
0 = Comparator event has not occurred

bit 8 **COUT:** Comparator x Output bit
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

bit 7-6 **EVPOL[1:0]:** Trigger/Event/Interrupt Polarity Select bits[2]
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on the high-to-low transition of the comparator output
01 = Trigger/event/interrupt is generated on the low-to-high transition of the comparator output
00 = Trigger/event/interrupt generation is disabled

bit 5-4 **CREF[1:0]:** Comparator x Reference Select bits (noninverting input)
11 = Noninverting input connects to the DAC2 output
10 = Noninverting input connects to the DAC1 output
01 = Noninverting input connects to the internal CV_{REF} voltage
00 = Noninverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as ‘0’

Note 1: BGBUF1 voltage is configured by BUFREF1[1:0] (BUFCON0[1:0]).
2: If the EVPOL[1:0] bits are set to a value other than ‘00’, the first interrupt generated will occur on any transition of COUT. Subsequent interrupts will occur based on the EVPOLx bits setting.

REGISTER 22-1: CMxCON: COMPARATOR x CONTROL REGISTERS (CONTINUED)

bit 1-0 **CCH[1:0]:** Comparator x Channel Select bits
`11` = Inverting input of the comparator connects to BGBUF1[(1)]
`10` = Inverting input of the comparator connects to the CxIND pin
`01` = Inverting input of the comparator connects to the CxINC pin
`00` = Inverting input of the comparator connects to the CxINB pin

Note 1: BGBUF1 voltage is configured by BUFREF1[1:0] (BUFCON0[1:0]).
2: If the EVPOL[1:0] bits are set to a value other than '`00`', the first interrupt generated will occur on any transition of COUT. Subsequent interrupts will occur based on the EVPOLx bits setting.

REGISTER 22-2: CMSTAT: COMPARATOR MODULE STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
CMIDL	—	—	—	—	C3EVT[(1)]	C2EVT[(1)]	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
—	—	—	—	—	C3OUT[(1)]	C2OUT[(1)]	C1OUT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL:** Comparator x Stop in Idle Mode bit
`1` = Comparator interrupts are disabled in Idle mode; enabled comparators remain operational
`0` = Continues operation of all enabled comparators in Idle mode

bit 14-11 **Unimplemented:** Read as '`0`'

bit 10 **C3EVT:** Comparator 3 Event Status bit (read-only)[(1)]
Shows the current event status of Comparator 3 (CM3CON[9]).

bit 9 **C2EVT:** Comparator 2 Event Status bit (read-only)[(1)]
Shows the current event status of Comparator 2 (CM2CON[9]).

bit 8 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON[9]).

bit 7-3 **Unimplemented:** Read as '`0`'

bit 2 **C3OUT:** Comparator 3 Output Status bit (read-only)[(1)]
Shows the current output of Comparator 3 (CM3CON[8]).

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)[(1)]
Shows the current output of Comparator 2 (CM2CON[8]).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON[8]).

Note 1: Comparator 2 and Comparator 3 are only available on PIC24F(V)16KM2XX devices.

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23.0 COMPARATOR VOLTAGE REFERENCE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator Voltage Reference, refer to **"Comparator Voltage Reference Module"** (www.microchip.com/DS39709) in the *"dsPIC33/PIC24F Family Reference Manual"*.

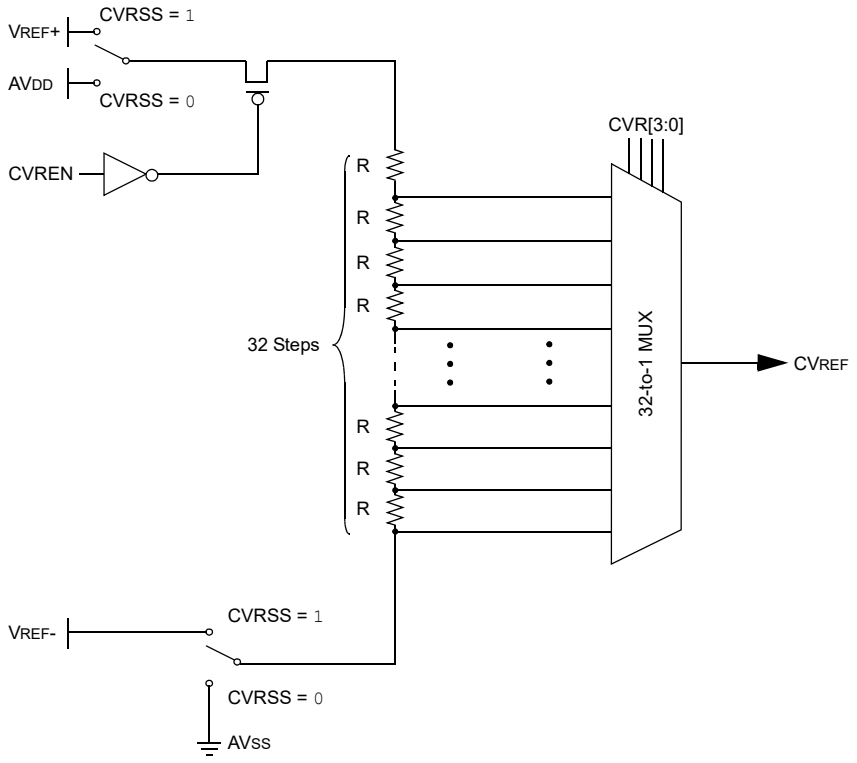
23.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCON register (Register 23-1). The comparator voltage reference provides a range of output voltages with 32 distinct levels.

The comparator voltage reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON[5]).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 23-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



REGISTER 23-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = CV_{REF} circuit is powered on
0 = CV_{REF} circuit is powered down

bit 6 **CVROE:** Comparator V_{REF} Output Enable bit
1 = CV_{REF} voltage level is output on the CV_{REF} pin
0 = CV_{REF} voltage level is disconnected from the CV_{REF} pin

bit 5 **CVRSS:** Comparator V_{REF} Source Selection bit
1 = Comparator reference source, $CV_{RSRC} = V_{REF}+ – V_{REF}-$
0 = Comparator reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 4-0 **CVR[4:0]:** Comparator V_{REF} Value Selection 0 ≤ CVR[4:0] ≤ 31 bits
When CVRSS = 1:
$CV_{REF} = (V_{REF}-) + (CVR[4:0]/32) \cdot (V_{REF}+ – V_{REF}-)$
When CVRSS = 0:
$CV_{REF} = (AV_{SS}) + (CVR[4:0]/32) \cdot (AV_{DD} – AV_{SS})$

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24.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Charge Time Measurement Unit, refer to **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (www.microchip.com/DS30009743) in the *"dsPIC33/PIC24F Family Reference Manual"*.

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides charge measurement, accurate differential time measurement between pulse sources and asynchronous pulse generation. Its key features include:

- Thirteen External Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edge Levels or Edge Transitions
- Time Measurement Resolution of One Nanosecond
- Accurate Current Source Suitable for Capacitive Measurement

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock. The CTMU module is ideal for interfacing with capacitive-based touch sensors.

The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 enables the module and controls the mode of operation of the CTMU, as well as controlling edge sequencing. CTMUCON2 controls edge source selection and edge source polarity selection. The CTMUICON register selects the current range of current source and trims the current.

24.1 Measuring Capacitance

The CTMU module measures capacitance by generating an output pulse, with a width equal to the time between edge events, on two separate input channels. The pulse edge events to both input channels can be selected from several internal peripheral modules (OC1, Timer1, any input capture or comparator module) and up to 13 external pins (CTED1 through CTED13). This pulse is used with the module's precision current source to calculate capacitance according to the relationship:

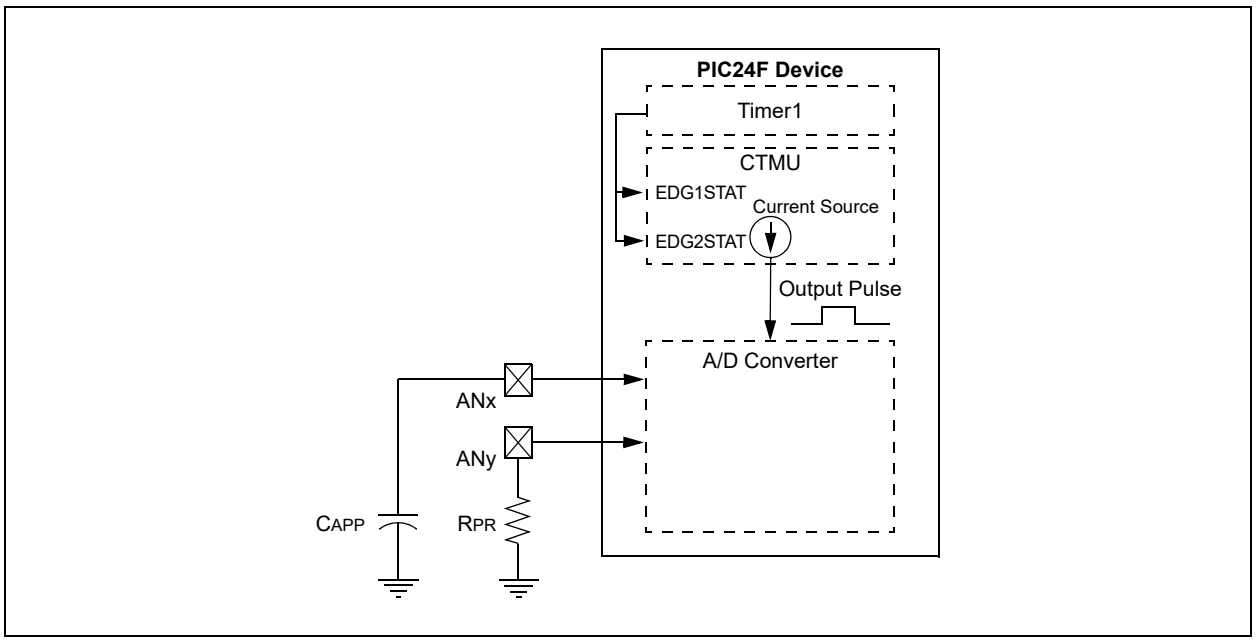
EQUATION 24-1:

$$I = C \cdot \frac{dV}{dT}$$

For capacitance measurements, the A/D Converter samples an External Capacitor (C_{APP}) on one of its input channels after the CTMU output's pulse. A Precision Resistor (R_{PR}) provides current source calibration on a second A/D channel. After the pulse ends, the converter determines the voltage on the capacitor. The actual calculation of capacitance is performed in software by the application.

Figure 24-1 illustrates the external connections used for capacitance measurements, and how the CTMU and A/D modules are related in this application. This example also shows the edge events coming from Timer1, but other configurations using external edge sources are possible. A detailed discussion on measuring capacitance and time with the CTMU module is provided in the *"dsPIC33/PIC24F Family Reference Manual"*.

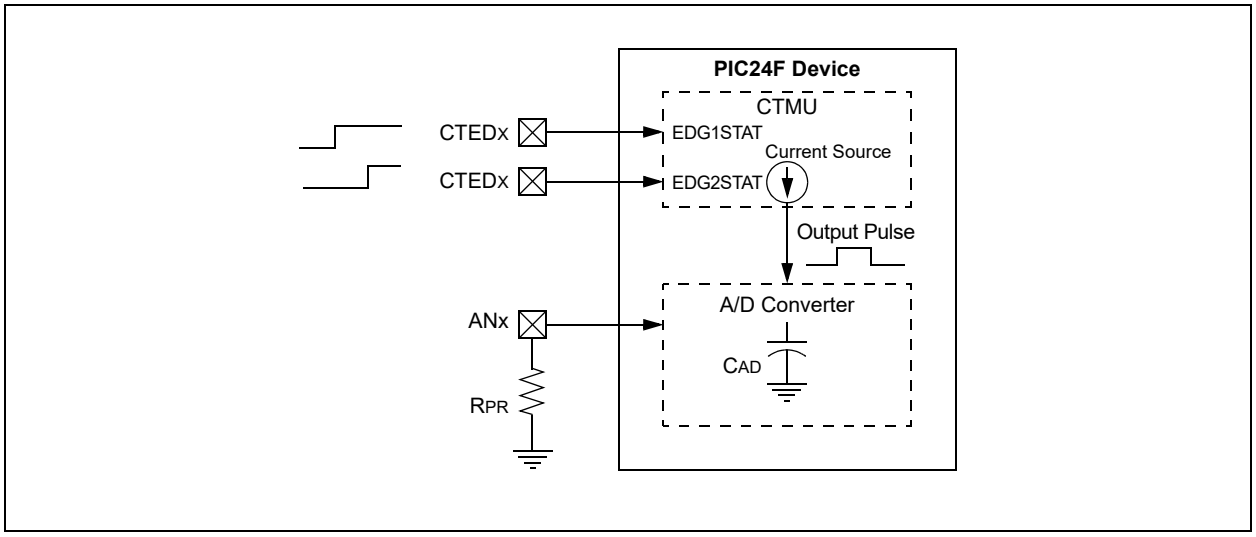
FIGURE 24-1: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR CAPACITANCE MEASUREMENT



24.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's Internal Capacitor (CAD) and a precision resistor for current calibration. Figure 24-2 displays the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTEDx pins, but other configurations using internal edge sources are possible.

FIGURE 24-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT



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24.3 Pulse Generation and Delay

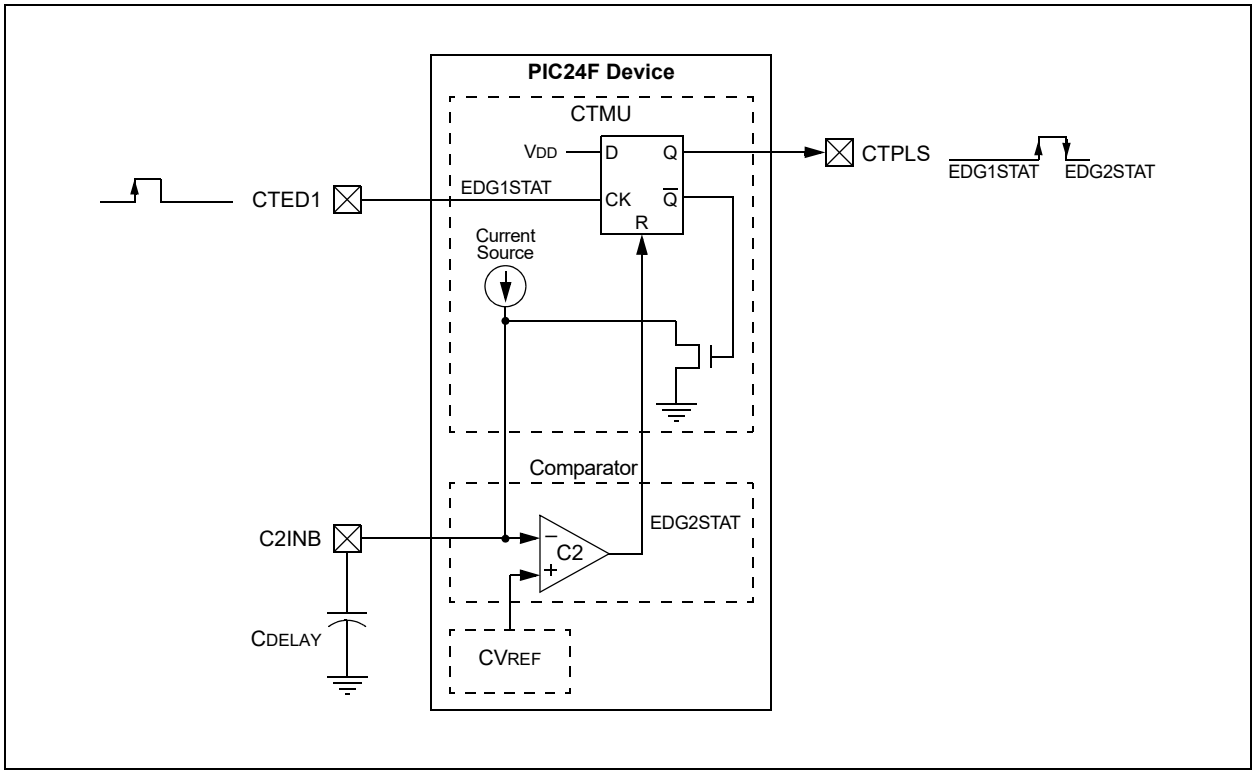
The CTMU module can also generate an output pulse with edges that are not synchronous with the device's system clock. More specifically, it can generate a pulse with a programmable delay from an edge event input to the module.

When the module is configured for pulse generation delay by setting the TGEN bit (CTMUCON1L[12]), the internal current source is connected to the B input of Comparator 2. A capacitor (C_{DELAY}) is connected to the Comparator 2 pin, C2INB, and the Comparator Voltage Reference, CV_{REF}, is connected to C2INA. CV_{REF} is then configured for a specific trip point. The module begins to charge C_{DELAY} when an edge event is detected. While CV_{REF} is greater than the voltage on C_{DELAY}, the CTPLS pin is high.

When the voltage on C_{DELAY} equals CV_{REF}, CTPLS goes low. With Comparator 2 configured as the second edge, this stops the CTMU from charging. In this state event, the CTMU automatically connects to ground. The IDISSEN bit doesn't need to be set and cleared before the next CTPLS cycle.

Figure 24-3 illustrates the external connections for pulse generation, as well as the relationship of the different analog modules required. While CTED1 is shown as the input pulse source, other options are available. A detailed discussion on pulse generation with the CTMU module is provided in the *"dsPIC33/PIC24F Family Reference Manual"*.

FIGURE 24-3: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR PULSE DELAY GENERATION



REGISTER 24-1: CTMUCON1L: CTMU CONTROL 1 LOW REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** CTMU Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM[5:0]:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG[1:0]
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG[1:0]:** Current Source Range Select bits
11 = 100 × Base Current
10 = 10 × Base Current
01 = Base Current Level (0.55 µA nominal)
00 = 1000 × Base Current

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REGISTER 24-2: CTMUCON1H: CTMU CONTROL 1 HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL[3:0]:** Edge 1 Source Select bits
1111 = Edge 1 source is the Comparator 3 output
1110 = Edge 1 source is the Comparator 2 output
1101 = Edge 1 source is the Comparator 1 output
1100 = Edge 1 source is CLC2
1011 = Edge 1 source is CLC1
1010 = Edge 1 source is the MCCP2 Compare Event Flag (CCP2IF)
1001 = Edge 1 source is CTED8(1)
1000 = Edge 1 source is CTED7(1)
0111 = Edge 1 source is CTED6
0110 = Edge 1 source is CTED5
0101 = Edge 1 source is CTED4
0100 = Edge 1 source is CTED3(2)
0011 = Edge 1 source is CTED1
0010 = Edge 1 source is CTED2
0001 = Edge 1 source is the MCCP1 Compare Event Flag (CCP1IF)
0000 = Edge 1 source is Timer1

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the current source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the current source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge
0 = Edge 2 is programmed for a negative edge

Note 1: Edge sources, CTED7 and CTED8, are not available on 28-pin and 20-pin devices.
2: Edge sources, CTED3, CTED9 and CTED11, are not available on 20-pin devices.

REGISTER 24-2: CTMUCON1H: CTMU CONTROL 1 HIGH REGISTER (CONTINUED)

bit 5-2 **EDG2SEL[3:0]:** Edge 2 Source Select bits

1111 = Edge 2 source is the Comparator 3 output
1110 = Edge 2 source is the Comparator 2 output
1101 = Edge 2 source is the Comparator 1 output
1100 = Unimplemented; do not use
1011 = Edge 2 source is CLC1
1010 = Edge 2 source is the MCCP2 Compare Event Flag (CCP2IF)
1001 = Unimplemented; do not use
1000 = Edge 2 source is CTED13
0111 = Edge 2 source is CTED12
0110 = Edge 2 source is CTED11(2)
0101 = Edge 2 source is CTED10
0100 = Edge 2 source is CTED9(2)
0011 = Edge 2 source is CTED1
0010 = Edge 2 source is CTED2
0001 = Edge 2 source is the MCCP1 Compare Event Flag (CCP1IF)
0000 = Edge 2 source is Timer1

bit 1-0 **Unimplemented:** Read as '0'

Note 1: Edge sources, CTED7 and CTED8, are not available on 28-pin and 20-pin devices.
2: Edge sources, CTED3, CTED9 and CTED11, are not available on 20-pin devices.

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REGISTER 24-3: CTMUCON2L: CTMU CONTROL 2 LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	IRSTEN	—	DISCHS2	DISCHS1	DISCHS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **IRSTEN:** CTMU Current Source Reset Enable bit
- 1 = Signal selected by the DISCHS[2:0] bits or the IDISSEN control bit will reset the CTMU edge detect logic
- 0 = CTMU edge detect logic will not occur

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DISCHS[2:0]:** Discharge Source Select bits
- 111 = CLC2 output
- 110 = CLC1 output
- 101 = Reserved; do not use.
- 100 = A/D end of conversion signal
- 011 = SCCP5 auxiliary output
- 110 = MCCP2 auxiliary output
- 001 = MCCP1 auxiliary output
- 000 = No discharge source selected, use the IDISSEN bit

NOTES:

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25.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Watchdog Timer, High-Level Device Integration and Programming Diagnostics, refer to the individual sections of the *"dsPIC33/PIC24F Family Reference Manual"* provided below:

- **"Watchdog Timer (WDT)"** (www.microchip.com/DS39697)
- **"Programming and Diagnostics"** (www.microchip.com/DS39716)

PIC24FXXXXX family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

25.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped, starting at program memory location, F80000h. A complete list of Configuration register locations is provided in Table 25-1. A detailed explanation of the various bit functions is provided in Register 25-1 through Register 25-9.

The address, F80000h, is beyond the user program memory space. In fact, it belongs to the configuration memory space (800000h-FFFFFFh), which can only be accessed using Table Reads and Table Writes.

TABLE 25-1: CONFIGURATION REGISTERS LOCATIONS

Configuration Register	Address
FBS	F80000
FGS	F80004
FOSCSEL	F80006
FOSC	F80008
FWDT	F8000A
FPOR	F8000C
FICD	F8000E

REGISTER 25-1: FBS: BOOT SEGMENT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	BSS2	BSS1	BSS0	BWRP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-1 **BSS[2:0]:** Boot Segment Program Flash Code Protection bits
111 = No boot program Flash segment
011 = Reserved
110 = Standard security, boot program Flash segment starts at 200h, ends at 000AFEh
010 = High-security, boot program Flash segment starts at 200h, ends at 000AFEh
101 = Standard security, boot program Flash segment starts at 200h, ends at 0015FEh(1)
001 = High-security, boot program Flash segment starts at 200h, ends at 0015FEh(1)
100 = Reserved
000 = Reserved

bit 0 **BWRP:** Boot Segment Program Flash Write Protection bit
1 = Boot Segment may be written
0 = Boot Segment is write-protected

Note 1: This selection should not be used in PIC24FV08KMXXX devices.

REGISTER 25-2: FGS: GENERAL SEGMENT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
—	—	—	—	—	—	GCP	GWRP
bit 7							bit 0

Legend:			
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **GCP:** General Segment Code Flash Code Protection bit
1 = No protection
0 = Standard security is enabled

bit 0 **GWRP:** General Segment Code Flash Write Protection bit
1 = General Segment may be written
0 = General Segment is write-protected

REGISTER 25-3: FOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1
IESO	LPRCSEL	SOSCSRC	—	—	FNOSC2	FNOSC1	FNOSC0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **LPRCSEL:** Internal LPRC Oscillator Power Select bit
1 = High-Power/High-Accuracy mode
0 = Low-Power/Low-Accuracy mode

bit 5 **SOSCSRC:** Secondary Oscillator Clock Source Configuration bit
1 = SOSC analog crystal function is available on the SOSCI/SOSCO pins
0 = SOSC crystal is disabled; digital SCLKI function is selected on the SOSCO pin

bit 4-3 **Unimplemented:** Read as ‘0’

bit 2-0 **FNOSC[2:0]:** Oscillator Selection bits
000 = Fast RC Oscillator (FRC)
001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCDIV+PLL)
010 = Primary Oscillator (XT, HS, EC)
011 = Primary Oscillator with PLL module (HS+PLL, EC+PLL)
100 = Secondary Oscillator (SOSC)
101 = Low-Power RC Oscillator (LPRC)
110 = 500 kHz Low-Power FRC Oscillator with Divide-by-N (LPFRCDIV)
111 = 8 MHz FRC Oscillator with Divide-by-N (FRCDIV)

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REGISTER 25-4: FOSC: OSCILLATOR CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCKSM1	FCKSM0	SOSCSEL	POSCFREQ1	POSCFREQ0	OSCIOFNC	POSCMOD1	POSCMOD0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **FCKSM[1:0]:** Clock Switching and Fail-Safe Clock Monitor Selection Configuration bits
`1x` = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
`01` = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
`00` = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5 **SOSCSEL:** Secondary Oscillator Power Selection Configuration bit
`1` = Secondary Oscillator is configured for high-power operation
`0` = Secondary Oscillator is configured for low-power operation

bit 4-3 **POSCFREQ[1:0]:** Primary Oscillator Frequency Range Configuration bits
`11` = Primary Oscillator/External Clock input frequency is greater than 8 MHz
`10` = Primary Oscillator/External Clock input frequency is between 100 kHz and 8 MHz
`01` = Primary Oscillator/External Clock input frequency is less than 100 kHz
`00` = Reserved; do not use

bit 2 **OSCIOFNC:** CLKO Enable Configuration bit
`1` = CLKO output signal is active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock (EC) mode for the CLKO to be active (POSCMOD[1:0] = `11` or `00`)
`0` = CLKO output is disabled

bit 1-0 **POSCMOD[1:0]:** Primary Oscillator Configuration bits
`11` = Primary Oscillator mode is disabled
`10` = HS Oscillator mode is selected
`01` = XT Oscillator mode is selected
`00` = External Clock mode is selected

REGISTER 25-5: FWDT: WATCHDOG TIMER CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FWDTEN1	WINDIS	FWDTEN0	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7,5 **FWDTEN[1:0]:** Watchdog Timer Enable bits
- `11` = WDT is enabled in hardware
- `10` = WDT is controlled with the SWDTEN bit setting
- `01` = WDT is enabled only while the device is active, WDT is disabled in Sleep; SWDTEN bit is disabled
- `00` = WDT is disabled in hardware; SWDTEN bit is disabled

bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
- `1` = Standard WDT is selected; windowed WDT is disabled
- `0` = Windowed WDT is enabled; note that executing a `CLRWDT` instruction while the WDT is disabled in hardware and software (FWDTEN[1:0] = `00` and SWDTEN (RCON[5]) = `0`) will not cause a device Reset

bit 4 **FWPSA:** WDT Prescaler bit
- `1` = WDT prescaler ratio of 1:128
- `0` = WDT prescaler ratio of 1:32

bit 3-0 **WDTPS[3:0]:** Watchdog Timer Postscale Select bits
- `1111` = 1:32,768
- `1110` = 1:16,384
- `1101` = 1:8,192
- `1100` = 1:4,096
- `1011` = 1:2,048
- `1010` = 1:1,024
- `1001` = 1:512
- `1000` = 1:256
- `0111` = 1:128
- `0110` = 1:64
- `0101` = 1:32
- `0100` = 1:16
- `0011` = 1:8
- `0010` = 1:4
- `0001` = 1:2
- `0000` = 1:1

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REGISTER 25-6: FPOR: RESET CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
MCLRE(2)	BORV1(3)	BORV0(3)	I2C1SEL(1)	PWRTEN	RETCFG(1)	BOREN1	BOREN0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **MCLRE:** $\overline{\text{MCLR}}$ Pin Enable bit(2)
1 = $\overline{\text{MCLR}}$ pin is enabled; RA5 input pin is disabled
0 = RA5 input pin is enabled; $\overline{\text{MCLR}}$ is disabled

bit 6-5 **BORV[1:0]:** Brown-out Reset Voltage Level bits(3)
11 = Brown-out Reset is set to the lowest voltage
10 = Brown-out Reset is set to the middle voltage
01 = Brown-out Reset is set to the highest voltage
00 = Downside protection on POR is enabled – Low-Power BOR (LPBOR) is selected

bit 4 **I2C1SEL:** Alternate I2C1 Pin Mapping bit(1)
1 = Default location for SCL1/SDA1 pins
0 = Alternate location for SCL1/SDA1 pins

bit 3 **PWRTEN:** Power-up Timer Enable bit
1 = PWRT is enabled
0 = PWRT is disabled

bit 2 **RETCFG:** Retention Regulator Configuration bit(1)
1 = Low-voltage regulator is not available
0 = Low-voltage regulator is available and controlled by the RETEN bit (RCON[12]) during Sleep

bit 1-0 **BOREN[1:0]:** Brown-out Reset Enable bits
11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled
01 = Brown-out Reset is controlled with the SBOREN bit setting
00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

Note 1: This setting only applies to the “FV” devices. This bit is reserved and should be maintained as ‘1’ on “F” devices.

2: The MCLRE fuse can only be changed when using the VPP-based ICSP™ mode entry. This prevents a user from accidentally locking out the device from the low-voltage test entry.

3: Refer to **Section 27.0 “Electrical Characteristics”** for BOR voltages.

REGISTER 25-7: FICD: IN-CIRCUIT DEBUGGER CONFIGURATION REGISTER

R/P-1	U-0	U-0	U-0	U-0	U-0	R/P-1	R/P-1
$\overline{\text{DEBUG}}$	—	—	—	—	—	FICD1	FICD0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{DEBUG}}$:** Background Debugger Enable bit
1 = Background debugger is disabled
0 = Background debugger functions are enabled

bit 6-2 **Unimplemented:** Read as ‘0’

bit 1-0 **FICD[1:0:]:** ICD Pin Select bits
11 = PGEC1/PGED1 are used for programming and debugging the device
10 = PGEC2/PGED2 are used for programming and debugging the device
01 = PGEC3/PGED3 are used for programming and debugging the device
00 = Reserved; do not use

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REGISTER 25-8: DEVID: DEVICE ID REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID[7:0]							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15-8 **FAMID[7:0]:** Device Family Identifier bits
01000101 = PIC24FV16KM204 family

bit 7-0 **DEV[7:0]:** Individual Device Identifier bits
00011111 = PIC24FV16KM204
00011011 = PIC24FV16KM202
00010111 = PIC24FV08KM204
00010011 = PIC24FV08KM202
00001111 = PIC24FV16KM104
00001011 = PIC24FV16KM102
00000011 = PIC24FV08KM102
00000001 = PIC24FV08KM101
00011110 = PIC24F16KM204
00011010 = PIC24F16KM202
00010110 = PIC24F08KM204
00010010 = PIC24F08KM202
00001110 = PIC24F16KM104
00001010 = PIC24F16KM102
00000010 = PIC24F08KM102
00000000 = PIC24F08KM101

REGISTER 25-9: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-4 **Unimplemented:** Read as ‘0’

bit 3-0 **REV[3:0]:** Minor Revision Identifier bits

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25.2 On-Chip Voltage Regulator

All of the PIC24FXXXXX family devices power their core digital logic at a nominal 3.0V. This may create an issue for designs that are required to operate at a higher typical voltage, as high as 5.0V. To simplify system design, all devices in the "FV" family incorporate an on-chip regulator that allows the device core to run at 3.0V, while the I/O is powered by VDD at a higher voltage.

The regulator is always enabled and provides power to the core from the other VDD pins. A low-ESR capacitor (such as ceramic) must be connected to the VCAP pin (Figure 25-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 27.1 "DC Characteristics"** and discussed in detail in **Section 2.0 "Guidelines for Getting Started with 16-Bit Microcontrollers"**.

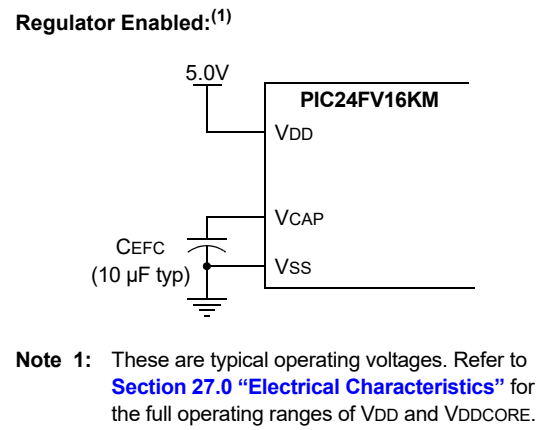
In all of the "F" family of devices, the regulator is disabled. Instead, the core logic is directly powered from VDD. "F" devices operate at a lower range of VDD voltage, from 1.8V-3.6V.

25.2.1 VOLTAGE REGULATOR TRACKING MODE AND LOW-VOLTAGE DETECTION

For all PIC24FXXXXX devices, the on-chip regulator provides a constant voltage of 3.0V nominal to the digital core logic. The regulator can provide this level from a VDD of about 3.2V, all the way up to the device's VDDMAX. It does not have the capability to boost VDD levels below 3.2V. In order to prevent "brown out" conditions when the voltage drops too low for the regulator, the regulator enters Tracking mode. In Tracking mode, the regulator output follows VDD with a typical voltage drop of 150 mV.

When the device enters Tracking mode, it is no longer possible to operate at full speed. To provide information about when the device enters Tracking mode, the on-chip High/Low-Voltage Detect (HLVD) module can be used. The HLVD trip point should be configured so that if VDD drops close to the minimum voltage for the operating frequency of the device, the HLVD Interrupt Flag, HLVDIF (IFS4[8]), will occur. This can be used to generate an interrupt and put the application into a low-power operational mode or trigger an orderly shutdown. Refer to **Section 27.1 "DC Characteristics"** for the specifications detailing the maximum operating speed based on the applied VDD voltage.

FIGURE 25-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR



25.2.2 VOLTAGE REGULATOR START-UP TIME

For PIC24FXXXXX family devices, it takes a short time, designated as TPM, for the regulator to generate a stable output. During this time, code execution is disabled. TPM is applied every time the device resumes operation after any power-down, including Sleep mode. TPM is specified in **Section 27.2 "AC Characteristics and Timing Parameters"**.

25.3 Watchdog Timer (WDT)

For the PIC24FXXXXX family of devices, the WDT is driven by the LPRC Oscillator. When the WDT is enabled, the clock source is also enabled.

The nominal WDT clock source from LPRC is 31 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the FWPSA Configuration bit. With a 31 kHz input, the prescaler yields a nominal WDT Time-out period (TWDT) of 1 ms in 5-bit mode or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the Configuration bits, WDTPS[3:0] (FWDT[3:0]), which allow the selection of a total of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler time-out periods, ranges from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

If the WDT is enabled in hardware (FWDTEN[1:0] = 11), it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON[3:2]) will need to be cleared in software after the device wakes up.

The WDT Flag bit, WDTO (RCON[4]), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note:	The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

25.3.1 WINDOWED OPERATION

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, CLRWDT instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A CLRWDT instruction executed before that window causes a WDT Reset, similar to a WDT time-out.

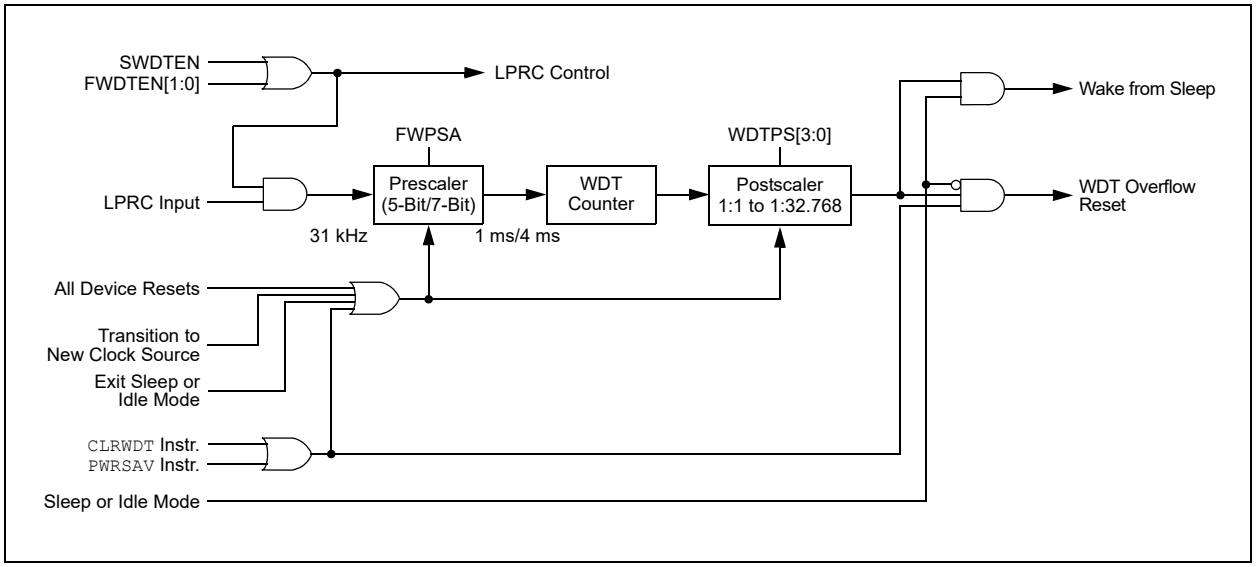
Windowed WDT mode is enabled by programming the Configuration bit, WINDIS (FWDT[6]), to '0'.

25.3.2 CONTROL REGISTER

The WDT is enabled or disabled by the FWDTEN[1:0] Configuration bits. When both of the FWDTEN[1:0] Configuration bits are set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN[1:0] Configuration bits have been programmed to '10'. The WDT is enabled in software by setting the SWDTEN control bit (RCON[5]). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments, and disable the WDT during non-critical segments, for maximum power savings. When the FWDTEN[1:0] bits are set to '01', the WDT is only enabled in Run and Idle modes, and is disabled in Sleep. Software control of the SWDTEN bit (RCON[5]) is disabled with this setting.

FIGURE 25-2: WDT BLOCK DIAGRAM



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25.4 Program Verification and Code Protection

Note: Code-protect bits (BSS, BWRP, GSS, GWRP) are in a group that are subject to write restrictions. If any bit is cleared, the rest cannot be cleared on a subsequent operation. All bits must be cleared using one operation.

For all devices in the PIC24FXXXXX family, code protection for the Boot Segment is controlled by the Configuration bit, BSS0, and the General Segment by the Configuration bit, GCP. These bits inhibit external reads and writes to the program memory space This has no direct effect in normal execution mode.

Write protection is controlled by bit, BWRP, for the Boot Segment and bit, GWRP, for the General Segment in the Configuration Word. When these bits are programmed to '0', internal write and erase operations to program memory are blocked.

25.5 In-Circuit Serial Programming

PIC24FXXXXX family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock (PGECx) and data (PGEDx), and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

25.6 In-Circuit Debugger

When MPLAB® ICD 3, MPLAB REAL ICE™ or PICkit™ 3 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx and PGEDx pins.

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{\text{MCLR}}$, V_{DD}, V_{SS}, PGECx, PGEDx and the pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

NOTES:

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26.0 DEVELOPMENT SUPPORT

Move a design from concept to production in record time with Microchip's award-winning development tools. Microchip tools work together to provide state of the art debugging for any project with easy-to-use Graphical User Interfaces (GUIs) in our free MPLAB® X and Atmel Studio Integrated Development Environments (IDEs), and our code generation tools. Providing the ultimate ease-of-use experience, Microchip's line of programmers, debuggers and emulators work seamlessly with our software tools. Microchip development boards help evaluate the best silicon device for an application, while our line of third party tools round out our comprehensive development tool solutions.

Microchip's MPLAB X and Atmel Studio ecosystems provide a variety of embedded design tools to consider, which support multiple devices, such as PIC® MCUs, AVR® MCUs, SAM MCUs and dsPIC® DSCs. MPLAB X tools are compatible with Windows®, Linux® and Mac® operating systems while Atmel Studio tools are compatible with Windows.

Go to the following website for more information and details:

https://www.microchip.com/development-tools/

NOTES:

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27.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FV16KM204 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FV16KM204 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(†)

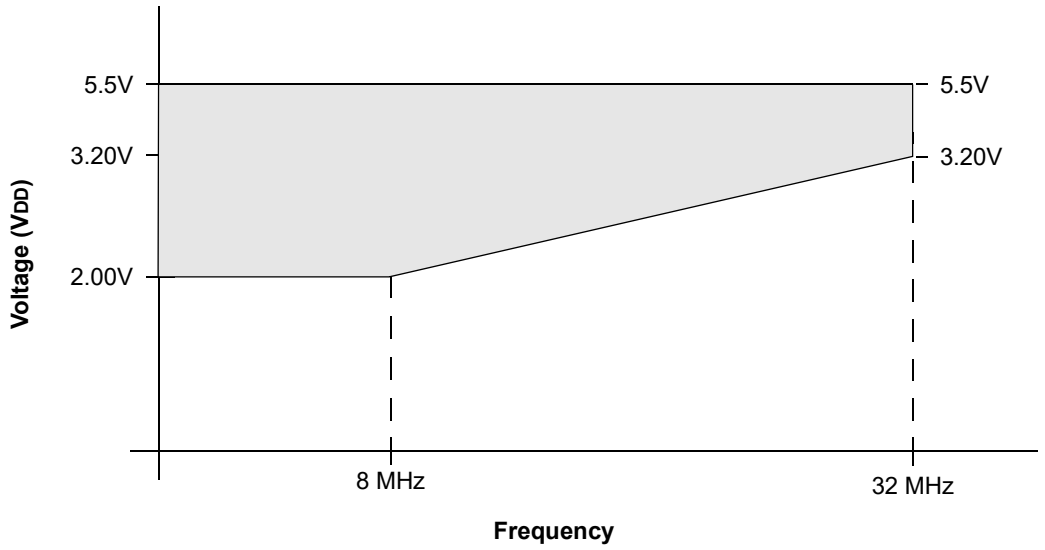
Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on VDD with respect to VSS (PIC24FXXKMXXX) ..... -0.3V to +4.5V
Voltage on VDD with respect to VSS (PIC24FVXXKMXXX) ..... -0.3V to +6.5V
Voltage on any combined analog and digital pin with respect to VSS ..... -0.3V to (VDD + 0.3V)
Voltage on any digital only pin with respect to VSS ..... -0.3V to (VDD + 0.3V)
Voltage on $\overline{\text{MCLR}}$/VPP pin with respect to VSS ..... -0.3V to +9.0V
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin(1) ..... 250 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports(1) ..... 200 mA

Note 1: Maximum allowable current is a function of device maximum power dissipation (see Table 27-1).

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

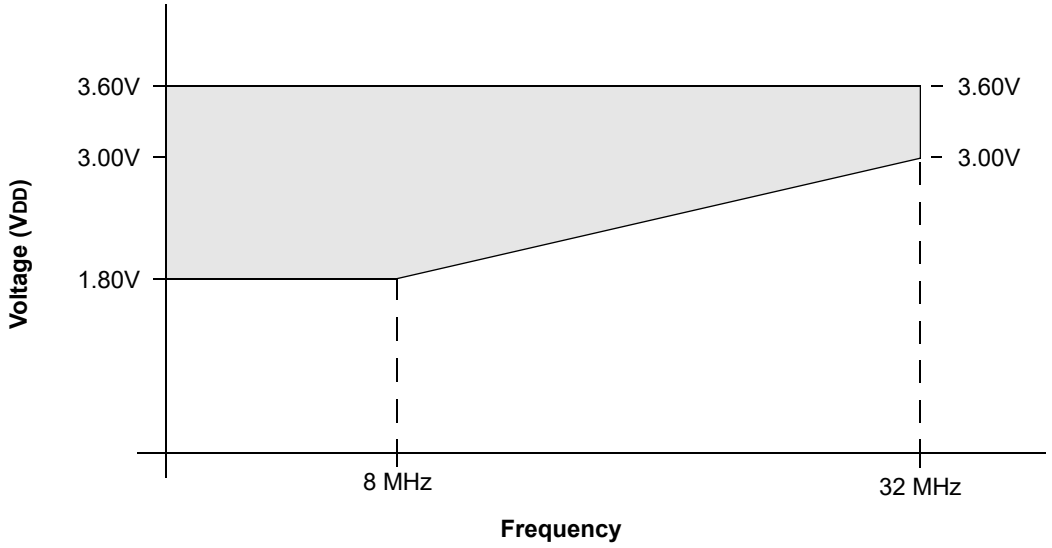
27.1 DC Characteristics

FIGURE 27-1: PIC24FV16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note: For frequencies between 8 MHz and 32 MHz, F_{MAX} = 20 MHz * (V_{DD} – 2.0) + 8 MHz.

FIGURE 27-2: PIC24F16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note: For frequencies between 8 MHz and 32 MHz, F_{MAX} = 20 MHz * (V_{DD} – 1.8) + 8 MHz.

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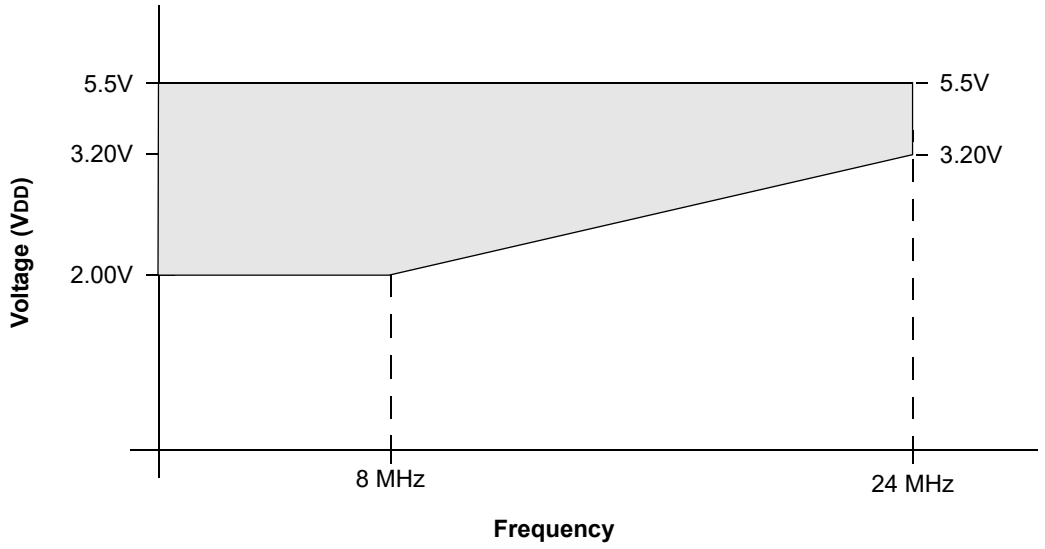
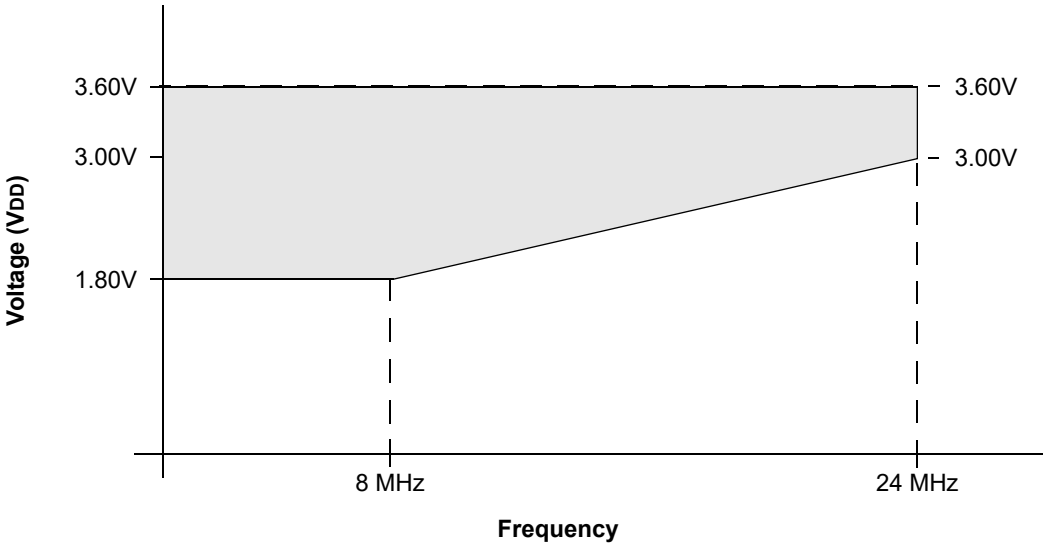
FIGURE 27-3: PIC24FV16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED)



Note: For frequencies between 8 MHz and 24 MHz, F_{MAX} = 13.33 MHz * (V_{DD} – 2.0) + 8 MHz.

FIGURE 27-4: PIC24F16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED)



Note: For frequencies between 8 MHz and 24 MHz, F_{MAX} = 13.33 MHz * (V_{DD} – 1.8) + 8 MHz.

TABLE 27-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Operating Junction Temperature Range	T_J	-40	—	+140	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 27-2: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 20-Pin PDIP	θ_{JA}	62.4	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	60	—	°C/W	1
Package Thermal Resistance, 20-Pin SSOP	θ_{JA}	108	—	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θ_{JA}	71	—	°C/W	1
Package Thermal Resistance, 20-Pin SOIC	θ_{JA}	75	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	80.2	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN	θ_{JA}	32	—	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	29	—	°C/W	1
Package Thermal Resistance, 44-Pin TQFP	θ_{JA}	40	—	°C/W	1
Package Thermal Resistance, 48-Pin UQFN	θ_{JA}	41	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 27-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KMXXX) 2.0V to 5.5V (PIC24FV16KMXXX) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DC10	V_{DD}	**Supply Voltage**	1.8	—	3.6	V	For PIC24F devices
			2.0	—	5.5	V	For PIC24FV devices
DC12	V_{DR}	**RAM Data Retention Voltage(2)**	1.6	—	—	V	For PIC24F devices
			1.8	—	—	V	For PIC24FV devices
DC16	V_{POR}	**V_{DD} Start Voltage** to Ensure Internal Power-on Reset Signal	V_{SS}	—	0.7	V	
DC17	SV_{DD}	**V_{DD} Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms

Note 1: Data in "Typ" column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which V_{DD} can be lowered without losing RAM data.

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TABLE 27-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204)
2.0V to 5.5V (PIC24FV16KM204)
Operating temperature -40°C ≤ TA ≤ +85°C for Industrial
-40°C ≤ TA ≤ +125°C for Extended

Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL[3:0] = 0000(2)	—	—	2	V	
			HLVDL[3:0] = 0001	1.84	—	2.23	V	
			HLVDL[3:0] = 0010	2.05	—	2.45	V	
			HLVDL[3:0] = 0011	2.21	—	2.63	V	
			HLVDL[3:0] = 0100	2.31	—	2.72	V	
			HLVDL[3:0] = 0101	2.51	—	2.94	V	
			HLVDL[3:0] = 0110	2.76	—	3.2	V	
			HLVDL[3:0] = 0111	2.91	—	3.35	V	
			HLVDL[3:0] = 1000	3.05	—	3.51	V	
			HLVDL[3:0] = 1001(1)	3.23	—	3.69	V	
			HLVDL[3:0] = 1010(1)	3.42	—	3.89	V	
			HLVDL[3:0] = 1011(1)	3.58	—	4.11	V	
			HLVDL[3:0] = 1100(1)	3.87	—	4.36	V	
			HLVDL[3:0] = 1101(1)	4.14	—	4.65	V	
			HLVDL[3:0] = 1110(1)	4.45	—	4.97	V	

Note 1: These trip points should not be used on PIC24FXXKMXXX devices.
2: This trip point should not be used on PIC24FVXXKMXXX devices.

TABLE 27-5: BOR TRIP POINTS

Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204)
2.0V to 5.5V (PIC24FV16KM204)
Operating temperature -40°C ≤ TA ≤ +85°C for Industrial
-40°C ≤ TA ≤ +125°C for Extended

Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC15		BOR Hysteresis		—	5	—	mV	
DC19		BOR Voltage on VDD Transition	BORV[1:0] = 00	—	—	—	—	Valid for LPBOR (**Note 1**)
			BORV[1:0] = 01	2.90	3	3.38	V	
			BORV[1:0] = 10	2.53	2.7	3.07	V	
			BORV[1:0] = 11	1.75	1.85	2.05	V	**Note 2**
			BORV[1:0] = 11	1.95	2.05	2.16	V	**Note 3**

Note 1: LPBOR re-arms the POR circuit but does not cause a BOR.
2: This is valid for PIC24F (3.3V) devices.
3: This is valid for PIC24FV (5V) devices.

TABLE 27-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KMXXX) 2.0V to 5.5V (PIC24FV16KMXXX) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Device**	**Typical**	**Max**	**Units**	**Conditions**	
IDD Current						
D20	PIC24FV16KMXXX	269	450	μA	2.0V	0.5 MIPS, FOSC = 1 MHz(1)
		465	830	μA	5.0V	
	PIC24F16KMXXX	200	330	μA	1.8V	
		410	750	μA	3.3V	
DC22	PIC24FV16KMXXX	490	—	μA	2.0V	1 MIPS, FOSC = 2 MHz(1)
		880	—	μA	5.0V	
	PIC24F16KMXXX	407	—	μA	1.8V	
		800	—	μA	3.3V	
DC24	PIC24FV16KMXXX	13.0	15.0	mA	5.0V	16 MIPS, FOSC = 32 MHz(1)
	PIC24F16KMXXX	12.0	13.0	mA	3.3V	
DC26	PIC24FV16KMXXX	2.0	—	mA	2.0V	FRC (4 MIPS), FOSC = 8 MHz
		3.5	—	mA	5.0V	
	PIC24F16KMXXX	1.80	—	mA	1.8V	
		3.40	—	mA	3.3V	
DC30	PIC24FV16KMXXX	48.0	250	μA	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
		75.0	275	μA	5.0V	
	PIC24F16KMXXX	8.1	28.0	μA	1.8V	
		13.50	55.00	μA	3.3V	

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: The oscillator is in External Clock mode (FOSCSEL[2:0] = `010`, FOSC[1:0] = `00`).

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TABLE 27-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KMXXX) 2.0V to 5.5V (PIC24FV16KMXXX) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Device**	**Typical**	**Max**	**Units**	**Conditions**	
Idle Current (IIDLE)						
DC40	PIC24FV16KMXXX	120	200	μA	2.0V	0.5 MIPS, FOSC = 1 MHz(1)
		160	430	μA	5.0V	
	PIC24F16KMXXX	50	100	μA	1.8V	
		90	370	μA	3.3V	
DC42	PIC24FV16KMXXX	165	—	μA	2.0V	1 MIPS, FOSC = 2 MHz(1)
		260	—	μA	5.0V	
	PIC24F16KMXXX	95	—	μA	1.8V	
		180	—	μA	3.3V	
DC44	PIC24FV16KMXXX	3.1	6.5	mA	5.0V	16 MIPS, FOSC = 32 MHz(1)
	PIC24F16KMXXX	2.9	6.0	mA	3.3V	
DC46	PIC24FV16KMXXX	0.65	—	mA	2.0V	FRC (4 MIPS), FOSC = 8 MHz
		1.0	—	mA	5.0V	
	PIC24F16KMXXX	0.55	—	mA	1.8V	
		1.0	—	mA	3.3V	
DC50	PIC24FV16KMXXX	42	200	μA	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
		65	225	μA	5.0V	
	PIC24F16KMXXX	2.2	18	μA	1.8V	
		4.0	40	μA	3.3V	

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: The oscillator is in External Clock mode (FOSCSEL[2:0] = `010`, FOSC[1:0] = `00`).

TABLE 27-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Parameter No.	**Device**	**Typical(1)**	**Max**	**Units**	**Conditions**		
Power-Down Current (IPD)							
DC60	PIC24FV16KMXXX	6.0	—	μA	-40°C	2.0V	Sleep Mode(2)
			8.0		+25°C		
			8.5		+60°C		
			9.0		+85°C		
			15.0		+125°C		
		6.0	—	μA	-40°C	5.0V	
			8.0		+25°C		
			9.0		+60°C		
			10.0		+85°C		
			15.0		+125°C		
	PIC24F16KMXXX	0.025	—	μA	-40°C	1.8V	
			0.80		+25°C		
			1.5		+60°C		
			2.0		+85°C		
			7.5		+125°C		
		0.040	—	μA	-40°C	3.3V	
			1.0		+25°C		
			2.0		+60°C		
			3.0		+85°C		
			7.5		+125°C		
DC61	PIC24FV16KMXXX	0.25	—	μA	+85°C	2.0V	Low-Voltage Sleep Mode(2)
			7.5		+125°C		
		0.35	3.0	μA	+85°C	5.0V	
			7.5		+125°C		

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: Data in the Typical column are at 3.3V, +25°C (PIC24F16KMXXX) or 5.0V, +25°C (PIC24FV16KMXXX) unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low. PMSLP is set to '0' and WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

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TABLE 27-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Device**	**Typical(1)**	**Max**	**Units**	**Conditions**	
Module Differential Current (ΔIPD)(3)						
DC71	PIC24FV16KMXXX	0.50	—	μA	2.0V	Watchdog Timer Current: ΔWDT
		0.70	1.5	μA	5.0V	
	PIC24F16KMXXX	0.50	—	μA	1.8V	
		0.70	1.5	μA	3.3V	
DC72	PIC24FV16KMXXX	0.80	—	μA	2.0V	32 kHz Crystal with RTCC, DSWDT or Timer1: ΔSOSC (SOSCSEL = 0)
		1.50	2.0	μA	5.0V	
	PIC24F16KMXXX	0.70	—	μA	1.8V	
		1.0	1.5	μA	3.3V	
DC75	PIC24FV16KMXXX	5.4	—	μA	2.0V	ΔHLVD
		8.1	14.0	μA	5.0V	
	PIC24F16KMXXX	4.9	—	μA	1.8V	
		7.5	14.0	μA	3.3V	
DC76	PIC24FV16KMXXX	5.6	—	μA	2.0V	ΔBOR
		6.5	11.2	μA	5.0V	
	PIC24F16KMXXX	5.6	—	μA	1.8V	
		6.0	11.2	μA	3.3V	
DC78	PIC24FV16KMXXX	0.03	—	μA	2.0V	Low-Power BOR: ΔLPBOR
		0.05	0.3	μA	5.0V	
	PIC24F16KMXXX	0.03	—	μA	1.8V	
		0.05	0.3	μA	3.3V	

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: Data in the Typical column are at 3.3V, +25°C (PIC24F16KMXXX) or 5.0V, +25°C (PIC24FV16KMXXX) unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low. PMSLP is set to '0' and WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

TABLE 27-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage(4)**					
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI16		OSCI (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSCI (HS mode)	VSS	—	0.2 VDD	V	
DI18		I/O Pins with I²C Buffer	VSS	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SMBus Buffer	VSS	—	0.8	V	SMBus enabled
	VIH	**Input High Voltage(4,5)**					
DI20		I/O Pins:					
		with Analog Functions	0.8 VDD	—	VDD	V	
		Digital Only	0.8 VDD	—	VDD	V	
DI25		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI28		I/O Pins with I²C Buffer:					
		with Analog Functions	0.7 VDD	—	VDD	V	
		Digital Only	0.7 VDD	—	VDD	V	
DI29		I/O Pins with SMBus	2.1	—	VDD	V	2.5V ≤ VPIN ≤ VDD
DI30	ICNPU	**CNx Pull-up Current**	50	250	500	μA	VDD = 3.3V, VPIN = VSS
DI31	IPU	**Maximum Load Current for Digital High Detection w/Internal Pull-up**	—	—	30	μA	VDD = 2.0V
			—	—	1000	μA	VDD = 3.3V
	IIL	**Input Leakage Current(2,3)**					
DI50		I/O Ports	—	0.050	±0.100	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Pins with OAxOUT Functions (RB15 and RB3)	—	0.100	±0.200	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance

Note 1: Data in "Typ" column are at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Refer to Table 1-4 and Table 1-5 for I/O pin buffer types.

5: VIH requirements are met when the internal pull-ups are enabled.

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TABLE 27-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**	
	VOL	**Output Low Voltage**						
DO10		All I/O Pins	—	—	0.4	V	IOL = 8.0 mA	VDD = 4.5V
			—	—	0.4	V	IOL = 4.0 mA	VDD = 3.6V
			—	—	0.4	V	IOL = 3.5 mA	VDD = 2.0V
DO16		OSC2/CLKO	—	—	0.4	V	IOL = 2.0 mA	VDD = 4.5V
			—	—	0.4	V	IOL = 1.2 mA	VDD = 3.6V
			—	—	0.4	V	IOL = 0.4 mA	VDD = 2.0V
	VOH	**Output High Voltage**						
DO20		All I/O Pins	3.8	—	—	V	IOH = -3.5 mA	VDD = 4.5V
			3	—	—	V	IOH = -3.0 mA	VDD = 3.6V
			1.6	—	—	V	IOH = -1.0 mA	VDD = 2.0V
DO26		OSC2/CLKO	3.8	—	—	V	IOH = -2.0 mA	VDD = 4.5V
			3	—	—	V	IOH = -1.0 mA	VDD = 3.6V
			1.6	—	—	V	IOH = -0.5 mA	VDD = 2.0V

Note 1: Data in “Typ” column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 27-11: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000(2)	—	—	E/W	
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D133A	TIW	Self-Timed Write Cycle Time	—	2	—	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current During Programming	—	10	—	mA	

Note 1: Data in “Typ” column are at 3.3V, +25°C unless otherwise stated.
2: Self-write and block erase.

TABLE 27-12: DC CHARACTERISTICS: DATA EEPROM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Data EEPROM Memory					
D140	EPD	Cell Endurance	100,000	—	—	E/W	
D141	VPRD	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D143A	TIWD	Self-Timed Write Cycle Time	—	4	—	ms	
D143B	TREF	Number of Total Write/Erase Cycles Before Refresh	—	10M	—	E/W	
D144	TRETDD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D145	IDDPD	Supply Current During Programming	—	7	—	mA	

Note 1: Data in “Typ” column are at 3.3V, +25°C unless otherwise stated.

TABLE 27-13: DC CHARACTERISTICS: COMPARATOR

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D300	VIOFF	Input Offset Voltage	—	20	40	mV	
D301	VICM	Input Common-Mode Voltage	0	—	VDD	V	
D302	CMRR	Common-Mode Rejection Ratio	55	—	—	dB	

TABLE 27-14: DC CHARACTERISTICS: COMPARATOR VOLTAGE REFERENCE

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
VRD310	CVRES	Resolution	—	—	VDD/32	LSb	
VRD311	CVRAA	Absolute Accuracy	—	—	1	LSb	AVDD = 3.3V-5.5V
VRD312	CVRUR	Unit Resistor Value (R)	—	2k	—	Ω	

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TABLE 27-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated) -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VBG	Band Gap Reference Voltage	0.973	1.04	1.075	V	For PIC24F devices(1)
			0.973	1.024	1.075	V	For PIC24FV devices(1)
	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
	VRGOUT	Regulator Output Voltage	3.1	3.3	3.6	V	
	CEFC	External Filter Capacitor Value	4.7	10	—	µF	Series resistance < 3 Ohm recommended; < 5 Ohm is required.
	VLVR	Low-Voltage Regulator Output Voltage	—	2.6	—	V	

Note 1: VDD > 4.5V for 4 * VBG reference, VDD > 2.3V for 2 * VBG reference.

TABLE 27-16: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Comments**	**Conditions**
	IOUT1	CTMU Current Source, Base Range	—	550	—	nA	CTMUCON1L[1:0] = 01	2.5V < VDD < VDDMAX
	IOUT2	CTMU Current Source, 10x Range	—	5.5	—	µA	CTMUCON1L[1:0] = 10	
	IOUT3	CTMU Current Source, 100x Range	—	55	—	µA	CTMUCON1L[1:0] = 11	
	IOUT4	CTMU Current Source, 1000x Range	—	550	—	µA	CTMUCON1L[1:0] = 00 (Note 2)	
	VF	Temperature Diode Forward Voltage	—	.76	—	V		
	VΔ	Voltage Change per Degree Celsius	—	1.6	—	mV/°C		

Note 1: Nominal value at the center point of the current trim range (CTMUCON1L[7:2] = 000000). On PIC24F16KM parts, the current output is limited to the typical current value when IOUT4 is chosen.

2: Do not use this current range with a temperature sensing diode.

TABLE 27-17: OPERATIONAL AMPLIFIER SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**	**Comments**
	GBWP	Gain Bandwidth Product	—	5	—	MHz	SPDSEL = 1
			—	0.5	—	MHz	SPDSEL = 0
	SR	Slew Rate	—	1.2	—	V/µs	SPDSEL = 1
			—	0.3	—	V/µs	SPDSEL = 0
	AOL	DC Open-Loop Gain	—	90	—	dB	
	VIOFF	Input Offset Voltage	—	±2	±50	mV	
	VIBC	Input Bias Current	—	—	—	nA	Note 1
	VICM	Common-Mode Input Voltage Range	AVSS	—	AVDD - 850	mV	
	CMRR	Common-Mode Rejection Ratio	—	60	—	db	
	PSRR	Power Supply Rejection Ratio	—	60	—	dB	
	VOR	Output Voltage Range	AVSS + 200	AVSS + 5 to AVDD – 5	AVDD – 200	mV	0.5V input overdrive, no output loading
	ROUT	Output Impedance	—	6.668	—	Ω	Low-Power mode, VIN = 0.2V(2)
			—	3.890	—	Ω	Low-Power mode, VIN = 1.8V(2)
			—	0.246	—	Ω	Low-Power mode, VIN = 0.2V(2)
			—	0.277	—	Ω	Low-Power mode, VIN = 1.8V(2)

Note 1: The op amps use CMOS input circuitry with negligible input bias current. The maximum “effective bias current” is the I/O pin leakage specified by electrical Parameter DI50.

2: To receive the “Typ” values, AVDD = 2V was used.

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27.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC24FV16KM204 family AC characteristics and timing parameters.

TABLE 27-18: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 1.8V to 3.6V** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 27.1 "DC Characteristics"**.

FIGURE 27-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

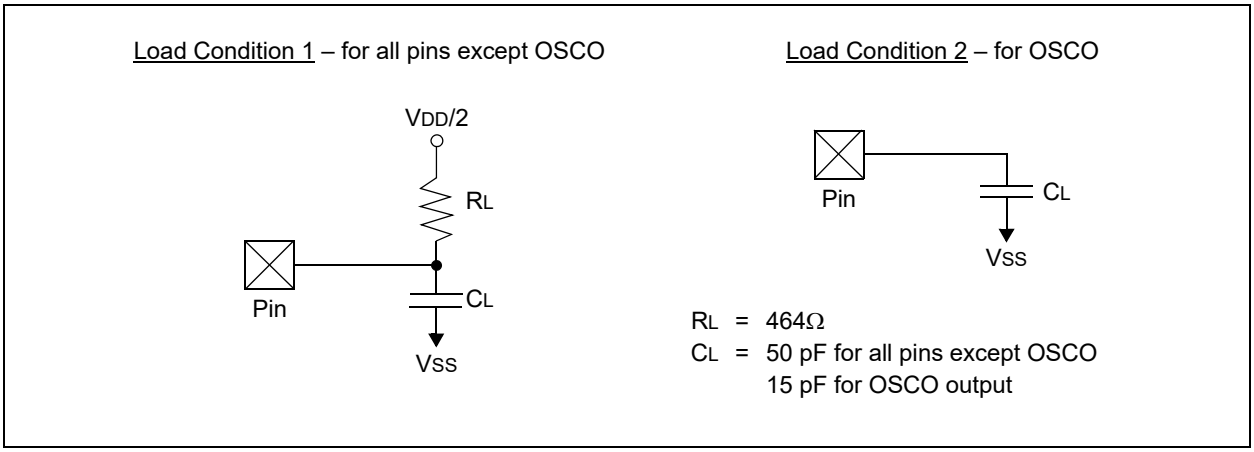

TABLE 27-19: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
DO50	COSC2	OSCO/CLKO Pin	—	—	15	pF	In XT and HS modes when External Clock is used to drive OSCI
DO56	CIO	All I/O Pins and OSCO	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

Note 1: Data in "Typ" column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 27-6: EXTERNAL CLOCK TIMING

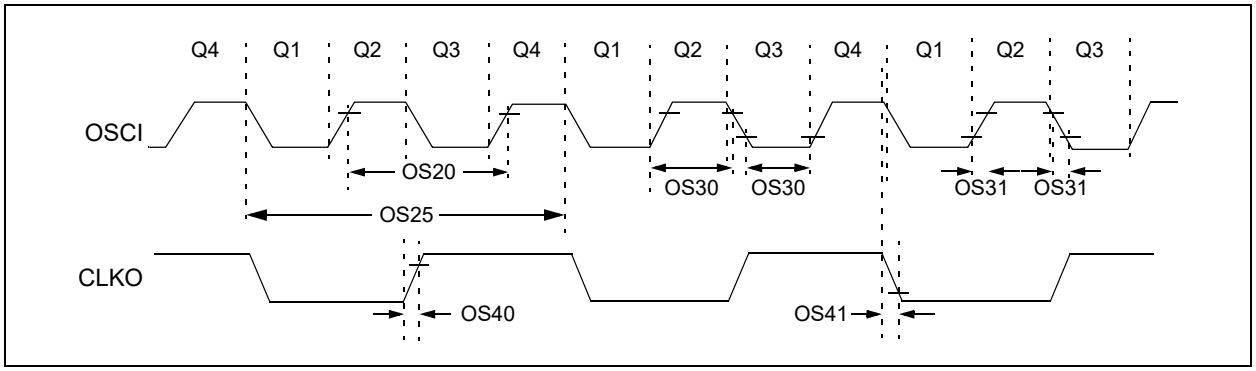

TABLE 27-20: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External Clocks allowed only in EC mode)	DC 4 DC 4	— — — —	32 8 24 6	MHz MHz MHz MHz	EC: -40°C < TA < +85°C ECPLL: -40°C < TA < +85°C EC: -40°C < TA < +125°C ECPLL: -40°C < TA < +125°C
		Oscillator Frequency	0.2 4 4 4 31	— — — — —	4 25 8 6 33	MHz MHz MHz MHz kHz	XT HS XTPLL: -40°C < TA < +85°C XTPLL: -40°C < TA < +125°C SOSC
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See Parameter OS10 for FOSC value
OS25	TCY	Instruction Cycle Time(2)	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x TOSC	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	6	10	ns	
OS41	TckF	CLKO Fall Time(3)	—	6	10	ns	

Note 1: Data in “Typ” column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Min.” values with an External Clock applied to the OSCI/CLKI pin. When an External Clock input is used, the “Max.” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 TCY) and high for the Q3-Q4 period (1/2 TCY).

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TABLE 27-21: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
OS50	FPLLI	PLL Input Frequency Range	4	—	8	MHz	ECPLL, HSPLL modes, -40°C ≤ TA ≤ +85°C
OS51	FSYS	PLL Output Frequency Range	16	—	32	MHz	-40°C ≤ TA ≤ +85°C
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	1	2	ms	
OS53	DCLK	CLKO Stability (Jitter)	-2	1	2	%	Measured over 100 ms period

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 27-22: INTERNAL RC OSCILLATOR ACCURACY(3)

AC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
F20	FRC @ 8 MHz(1)	-2	—	+2	%	+25°C	3.0V ≤ VDD ≤ 3.6V, F device 3.2V ≤ VDD ≤ 5.5V, FV device
		-5	—	+5	%	-40°C ≤ TA ≤ +125°C	1.8V ≤ VDD ≤ 3.6V, F device 2.0V ≤ VDD ≤ 5.5V, FV device
F21	LPRC @ 31 kHz(2)	-15	—	+15	%	-40°C ≤ TA ≤ +125°C	1.8V ≤ VDD ≤ 3.6V, F device 2.0V ≤ VDD ≤ 5.5V, FV device

Note 1: The frequency is calibrated at +25°C and 3.3V. The OSCTUN bits can be used to compensate for temperature drift.

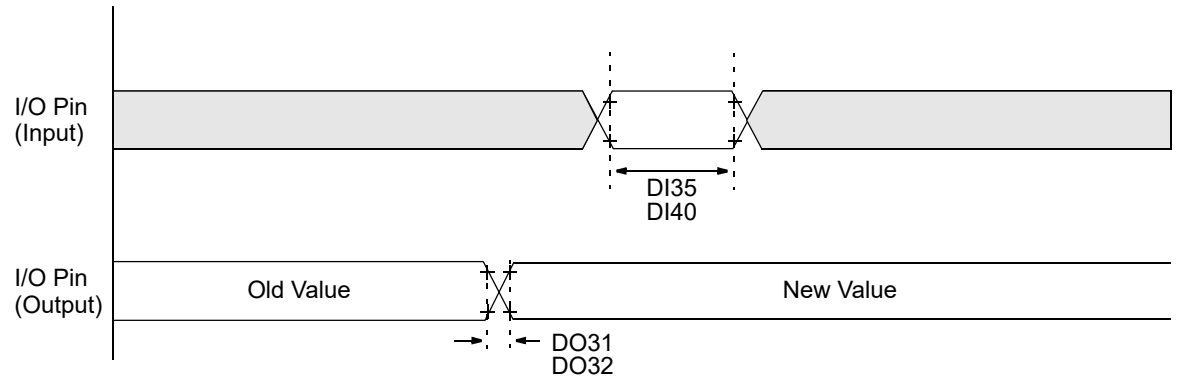
2: The change of LPRC frequency as VDD changes.

3: In High-Power/High-Accuracy mode, the Configuration bit, LPRCSEL = 1.

TABLE 27-23: INTERNAL RC OSCILLATOR SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	TFRC	FRC Start-up Time	—	5	—	μs	
	TLPRC	LPRC Start-up Time	—	70	—	μs	

FIGURE 27-7: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-24: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (output)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in “Typ” column are at 3.3V, +25°C unless otherwise stated.

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FIGURE 27-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS

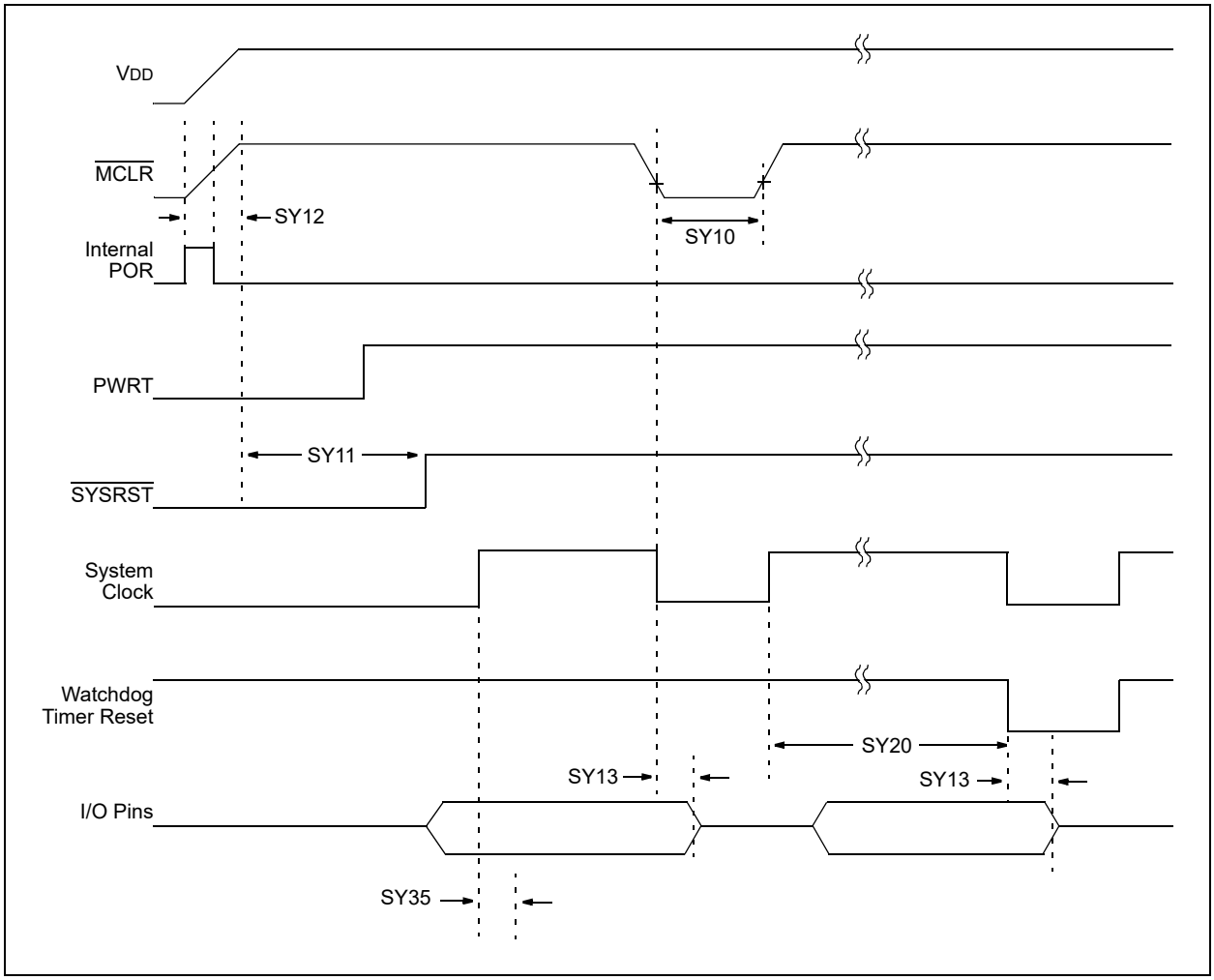

FIGURE 27-9: BROWN-OUT RESET CHARACTERISTICS

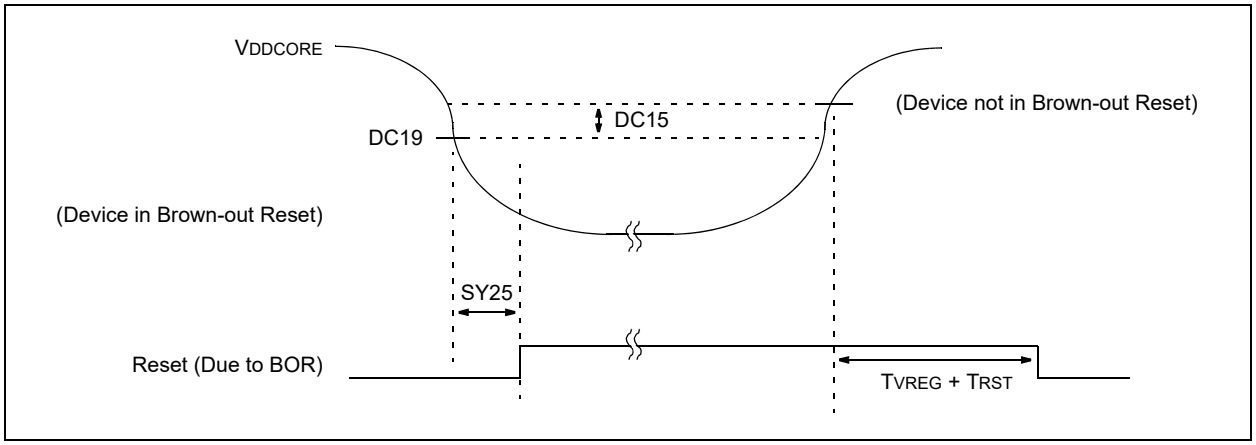

TABLE 27-25: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
SY10	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	
SY11	TPWRT	Power-up Timer Period	50	64	90	ms	
SY12	TPOR	Power-on Reset Delay	1	5	10	μs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	100	ns	
SY20	TWDT	Watchdog Timer Time-out Period	0.85	1.0	1.15	ms	1.32 prescaler
			3.4	4.0	4.6	ms	1:128 prescaler
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	2.0	2.3	μs	
SY45	TRST	Internal State Reset Time	—	5	—	μs	
SY50	TVREG	On-Chip Voltage Regulator Output Delay	—	10	—	μs	**Note 2**
SY55	TLOCK	PLL Start-up Time	—	100	—	μs	
SY65	TOST	Oscillator Start-up Time	—	1024	—	TOSC	
SY71	TPM	Program Memory Wake-up Time	—	1	—	μs	Sleep wake-up with PMSLP = 0
SY72	TLVR	Low-Voltage Regulator Wake-up Time	—	250	—	μs	

Note 1: Data in “Typ” column are at 3.3V, +25°C unless otherwise stated.

2: This applies to PIC24FV16KMXXX devices only.

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TABLE 27-26: COMPARATOR TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
300	TRESP	Response Time*(1)	—	150	400	ns	
301	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	μs	

* Parameters are characterized but not tested.

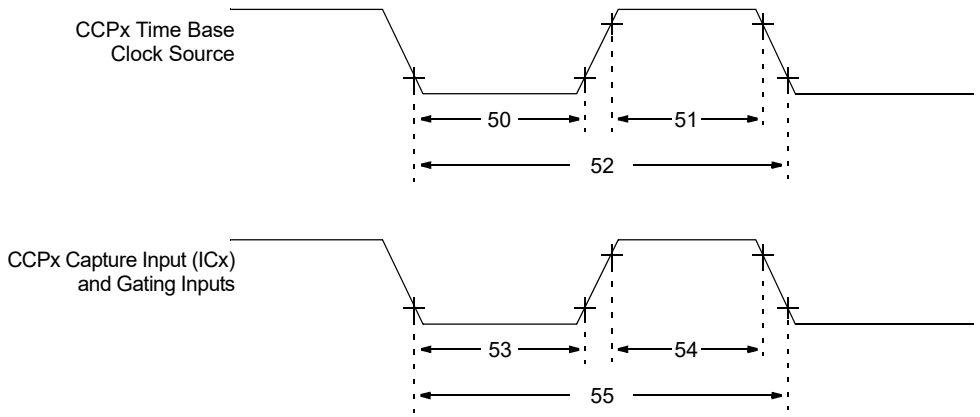
Note 1: Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

TABLE 27-27: COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
VR310	TSET	Settling Time(1)	—	—	10	μs	

Note 1: Settling time is measured while CVRSS = 1 and the CVR[3:0] bits transition from '0000' to '1111'.

FIGURE 27-10: CAPTURE/COMPARE/PWM TIMINGS (MCCPx, SCCPx MODULES)

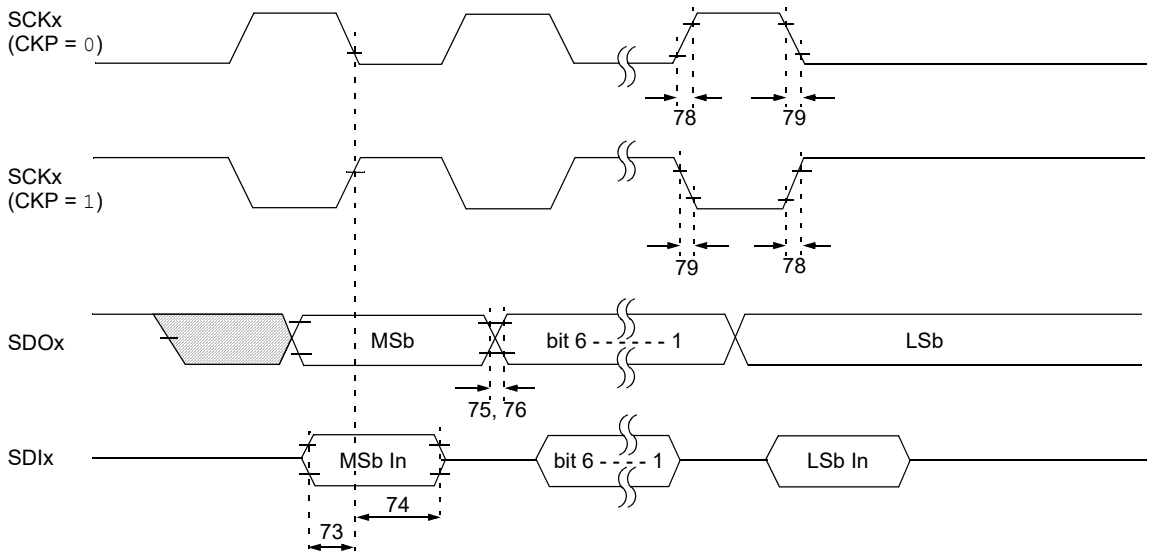


Note: Refer to Figure 27-5 for load conditions.

TABLE 27-28: CAPTURE/COMPARE/PWM REQUIREMENTS (MCCPx, SCCPx MODULES)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
50	TCLKL	CCPx Time Base Clock Source Low Time	TCY/2	—	ns	
51	TCLKH	CCPx Time Base Clock Source High Time	TCY/2	—	ns	
52	TCLK	CCPx Time Base Clock Source Period	TCY	—	ns	
53	TCCL	CCPx Capture or Gating Input Low Time	TCLK	—	ns	
54	TCCH	CCPx Capture or Gating Input High Time	TCLK	—	ns	
55	TCCP	CCPx Capture or Gating Input Period	2 * TCLK/N	—	ns	N = Prescale Value (1, 4 or 16)

FIGURE 27-11: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-29: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
73	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	20	—	ns	
74	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	40	—	ns	
75	TDOR	SDOx Data Output Rise Time	—	25	ns	
76	TDOF	SDOx Data Output Fall Time	—	25	ns	
78	TSCR	SCKx Output Rise Time (Master mode)	—	25	ns	
79	TSCF	SCKx Output Fall Time (Master mode)	—	25	ns	
	FSCK	SCKx Frequency	—	10	MHz	

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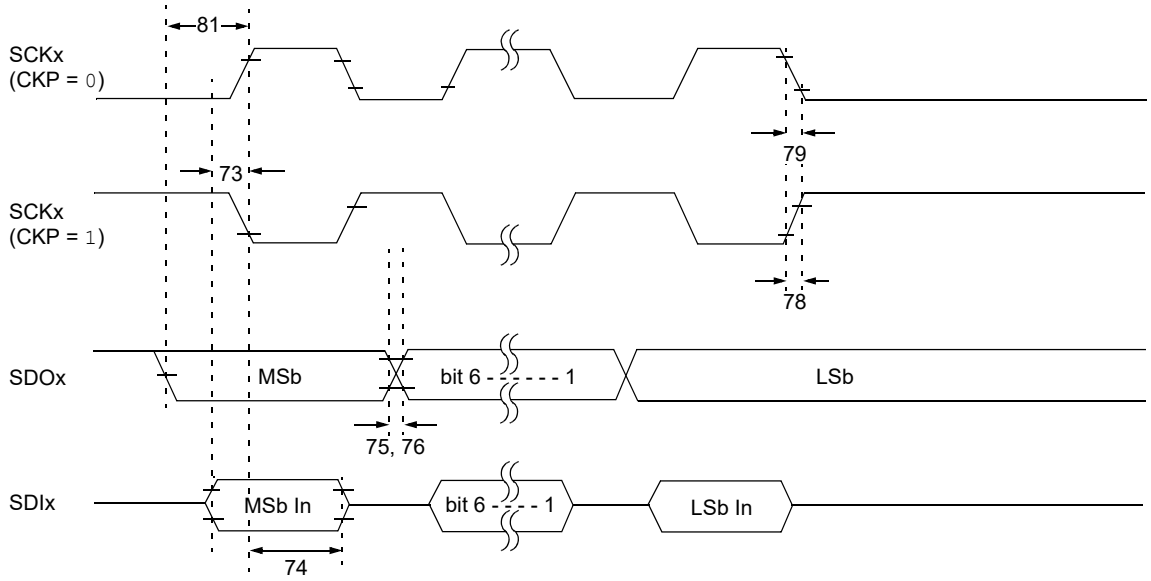
FIGURE 27-12: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)

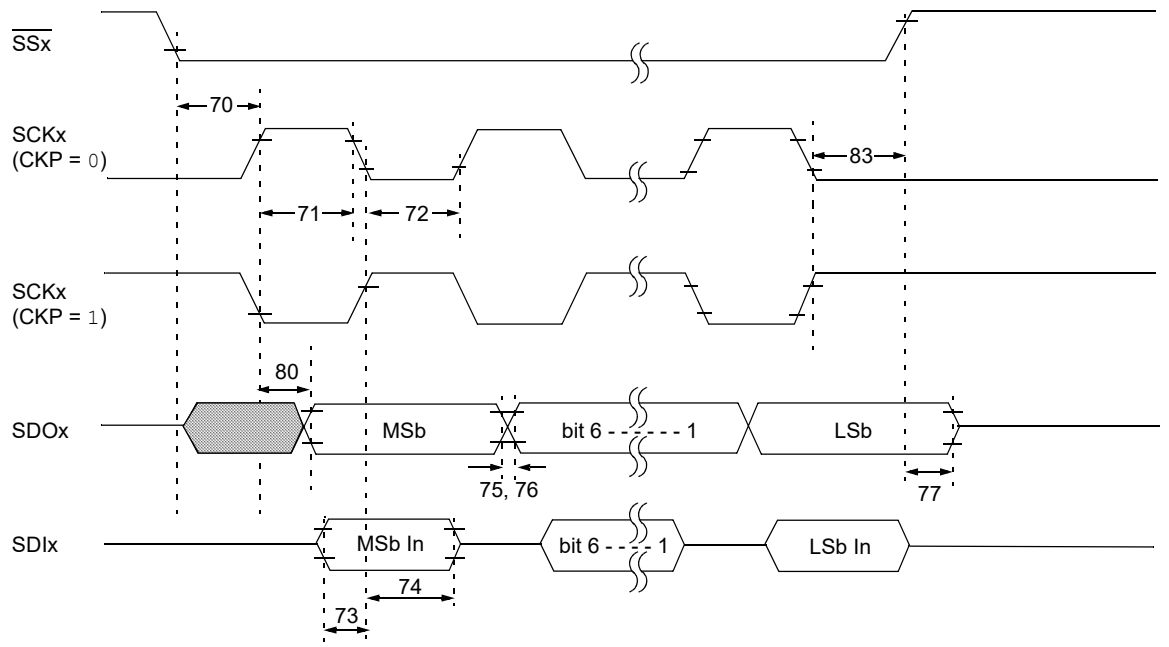


Note: Refer to Figure 27-5 for load conditions.

TABLE 27-30: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
73	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	35	—	ns	
74	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	40	—	ns	
75	TDOR	SDOx Data Output Rise Time	—	25	ns	
76	TDOF	SDOx Data Output Fall Time	—	25	ns	
78	TSCR	SCKx Output Rise Time (Master mode)	—	25	ns	
79	TSCF	SCKx Output Fall Time (Master mode)	—	25	ns	
81	TDOV2SCH, TDOV2SCL	SDOx Data Output Setup to SCKx Edge	TCY	—	ns	
	FSCK	SCKx Frequency	—	10	MHz	

FIGURE 27-13: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-31: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TSSL2SCH, TSSL2SCL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input		3 TCY	—	ns	
70A	TSSL2WB	$\overline{SSx}$ to Write to SSPxBUF		3 TCY	—	ns	
71	TSCH	SCKx Input High Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
71A			Single Byte	40	—	ns	**Note 1**
72	TSCL	SCKx Input Low Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
72A			Single Byte	40	—	ns	**Note 1**
73	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge		20	—	ns	
73A	TB2B	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 TCY + 40	—	ns	**Note 2**
74	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TDOR	SDOx Data Output Rise Time		—	25	ns	
76	TDOF	SDOx Data Output Fall Time		—	25	ns	
77	TSSH2DOZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance		10	50	ns	
80	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid After SCKx Edge		—	50	ns	
83	TSCH2SSH, TSCL2SSH	$\overline{SSx}$ ↑ After SCKx Edge		1.5 TCY + 40	—	ns	
	FSCK	SCKx Frequency		—	10	MHz	

Note 1: Requires the use of Parameter 73A.

2: Only if Parameters 71A and 72A are used.

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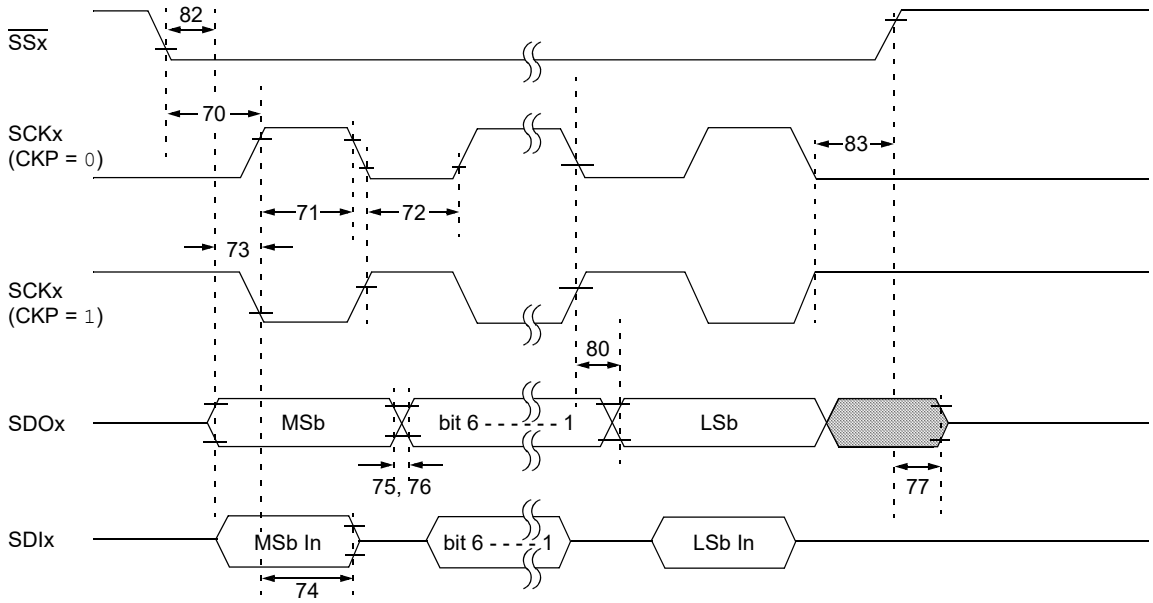
FIGURE 27-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)



Note: Refer to Figure 27-5 for load conditions.

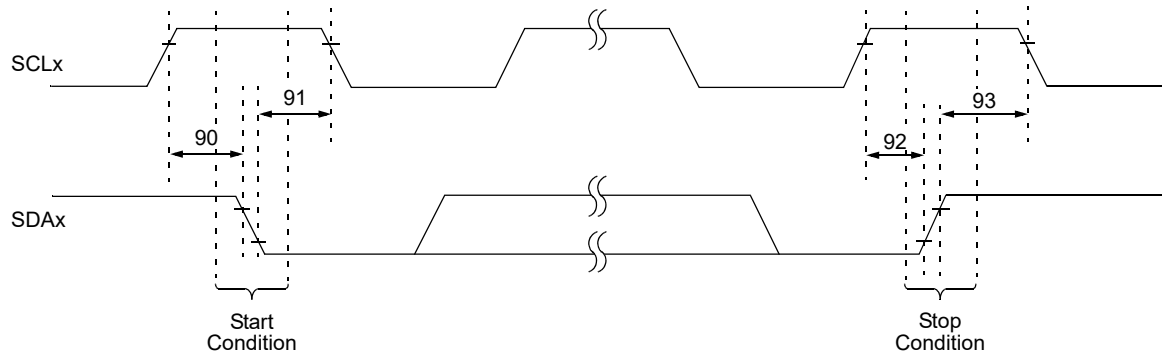
TABLE 27-32: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TSSL2SCH, TSSL2SCL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input		3 TCY	—	ns	
70A	TSSL2WB	$\overline{SSx}$ to Write to SSPxBUF		3 TCY	—	ns	
71	TSCH	SCKx Input High Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
71A			Single Byte	40	—	ns	**Note 1**
72	TSCL	SCKx Input Low Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
72A			Single Byte	40	—	ns	**Note 1**
73A	TB2B	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 TCY + 40	—	ns	**Note 2**
74	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TDOR	SDOx Data Output Rise Time		—	25	ns	
76	TDOF	SDOx Data Output Fall Time		—	25	ns	
77	TSSH2DOZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance		10	50	ns	
80	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid After SCKx Edge		—	50	ns	
82	TSSL2DOV	SDOx Data Output Valid After $\overline{SSx}$ ↓ Edge		—	50	ns	
83	TSCH2SSH, TSCL2SSH	$\overline{SSx}$ ↑ After SCKx Edge		1.5 TCY + 40	—	ns	
	FSCK	SCKx Frequency		—	10	MHz	

Note 1: Requires the use of Parameter 73A.

2: Only if Parameters 71A and 72A are used.

FIGURE 27-15: I²C BUS START/STOP BITS TIMING

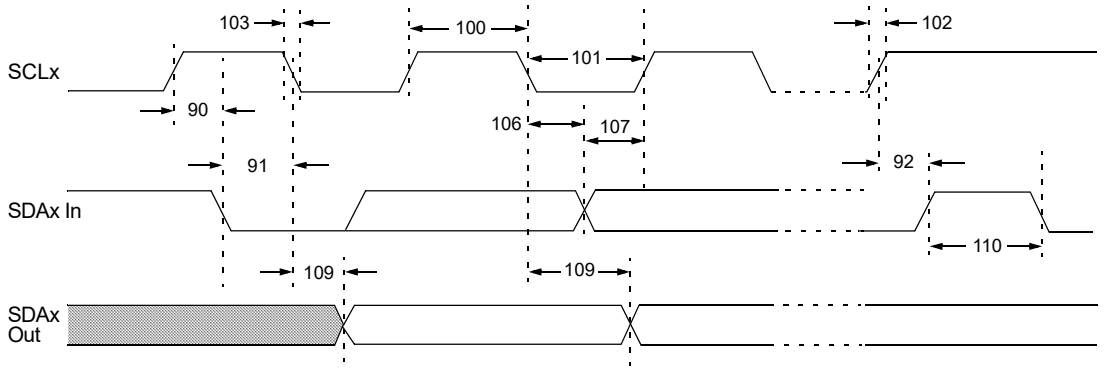


Note: Refer to Figure 27-5 for load conditions.

TABLE 27-33: I²C BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	4700	—	ns	
			400 kHz mode	600	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—		

FIGURE 27-16: I²C BUS DATA TIMING



Note: Refer to Figure 27-5 for load conditions.

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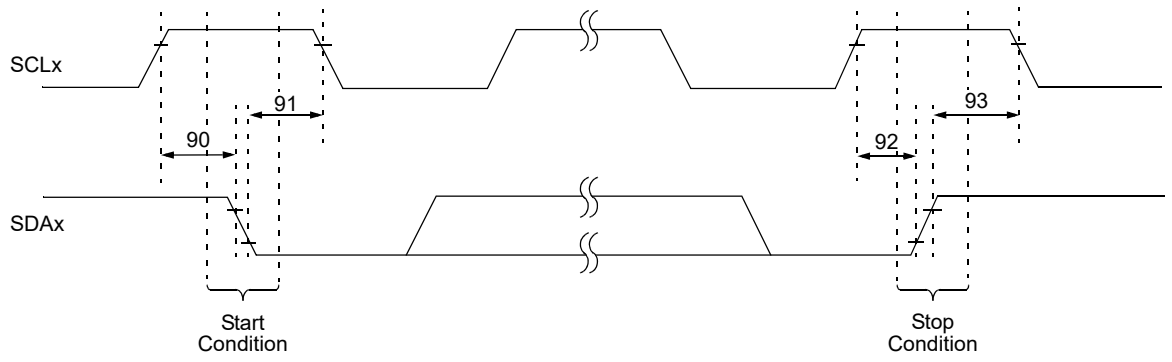
TABLE 27-34: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock High Time	100 kHz mode	4.0	—	μs	Must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Must operate at a minimum of 10 MHz
			MSSPx module	1.5 TCY	—	—	
101	TLOW	Clock Low Time	100 kHz mode	4.7	—	μs	Must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Must operate at a minimum of 10 MHz
			MSSPx module	1.5 TCY	—	—	
102	TR	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10 to 400 pF
103	TF	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10 to 400 pF
90	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
91	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**Note 2**
			400 kHz mode	100	—	ns	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	**Note 1**
			400 kHz mode	—	—	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
D102	CB	Bus Capacitive Loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCLx to avoid unintended generation of Start or Stop conditions.

2: A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement, TSU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCLx line is released.

FIGURE 27-17: MSSPx I²C BUS START/STOP BITS TIMING WAVEFORMS



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-35: I²C BUS START/STOP BITS REQUIREMENTS (MASTER MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	2(TOSC)(BRG + 1)	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—		

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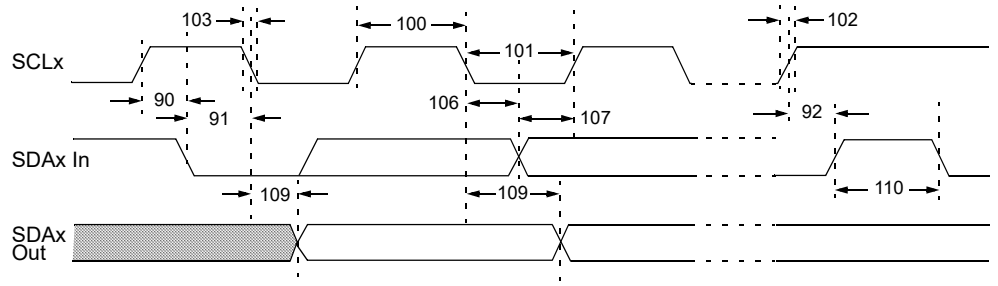
FIGURE 27-18: MSSPx I²C BUS DATA TIMING



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-36: I²C BUS DATA REQUIREMENTS (MASTER MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock High Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
101	TLOW	Clock Low Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
102	TR	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
103	TF	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	Only relevant for Repeated Start condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	After this period, the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**Note 1**
			400 kHz mode	100	—	ns	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
D102	CB	Bus Capacitive Loading		—	400	pF	

Note 1: A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but Parameter 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, Parameter 102 + Parameter 107 = 1000 + 250 = 1250 ns (for 100 kHz mode), before the SCLx line is released.

TABLE 27-37: A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 1.8	—	Lesser of: VDD + 0.3 or 3.6	V	PIC24FXXKMXXX devices
			Greater of: VDD – 0.3 or 2.0	—	Lesser of: VDD + 0.3 or 5.5	V	PIC24FVXXKMXXX devices
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.7	—	AVDD	V	
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 1.7	V	
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD08	IVREF	Reference Voltage Input Current	—	1.25	—	mA	
AD09	ZVREF	Reference Input Impedance	—	10k	—	Ω	
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	Note 2
AD11	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD12	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	1k	Ω	12-bit
A/D Accuracy							
AD20b	NR	Resolution	—	12	—	bits	
AD21b	INL	Integral Nonlinearity	—	±1	±9	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V
AD22b	DNL	Differential Nonlinearity	—	±1	±5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V
AD23b	GERR	Gain Error	—	±1	±9	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V
AD24b	EOFF	Offset Error	—	±1	±5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V
AD25b		Monotonicity(1)	—	—	—	—	Guaranteed

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

2: Measurements are taken with external VREF+ and VREF- used as the A/D voltage reference.

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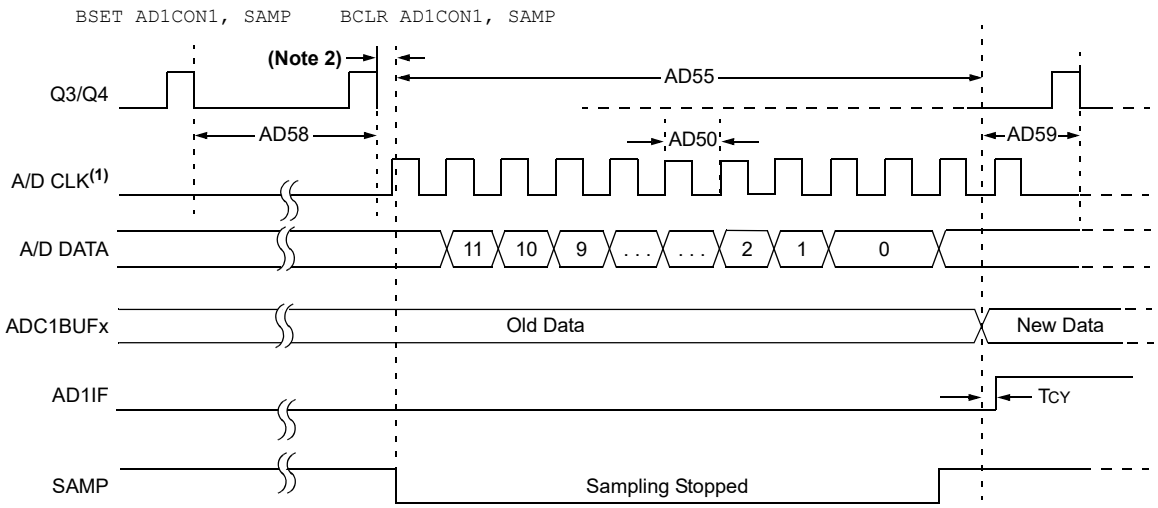
FIGURE 27-19: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

2: This is a minimal RC delay (typically 100 ns) which also disconnects the holding capacitor from the analog input.

TABLE 27-38: A/D CONVERSION TIMING REQUIREMENTS(1)

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	A/D Clock Period	600	—	—	ns	TCY = 75 ns, AD1CON3 in Default state
AD51	TRC	A/D Internal RC Oscillator Period	—	1.67	—	μs	
Conversion Rate							
AD55	TCONV	Conversion Time	— —	12 14	— —	TAD TAD	10-bit results 12-bit results
AD56	FCNV	Throughput Rate	—	—	100	ksps	
AD57	TSAMP	Sample Time	—	1	—	TAD	
AD58	TACQ	Acquisition Time	750	—	—	ns	**Note 2**
AD59	TSWC	Switching Time from Convert to Sample	—	—	**Note 3**		
AD60	TDIS	Discharge Time	12	—	—	TAD	
Clock Parameters							
AD61	TPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	TAD	

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

2: The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD).

3: On the following cycle of the device clock.

TABLE 27-39: 8-BIT DIGITAL-TO-ANALOG CONVERTER SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Comments**
		Resolution	8	—	—	bits	
		DACREF[1:0] Input Voltage Range	AVSS + 1.8	—	AVDD	V	
		Differential Linearity Error (DNL)	—	—	±0.5	LSb	
		Integral Linearity Error (INL)	—	—	±1.5	LSb	
		Offset Error	—	—	±0.5	LSb	
		Gain Error	—	—	±3.0	LSb	
		Monotonicity	—	—	—	—	**Note 1**
		Output Voltage Range	AVSS + 50	AVSS + 5 to AVDD – 5	AVDD – 50	mV	0.5V input overdrive, no output loading
		Slew Rate	—	5	—	V/µs	
		Settling Time	—	10	—	µs	
		Unit Resistor Resistance	—	410	—	Ω	

Note 1: DAC output voltage never decreases with an increase in the data code.

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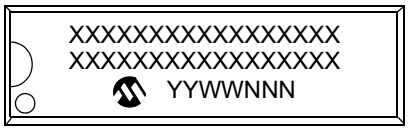
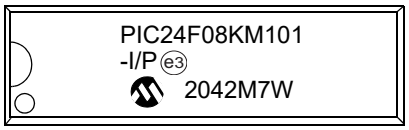
28.0 PACKAGING INFORMATION

28.1 Package Marking Information

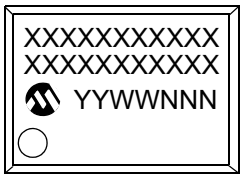
20-Lead PDIP (300 mil)



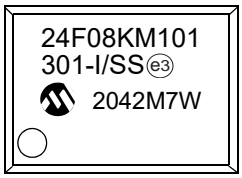
Example



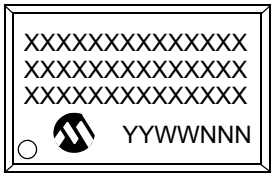
20-Lead SSOP (5.30 mm)



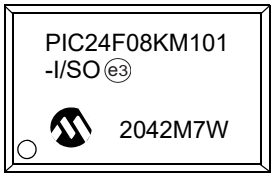
Example



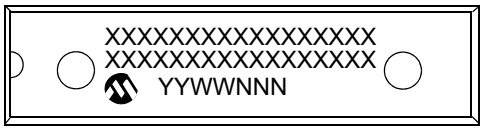
20-Lead SOIC (7.50 mm)



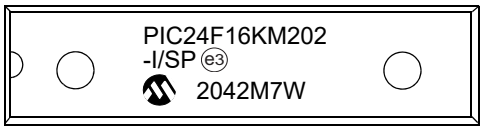
Example



28-Lead SPDIP (.300")

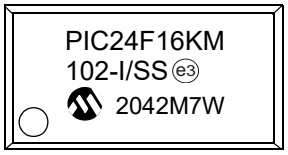


Example



28-Lead SSOP (5.30 mm)

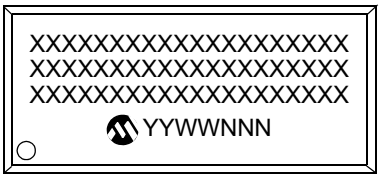
Example



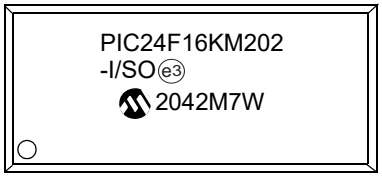
Legend:	XX...X	Product-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

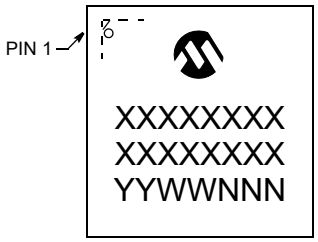
28-Lead SOIC (7.50 mm)



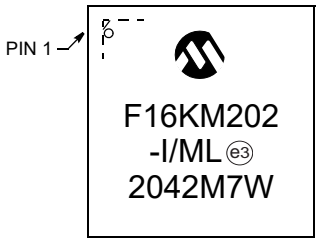
Example



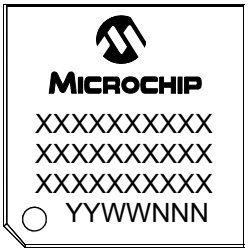
28-Lead QFN (6x6 mm)



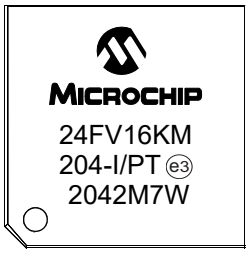
Example



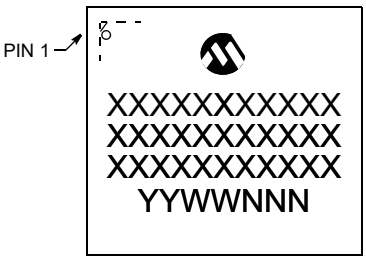
44-Lead TQFP (10x10x1 mm)



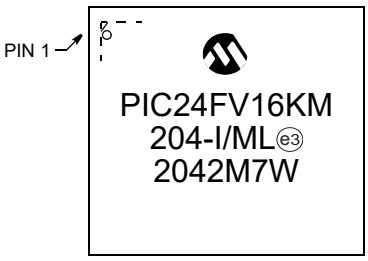
Example



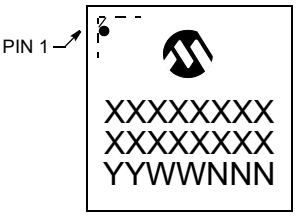
44-Lead QFN (8x8x0.9 mm)



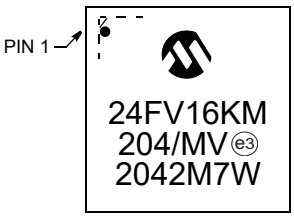
Example



48-Lead UQFN (6x6x0.5 mm)



Example



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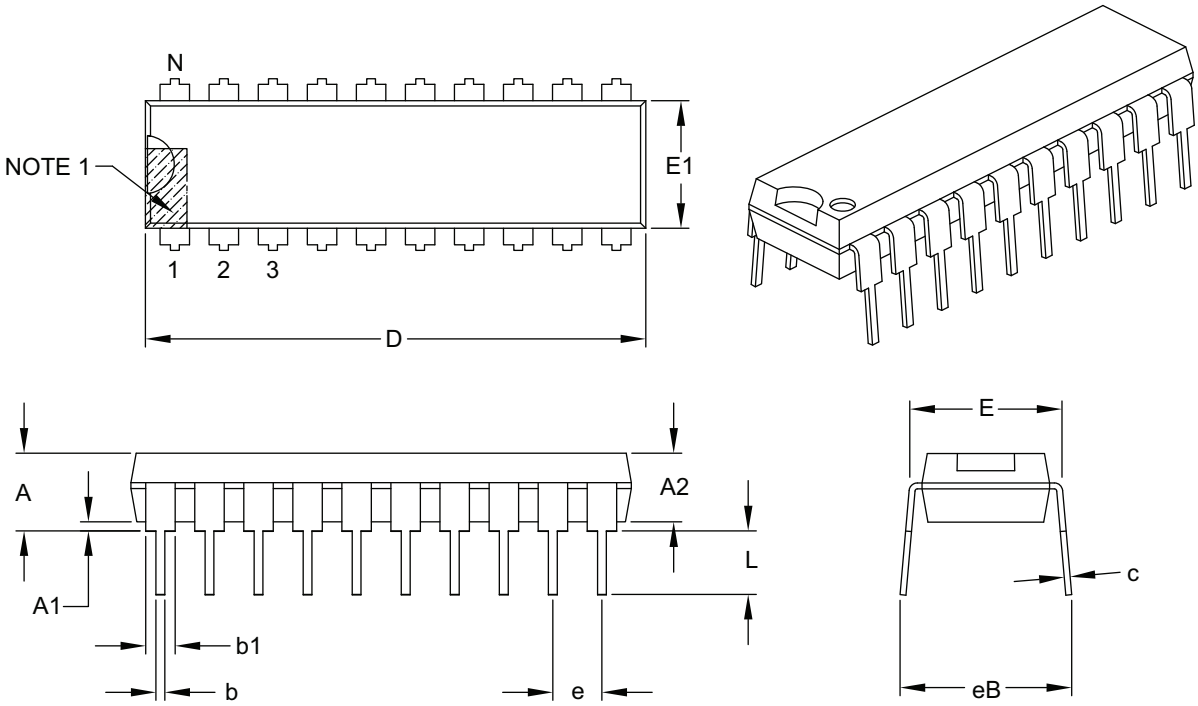
28.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



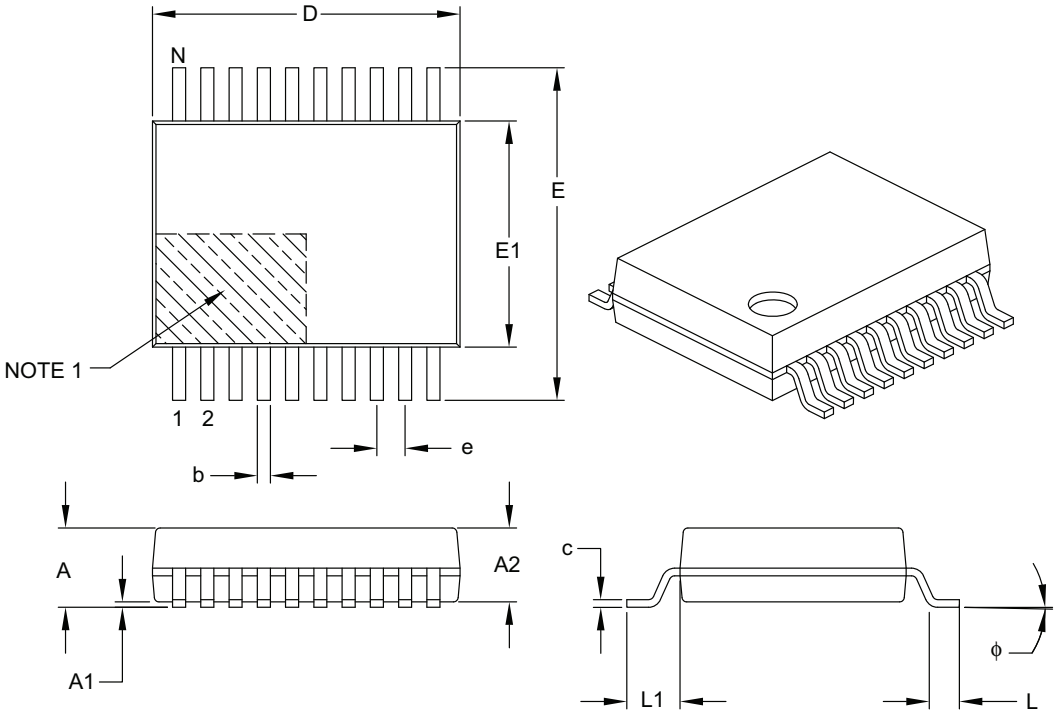
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

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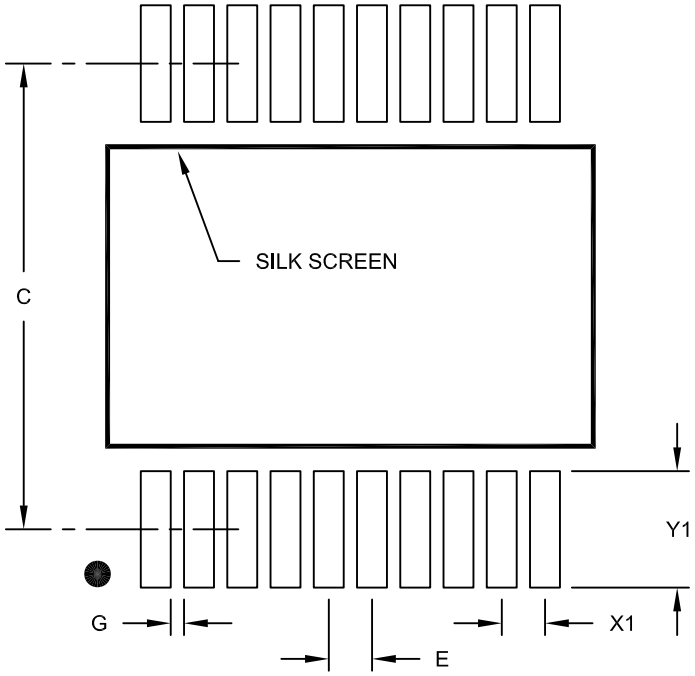
20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

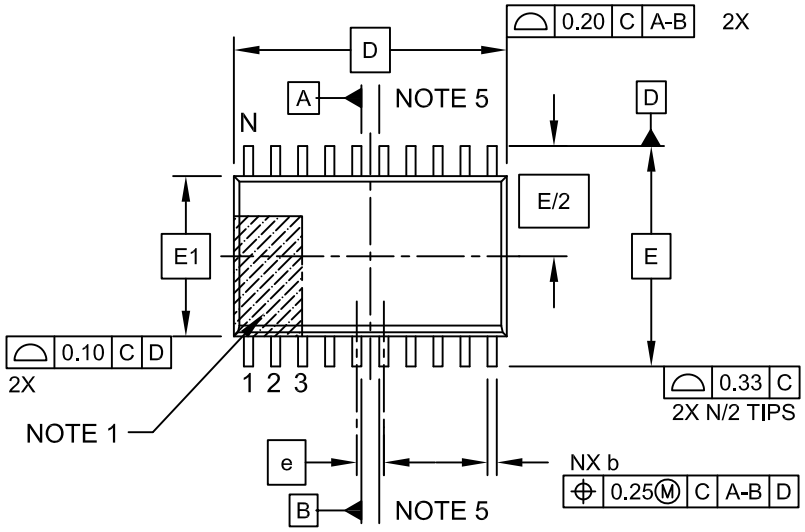
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

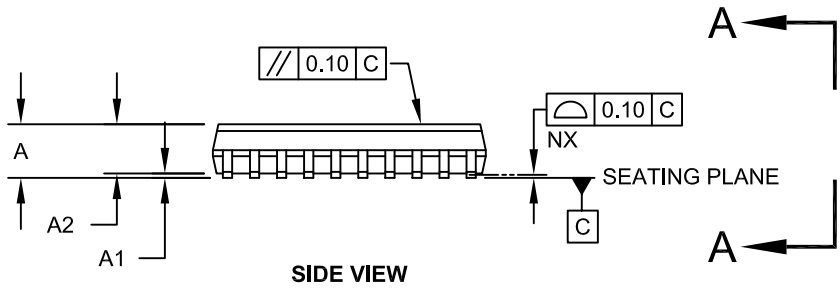
Microchip Technology Drawing No. C04-2072A

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

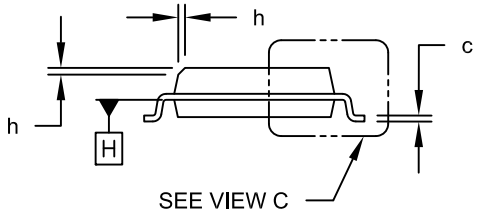
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-094C Sheet 1 of 2

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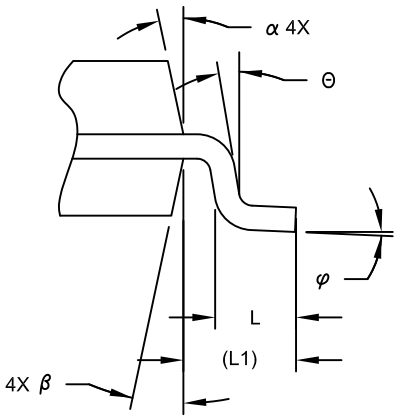
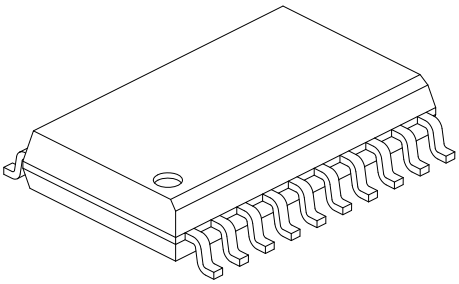
20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	12.80 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

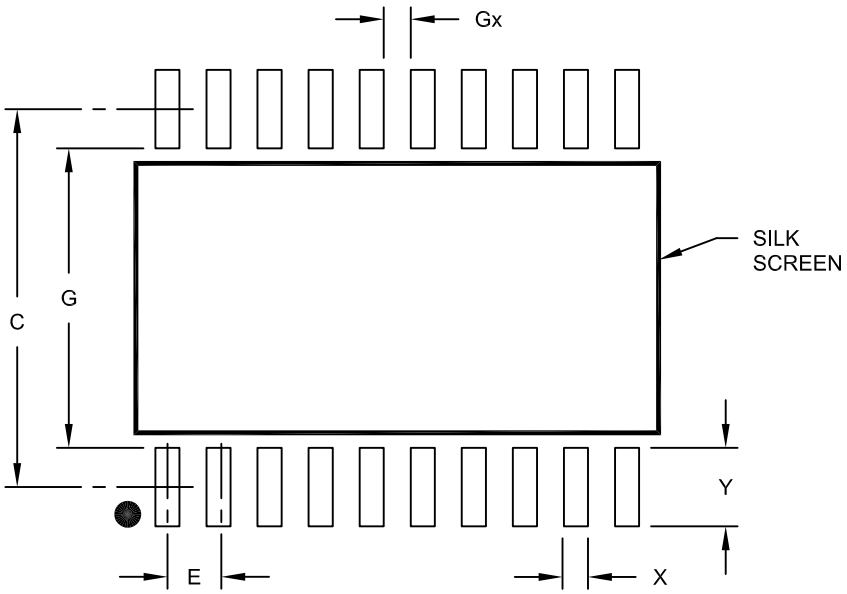
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X20)	X			0.60
Contact Pad Length (X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A

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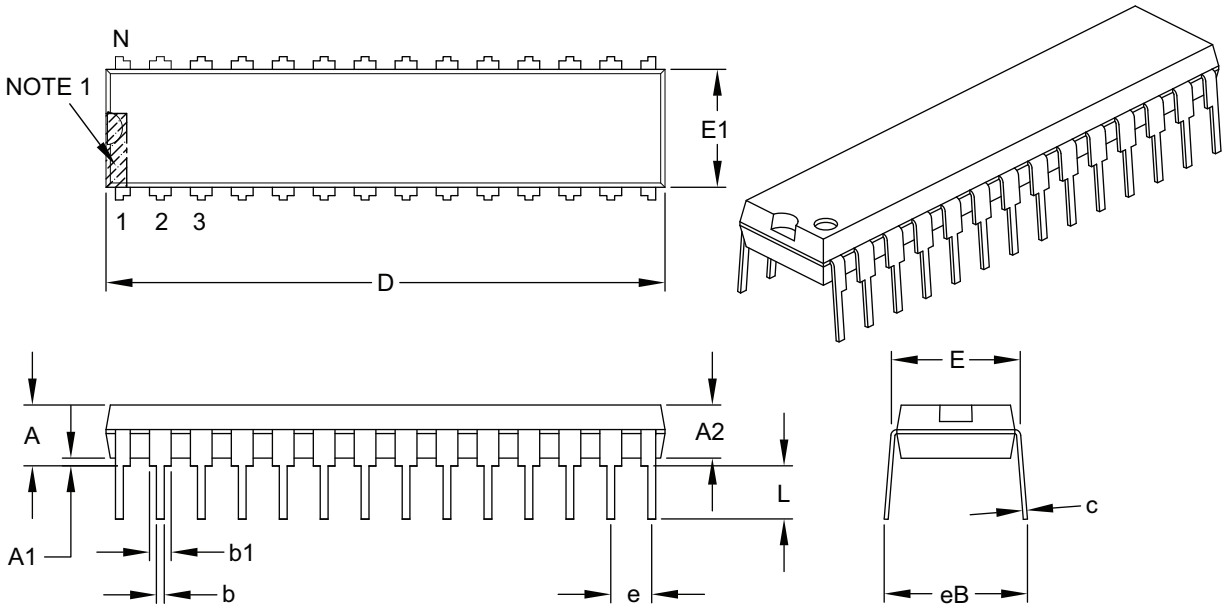
28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



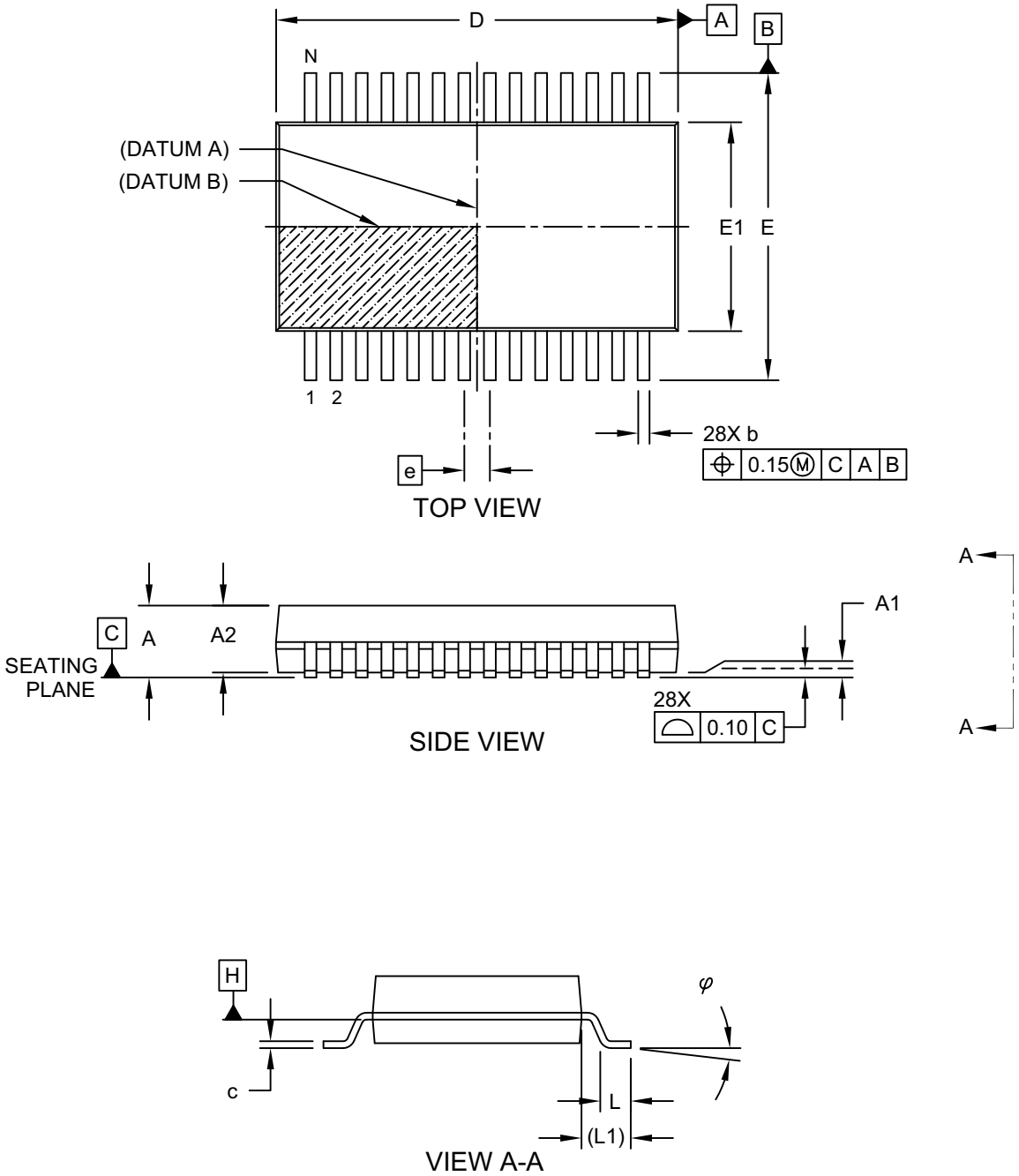
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-073 Rev C Sheet 1 of 2

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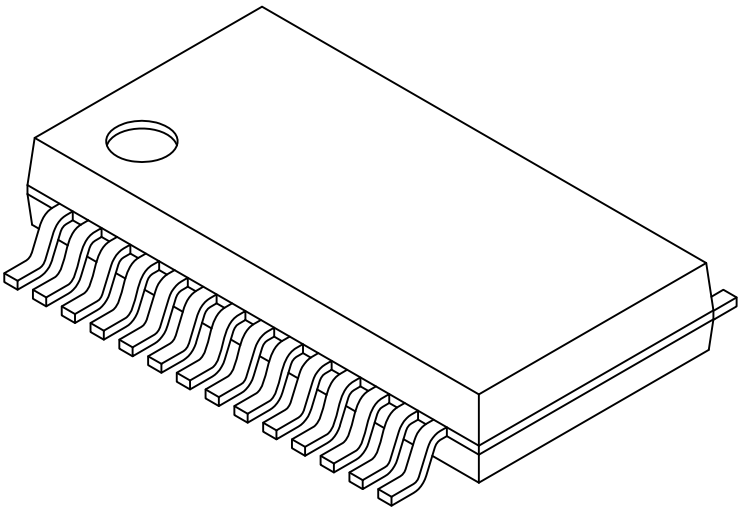
28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	-	-
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	-	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

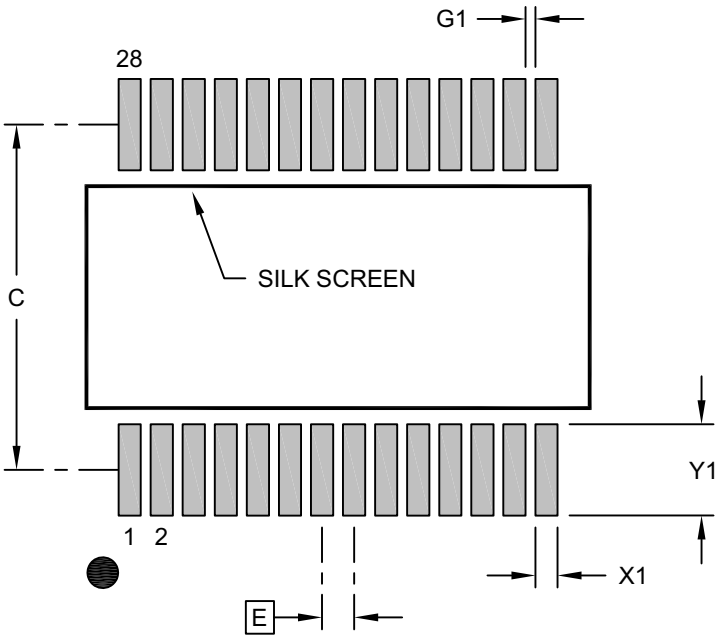
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073 Rev C Sheet 2 of 2

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.00	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.85
Contact Pad to Center Pad (X26)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2073 Rev B

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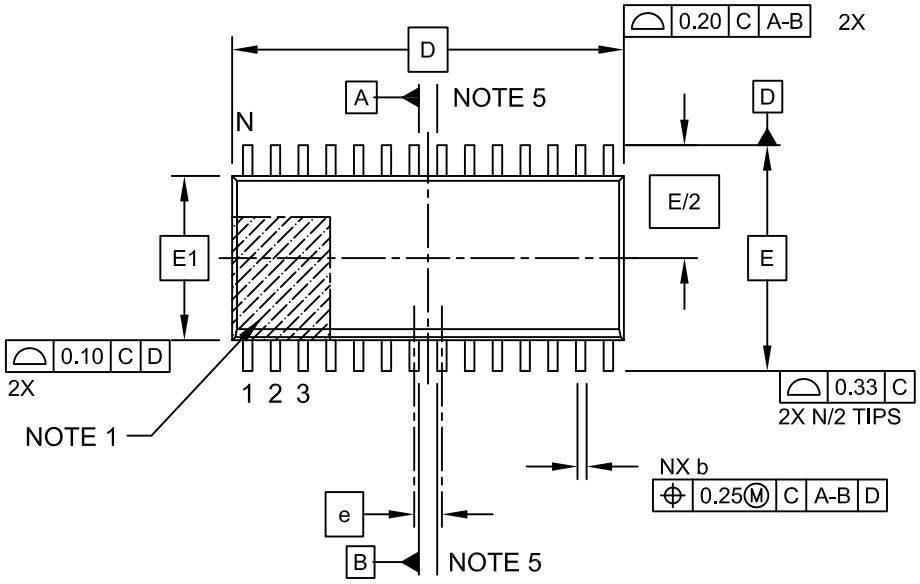
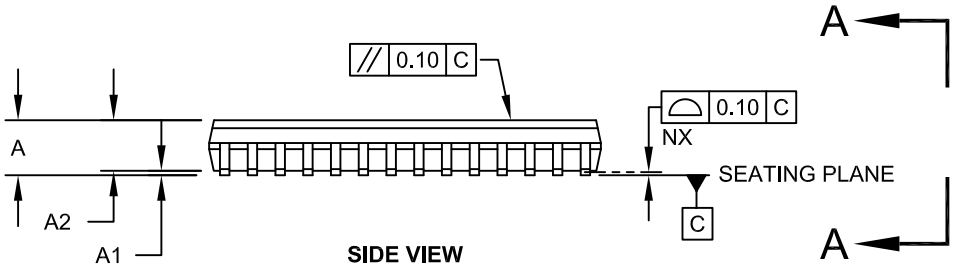
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

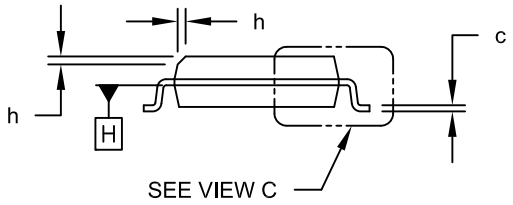
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

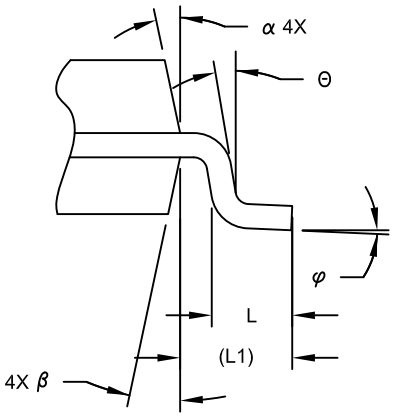


VIEW A-A

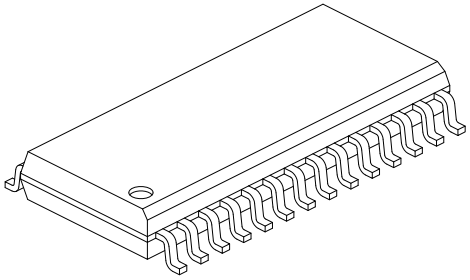
Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

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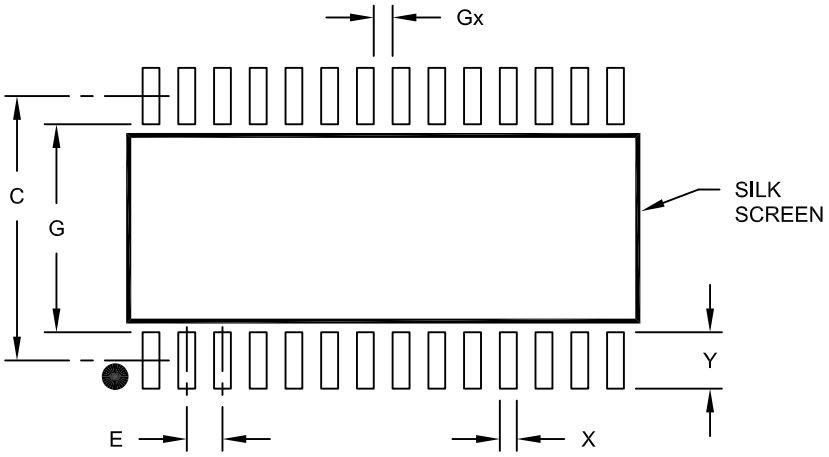
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

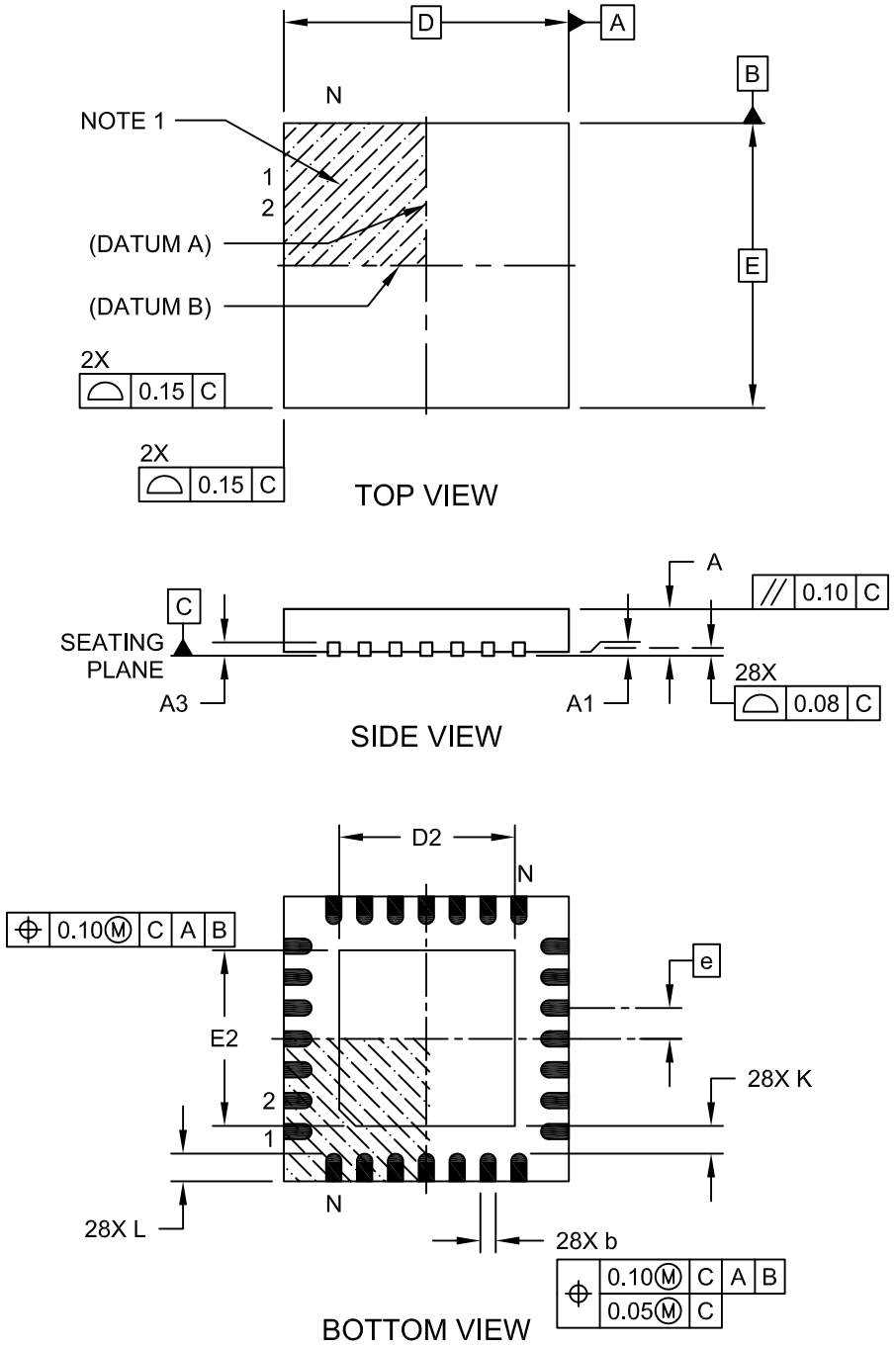
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-105C Sheet 1 of 2

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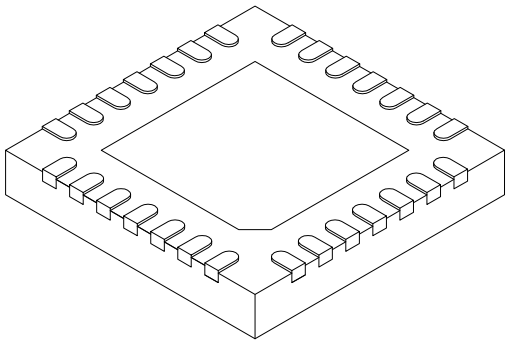
28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.50	0.55	0.70
Terminal-to-Exposed Pad	K	0.20	-	-

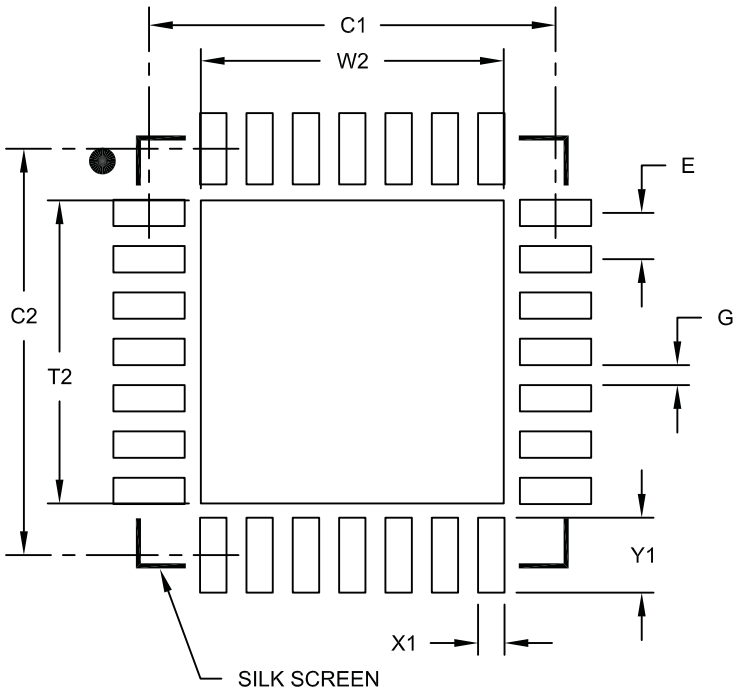
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

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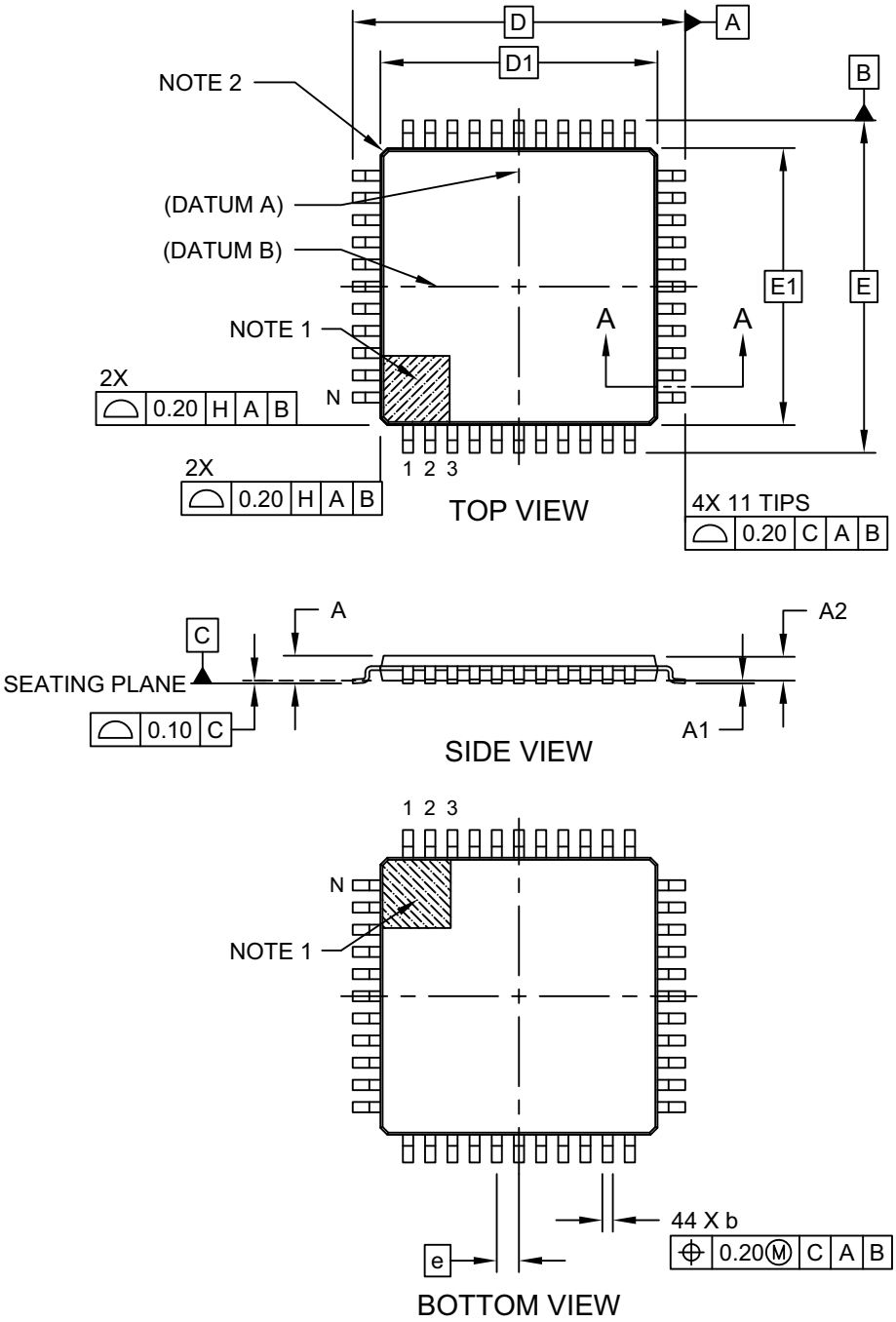
44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

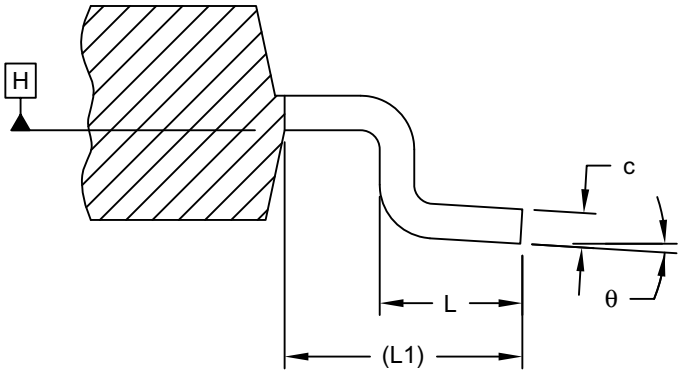
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



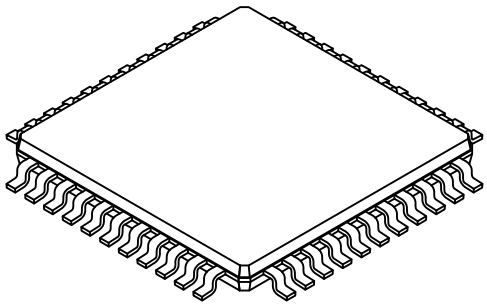
Microchip Technology Drawing C04-076C Sheet 1 of 2

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Width	E	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	θ	0°	3.5°	7°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2

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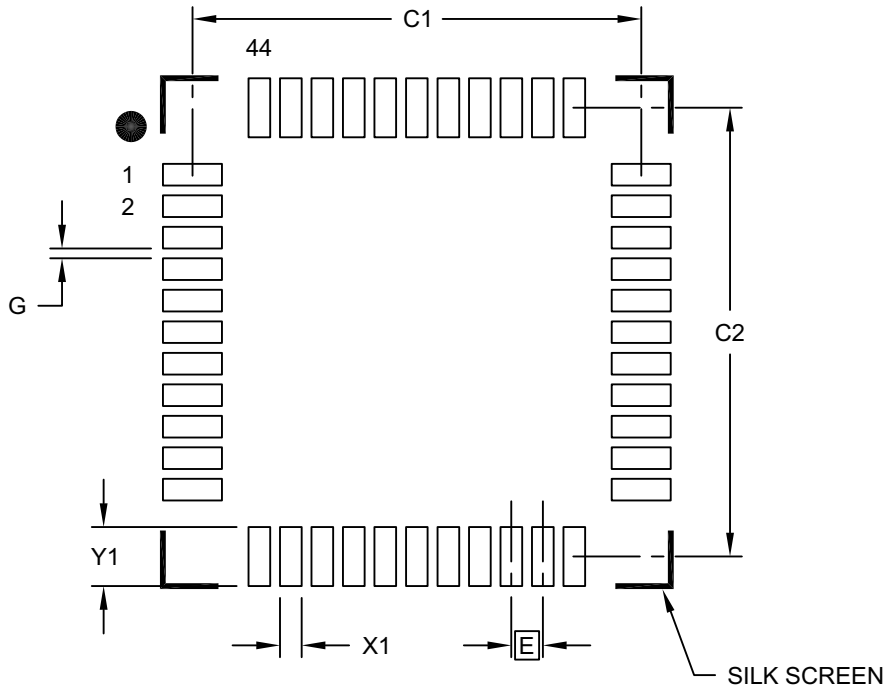
44-Lead Plastic Thin Quad Flatpack (PT) - 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

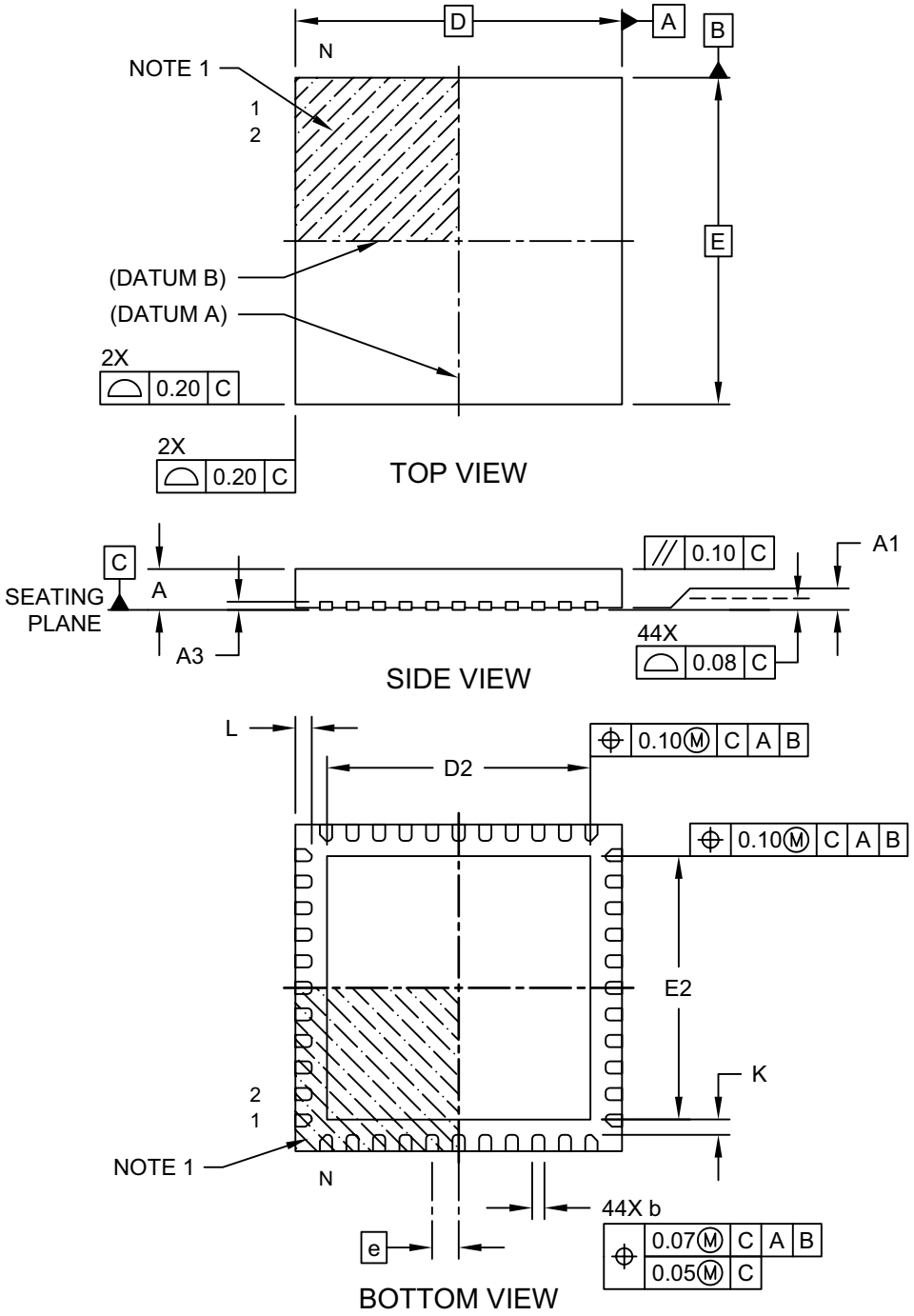
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103D Sheet 1 of 2

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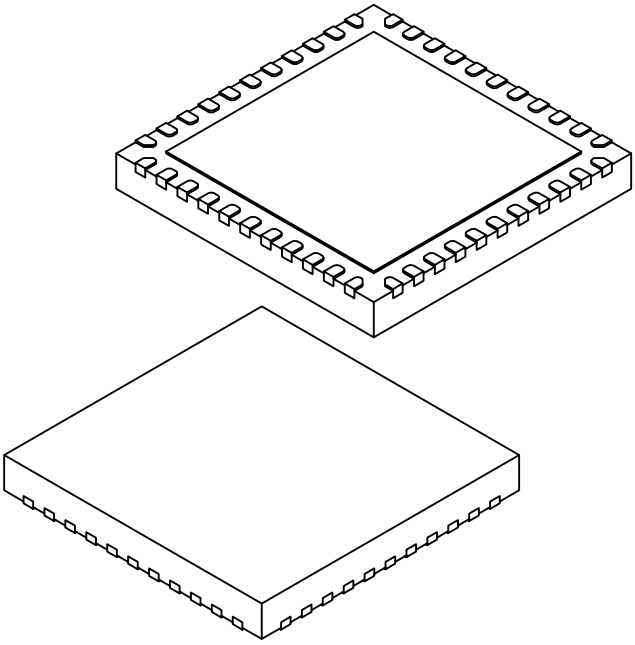
44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

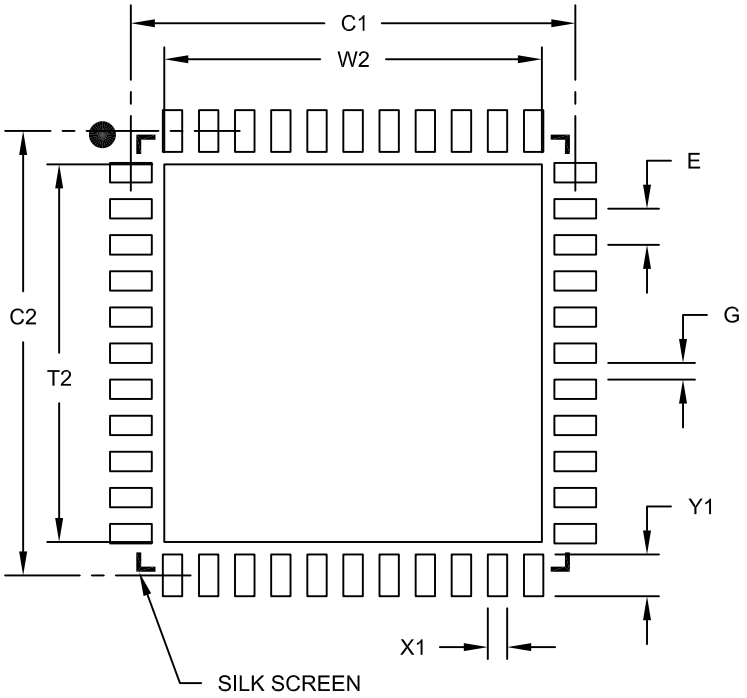
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

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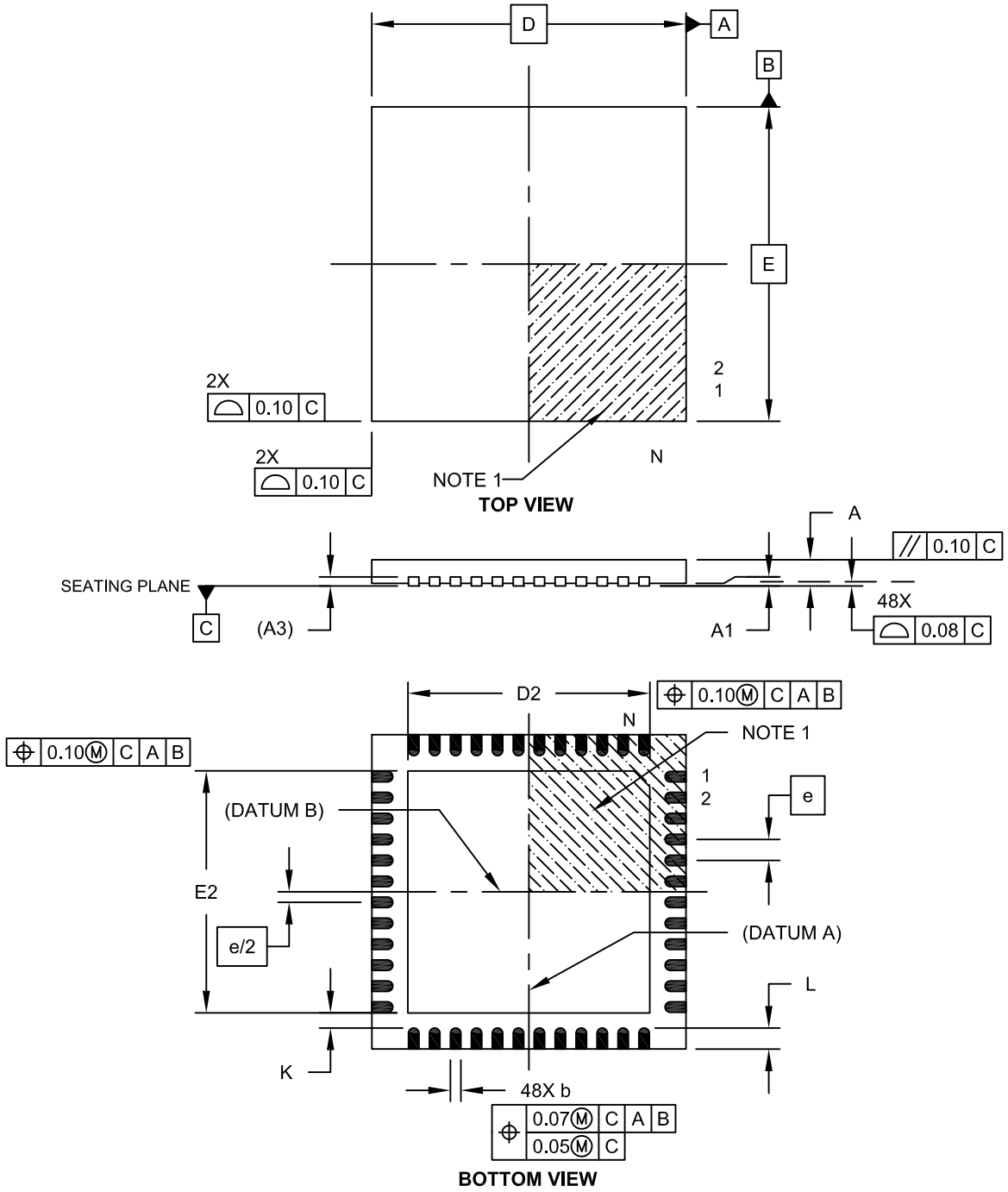
48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

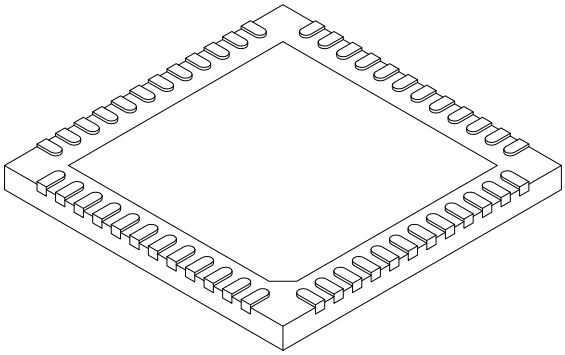
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-153A Sheet 1 of 2

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	48		
Pitch	e	0.40 BSC		
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.127 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	4.45	4.60	4.75
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.45	4.60	4.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2

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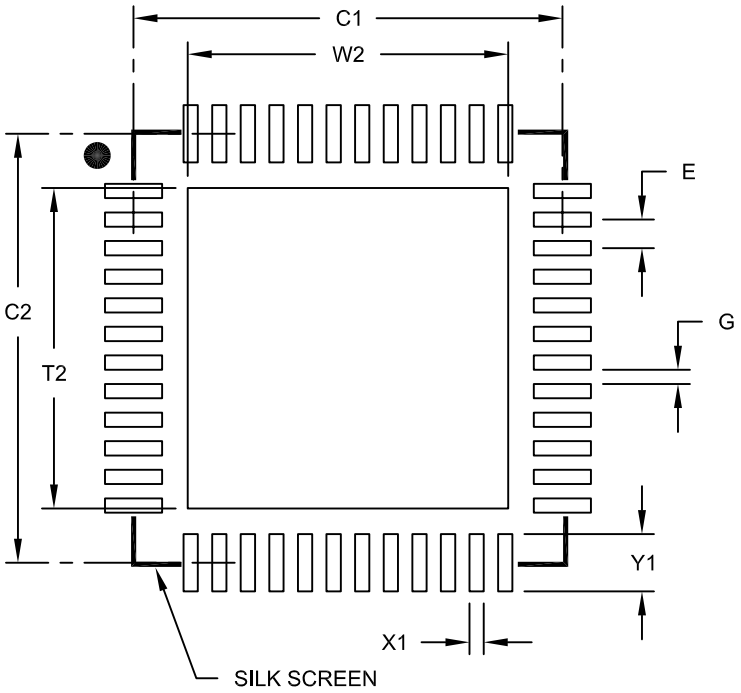
48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (February 2013)

Original data sheet for the PIC24FV16KM204 family of devices.

Revision B (July 2013)

Updates all references to PGCx and PGDx pin functions throughout the document to PGECx and PGEDx.

Updates **Section 4.0 "Memory Organization"** to change bit 12 in the following registers to reserved ("r" designation):

- CCP1CON1L (Table 4-8)
- CCP2CON1L (Table 4-9)
- CCP3CON1L (Table 4-10)
- CCP4CON1L (Table 4-11)
- CCP5CON1L (Table 4-12)

Updates **Section 13.0 "Capture/Compare/PWM/ Timer Modules (MCCP and SCCP)"**:

- Replaces bit 12 of CCPxCON1L (CCPSLP) and its description with a reserved bit
- Removes references to asynchronous operation in Sleep mode (and in other occurrences throughout the document)
- Modifies **Section 13.1 "Time Base Generator"** to add synchronous operation limitations; adds Table 13-1 to list valid clock options for all operating modes
- Removes the system clock as a time base input option
- Removes external input sources, comparators and CTMU as synchronization sources in Table 13-6; clarifies that other selected sources must be synchronous

Removes the input buffer from the band gap reference input in Figure 20-1.

Adds BUFCON0 register description (Register 20-2) to **Section 20.0 "8-Bit Digital-to-Analog Converter (DAC)"**.

Changes references to internal band gap voltages (V_{BG}, $V_{BG}/2$ and BGBUF0) in **Section 20.0 "8-Bit Digital-to-Analog Converter (DAC)"** and **Section 22.0 "Comparator Module"** to BGBUF1.

Adds minimum V_{DD} conditions for V_{BG} specification in Table 27-15 (Internal Voltage Regulator Specifications).

Other minor typographical corrections throughout the document.

Revision C (March 2020)

Updates the device name in the 20-Pin PDIP/SSOP/SOIC pin diagram to PIC24FV08KM101.

Removes all 20-Pin QFN information from the data sheet.

Adds AV_{DD} and AV_{SS} pin information to the 28-pin QFN pin diagram.

Updates the note references in Table 4-25.

Updates Table 8-2 with all new content.

Updates Example 6-2.

Changes all instances of POSCMD to POSCMOD.

Adds a third note to **Section 9.4.2 "Oscillator Switching Sequence"**.

Removes RTC content from the first paragraph in **Section 12.0 "Timer1"**.

Updates **Section 13.0 "Capture/Compare/PWM/ Timer Modules (MCCP and SCCP)"**:

- Adds additional MCCP/SCCP FRM information to the first note.
- Adds a note to Table 13-3.
- Updates the CLKSEL bit in Register 13-1.
- Updates multiple rows in Table 13-6.
- Changes the OCAEN bit in Register 13-4 from R/W-0 to R/W-1.

Adds additional MSSP FRM information to the first note in **Section 14.0 "Master Synchronous Serial Port (MSSP)"**.

Adds CLC FRM information to the beginning of **Section 17.0 "Configurable Logic Cell (CLC)"**.

Updates Register 17-4 with corrected inverted signal information.

Updates Capture/Compare Event or Timer information for SSRC bit in Register 19-1.

Corrects CHH, CSS and CTMEN bit locations in Register 19-6, Register 19-8 and Register 19-10.

Updates **Section 20.0 "8-Bit Digital-to-Analog Converter (DAC)"**:

- Removes the first note and removes the buffered output voltage bullet.

Changes the CREF bit range from CREF[4-3] to CREF[5-4] and increases the unimplemented bit range to 3-2 in Register 22-1.

Adds a note to **Section Register 25-4: "FOSC: Oscillator Configuration Register"**.

Updates the following tables in **Section 27.0 "Electrical Characteristics"**:

- Table 27-2, Table 27-4, Table 27-15, Table 27-17, Table 27-22 and Table 27-39.

Other minor typographical corrections throughout the document.

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PIC 24 FV 16 KM2 04 T - I / PT - XXX

- **Microchip Trademark**
- **Architecture**
- **Flash Memory Family**
- **Program Memory Size (Kbytes)**
- **Product Group**
- **Pin Count**
- **Tape and Reel Flag (if applicable)**
- **Temperature Range**
- **Package**
- **Pattern**

Architecture	24	= 16-bit modified Harvard without DSP
Flash Memory Family	F	= Standard voltage range Flash program memory
	FV	= Wide voltage range Flash program memory
Product Group	KM2	= General Purpose PIC24F Lite Microcontroller
	KM1	= General Purpose PIC24F Lite Microcontroller with Reduced Feature Set
Pin Count	01	= 20-pin
	02	= 28-pin
	04	= 44-pin
Temperature Range	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package	SP	= SPDIP
	SO	= SOIC
	SS	= SSOP
	ML	= QFN
	P	= PDIP
	PT	= TQFP
	MV	= UQFN
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample

Examples:

a) PIC24FV16KM204-I/ML: Wide Voltage Range, General Purpose, 16-Kbyte Program Memory, 44-Pin, Industrial Temp., QFN Package

b) PIC24F08KM102-I/SS: Standard Voltage Range, General Purpose with Reduced Feature Set, 8-Kbyte Program Memory, 28-Pin, Industrial Temp., SSOP Package

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ISBN: 978-1-5224-5856-2

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Fax: 34-91-708-08-91

Sweden - Gothenberg
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Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

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