Capture/Compare/PWM/Timer (MCCP and SCCP)

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.

Please consult the note at the beginning of the **"Capture/Compare/PWM/Timer Modules (SCCP/MCCP)"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Website at: http://www.microchip.com

1.0 INTRODUCTION

Select dsPIC33/PIC24 family devices include one or more Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 16-bit microcontrollers. They also provide the functionality of the comparable Input Capture, Output Compare and General Purpose Timer peripherals found in all other devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single output modules (SCCPs) provide only one PWM output. Multiple output modules (MCCPs) can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features.

- User-Selectable Clock Inputs, Including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for Module Interrupt Events or Triggers
- Synchronization Output Signal for Coordinating Other MCCP/SCCP Modules with User-Configurable Alternate and Auxiliary Source Options
- Fully Asynchronous Operation in All Modes and in Low-Power Operation
- Special Output Trigger for A/D Conversions
- 16-Bit and 32-Bit General Purpose Timer Modes with Optional Gated Operation for Simple Time Measurements
- Capture Modes:
  - Backward compatible with previous Input Capture peripherals of the dsPIC33/PIC24 families
  - 16-bit or 32-bit capture of time base on external event
  - Up to four-level deep FIFO capture buffer
  - Capture source input multiplexer
  - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM Modes:
  - Backward compatible with previous Output Compare peripherals of the dsPIC33/PIC24 families
  - Single Edge and Dual Edge Compare modes
  - Center-Aligned Compare mode
  - Variable Frequency Pulse mode
  - External Input mode

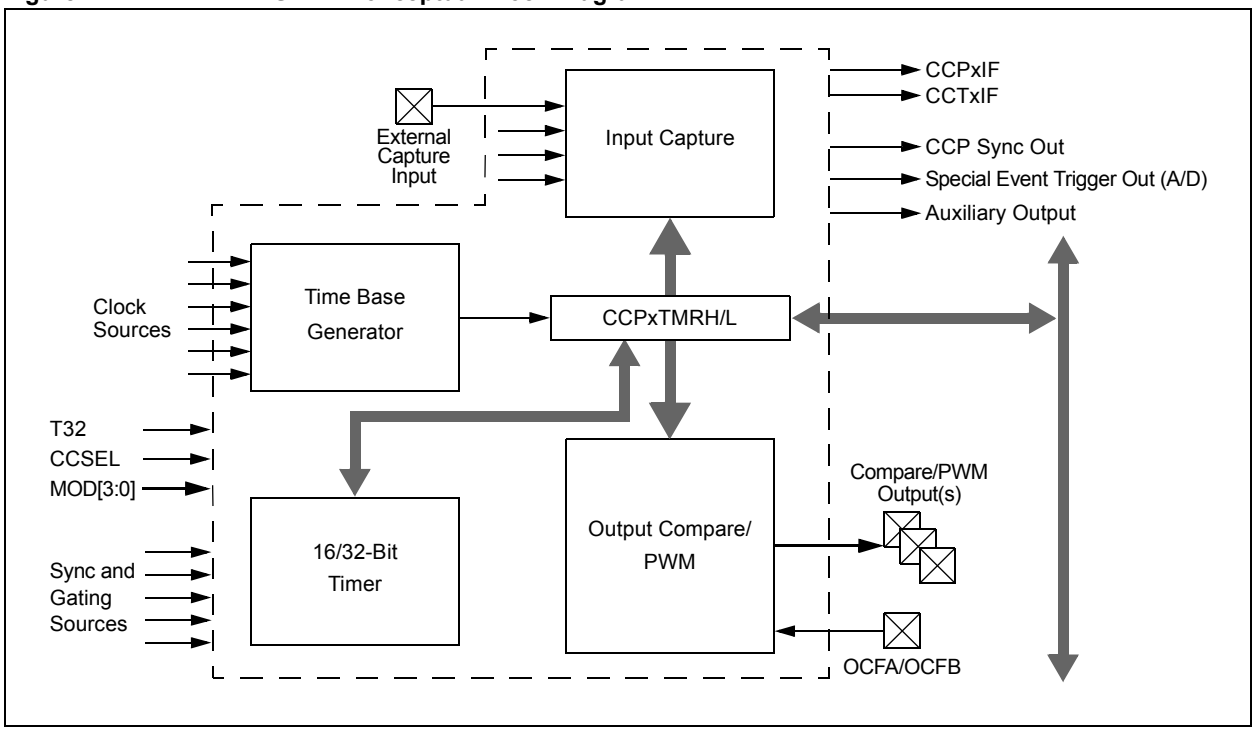
MCCP modules also include these extended PWM features:

- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) Modes
- Half-Bridge with Dead-Time Delay
- Push-Pull PWM Mode
- Output Scan Mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can be operated only in one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in Figure 1-1. All three modes use the Time Base Generator and the common Timer register pair (CCPxTMRH/L). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

Figure 1-1: MCCP/SCCP Conceptual Block Diagram



2.0 REGISTERS

Each MCCP/SCCP module has up to seven control and status registers and eight buffer/counter registers:

- CCPxTMRH and CCPxTMRL are the 32-Bit Timer/Counter register pair
- CCPxPRH and CCPxPRL are the 32-Bit Timer Period register pair
- CCPxRA is the 16-bit primary data buffer for Output Compare operations
- CCPxRB is the 16-bit secondary data buffer for Output Compare operations
- CCPxBUFH and CCPxBUFL are the 32-Bit Buffer register pair, which are used in Input Capture FIFO operations

3.0 REGISTER MAP

A summary of the registers associated with the CCP modules (MCCP and SCCP) is shown in Table 3-1. This represents the superset MCCP module; registers and individual bits that are not implemented in the SCCP module are noted.

Table 3-1: MCCP/SCCP Module Register Map

Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCPxCON1L	CCPON	—	CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]			TMRPS[1:0]		T32	CCSEL	MOD[3:0]				0000
CCPxCON1H	OPSSRC	RTRGEN	—	—	OPS[3:0]				TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]					0000
CCPxCON2L	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG[7:0]								0000
CCPxCON2H	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM[1:0]		—	AUXOUT[1:0]		ICS[2:0]			0100
CCPxCON3L	—	—	—	—	—	—	—	—	—	—	DT[5:0]						0000
CCPxCON3H	OETRIG	OSCNT[2:0]			—	OUTM[2:0}			—	—	POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]		0000
CCPxSTATL	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCPxTMRL	CCPx Time Base Register, Low Word																0000
CCPxTMRH	CCPx Time Base Register, High Word																0000
CCPxPRL	CCPx Period Register, Low Word																FFFF
CCPxPRH	CCPx Period Register, High Word																FFFF
CCPxRA	CCPx Primary Compare Register																0000
CCPxRB	CCPx Secondary Compare Register																0000
CCPxBUFL	CCPx Capture Buffer Register, Low Word																0000
CCPxBUFH	CCPx Capture Buffer Register, High Word																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Register 3-1: CCPxCON1L: Capture/Compare/PWMx Control 1 Low Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCPON	—	CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0](1)		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CCPON:** CCPx Module Enable
1 = Module is enabled with operating mode specified by MOD[3:0]
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CCPSIDL:** CCPx Stop in Idle Mode Bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **CCPSLP:** CCPx Sleep Mode Enable bit
1 = Module continues to operate in Sleep modes
0 = Module does not operate in Sleep modes

bit 11 **TMRSYNC:** Time Base Clock Synchronization bit
1 = Module time base clock is synchronized to internal system clocks; timing restrictions apply
0 = Module time base clock is not synchronized to internal system clocks

bit 10-8 **CLKSEL[2:0]:** CCPx Time Base Clock Select bits(1)
111 = Clock 7
110 = Clock 6
101 = Clock 5
100 = Clock 4
011 = Clock 3
010 = Clock 2
001 = Clock 1
000 = System Clock (TCY)

bit 7-6 **TMRPS[1:0]:** CCPx Time Base Prescale Select bits
11 = 1:64 Prescaler
10 = 1:16 Prescaler
01 = 1:4 Prescaler
00 = 1:1 Prescaler

bit 5 **T32:** 32-Bit Time Base Select bit
1 = 32-bit time base for timer, single edge Output Compare or Input Capture function
0 = 16-bit time base for timer, single edge Output Compare or Input Capture function

bit 4 **CCSEL:** Capture/Compare Mode Select bit
1 = Input Capture mode
0 = Output Compare/PWM or Timer mode (exact function selected by MOD[3:0] bits)

Note 1: Refer to the device data sheet for available clock sources for a specific device family.

Register 3-1: CCPxCON1L: Capture/Compare/PWMx Control 1 Low Register (Continued)

bit 3-0 **MOD[3:0]:** CCPx Mode Select bits

CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)

CCSEL = 0 (Output Compare modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS[2:0]
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode
0110 = Center-Aligned Pulse Compare mode, buffered
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode: Toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode: Drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode: Drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode: Output functions are disabled

Note 1: Refer to the device data sheet for available clock sources for a specific device family.

Register 3-2: CCPxCON1H: Capture/Compare/PWMx Control 1 High Register

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
OPSSRC(1)	RTRGEN(2)	—	—	OPS[3:0](3)			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0](3)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OPSSRC:** Output Postscaler Source Select bit(1)
1 = Output postscaler scales Special Event Trigger output events
0 = Output postscaler scales timer interrupt events

bit 14 **RTRGEN:** Retrigger Enable bit(2)
1 = Time base can be retriggered when CCPTRIG = 1
0 = Time base may not be retriggered when CCPTRIG = 1

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **OPS[3:0]:** CCPx Interrupt Output Postscale Select bits(3)
1111 = Interrupt every 16th time base period match
1110 = Interrupt every 15th time base period match
. . .
0100 = Interrupt every 5th time base period match
0011 = Interrupt every 4th time base period match or 4th Input Capture event
0010 = Interrupt every 3rd time base period match or 3rd Input Capture event
0001 = Interrupt every 2nd time base period match or 2nd Input Capture event
0000 = Interrupt after each time base period match or Input Capture event

bit 7 **TRIGEN:** CCPx Triggered Enable bit
1 = Triggered operation of timer is enabled
0 = Triggered operation of timer is disabled

bit 6 **ONESHOT:** One-Shot Mode Enable bit
1 = One-Shot Triggered mode is enabled; trigger duration is set by OSCNT[2:0]
0 = One-Shot Triggered mode is disabled

bit 5 **ALTSYNC:** CCPx Alternate Synchronization Output Signal Select bit
1 = An alternate signal is used as the module synchronization output signal
0 = The module synchronization output signal is the Time Base Reset/rollover event

bit 4-0 **SYNC[4:0]:** CCPx Synchronization Source Select bits(4)
11111 = Timer is in the Free-Running mode and rolls over at FFFFh (period register is ignored)
11110 = Timer is synchronized to Source #30
. . .
00001 = Time base is synchronized to Source #1
00000 = No external synchronization; timer rolls over at FFFFh or matches with period register

Note 1: Control bit has no function in Input Capture modes.
2: Control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.
4: Refer to the device data sheet for Sync sources for a specific device family.

Register 3-3: CCPxCON2L: Capture/Compare/PWMx Control 2 Low Register

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
PWMRSEN	ASDGM	—	SSDG	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASDG[7:0](1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
- 1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
- 0 = ASEVT bit must be cleared in software to resume PWM activity on output pins

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
- 1 = Waits until next Time Base Reset or rollover for shutdown to occur
- 0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
- 1 = Manually forces auto-shutdown, timer clock gate or Input Capture signal gate event (setting of ASDGM bit still applies)
- 0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG[7:0]:** CCPx Auto-Shutdown/Gating Source Enable bits(1)
- 1 = Auto-Shutdown/Gating Source n is enabled
- 0 = Auto-Shutdown/Gating Source n is disabled

Note 1: Refer to the device data sheet for the specific gating sources implemented for a device family.

Register 3-4: CCPxCON2H: Capture/Compare/PWMx Control 2 High Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICGSM[1:0]		—	AUXOUT[1:0](2)		ICS[2:0](3)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **OC[F:A]EN:** Output Enable/Steering Control bits(1)
1 = OCx pin is controlled by the CCPx module and produces an Output Compare or PWM signal
0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 7-6 **ICGSM[1:0]:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events.

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **AUXOUT[1:0]:** Auxiliary Output Signal on Event Selection bits(2)
11 = Input Capture or Output Compare event; no signal in Timer mode
10 = Signal output depends on module operating mode (see Table 8-2)
01 = Time base rollover event (all modes)
00 = Disabled

bit 2-0 **ICS[2:0]:** Input Capture Source Select bits(3)
111 = Capture Source 8
110 = Capture Source 7
101 = Capture Source 6
100 = Capture Source 5
011 = Capture Source 4
010 = Capture Source 3
001 = Capture Source 2
000 = Capture Source 1 (ICx pin)

Note 1: OCFEN through OCBEN (bits[13:9]) are implemented in MCCP modules only.
2: Auxiliary output is not implemented in all devices. Refer to the device data sheet for details.
3: Refer to the device data sheet for specific Input Capture sources.

Register 3-5: CCPxCON3L: Capture Compare PWMx Control 3 Low Register(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DT[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **DT[5:0]:** PWM Dead-Time Select bits

111111 = Inserts 63 dead-time delay periods between complementary output signals
111110 = Inserts 62 dead-time delay periods between complementary output signals
. . .
000010 = Inserts 2 dead-time delay periods between complementary output signals
000001 = Inserts 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: This register is implemented in MCCP modules only.

Register 3-6: CCPxCON3H: Capture/Compare/PWMx Control 3 High Register

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT[2:0]			—	OUTM[2:0](1)		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	POLBDF(1)	PSSACE[1:0]		PSSBDF[1:0](1)	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** PWM Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1), module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT[2:0]:** One-Shot Event Count bits
Extends the duration of a one-shot trigger event by an additional n clock cycles (n+1 total cycles)
111 = 7 timer count periods (8 cycles total)
110 = 6 timer count periods (7 cycles total)
101 = 5 timer count periods (6 cycles total)
100 = 4 timer count periods (5 cycles total)
011 = 3 timer count periods (4 cycles total)
010 = 2 timer count periods (3 cycles total)
001 = 1 timer count period (2 cycles total)
000 = Does not extend one-shot trigger event (the event takes 1 timer count period)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OUTM[2:0]:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 4 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit(1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 3-2 **PSSACE[1:0]:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in high-impedance state when a shutdown event occurs

bit 1-0 **PSSBDF[1:0]:** PWMx Output Pins, OCxB, OCxD, and OCxF, Shutdown State Control bits(1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in MCCP modules only.

Register 3-7: CCPxSTATL: Capture/Compare/PWMx Status Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	W1-0	W1-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
bit 7							bit 0

Legend:	C = Clearable Only bit		
R = Readable bit	W1 = Write ‘1’ Only bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **CCPTRIG:** CCPx Trigger Status bit
1 = Timer has been triggered and is running (set by hardware or writing to TRSET)
0 = Timer has not been triggered and is held in Reset (cleared by writing to TRCLR)

bit 6 **TRSET:** CCPx Trigger Set Request bit
Writes ‘1’ to this location to trigger the timer when TRIGEN = 1 (location always reads ‘0’).

bit 5 **TRCLR:** CCPx Trigger Clear Request bit
Writes ‘1’ to this location to cancel the timer trigger when TRIGEN = 1 (location always reads ‘0’).

bit 4 **ASEVT:** CCPx Auto-shutdown Event Status/Control bit
1 = A shutdown event is in progress; CCPx outputs are in the Shutdown state
0 = CCPx outputs operate normally

bit 3 **SCEVT:** Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred

bit 2 **ICDIS:** Input Capture Disable bit
1 = Event on Input Capture pin does not generate a capture event
0 = Event on Input Capture pin will generate a capture event

bit 1 **ICOV:** Input Capture Buffer Overflow Status bit
1 = The Input Capture FIFO buffer has overflowed
0 = The Input Capture FIFO buffer has not overflowed

bit 0 **ICBNE:** Input Capture Buffer Status bit
1 = Input Capture buffer has data available
0 = Input Capture buffer is empty

Register 3-8: CCPxTMRL: CCPx Time Base Low Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **TMRL[15:0]:** 16-Bit Time Base Value bits

Register 3-9: CCPxTMRH: CCPx Time Base High Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR[31:24]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **TMRH[31:16]:** 16-Bit Time Base Value bits

Register 3-10: CCPxPRL: CCPx Period Low Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PRL[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PRL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PRL[15:0]:** Period Register bits

Register 3-11: CCPxPRH: CCPx Period High Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PRH[31:24]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PRH[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PRH[31:16]:** Period Register bits

Register 3-12: CCPxRA: CCPx Primary Compare Register (Timer/Compare Modes Only)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMP[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMP[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CMP[15:0]:** Compare Value bits
The 16-bit value to be compared against the CCPx time base.

Register 3-13: CCPxRB: CCPx Secondary Compare Register (Timer/Compare Modes Only)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMP[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMP[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CMP[15:0]:** Compare Value bits
The 16-bit value to be compared against the CCPx time base.

Register 3-14: CCPxBUFL: CCPx Capture Buffer Low Register (Capture Modes Only)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUF[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUF[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **BUF[15:0]:** Compare Buffer Value bits
Indicates the oldest captured time base value in the FIFO.

Register 3-15: CCPxBUFH: CCPx Capture Buffer High Register (Capture Modes Only)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUF[31:24]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUF[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **BUF[31:16]:** Compare Buffer Value bits
Indicates the oldest captured time base value in the FIFO.

4.0 TIME BASE GENERATOR

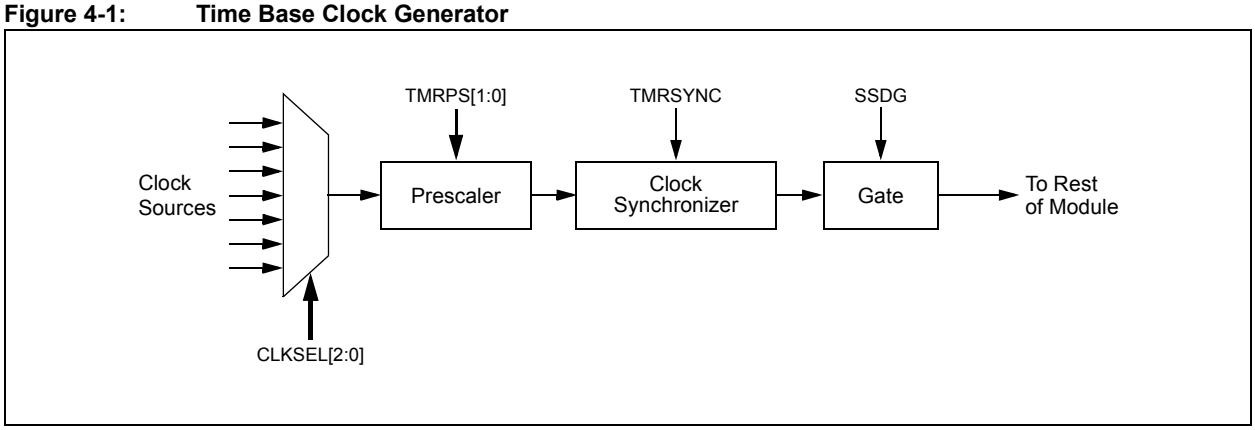
The Time Base Generator (TBG) provides a time base for the rest of the module using clock signals available on the microcontroller. This serves not only as the time base for the Timer modes, but also allows Input Capture and Output Compare pre-modes to operate without depending on another on-chip timer module.

Up to eight clock inputs are available to the clock generator, including the system clock (TCY) and other on-chip oscillator sources. Depending on the device, external clock inputs may also be available. A prescaler divides the selected clock source to a suitable frequency for use by the module.

The TBG has the ability to synchronize its operation with the selected clock source, subject to input timing restrictions or the module's operating conditions. Setting the TMRSYNC bit (CCPxCON1L[11]) enables synchronization of the time base with the clock input.

The TBG is shown in Figure 4-1.

Figure 4-1: Time Base Clock Generator



4.1 Gating Logic

The Time Base Generator incorporates a hardware gate that can disable the timer increment clock to the timer gate, which is available on Timer modes only.

Gating is controlled using the ASDG[7:0] control bits (CCPxCON2L[7:0]) and the SSDG bit (CCPxCON2L[12]). All of these bits are logically ORed together to generate a gating enable signal for the TBG.

Setting any one of the ASDGx bits enables its corresponding hardware trigger; any or all of the bits may be set to select multiple sources. The available sources for gating and auto-shutdown are device-dependent, and typically include such sources as comparator outputs, I/O pins (including OCFA and OCFB for PWM operation), software control and so on. Any output signal from any of the enabled sources disables the TBG output. Events are generally level-sensitive and not edge-triggered.

The SSDG bit is simply a gating source that can be manipulated in software. Setting SSDG has the same effect as an input from any of the hardware sources.

The gating feature is described in the following sections:

- Timer Gating (see **Section 5.3 "Clock Gating For Timer Modes"**)
- Auto-Shutdown for Output Compare, MCCP modules (see **Section 7.6.11 "Auto-Shutdown Control"**)
- Gated Input Capture (see **Section 6.4.1 "Input Capture Signal Gating"**)

Regardless of the operating mode, interrupt events are not generated by the CCP module based on the status of the gating inputs. If an interrupt is required for a gating event, the gating source itself must be used to generate the interrupt.

5.0 TIMER MODES

When CCSEL = 0 and MOD[3:0] = 0000, the module functions as a timer. There are two basic Timer modes, selected by the T32 bit (CCPxCON1L[5]); these are shown in Table 5-1. In either mode, the timer can operate as a free-running timer/counter, operate synchronously with other modules, or be triggered by other modules or external events.

Table 5-1: Timer Operating Modes

T32	Operating Mode
0	Dual Timer Mode (16-bit)
1	Timer Mode (32-bit)

5.1 Dual 16-Bit Timer Mode

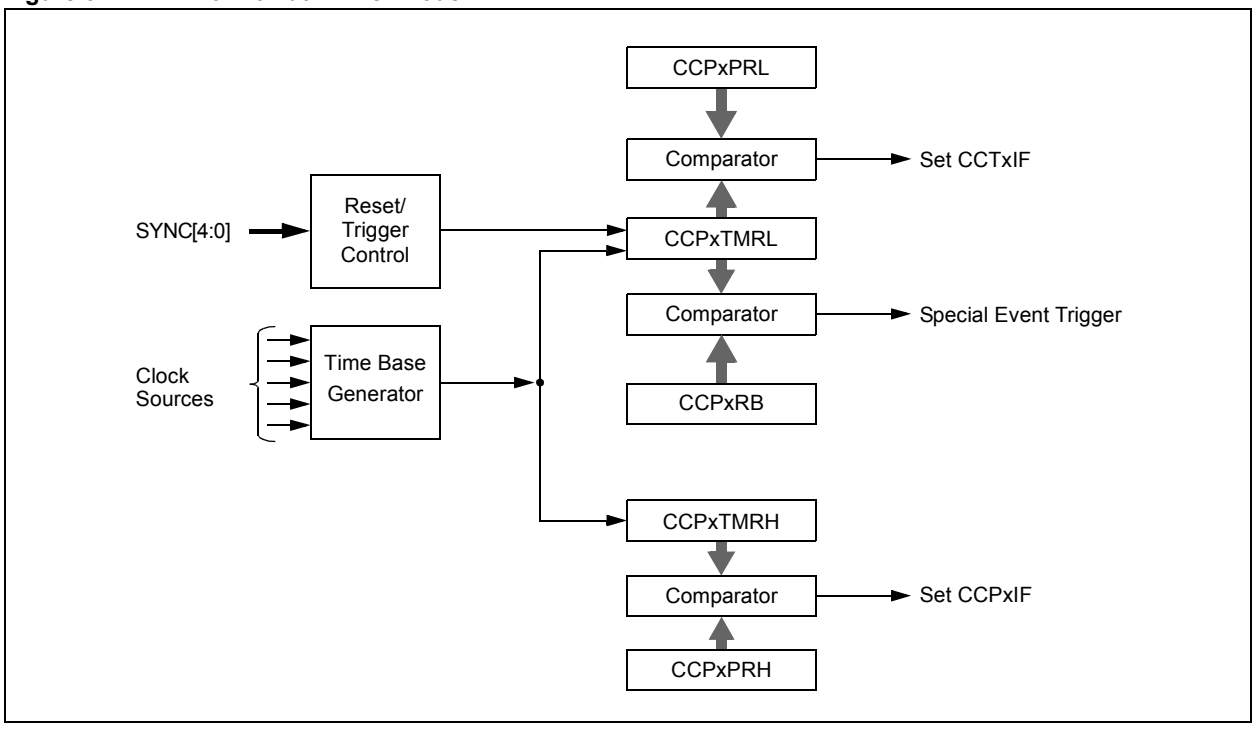
Dual 16-Bit Timer mode is selected when T32 = 0. This mode is useful for the following functions:

- Periodic CPU Interrupts
- Master Time Base Function for Synchronizing Other CCP Modules
- Triggering Periodic A/D Conversion
- Periodic Wake from Sleep (if an appropriate clock source is available)

Note: The CCPxTMRH/L registers may not be readable by the user if a high-speed asynchronous clock source is used to clock the time base. For a low-speed read, a double read can be done and the results compared.

Dual 16-Bit Timer mode provides a simple timer function with two independent 16-bit timer/counters, as shown in Figure 5-1. The primary timer, based on the lower word of the CCPxTMR pair (CCPxTMRL), is fully functional and can interact with other modules on the device. It can generate the CCP Sync signals for use by other MCCP modules. It can also use the SYNC[4:0] signal generated by other modules. The secondary timer, based on the upper word of CCPxTMR (CCPxTMRH), has limited functionality. It is intended to be used only as a periodic interrupt source for scheduling CPU events. It does not generate an output trigger signal like the primary time base.

Figure 5-1: 16-Bit Dual Timer Mode



Both the primary and secondary timers use the same clock source from the TBG, as selected by CLKSEL[2:0]. The CCPxTMRH/L registers provide user access to the two 16-bit time bases. Both Timer registers (CCPxTMRL and CCPxTMRH) increment at the same time, based on the timer input; however, only the primary timer (CCPxTMRL) can use the timer Sync functionality. The secondary timer (CCPxTMRH) does not have timer Sync functionality.

The CCPxPRL register controls the period for the primary 16-bit time base when SYNC[4:0] = 00000. When the module is configured to use an external synchronization source, the primary 16-bit time base is reset when the source selected by SYNC[4:0] is asserted. The module's Sync signal is generated whenever the time base rolls over or is reset to '0'.

The primary timer can generate the CCP interrupt when the value of CCPxTMRL resets to 0000h. When SYNC[4:0] = 00000, this occurs when CCPxTMRL matches CCPxPRL. If SYNC[4:0] is not '00000', CCPxTMRL resets and generates a CCT Interrupt Flag (CCTxIF) event whenever the signal selected by SYNC[4:0] is asserted.

The CCPxPRH register controls the count period of the secondary 16-bit timer. The secondary timer does not support external synchronization and is not affected by the selected SYNC[4:0] input. The secondary time base begins counting when the CCPON bit (CCPxCON1L[15]) is set. When a match occurs between the CCPxPRH register and the CCPxTMRH count value, the secondary 16-bit time base is reset and a timer rollover interrupt event (CCPxIF) is generated.

If either of the 16-bit timers is not used in the application, the timer can be disabled by writing 0000h to the corresponding period register. The timer is held in Reset, and no interrupts are generated, as long as the period register's value is 0. The CCPxPRH and CCPxPRL registers are not buffered in this operating mode.

To use the module in Dual 16-Bit Timer mode:

1. Set CCSEL = 0 to select the Time Base/Output Compare mode of the module.
2. Set T32 = 0 to select the 16-bit time base operation.
3. Set MOD[3:0] = 0000 to select the Time Base mode.
4. Set SYNC[4:0] to the desired time base synchronization source:
   - Configure and enable the external source selected by SYNC[4:0] before enabling the timer.
   - If the timer is not using an external Sync source (SYNC[4:0] = 00000), or if the module is synchronizing to itself (the SYNC[4:0] bits select the module's own value as a Sync source), write the desired count period of the primary 16-bit time base to CCPxPRL.
5. If the secondary timer is also being used, write a non-zero value to CCPxPRH to specify the count period.
6. If the special A/D trigger is being used, set CCPxRB for the desired trigger output time
7. Enable the module by setting the CCPON bit.
8. If an external synchronization source is selected in Step 4, configure and enable that source to allow the primary 16-bit time base to begin counting.

5.1.1 SPECIAL EVENT TRIGGER

In select devices, the Dual 16-Bit Timer mode can be used to generate a Special Event Trigger output signal. Refer to the device-specific data sheet's ADC trigger source for availability. The primary timer can be used to start A/D conversions and trigger other peripheral events. The trigger period is set by the value of the CCPxRB register and must be less than the counter period, as defined by the CCPxPRL register.

5.2 32-Bit Timer Mode

The 32-Bit Timer mode is selected when T32 = 1. In this mode, the CCPxTMRL and CCPxTMRH registers function together as a 32-bit timer. When CCPxTMRL overflows, CCPxTMRH increments by one.

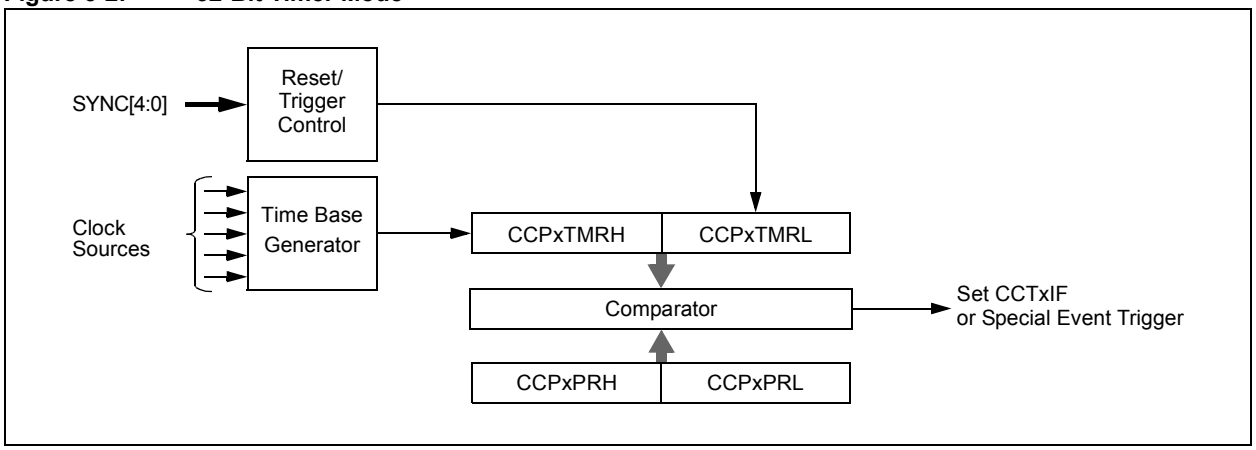
This mode provides a simple timer function when it is important to track long time periods. It is useful for the following functions:

- Periodic CPU Interrupts
- Synchronization and Trigger Generation for Other CCP Modules
- Periodic ADC Conversion Triggering
- Periodic Wake from Sleep (if an appropriate clock source is available)

No input or output functions are available from the CCP module in this operating mode.

Note:	To avoid reading during an overflow, read the CCPxTMRL register first to make certain that it is not about to roll over.

Figure 5-2: 32-Bit Timer Mode



When external synchronization is not selected (SYNC[4:0] = 00000), the CCPxPRH/L registers set the count period for the timer. A match between the CCPxTMR and the CCPxPRH registers also automatically generates the Sync output signal whenever the module is enabled (CCPON = 1).

To use the module in 32-Bit Timer mode:

1. Set CCSEL = 0 to select the Time Base/Output Compare mode of the module.
2. Set T32 = 1 to select the 32-bit time base operation.
3. Set MOD[3:0] = 0000 to select the Time Base mode.
4. Set SYNC[4:0] to the desired timer synchronization source:
   - Configure and enable the external source selected by SYNC[4:0] before enabling the timer.
   - If the timer is not using an external Sync source (SYNC[4:0] = 00000), or if the module is synchronizing to itself (SYNC[4:0] selects the module's own value as a Sync source), write the desired count period of the primary 16-bit time base to CCPxPRL/H.
5. Enable the module by setting the CCPON bit.

5.3 Clock Gating For Timer Modes

When operating in Timer mode, time base gating can be used to gate the timer's operation (see **Section 4.1 "Gating Logic"** for more information). This function provides a simple way to measure the time of an external event. Timer clock gating is enabled whenever one or more of the ASDG[7:0] bits (CCPxCON2L[7:0]) is set, or when the SSDG bit (CCPxCON2L[12]) is set.

6.0 INPUT CAPTURE MODES

When CCSEL = 1, the module is configured for Input Capture mode. This mode is used to capture a timer value from an independent timer base on the occurrence of an event on an input pin. This mode is useful in applications requiring frequency (time period) and pulse measurement.

Input Capture mode uses the CCPxTMR registers as a dedicated 16/32-bit synchronous, up counting timer used for event capture. This value is written to the FIFO buffer when a capture event occurs. The internal value may also be read with a synchronization delay from the CCPxTMR registers.

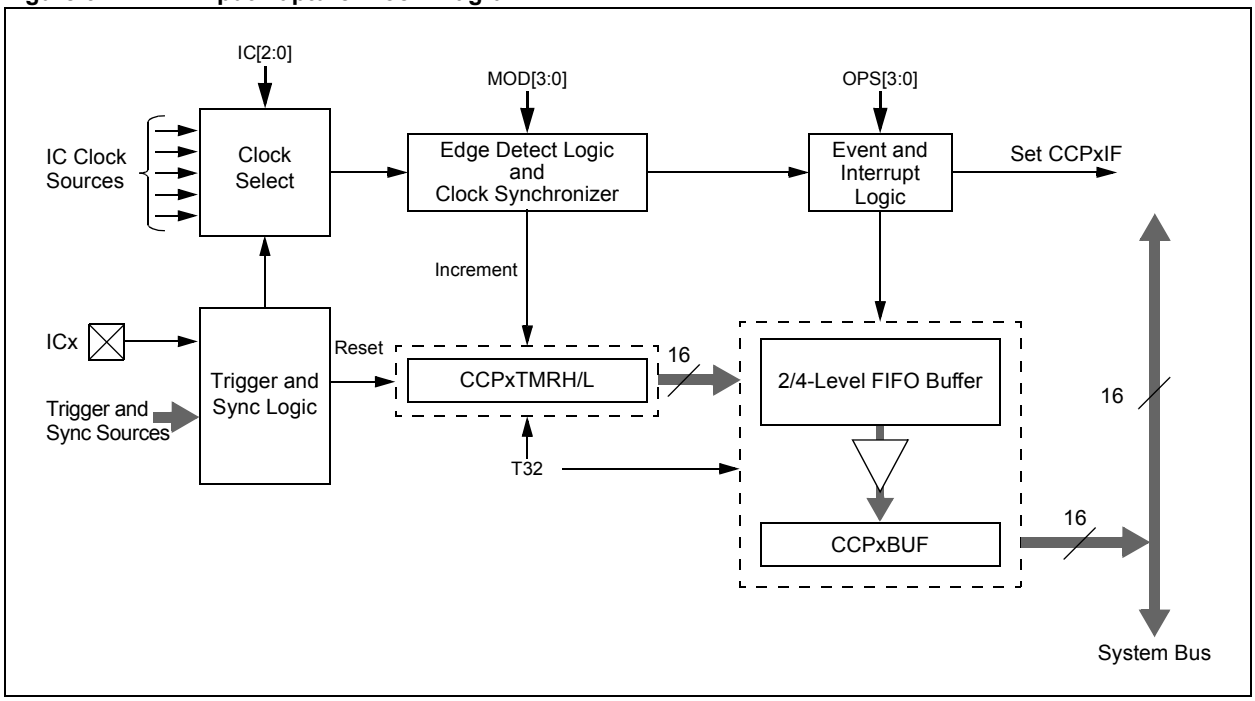
Input Capture mode is the only major mode available when CCSEL is set. The T32 and the MOD[3:0] bits determine the various Capture modes, as shown in Table 6-1.

Figure 6-1 provides a simplified block diagram of the Input Capture mode.

Table 6-1: Capture Modes

T32 (CCPxCON1L[5])	MOD[3:0] (CCPxCON1L[3:0])	Operating Mode
0	0000	Edge Detect (16-bit capture)
1	0000	Edge Detect (32-bit capture)
0	0001	Every Rising (16-bit capture)
1	0001	Every Rising (32-bit capture)
0	0010	Every Falling (16-bit capture)
1	0010	Every Falling (32-bit capture)
0	0011	Every Rise/Fall (16-bit capture)
1	0011	Every Rise/Fall (32-bit capture)
0	0100	Every 4th Rising (16-bit capture)
1	0100	Every 4th Rising (32-bit capture)
0	0101	Every 16th Rising (16-bit capture)
1	0101	Every 16th Rising (32-bit capture)

Figure 6-1: Input Capture Block Diagram



6.1 Initialization

Since the module can be used for Input Capture/Output Compare/PWM, selecting the correct operation required should be the first task. The best practice is to clear all the associated control registers.

When the CCP module is reset or disabled (CCPON = 0):

- The ICOV and ICBNE status flags are cleared
- CCPxBUFH/L and their FIFO buffer are cleared
- CCPxTMRH/L are reset to zero
- The capture prescaler counter is reset to zero
- The capture event counter for interrupt generation is reset to zero

6.1.1 MODE SELECTION

As with Timer and Output Capture/PWM modes, the MOD[3:0] bits selects the Capture mode and prescaler options. To avoid inadvertent interrupts, always disable the module by clearing the CCPON bit when changing Capture modes. It is recommended to set the CCSEL bit and configure the MOD[3:0] bits in a single operation, before enabling the module.

6.1.2 TIMER CLOCK SOURCE SELECTION

dsPIC33/PIC24 family devices may have one or more Input Capture channels. Each channel can select between one of eight clock sources for its time base by using the CLKSEL[2:0] bits (CCPxCON1L[10:8]), as described in **Section 4.0 "Time Base Generator"**. The module can be set to use the system clock source (FOSC/2) or use an external clock source applied at the TxCK pin, with Synchronization mode enabled, in the timer. The Input Capture pin (ICx) should be selected for Input Capture operation. It is recommended that the clock source be selected before enabling the module and not be changed during operation.

Refer to the specific device data sheet for the available timer inputs.

6.1.2.1 32-Bit Input Capture Support

The Input Capture modes have the ability to operate with a 32-bit time base. The 32-bit mode is selected by setting the T32 bit. All Input Capture functions are the same between 16-bit and 32-bit modes, with these changes in 32-bit operations:

- CCPxTMR is a 32-bit register (CCPxTMRH and CCPxTMRL)
- CCPxBUF is a 32-bit register (CCPxBUFH and CCPxBUFL)
- The FIFO buffer only has two levels available in 32-bit operating mode.

Example 6-1 shows a typical procedure for setting up Input Capture mode.

Example 6-1: Setup for Input Capture Mode (Every Rising Edge)

```
CCP1CON1Lbits.CCSEL=1;      // Input capture mode
CCP1CON1Lbits.CLKSEL=0;     // Set the clock source (Tcy)
CCP1CON1Lbits.T32=0;        // 16-bit Dual Timer mode
CCP1CON1Lbits.MOD= 1;       // Capture ever rising edge of the event
CCP1CON2Hbits.ICSEL= 0;     // Capture rising edge on the Pin
CCP1CON1Hbits.IOPS=0;       // Interrupt on every input capture event
CCP1CON1Lbits.TMRPS=0;      // Set the clock pre-scaler (1:1)
CCP1CON1Lbits.CCPON=1;      // Enable CCP/input capture
```

6.2 Capture Event Modes

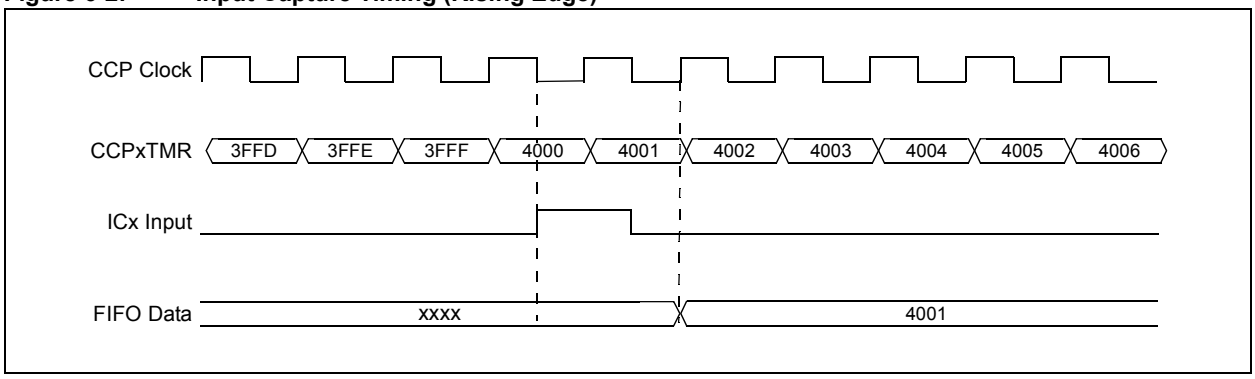
The module can capture a timer value on any of the following ICx pin transitions:

- Every rising edge (MOD[3:0] = 0001)
- Every falling edge (MOD[3:0] = 0010)
- Every rising and falling edge (MOD[3:0] = 0000, 0011)

Since the Input Capture pin is sampled on the falling edge of the timer clock when the prescaler is not used, the capture pulse width must be greater than the timer clock period, plus some margin.

Because of internal synchronization requirements, the timer value captured will be up to 1.5 CCP clock cycles after the time of the actual capture edge event, as shown in Figure 6-2.

Figure 6-2: Input Capture Timing (Rising Edge)

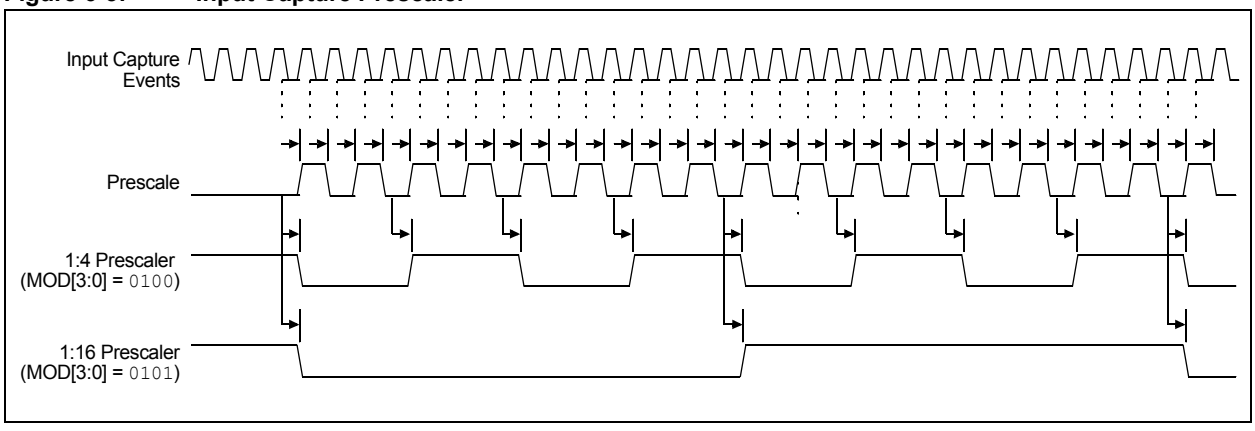


6.2.1 INPUT CAPTURE PRESCALER

Using the input prescaler, the Input Capture module can capture a timer value on every 4th edge (MOD[3:0] = 0100) or every 16th edge (MOD[3:0] = 0101) of the ICx input pin.

The capture pulse-width requirements are different than those for Simple Capture mode. Please refer to the specific device data sheet for the exact specification. Because of synchronization requirements inside, the timer value captured will be one to two timer clock cycles after the time of the edge capture, as shown in Figure 6-3.

Figure 6-3: Input Capture Prescaler



6.2.2 EDGE DETECT (HALL SENSOR) MODE

Edge Detect mode (MOD[3:0] = 0000) operates the same as Capture Every Edge mode (MOD[3:0] = 0011), except that capture interrupt events do not stop when the Input Capture Buffer Overflow Status (ICOV) flag becomes set. This allows a continuous stream of capture events to trigger interrupt events without the need to continuously empty the FIFO.

6.2.3 INPUT CAPTURE BUFFER

The Input Capture FIFO buffer is up to four levels deep, depending on the Capture mode selected. For 16-bit timer captures, there are four levels in the FIFO (16-bit wide); for 32-bit timer captures, there are two levels (32-bit wide). The number of capture events required to generate a CPU interrupt can be selected by the user.

There are two status flags that provide status on the FIFO buffer. The ICBNE status bit (CCPxSTATL[0]) indicates that at least one capture event has occurred. The ICOV status bit (CCPxSTATL[1]) indicates that there have been more events than the buffer's current depth (four in 16-bit mode, two in 32-bit mode). These status flags operate the same for 16-bit capture operations and 32-bit capture operations.

While the CCP module is in Reset or not in Capture mode:

- The ICOV status flag is cleared
- The ICBNE status flag is cleared
- The FIFO is marked as empty
- A read of the FIFO buffer will return '0'

The ICBNE status flag is set on the first capture event and remains set until all capture events have been read from the FIFO. For example, if three capture events have occurred, then three reads of the Capture FIFO buffer are required before the ICBNE flag will be cleared. Each read of the FIFO buffer will allow the remaining word(s) to move to the next available top location of the FIFO.

In the event that the FIFO buffer is full with capture events, and another capture event occurs prior to a read of the FIFO, an overflow condition will occur and the ICOV bit becomes set. In addition, the capture event which caused the overflow is not recorded and subsequent capture events will not be placed into the FIFO until the overflow condition is cleared by completely emptying the FIFO.

Overflow conditions cannot occur when the module is not in an Input Capture mode or when Edge Detect mode is enabled (MOD[3:0] = 0000).

Clearing of the overflow condition can be accomplished in one of the following ways:

1. Disable the module by clearing the CCPON bit.
2. Read the Input Capture buffer until ICBNE = 0 (twice for 32-bit captures, four times for 16-bit captures).
3. Clear the ICOV bit in software. This effectively discards all previously stored data in the FIFO by resetting the Data Pointers to the beginning of the FIFO buffer. Clearing the ICOV in software also causes the ICBNE bit to be cleared automatically.
4. Perform a device Reset.

Upon clearing the overflow condition, the ICOV and ICBNE status flags are cleared and the capture channel resumes normal operation. If the module is disabled, and then re-enabled in Input Capture mode later, the FIFO buffer contents will be undefined, and a read will yield indeterminate results.

In the event that a FIFO read is performed after the last read and no new capture event has been received, the FIFO Read and Write Pointers will be pointing to the first buffer location of the FIFO. A read of the FIFO will return the value held in the first buffer location.

The FIFO Pointer is adjusted whenever the most significant word of the buffer result is read by the CPU. This allows the results of a 32-bit Input Capture to be read by the 16-bit CPU.

6.3 Input Capture Interrupts

While in Input Capture mode, the module has the ability to generate an interrupt upon capture event. A capture event is defined by writing a timer value to the FIFO.

The OPS[3:0] control bits (CCPxCON1H[11:8]) select the interrupt postscaler, specifying the number of capture events that must occur before an interrupt is generated. Options range from an interrupt on every capture, to every fourth capture. The first capture event is defined as the capture event occurring after a mode change from the disabled state (CCPON = 0) or after ICBNE = 0.

On buffer overflow, the capture events cease and the interrupts stop unless OPS[3:0] = 0000 (interrupt on every capture). Clearing the FIFO by reading it also clears the internal interrupt counter and may affect when an interrupt is generated.

Applications often use the Input Capture pins as auxiliary external interrupt sources. In Edge Detect mode, interrupts occur regardless of FIFO overflow, as specified by OPS[3:0]. There is no need to perform a dummy read on the Input Capture buffer to clear the event, so as to prevent an overflow and inhibit all future interrupts.

For example, assume that OPS[3:0] = 0001, specifying an interrupt on every 2nd capture event. The following sequence of events will produce a single CCPxIF, as shown:

1. Turn on module; event count = 0.
2. Capture first event; FIFO contains one entry, event count = 1.
3. Read FIFO; FIFO is empty, event count = 0.
4. Capture second event; FIFO contains one entry, event count = 1.
5. Capture third event; FIFO contains two entries, event count = 2, set CCPxIF.
6. Clear interrupt count when interrupt is set (event count = 0).
7. Capture fourth event; FIFO contains three entries, event count = 1.
8. Read FIFO three times; FIFO is empty, interrupt count = 0.
9. Capture fifth event; FIFO contains one entry, event count = 1.
10. Read FIFO; FIFO is empty, event count = 0.

6.3.1 TIMER INTERRUPTS IN INPUT CAPTURE MODES

The module produces both timer interrupts (CCTxIF) as well as capture interrupts (CCPxIF) while operating in Input Capture mode. However, the timer interrupts only occur at the timer rollover, from FFFFh to 0000h, since there is no period register available to set the count period. If a shorter timer count period is desired, a second MCCP module, or external timer may be used to provide a synchronization source for the Input Capture time base.

6.4 Input Capture Operation with Synchronization and Triggering

By default, the MCCP module in Input Capture mode operates with a free-running timer. The CCPxPRH/L registers are not available to set a different timer period in Input Capture mode. It is recommended to keep SYNC[4:0] configured as '11111' to maintain the free-running timer.

The timer will be held at 0000h under either of these conditions:

- Triggered operation is enabled (TRIGEN = 1) and a trigger event has not occurred (CCPTRIG = 0).
- An external Sync source has been selected (SYNC[4:0] has a value other than '11111'), which has not been enabled.

In either case, Input Capture input events will occur; however, a value of 0000h will always be captured in the FIFO. For these reasons, triggered operation and externally synchronized operation are not recommended.

6.4.1 INPUT CAPTURE SIGNAL GATING

The Input Capture source can optionally be gated by software or hardware to allow windowed capture measurements. This feature provides noise immunity in sensing applications.

The ICDIS bit (CCPxSTATL[2]) provides the status of the input signal gating function. When the ICDIS bit is cleared, capture events generated by the edge detect logic are allowed. When the ICDIS bit is set, events from the edge detect logic are inhibited.

The time base gating logic is used for Input Capture signal gating (see **Section 4.1 "Gating Logic"** for more information). The ASDG[7:0] control bits (CCPxCON2L[7:0]) select one or more input sources that are used to clear the ICDIS status/control bit. The SSDG bit (CCPxCON2L[12]) may also be used to manually gate Input Capture signals in software.

The behavior of the ASDGx sources and the SSDG bit depends on the Gating Source mode, which is selected using the ICGSM[1:0] control bits (CCPxCON2H[7:6]). Three different options are available:

- When ICGSM[1:0] = `00`, gating is level-sensitive. A low input level from the gating source disables subsequent capture events and the ICDIS bit will be set to reflect this. A high input level enables subsequent capture events and the ICDIS bit will be cleared to reflect this.
- When ICGSM[1:0] = `01`, gating occurs with a rising edge of the gating source; the ICDIS bit is cleared, disabling subsequent capture events. This is a One-Shot mode; subsequent edges from the gating source will have no effect.
- When ICGSM[1:0] = `10`, gating occurs on the falling edge of the gating source; the ICDIS bit is set, enabling subsequent capture events. This is a One-Shot mode; subsequent edges from the gating source will have no effect.

Figure 6-4 shows the timing for gated capture events. Input events are sampled on the falling edge of the clock source. The example assumes that the Input Capture module is configured to capture every rising and falling edge (MOD[3:0] = `0011`).

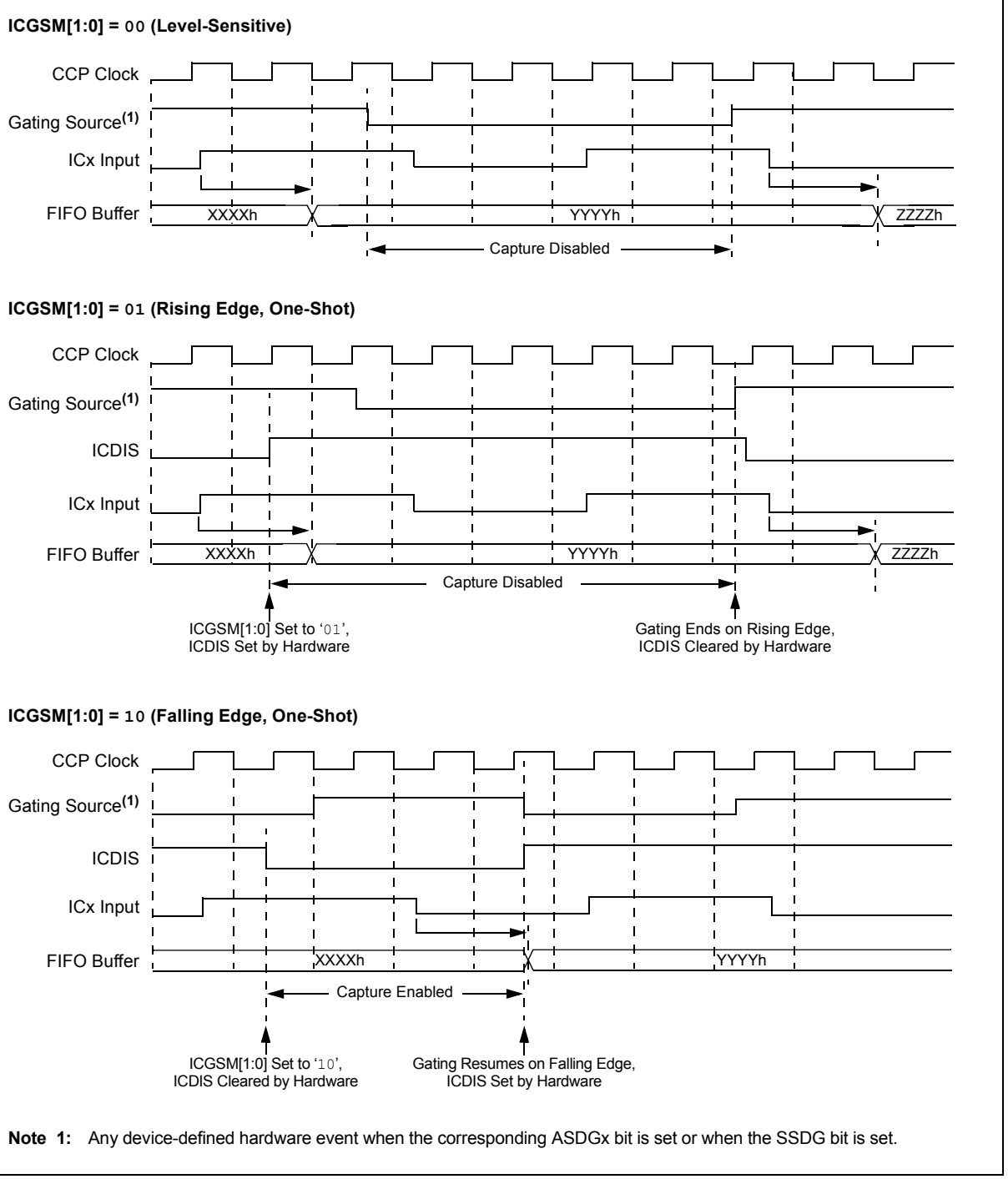
In the One-Shot modes, the edge detect logic is set to look for the appropriate edge event; the ICDIS bit remains set or clear (depending on the mode) until that type of event occurs. The user may re-arm the gating logic after a gating event by rewriting ICGSM[1:0]. This act of writing to these bits (even if the same value) resets the gate signal edge detection logic and also resets the ICDIS status bit to the appropriate value.

To use Input Capture gating:

1. Select and configure the gating source.
2. Enable the appropriate gating signal source(s) using the ASDG[7:0] bits; alternatively, set or clear the SSDG bit during the event for software only control.
3. Select the Gating mode using ICGSM[1:0].
4. Configure the module for the desired Input Capture mode and input source using the MOD[3:0] and ICS[2:0] control bits. The module is now armed for a gate event.

The next valid rising or falling input signal edge (depending on Capture mode), after ICDIS is cleared, will trigger a capture event.

Figure 6-4: Gated Input Capture Examples



Note 1: Any device-defined hardware event when the corresponding ASDGx bit is set or when the SSDG bit is set.

7.0 OUTPUT COMPARE AND PWM MODES

When CCSEL = 0 and the MOD[3:0] bits are any value other than '0000', the module operates in Output Compare mode.

Table 7-1 summarizes the various Output Compare modes.

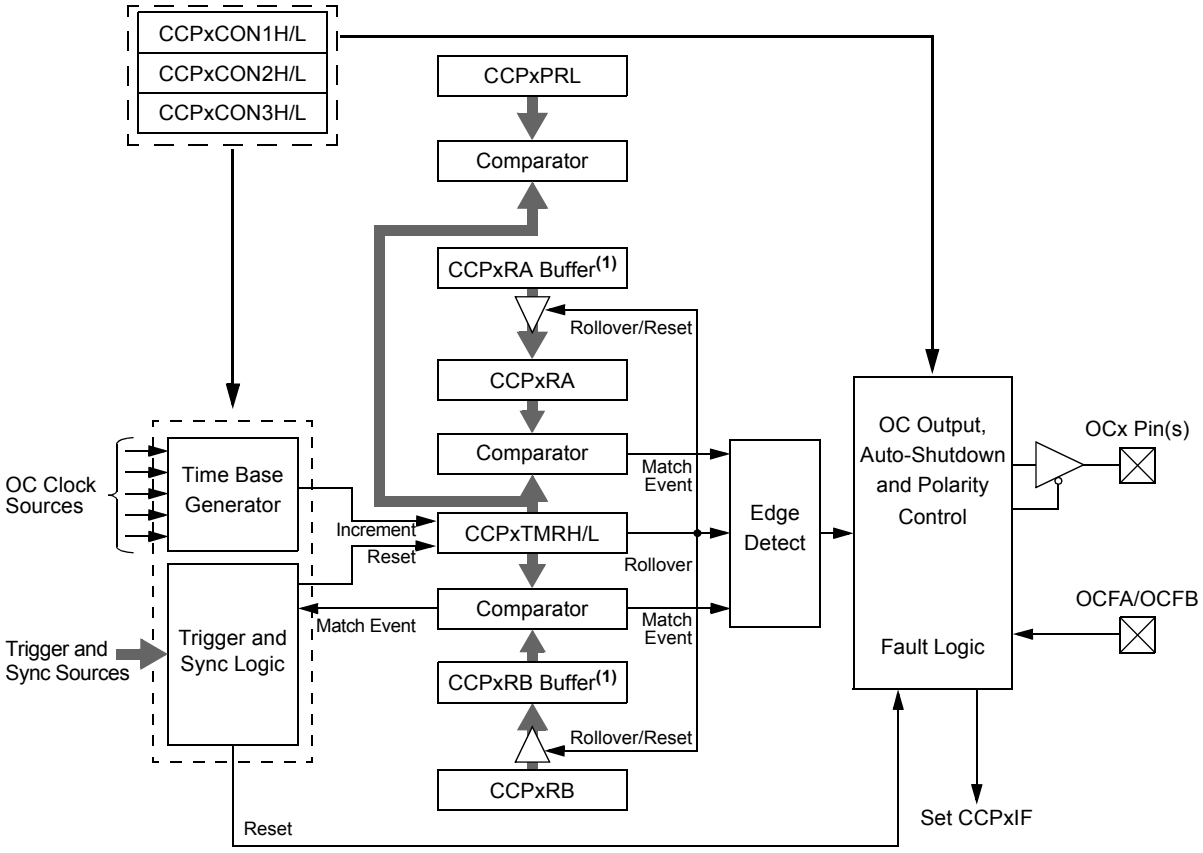
Table 7-1: Output Compare/PWM Modes

T32	MOD[3:0]	Operating Mode
0	0001	Output High on Compare (16 bit), Single Edge mode
1	0001	Output High on Compare (32 bit), Single Edge mode
0	0010	Output Low on Compare (16 bit), Single Edge mode
1	0010	Output Low on Compare (32 bit), Single Edge mode
0	0011	Output Toggle on Compare (16 bit), Single Edge mode
1	0011	Output Toggle on Compare (32 bit), Single Edge mode
0	0100	Dual Edge Compare (16-bit), Dual Edge mode
0	0101	Dual Edge Compare (16-bit buffered), PWM mode
0	0110	Center-Aligned Pulse (16-bit buffered), Center PWM mode
0	0111	Variable Frequency Pulse (16-bit)

The value of CCPxTMR is compared to one or two Compare registers, depending on its mode of operation. Output Compare mode can generate a single output transition, or a train of output pulses, and can generate interrupts on match-on-compare events. Figure 7-1 outlines the components used in Output Compare mode.

Like many previous dsPIC33/PIC24 modules, Output Compare mode can function as a PWM generator. In MCCP modules, multiple PWM outputs can be used for power or motor control applications.

Figure 7-1: Output Compare Block Diagram



Note 1: Buffered Output Compare and PWM modes only.

7.1 Single Edge Output Compare Modes

When MOD[3:0] = 0001, 0010 or 0011, the selected Output Compare channel is configured for these Single Output Compare Match modes:

- Compare forces pin high (MOD[3:0] = 0001)
- Compare forces pin low (MOD[3:0] = 0010)
- Compare toggles pin (MOD[3:0] = 0011)

In Single Compare mode, the CCPxRA register is used. The register is loaded with a value and is compared to the module Timer register. A CPU interrupt is generated on each compare event.

Single Edge Compare mode uses these Timer/Data registers:

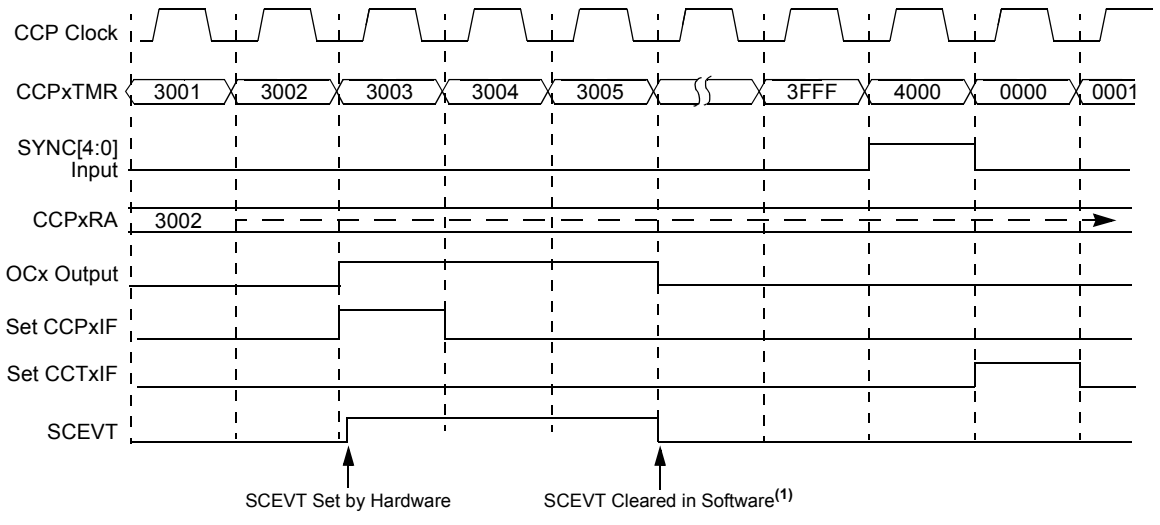
- CCPxTMRL as the Timer register (16-bit mode)
- CCPxTMRH/L as the Timer register pair (32-bit mode)
- CCPxRA as the Compare Value register (16-bit mode)
- CCRxRB:CCPxRA as the Compare Value register (32-bit mode)
- CCPxPRL as the Timer Period register (16-bit mode only)

7.1.1 SINGLE EDGE COMPARE MODE (HIGH OUTPUT)

In this mode (see Figure 7-2), the output pin is initially driven low, and remains low until a match occurs between the timer and CCPxRA register. The key timing events to note are:

- The output pin is driven high, one clock period after a match occurs between the Timer and CCPxRA registers. The output pin remains high until a mode change has been made or the module is disabled.
- The timer counts up until it rolls over, or until the selected SYNC[4:0] input is asserted (depending on the value of SYNC[4:0]), and then resets to 0000h on the next clock.
- The compare interrupt signal (to set CCPxIF) is asserted and the output pin is driven high.
- The timer interrupt signal (to set CCTxIF) is asserted for one clock period on a Time Base Reset or rollover event.

Figure 7-2: Single Compare Mode (High Output)



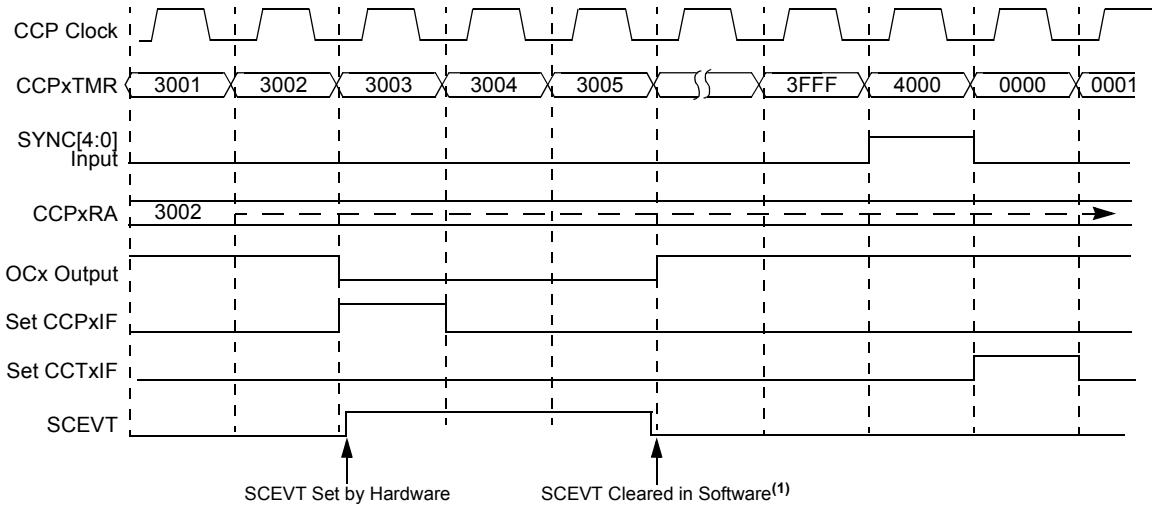
Note 1: SCEVT has to be cleared to enable the next capture.

7.1.2 SINGLE COMPARE MODE (LOW OUTPUT)

Once the Compare mode has been enabled (Figure 7-3), the output pin will initially be driven high, and remain high until a match occurs between the timer and CCPxRA register. The key timing events to note are:

- The output pin is driven low, one clock period after a match occurs between the timer and CCPxRA registers. The output pin remains low until a mode change has been made or the module is disabled.
- The timer counts up until it rolls over, or until the selected SYNC[4:0] input is asserted, and then resets to 0000h on the next clock.
- The compare interrupt signal (to set CCPxIF) is asserted and the output pin is driven low.
- The timer interrupt signal (to set CCTxIF) is asserted for one clock period on a Time Base Reset or rollover event.

Figure 7-3: Single Compare Mode (Low Output)



Note 1: SCEVT has to be cleared to enable the next capture.

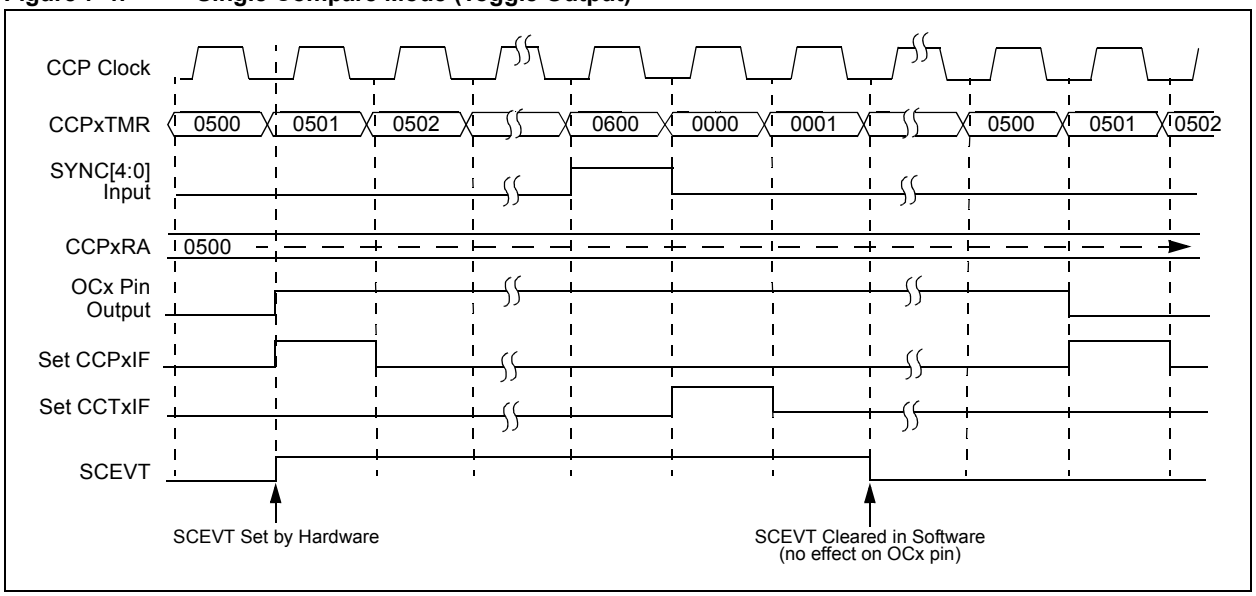
7.1.3 SINGLE COMPARE MODE (TOGGLED OUTPUT)

Once this Compare mode has been enabled (Figure 7-4), the output pin is initially driven low, and then toggled on each subsequent match event between the timer and CCPxRA register. The key timing events to note are:

- The state of the output pin is toggled, one clock period after a match occurs between the timer and CCPxRA registers. The output pin remains at its new state until the next toggle event, until a mode change has been made or the module is disabled.
- The timer counts up until it rolls over, or until the selected SYNC[4:0] input is asserted, and then resets to 0000h on the next clock.
- The respective channel interrupt output (CCPxIF) is asserted when the output pin is toggled.
- The time base interrupt signal (CCTxIF) is generated on a Timer Reset or rollover event.

Note:	The internal OCx pin output logic is set to a logic '0' on a device Reset; however, the initial output pin state for the Toggle mode can be reversed using the POLACE polarity control bit.

Figure 7-4: Single Compare Mode (Toggle Output)



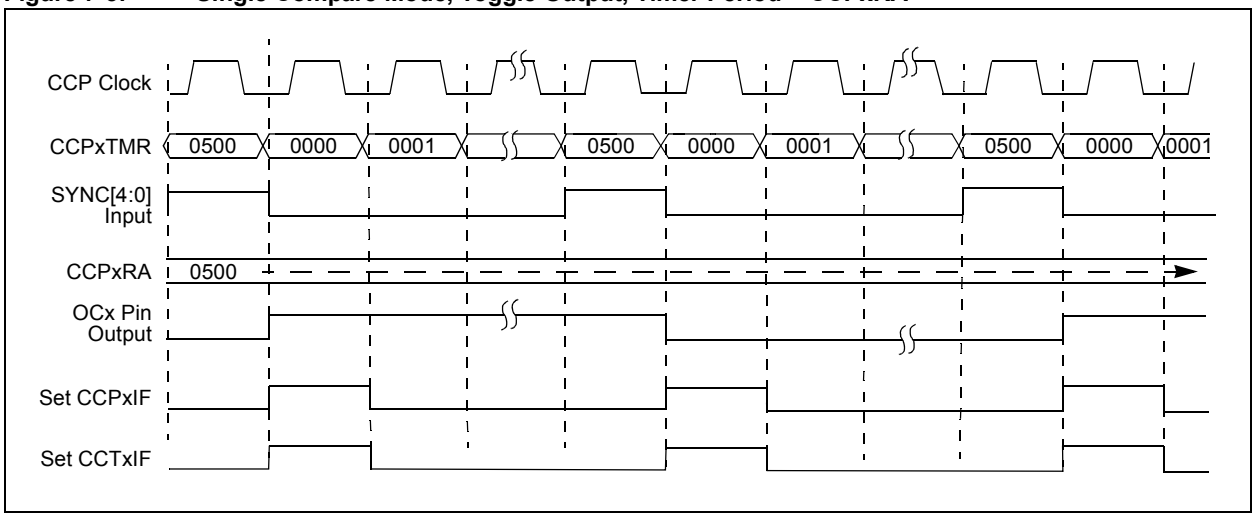
7.1.4 SPECIAL CASES OF SINGLE COMPARE MODE

In Single Edge Compare modes, there are several special cases to consider:

1. When the value of CCPxRA is greater than the timer period, the compare value will always be greater than the timer value. No compare event will ever occur and the compare output will remain at the initial condition.
2. When the value of CCPxRA equals the timer period, the compare interval is the same as the timer period. Combined with Toggle mode, this can be used to generate a fixed frequency square wave (Figure 7-5).
3. When CCPxRA = 0000h, the timer is held in Reset, either by an asserted trigger source or when CCPTRIG = 0 is the triggered operation. The compare output will remain at the initial condition. The compare output will change once the selected trigger source is deasserted, allowing the timer to operate.
4. If CCPxRA is cleared after a compare event, the SYNC[4:0] signal is asserted and the compare output will remain at its previous state.
5. If, after a compare event, the CCPxRA register is modified to a value greater than the current timer value, but less than the timer period, a second compare event will be generated within the count period. The SCEVT bit must also be cleared when MOD[3:0] is '0001' or '0010' to reset the output pin for the next compare event.

Note:	For all special cases, 'timer period' can be defined as either a CCPxPR match or an event by the selected SYNC[4:0] source.

Figure 7-5: Single Compare Mode, Toggle Output, Timer Period = CCPxRA



7.1.5 SINGLE EDGE OUTPUT COMPARE EVENT STATUS

The SCEVT bit (CCPxSTATL[3]) indicates the status of a single edge compare event and allows the application to re-arm a single edge compare event without changing the module operating mode or resetting the module. It only functions during single edge compare events; in all other modes, the bit always reads as '0'.

When MOD[3:0] = 0001, the OCx pin is asserted high after a compare event and SCEVT is set to '1' by hardware. The application may clear SCEVT in software. Once the bit is cleared, the OCx pin is reset to a low output and the compare logic is reset to allow the next rising edge compare event.

When MOD[3:0] = 0010, the OCx pin is asserted low after a compare event and SCEVT is set to '1' by hardware. The application may clear SCEVT in software. Once the bit is cleared, the OCx pin is reset to a high output and the compare logic is reset to allow the next falling edge compare event.

When MOD[3:0] = 0011, the OCx pin is toggled after a compare event and SCEVT is set to '1'. The application may clear SCEVT in software, but the state of the OCx pin will not change when the bit is cleared. In this mode, SCEVT only provides event status information and does not affect the OCx pin.

When MOD[3:0] = 0001 or 0010, the application may set SCEVT to '1' to inhibit single edge Output Compare events. This feature is useful when it is desired to delay an edge event during a particular interval, for example. No changes will occur to the OCx pin during this time. When the SCEVT bit is cleared by software, the OCx output pin will be reset to the initial state and a rising or falling edge will be generated when the next compare event occurs.

7.1.5.1 32-Bit Operation with Single Compare Modes

The previous examples all assume 16-bit single compare operations (T32 = 0). Single Edge Compare modes can also operate with a 32-bit time base, selected by setting T32 = 1. Operation in 32-bit mode is identical, except that the CCPxRB register is paired with CCPxRA to provide a 32-bit compare value for CCPxTMRH/L. CCPxRA is used for the upper 16 bits of the compare value.

No period register is available to set the count period of CCPxTMR. If a count period less than FFFF FFFFh is desired, the module can be synchronized to an external source to set the count period.

7.2 Dual Edge Compare Mode

When MOD[3:0] = 0100, the Output Compare channel is configured to produce a continuous series of pulses. The parameters for the pulse train are determined by the CCPxRA, CCPxRB and CCPxPRL registers.

Dual Edge Compare mode is only available in 16-bit mode. The T32 bit has no affect.

Dual Edge Compare mode uses these Timer/Data registers:

- CCPxTMRL as the Timer register
- CCPxRA for the Rising Edge Value register
- CCPxRB for the Falling Edge Value register
- CCPxPRL for the Timer Period register

Figure 7-6 depicts the signal timing for Dual Edge Compare mode. The typical operation in this mode is as follows:

1. When Dual Edge Compare mode is enabled, the pin state is driven low. At some point, the timer is enabled (triggered) by a hardware or software event to start the count process.
2. Upon the first timer compare match with Compare register, CCPxRA, the output pin will be driven high.
3. When the incrementing timer count matches Compare register, CCPxRB, the second and trailing edge (high-to-low) of the pulse is driven onto the output pin. At this second compare, the Output Compare Interrupt Flag (CCPxIF) is generated.
4. The Timer Interrupt Flag (CCTxIF) is generated, along with the CCP Sync signal, when the timer rolls over (when SYNC[4:0] = 00000) or an event defined by SYNC[4:0].
5. The output pulses continue repeatedly until the mode is terminated by the application or a device Reset.

This is the prototype case, where the timer period and the match registers are all different values, ordered as (Timer Period > CCPxRB > CCPxRA). There are special cases, however, where the conditions differ, resulting in a specific type of output. The cases are listed in Table 7-2, and are described in the following sections.

Figure 7-6: Typical Dual Edge Compare Timing Sequence

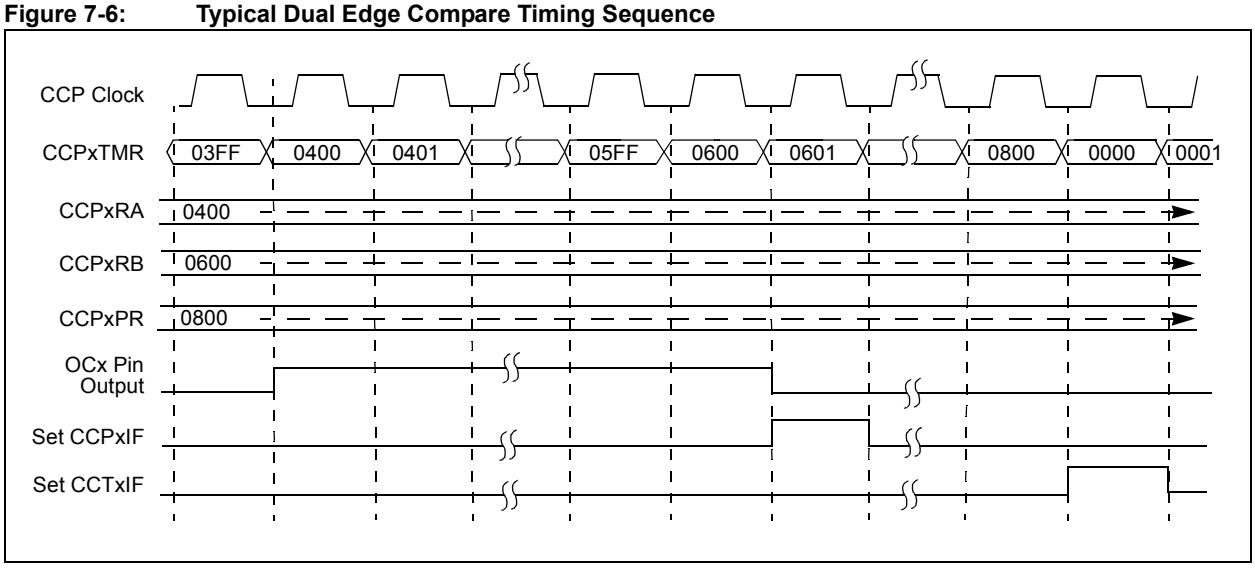


Table 7-2: Special Conditions for Dual Edge Compare Operations

Condition	Output	Output Compare Interrupt on Falling Edge of OCx Pin	Timer Interrupt When Timer Matches Period
CCPxRA = CCPxRB	No output, OCx pin remains low	None	Yes
CCPxRA = CCPxRB + 1	One pulse	Yes	Yes
Timer Period < CCPxRA(1)	No output	N/A(2)	Yes
Timer Period = CCPxRB(1)	OCx goes low at CCPxRB	Yes	Yes
Timer Period < CCPxRB(1)	Continuous high	None	Yes
Timer Period = CCPxRB, CCPxRA = 0(1)	CCP goes high when TMR = 1 and goes low when CCPxRB matches timer	Yes	Yes
CCPxRA > CCPxRB	Pulse train	Yes	Yes

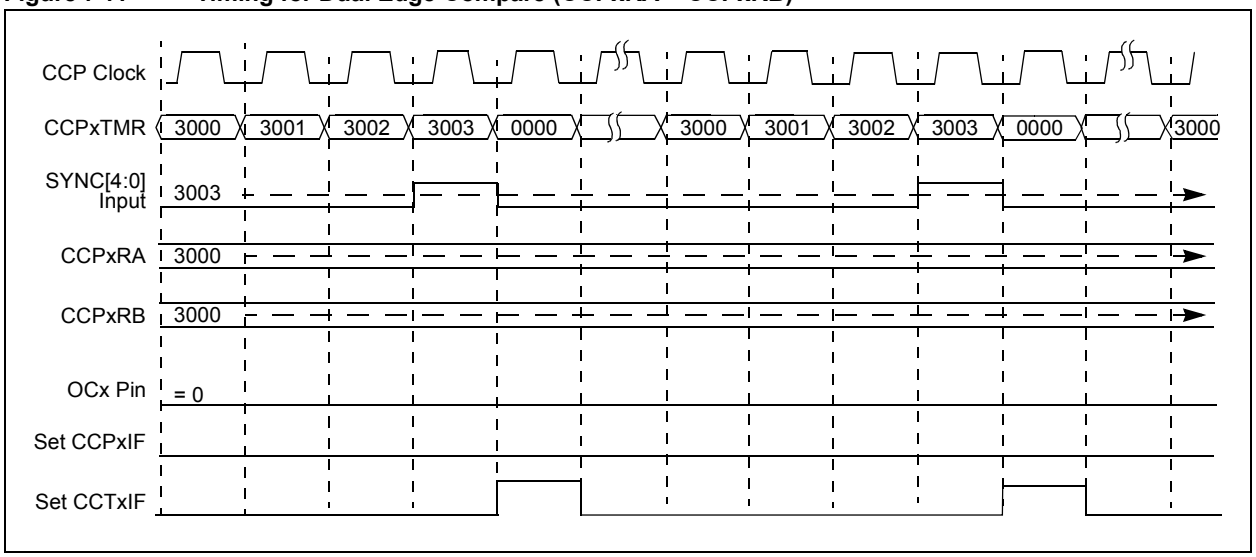
Note 1: Timer period is either the period register value or when the timer is reset by the input selected by SYNC[4:0].

2: If CCPxRB is also less than the timer period, an interrupt will be generated, even though there is no activity on the OCx pin.

7.2.1 CCPxRA = CCPxRB

If CCPxRA and CCPxRB have the same value, the output is initialized low and stays low; no pulses are generated and no Output Compare interrupt is generated (Figure 7-7). Put another way, the PWM duty cycle is 0. The Reset/clear-on-CCPxRB match logic overrides the set-on-CCPxRA match logic for a net result of no change in the output state.

Figure 7-7: Timing for Dual Edge Compare (CCPxRA = CCPxRB)



7.2.2 CCPXRB = CCPXRA + 1

When the value of CCPxRB is one greater than the value of CCPxRA, and both registers are less than the period register, an output pulse that is one CCP clock cycle wide is generated.

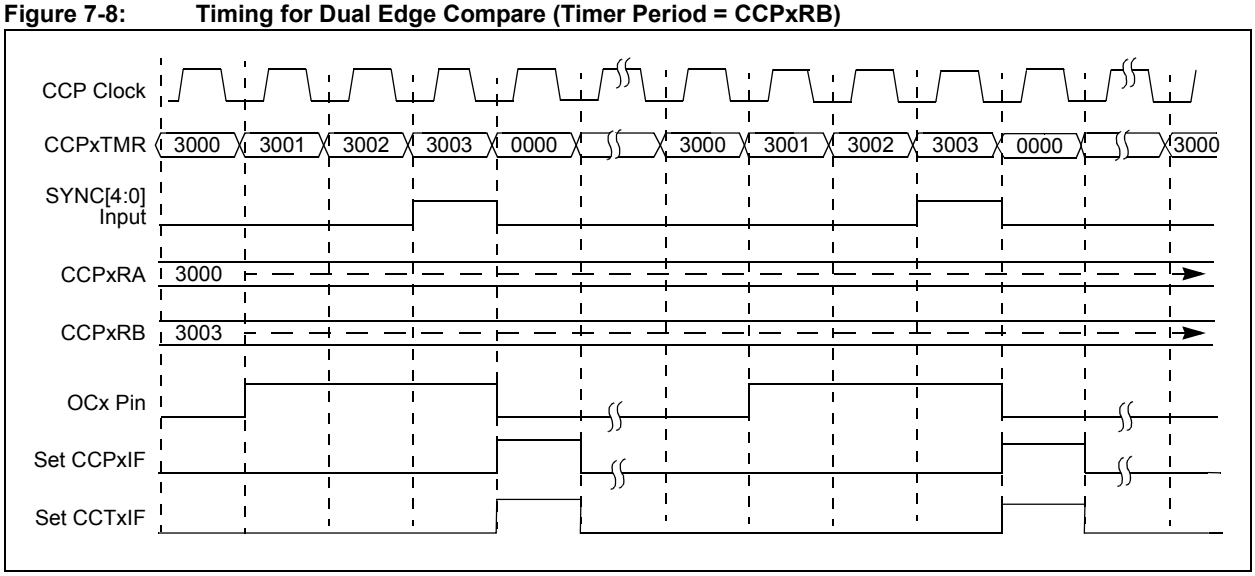
7.2.3 TIMER PERIOD < CCPxRA

When the value of CCPxRA is greater than the timer period, no output pulses are generated.

7.2.4 TIMER PERIOD = CCPxRB

The module will still generate the high-to-low transition when the value of CCPxRB equals the timer period. This is true whether the period is determined in Sync operation from an external source (as shown in Figure 7-8) or on a match with CCPxPRL.

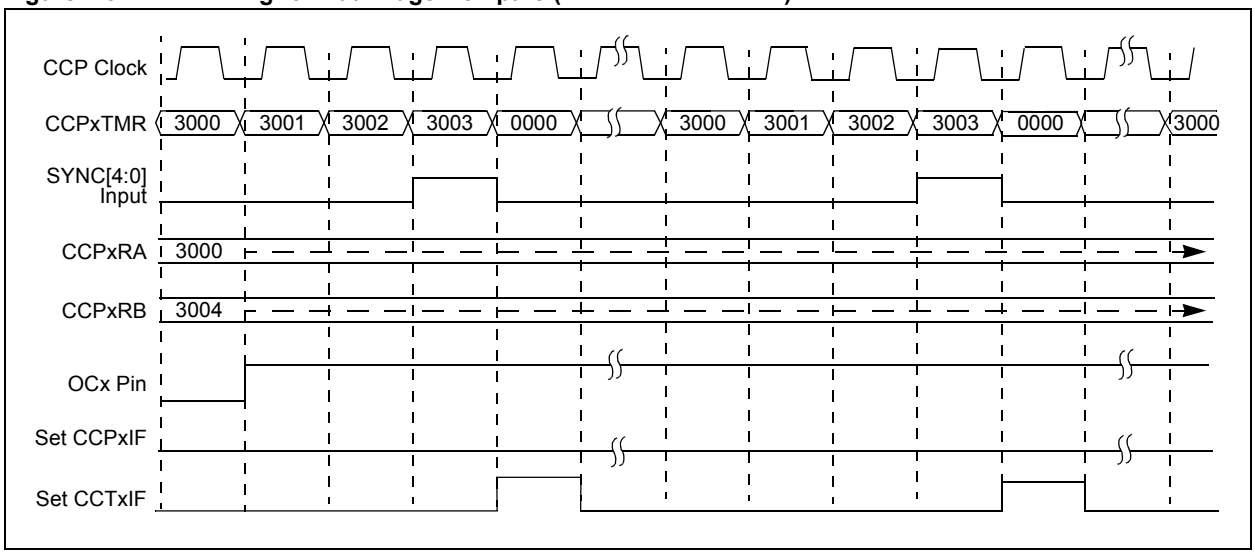
Figure 7-8: Timing for Dual Edge Compare (Timer Period = CCPxRB)



7.2.5 TIMER PERIOD < CCPxRB

If the value of the CCPxPR is less than that of CCPxRB, but greater than CCPxRA, only one pin transition will be generated until the CCPxRB register contents are changed to a value less than or equal to CCPxPR. No Output Compare interrupt is generated (Figure 7-9). This condition allows the module to produce a 100% duty cycle output.

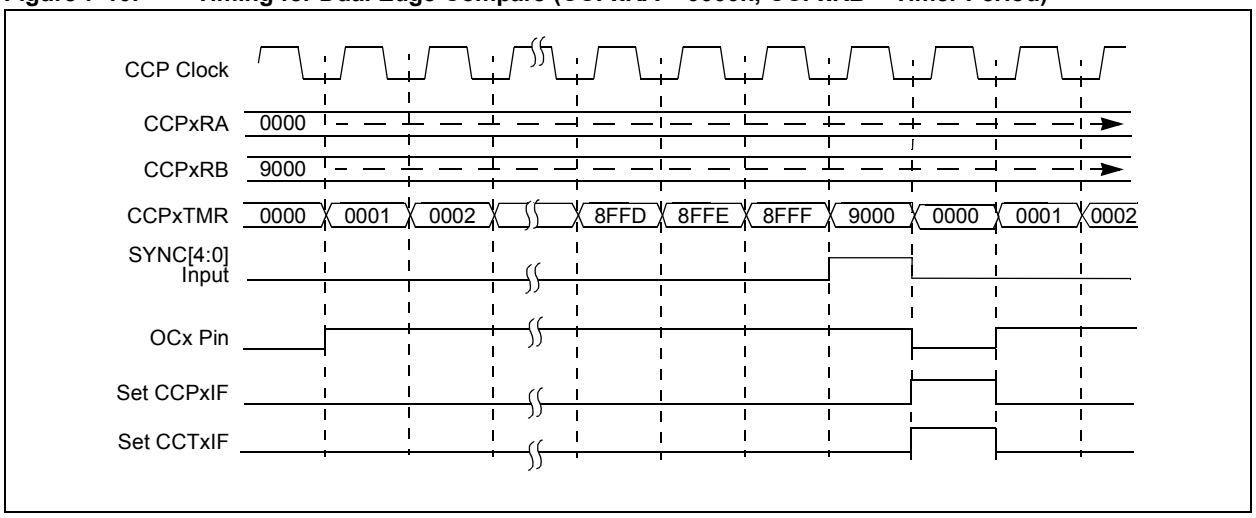
Figure 7-9: Timing for Dual Edge Compare (CCPxPR < CCPxRB)



7.2.6 CCPxTMR = CCPxRB AND CCPxRA = 0

In Sync operation, if CCPxRA is 0000h, the OCx output is asserted on the first clock after the Timer Reset (CCPxTMR = 0001h). It remains asserted until the value of CCPxRB matches the timer period (when the input selected by SYNC[4:0] is asserted). At this point, the OCx output is deasserted and the CCPxIF is generated on the falling edge (Figure 7-10).

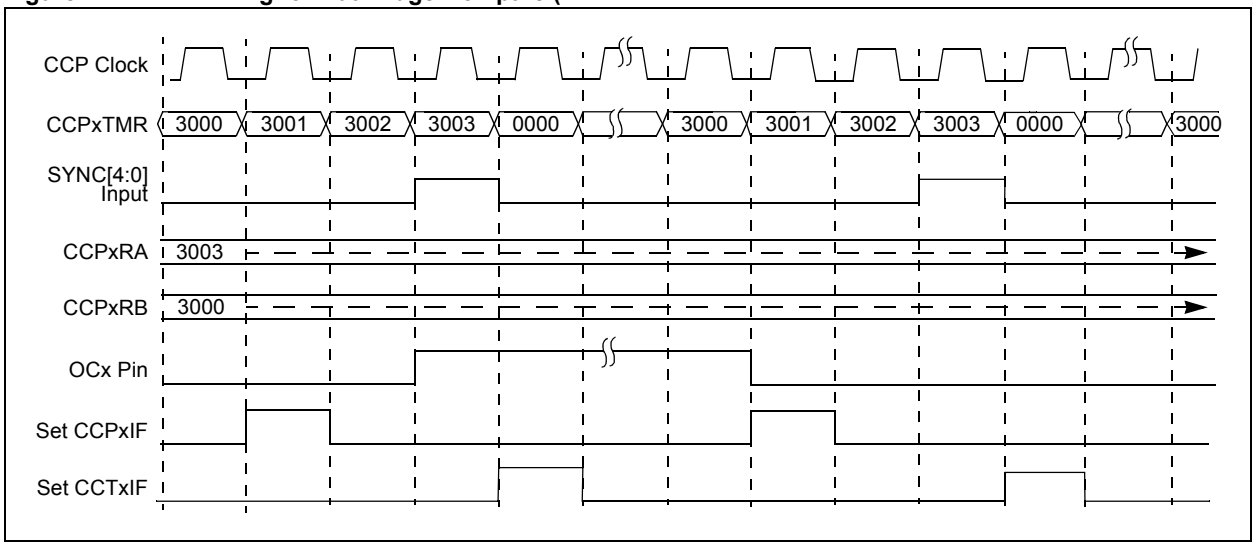
Figure 7-10: Timing for Dual Edge Compare (CCPxRA = 0000h, CCPxRB = Timer Period)



7.2.7 CCPXRA > CCPXRB

If CCPxRA > CCPxRB, a continuous train of pulses is generated. The timer counts up to the first match (CCPxTMR = CCPxRA) and the first (rising) edge is generated. CCPxTMR continues to count up, resetting when the Sync source selected by SYNC[4:0] is asserted. The timer then counts up to the second match (CCPxTMR = CCPxRB), at which time, the second (falling) edge of the signal is generated. The CCPxIF interrupt is generated on the falling edge of the output pulse. The sequence repeats until the module is disabled (Figure 7-11).

Figure 7-11: Timing for Dual Edge Compare (CCPxRA > CCPxRB



Note:	When operating in Dual Compare mode, the CCTxIF signal is asserted on a match between the CCPxRB register value and CCPxTMRL.

7.3 Dual Edge Buffered Compare (PWM) Mode

When MOD[3:0] = 0101, the module functions the same as in Dual Edge Compare mode, with the exception that CCPxRA and CCPxRB are double-buffered. In all other respects of output signal generation, operation is the same. Writes to the Data registers (CCPxRA and CCPxRB) are stored in holding buffers. The contents of the buffers are transferred to CCPxRA and CCPxRB on a Time Base Reset.

Dual Edge Buffered Compare mode is only available in 16-bit mode. The T32 bit has no affect.

Dual Edge Buffered Compare mode uses these Timer/Data registers:

- CCPxTMRL as the Timer register
- CCPxRA for the Rising Edge Value register of the next period
- CCPxRB for the Falling Edge Value register of the next period
- CCPxPRL for the Timer Period register

The Dual Edge Buffered Compare mode is used to create PWM signals. The buffering of the CCPxRA and CCPxRB registers allows the user to create glitch-free updates to the PWM signal edge times.

If edge-aligned PWM signals are desired, maintain CCPxRA with a value of 0000h. Using a non-zero value for CCPxRA creates PWM signals with arbitrary phase alignments.

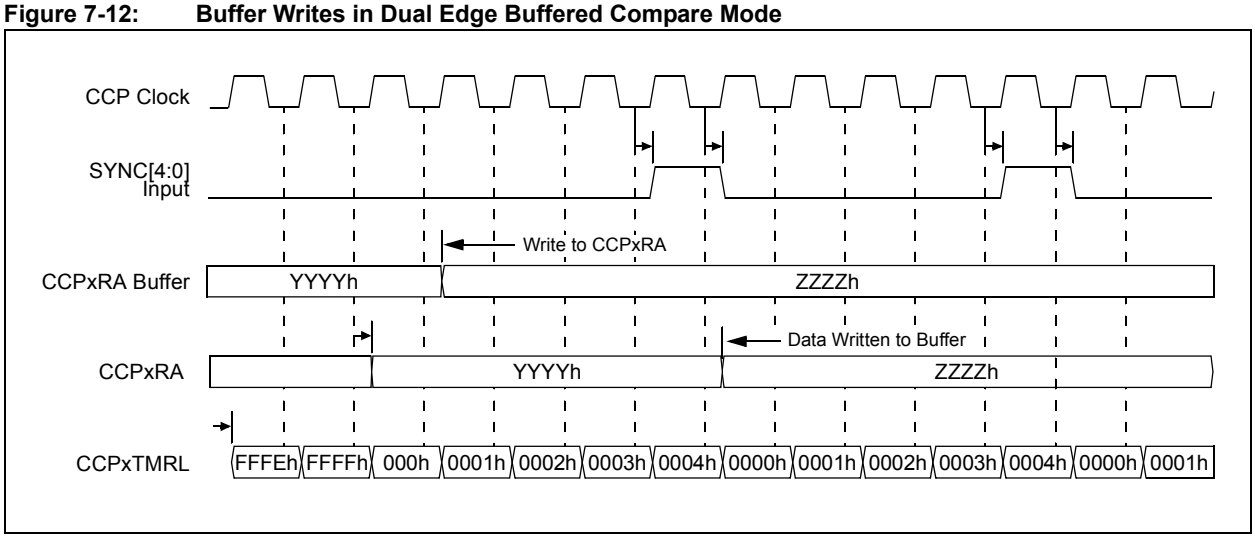
CCPxRA and CCPxRB are double-buffered. Data is written from the buffers to CCPxRA and CCPxRB under these conditions:

- When the timer is reset to 0000h on a Sync event (source selected by SYNC[4:0] is asserted)
- When the timer rolls over from FFFFh to 0000h
- When the module is disabled (CCPON = 0); any writes to CCPxRA and CCPxRB are immediately transferred to their Compare registers

Figure 7-12 shows the timing for writing to the buffer in Sync operation. CCPxRA and its buffer are shown; CCPxRB and its buffer operate in an identical manner. For output signal generation, refer to **Section 7.2 "Dual Edge Compare Mode"**.

The procedure for configuring the module for Dual Edge Buffered Compare mode is shown in Example 7-1.

Figure 7-12: Buffer Writes in Dual Edge Buffered Compare Mode



Example 7-1: Setup for Dual Edge Buffered Compare Mode

```
// Set MCCP operating mode
CCP1CON1Lbits.CCSEL = 0;       // Set MCCP operating mode (OC mode)
CCP1CON1Lbits.MOD = 0b0101;    // Set mode (Buffered Dual-Compare/PWM mode)

//Configure MCCP Timebase
CCP1CON1Lbits.T32 = 0;         // Set timebase width (16-bit)
CCP1CON1Lbits.TMRSYNC = 0;     // Set timebase synchronization (Synchronized)
CCP1CON1Lbits.CLKSEL = 0b000;  // Set the clock source (Tcy)
CCP1CON1Lbits.TMRPS = 0b00;    // Set the clock pre-scaler (1:1)
CCP1CON1Hbits.TRIGEN = 0;      // Set Sync/Triggered mode (Synchronous)
CCP1CON1Hbits.SYNC = 0b00000;  // Select Sync/Trigger source (Self-sync)

//Configure MCCP output for PWM signal
CCP1CON2Hbits.OCAEN = 1;       // Enable desired output signals (OC1A)
CCP1CON3Hbits.OUTM = 0b000;    // Set advanced output modes (Standard output)
CCP1CON3Hbits.POLACE = 0;      //Configure output polarity (Active High)
CCP1TMRL = 0x0000;             //Initialize timer prior to enable module.
CCP1PRL = 0xFFFF;              //Configure timebase period
CCP1RA = 0x1000;               // Set the rising edge compare value
CCP1RB = 0x8000;               // Set the falling edge compare value
CCP1CON1Lbits.CCPON = 1;       // Turn on MCCP module
```

7.4 Center-Aligned Pulse Mode

When MOD[3:0] = 0110, the Output Compare channel provides a PWM output in Center-Aligned Pulse mode. Center-aligned PWM signals are beneficial when multiple PWM generators are used to control power loads in an application. The active pulse time of each PWM signal is symmetrical around an imaginary center point. If the duty cycle of each PWM generator is different, the center alignment avoids simultaneous switching of each power load. This alignment of the signals also permits unique switching patterns to be generated.

In Center-Aligned Pulse mode, the CCPxPRL register is used to set the timer count period (if self-synchronized). The CCPxPRL register value is divided by two to determine a center reference point for pulse generation. A symmetrical pulse is generated around this reference point. The value of the CCPxRA register specifies the total pulse duration.

Center-Aligned Pulse mode is only available in 16-bit mode. The T32 bit has no affect.

Center-Aligned Pulse mode uses these Timer/Data registers:

- CCPxTMRL as the Timer register
- CCPxRA for the Pulse-Width register
- CCPxRB for the Trigger Output Value register
- CCPxPRL for the Timer Period register (affects rising/falling edge times and pulse center)

Center-Aligned mode uses a dedicated, 16-bit adder/subtracter and edge generation logic that is part of the CCP module's hardware. The count period for the time base is specified by the value in the CCPxPR register, which is double-buffered. The buffer contents are updated on a timer rollover event or when the Sync source selected by SYNC[4:0] is asserted. The upper 15 bits of the buffered CCPxPR register value are used as the center reference for the time base count period. The hardware adder in the module uses this value as the baseline for calculating the rising and falling edge times from the values in CCPxRA and CCPxPRL.

When the timer is reset and begins counting upward, the adder subtracts one-half the value of CCPxRA from one-half the value of CCPxPRL.The difference is compared to the timer value to determine when the rising edge of the PWM signal occurs.

After the rising edge has occurred, the adder adds one-half the value of CCPxRA to one-half the value of CCPxPRL. The sum is compared to the timer value to determine when the falling edge of the PWM signal occurs.

Note:	Updates to the CCPxRA register are buffered and become active in the next PWM period. The comparison of CCPxPRL is always done with the buffered value of CCPxRA.

Example 7-2 shows a typical case for how the rising and falling edge values are determined. Figure 7-13 shows the generation of the center-aligned pulse in relationship to the register values.

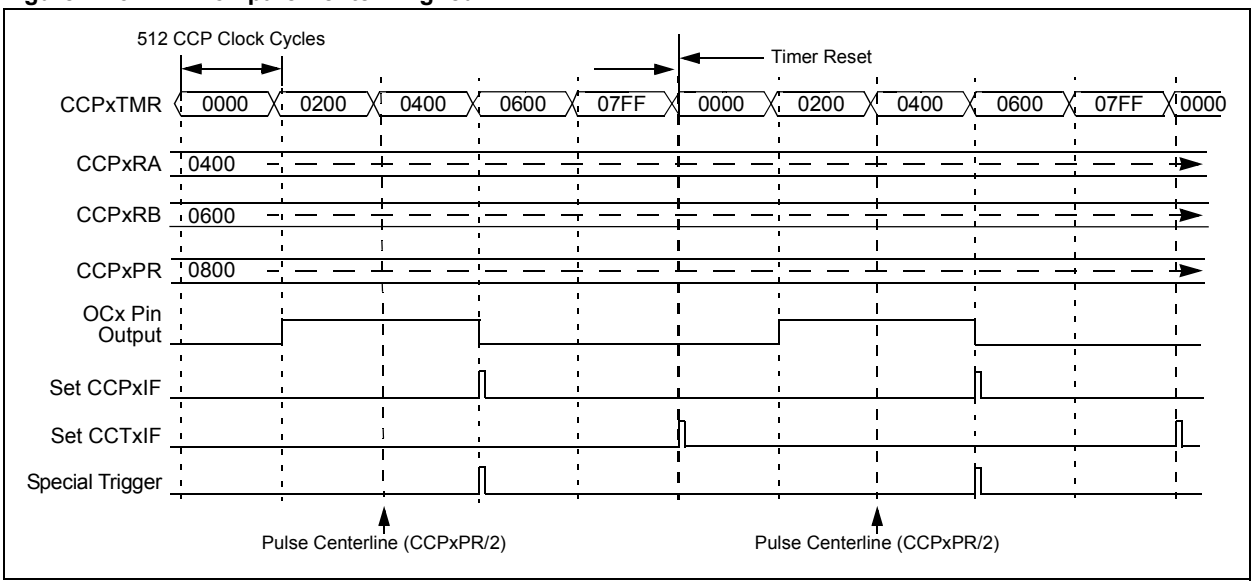
Example 7-2: Calculating Rising and Falling Edge Values in Center-Aligned Mode

For CCPxRA = 400h and CCPxPRL = 200h:

Rising Edge = (CCPxPRL/2) – (CCPxRA/2)
= 400h – 200h
= 200h

Falling Edge = (CCPxPRL/2) + (CCPxRA/2)
= 400h + 200h
= 600h

Figure 7-13: Compare Center-Aligned PWM



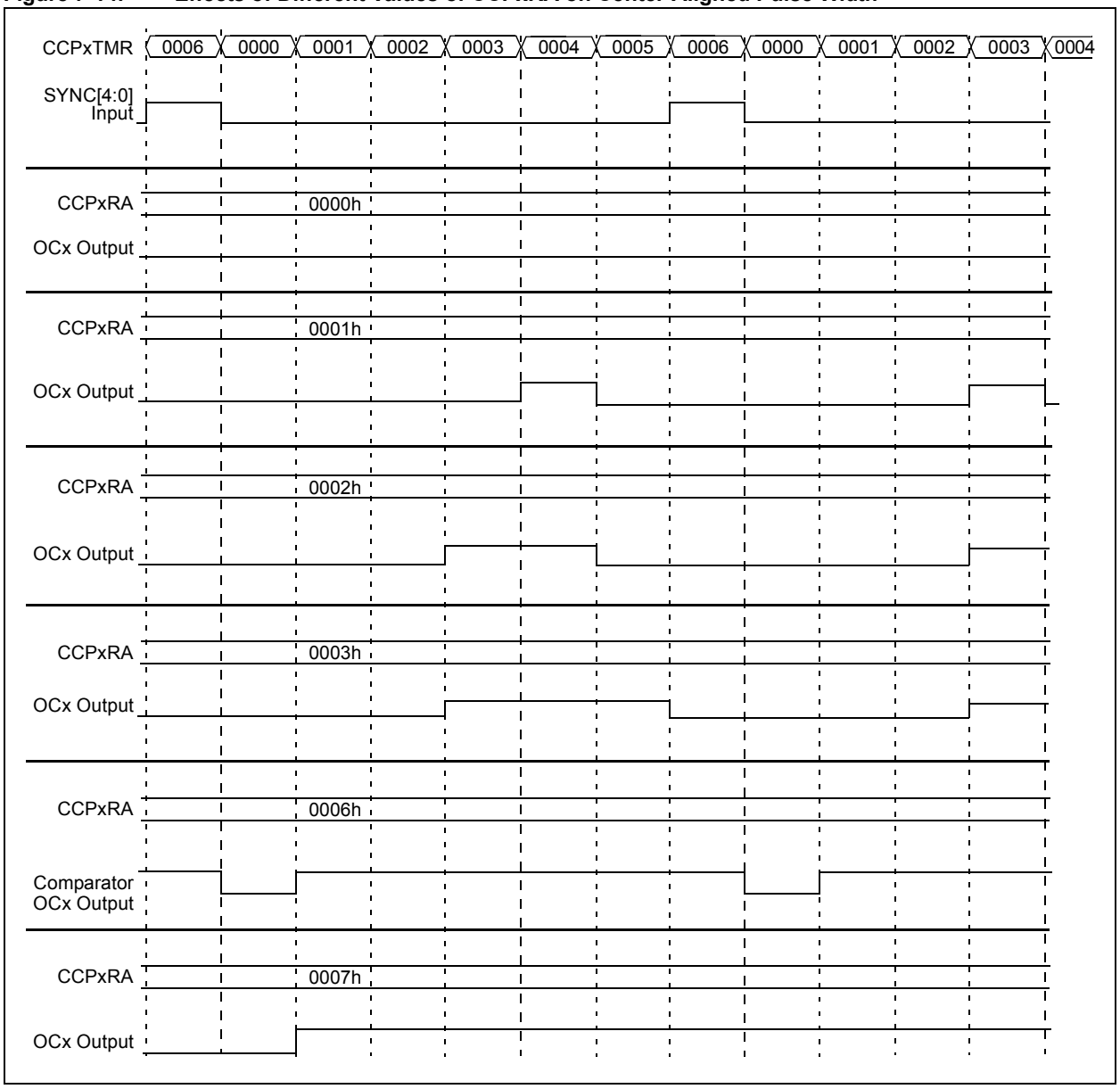
If the value of CCPxRA is even, it has no effect on the position of either the rising or falling edge. If the value is odd, the '1' in the Least Significant bit (LSb) is carried over by the adder for the falling edge compare event only. This increases the width of the active pulse by one timer cycle, producing an asymmetry of 1/2 count around the virtual center point value. If this asymmetry is undesirable, the application should only write even pulse-width values to CCPxRA.

Note: To permit the module to produce maximum duty cycle in Center-Aligned Pulse mode, the user must set the time base count period to an even value. A 100% duty cycle will be obtained when the CCPxRA register value is written to a value of (CCPxPR + 1).

Any applications should limit the maximum value written to the CCPxRA register, based on the value of CCPxPR. No pulses will be produced when CCPxRA is greater than (CCPxPR + 1).

Figure 7-14 shows the effect of increasing values of CCPxRA on the pulse width. It also demonstrates the effect when CCPxRA equals zero (no output), the timer period (when the pulse width equals the timer period) or when CCPxRA is greater than the period (output remains active after the initial edge event).

Figure 7-14: Effects of Different Values of CCPxRA on Center-Aligned Pulse Width



7.4.1 OUTPUT TRIGGER

The value of the CCPxRB register has no effect in determining the pulse width or timing. It is used instead, to determine the time of Special Event Triggers in relation to the center-aligned pulse events. For example, it may be useful to trigger an A/D conversion at the center of a PWM pulse or it may be better to trigger some other event at one of the pulse's edges. Users may write an appropriate value to CCPxRB, or use the values of CCPxRA and CCPxPRL, to automatically calculate an update for CCPxRB with the correct value.

The value of CCPxRB must be less than the period set by the CCPxPRL register or by events from the selected SYNC[4:0] input. The Special Event Trigger can be used to start an A/D conversion or trigger other peripheral events.

7.5 Variable Frequency Pulse Mode

When MOD[3:0] = 0110, the Output Compare channel provides a PWM output in Variable Frequency Pulse mode. This mode uses an Accumulator register and an Adder register to produce a variable frequency output signal with a fixed duty cycle of 50%.

Variable Frequency Pulse mode uses these data registers:

- CCPxTMRL as an accumulator
- CCPxRA to store the adder value for the next operation

The value in the Adder register is added to the accumulator on each rising edge of the time base. When the Accumulator register overflows, the output signal is toggled. The CCPxRB and CCPxPRL registers are not used in this mode.

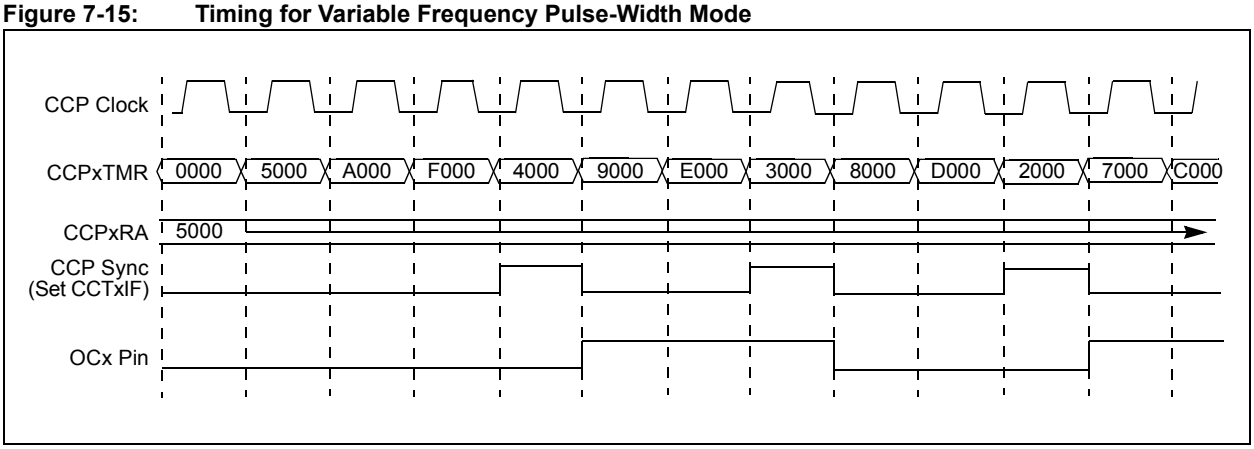
Variable Frequency Pulse mode is only available in 16-bit mode. The T32 bit has no affect.

The output frequency and the value of CCPxRA are related, as shown in Equation 7-1; it is possible to calculate one, given the other. The output frequency is a function of the module clock source frequency, FCLK, the adder value in the CCPxRA register and the accumulator size (2^{16}).

Equation 7-1: Relationship Between FOUT and CCPxRA Target Value

$$F_{OUT} = \frac{F_{CLK} \cdot CCPxRA}{2 \cdot 2^{16}} \qquad CCPxRA = \frac{2 \cdot 2^{16} \cdot F_{OUT}}{F_{CLK}}$$

Figure 7-15: Timing for Variable Frequency Pulse-Width Mode



7.6 Output Control for Compare/PWM Modes

When the module operates in an Output Compare mode, three blocks determine how the Output Compare signal is presented on the output pins:

- Output Mode Control Block (MCCP only)
- Auto-Shutdown Control Block
- Output Polarity Control Block

The Output mode control block is used in the MCCP version of the module to control the routing of the Output Compare signal to the six available output pins. This block implements the more advanced motor control and power control features of the multiple output PWM. It is not implemented in the SCCP version of the module.

The auto-shutdown control block responds to asynchronous external inputs or software control, placing all output pins under control of the module into a predetermined state.

The output polarity control block determines the output polarity on each pin under control of the module. This block takes effect after all other control of the output pins.

7.6.1 OUTPUT MODE SELECTION

The OUTM[2:0] control bits (CCPxCON3H[10:8]) are used to select the Output mode of the MCCP. When operating in an Output Compare mode, one of several Output modes may be selected that use the OCxA through OCxF output pins in different ways. In some Output modes, a dead-time delay generator is used to implement switching delays between the output pins.

The output control logic does not determine how the input signal is generated, only how the signal is routed to the output pins. The signal source for the output control logic can be any of the Output Compare operating modes that can be selected by the MOD[3:0] control bits.

The output control logic does interact with the input signal generation logic for synchronization purposes. In some operating modes, the output control logic will wait for an input signal period boundary to switch the signal to a different output pin.

These Output modes can be selected using OUTM[2:0]:

- Steerable Single Output mode (default)
- Brush DC (Motor) Output mode (forward and reverse)
- Half-Bridge Output mode
- Push-Pull Output mode
- Output Scan mode

7.6.2 OUTPUT PIN ENABLE (MCCP)

Each of the output pins controlled by the MCCP module may be enabled separately, using the OCxEN control bits (CCPxCON2H[13:8]). Each of the bits, OCAEN through OCFEN, controls a corresponding CCP output: OCxA through OCxF. If the OCxEN control bit is set, the corresponding I/O pin receives the Output Compare signal that is generated by the module. If the OCxEN control bit is cleared, the I/O pin is controlled by the port logic or another peripheral of higher priority. The user must use care to ensure that the I/O pin will be in the correct state when a OCxEN control bit is cleared.

The OCxEN control bits have no effect on module operation when the module is operated in an Input Capture mode or a Timer mode.

The OUTM[2:0] control bits affect the function of the OCxEN pins, depending on the mode selected. The bits can provide a steering function to redirect the Output Compare signal to different pins at specific times. This steering functionality is useful in motor and power control applications. The OCxEN bits can also be used to relocate the module output signals to different sets of output pins. For example, the Half-Bridge Output mode replicates the same pair of signals on the OCxA/OCxB, OCxC/OCxD and OCxE/OCxF pins. The user can enable any of these pin pairs using the OCxEN bits to move the signals to a convenient location.

The OCAEN pin resets to '1' on all CCP modules; this makes the default Output Compare output pin available by default on device Reset. For MCCP modules, all other OCxEN bits reset to '0', disabling the other OCx pins on Reset. For applications that use multiple MCCP output pins, it is the user's responsibility to initialize all output pins correctly.

7.6.2.1 Output Pin Enable (SCCP)

The SCCP module has only one output pin, OCxA, in Output Compare or PWM mode. The OCAEN bit (CCPxCON2H[8]) is the only implemented control bit. It determines whether or not the module has control of the output pin. By default, this OCxA output is enabled on device Resets.

7.6.3 STEERABLE SINGLE OUTPUT MODE

Steerable Single Output mode is the default Output mode of the control block, selected when OUTM[2:0] = 000. In this mode, the single signal produced by the Output Compare logic is routed to all available module output pins. The application can enable each output pin separately to produce the Output Compare signal by setting the appropriate OCxEN bit.

7.6.4 PUSH-PULL OUTPUT MODE

When OUTM[2:0] = 001, Push-Pull PWM mode is selected. In this mode, the Output Compare signal is multiplexed between the OCxA and OCxB output pins on alternate time base cycles.

For each cycle, one of the pins is connected to the Output Compare signal and the other pin is driven to the inactive state. The output and port control signals for the OCxA/OCxB pin pair are replicated for the OCxC/OCxD and OCxE/OCxF output pins in this Push-Pull mode. This allows the user to move the push-pull output signals to another pin pair using the OCxEN control bits. At least one pair of OCxEN control bits must be set to allow the module to control two output pins.

Pull-Pull mode is commonly used to drive transformers in DC/DC and DC/AC power supplies, as shown in Figure 7-17. Each PWM output pin drives one side of a transformer, winding through an external power transistor. The transformer has a center winding that is connected to a DC bus voltage. The application should make certain to produce the same pulse width for each side of the transformer to prevent DC current flow in the transformer winding; therefore, the duty cycle must remain the same for two time base periods.

A four-transistor push-pull circuit may also be used (Figure 7-18). This implementation uses a second pair of output pins driving a second power transistor pair. The connections with the second pair of transistors are intentionally swapped so that each pair of diagonal transistors is on at the same time.

Figure 7-16: Output and Interrupt Timing in Push-Pull Mode

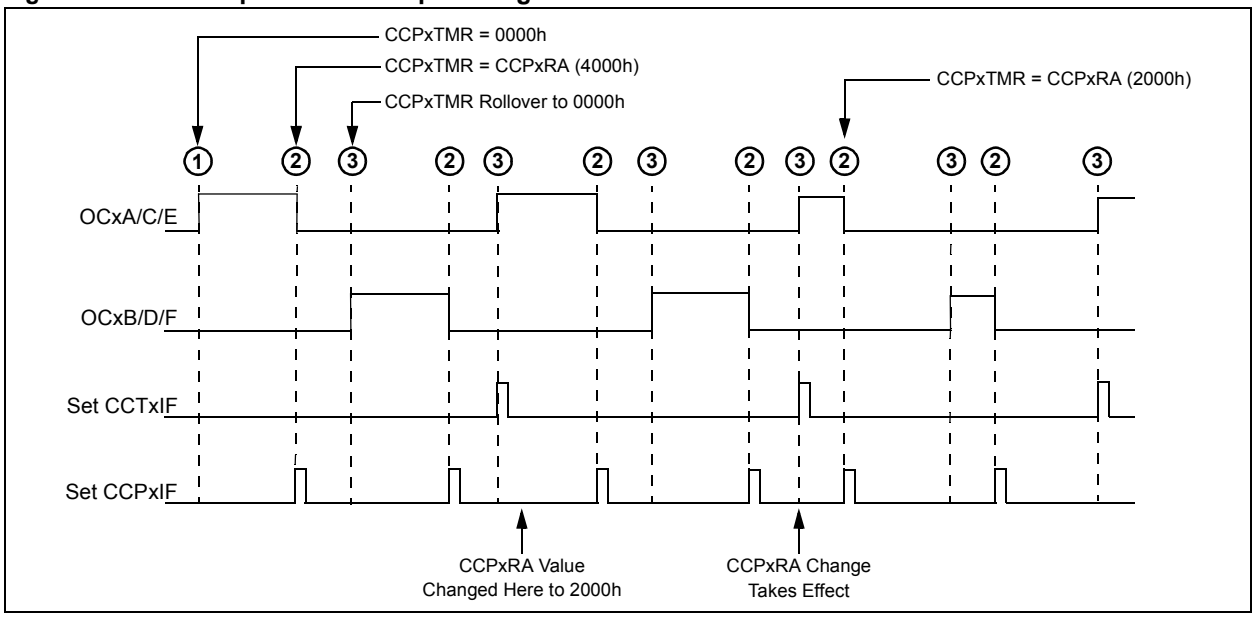


Figure 7-17: Typical Push-Pull Operation

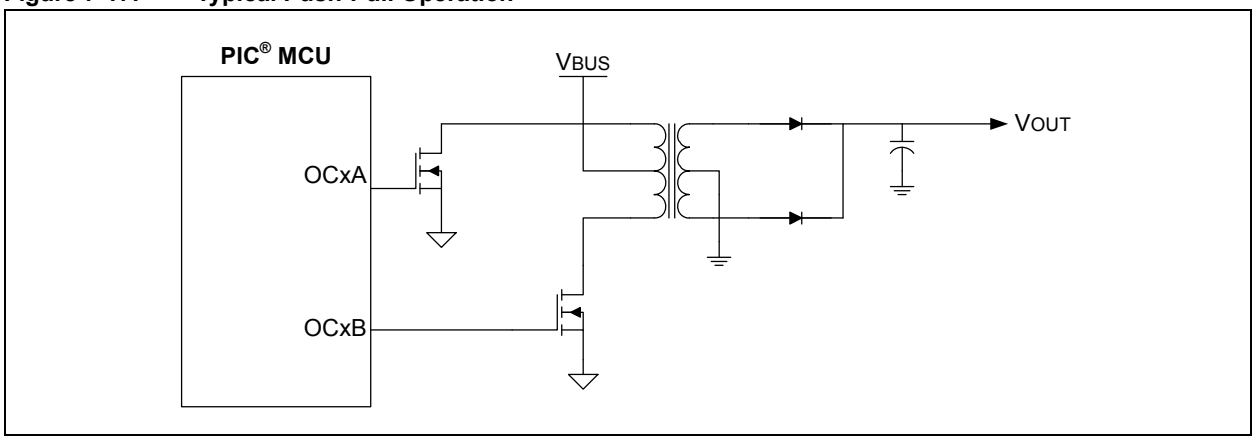
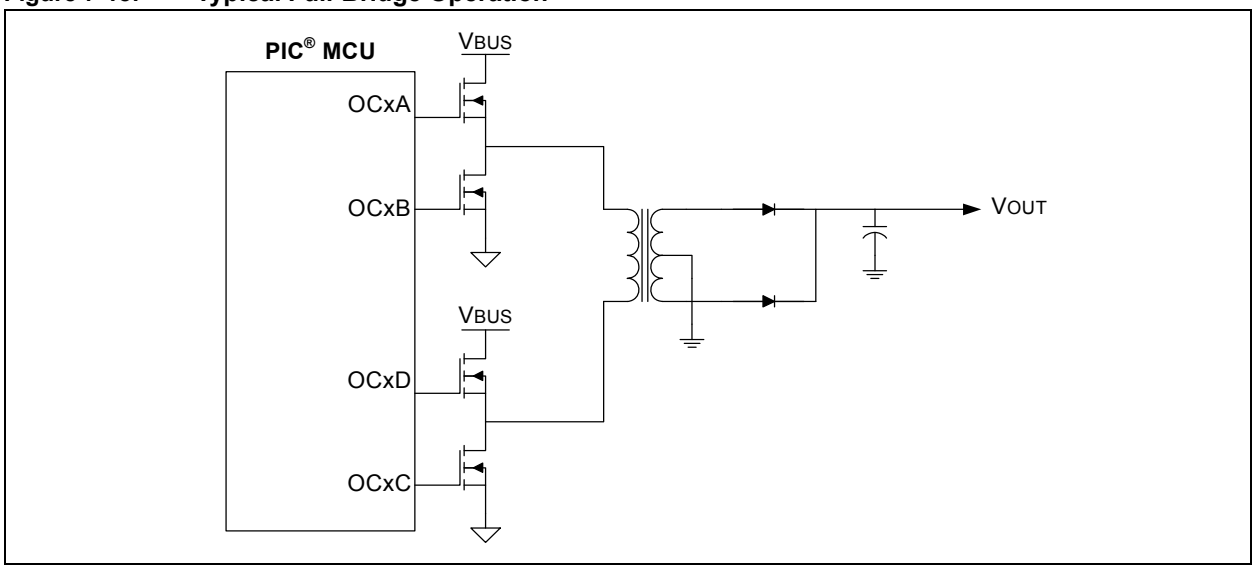


Figure 7-18: Typical Full-Bridge Operation



7.6.5 HALF-BRIDGE OUTPUT MODE

The Half-Bridge Output mode is selected when OUTM[2:0] = 010. In this mode, the module produces complementary output signals on OCxA and OCxB (Figure 7-19). The OCxB signal is the inverse of the OCxA signal. If a non-zero dead-time delay is used, it is inserted between the switching events of the two pins.

The output and port control signals for the OCxA/OCxB pin pair are replicated for the OCxC/OCxD and OCxE/OCxF output pins in Half-Bridge mode. This allows the user to move the complementary output signals to another pin pair using the OCxEN control bits. At least one pair of OCxEN control bits must be selected by the application to produce the half-bridge output signals.

Half-Bridge Output mode is typically used to control power circuits, such as the one shown in Figure 7-20. If a dead-time value other than zero is written to DT[5:0] (CCPxCON3L[5:0]), a delay is inserted between the switching edges of the OCxA and OCxB signals.

For more information on the dead-time generator, see **Section 7.6.10 "Dead-Time Delay Generator"**.

Figure 7-19: Half-Bridge Outputs

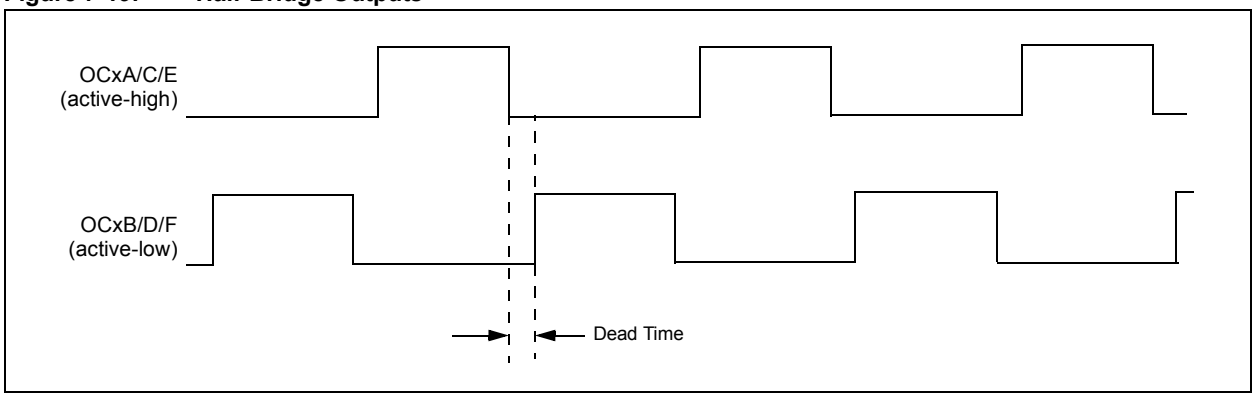
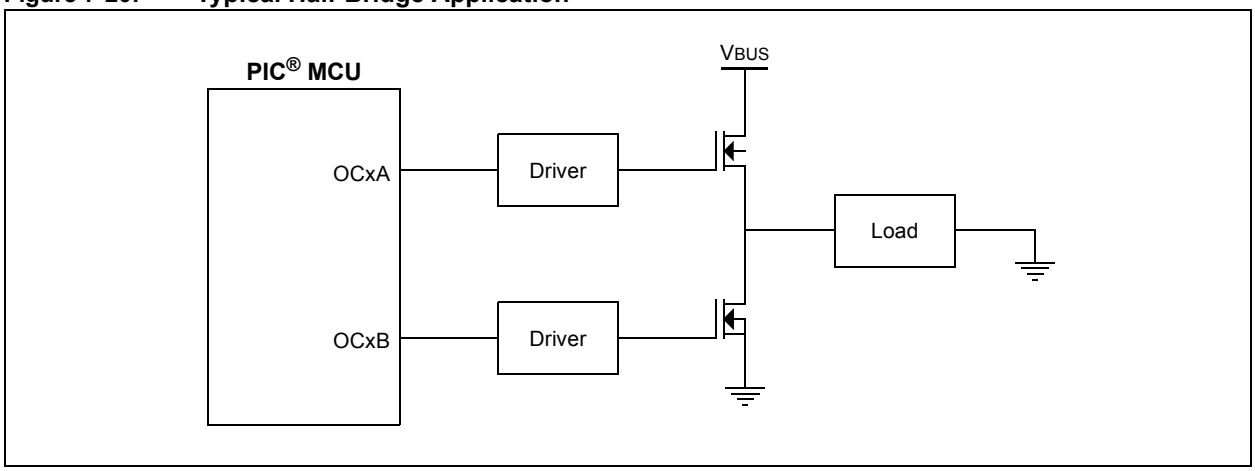


Figure 7-20: Typical Half-Bridge Application



7.6.6 BRUSH DC OUTPUT MODES

The Brush DC Output modes are selected when OUTM[2:0] = 101 (Forward mode) or 100 (Reverse mode). In these modes, the signal produced by the Output Compare logic is routed to four output pins: OCxA through OCxD. The corresponding OCAEN, OCBEN, OCCEN and OCDEN bits must be set by the application for the module to control these output pins.

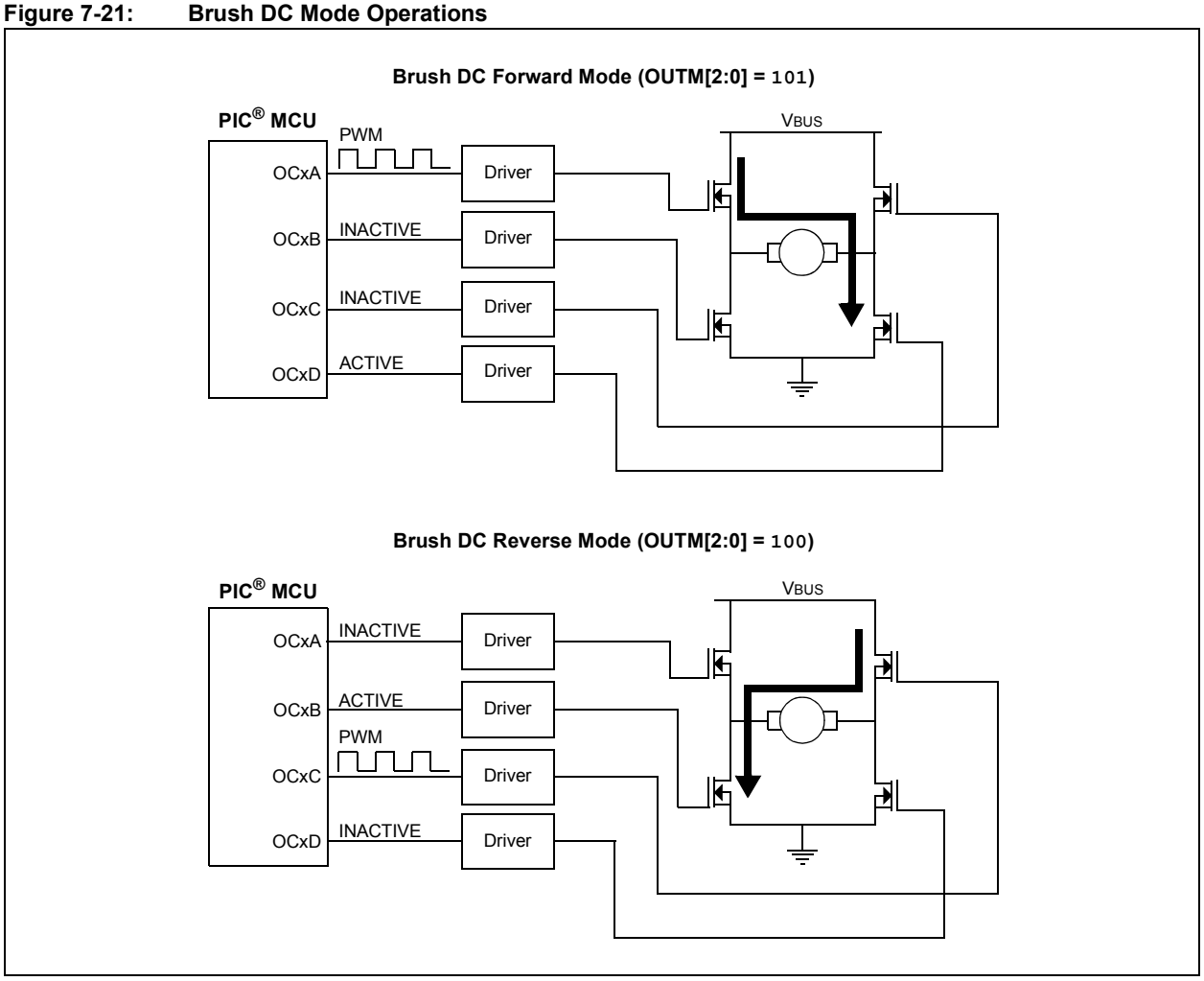
For each mode, only two of the four output pins are driven to the active state:

- Forward Mode (OUTM[2:0] = 101):
  - OCxA pin receives the PWM generator signal
  - OCxD pin is driven to the active state
  - OCxB and OCxC pins are driven inactive
- Reverse Mode (OUTM[2:0] = 100):
  - OCxC pin receives the PWM generator signal
  - OCxB pin is driven to the active state
  - OCxA and OCxD pins are driven inactive

The OCxE and OCxF output pins are not controlled by the module in the Brush DC modes. The user may enable these pins using the OCEEN and OCFEN control bits; however, the pins will remain in the inactive state.

Figure 7-21 shows how the four pins are connected and used to control external circuitry in a typical application. The actual polarity of the four output signals is determined by the output polarity control circuitry (see **Section 7.6.12 "Output Polarity Control"** for more information).

Figure 7-21: Brush DC Mode Operations



Dead-time delay for Brush DC modes is not required, except during a Direction mode change when the duty cycle is at or near 100%. It is expected that the user will switch between Forward mode and Reverse mode during run time. A direction change is accomplished by toggling the OUTM0 bit in the application software when OUTM[2:0] = 10x. The module logic detects when the OUTM[2:0] control bits are changed between the values of '100' and '101', and triggers the dead-time generator. The direction change is synchronized to the CCP timer period and occurs when the Sync source, selected by SYNC[4:0], is asserted.

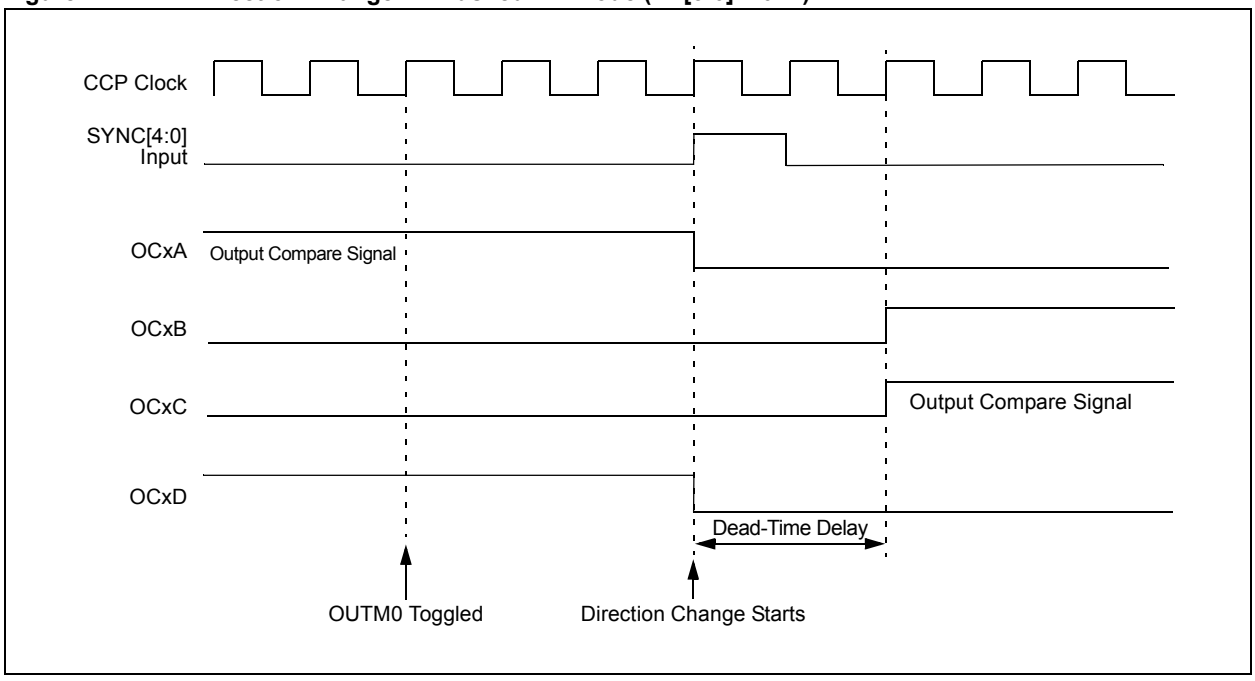
When a direction change is made with the PWM generator set for a low duty cycle, dead time is not required because the actively controlled switches will be turned off for a period of time before the direction change occurs. When the duty cycle is near 100%, dead time may be required to ensure that the top and bottom switches controlled by the module will be off for a minimum time.

The following sequence of events occurs on a direction change:

1. At the next PWM Time Base Reset boundary, the two currently active pins (OCxA and OCxD or OCxB and OCxC) are driven to their inactive states.
2. If the value of DT[5:0] is 000h, the new pair of output pins is made active immediately.
3. If the value of DT[5:0] is not zero, then the DT[5:0] bits are loaded into the dead-time delay counter when OUTM0 is toggled. The new pair of output pins is made active after the dead-time counter expires.

Figure 7-22 shows the timing of a direction change when the dead time is programmed to a value of two clock cycles (02h).

Figure 7-22: Direction Change in Brushed DC Mode (DT[5:0] = 02h)



7.6.7 OUTPUT SCAN MODE

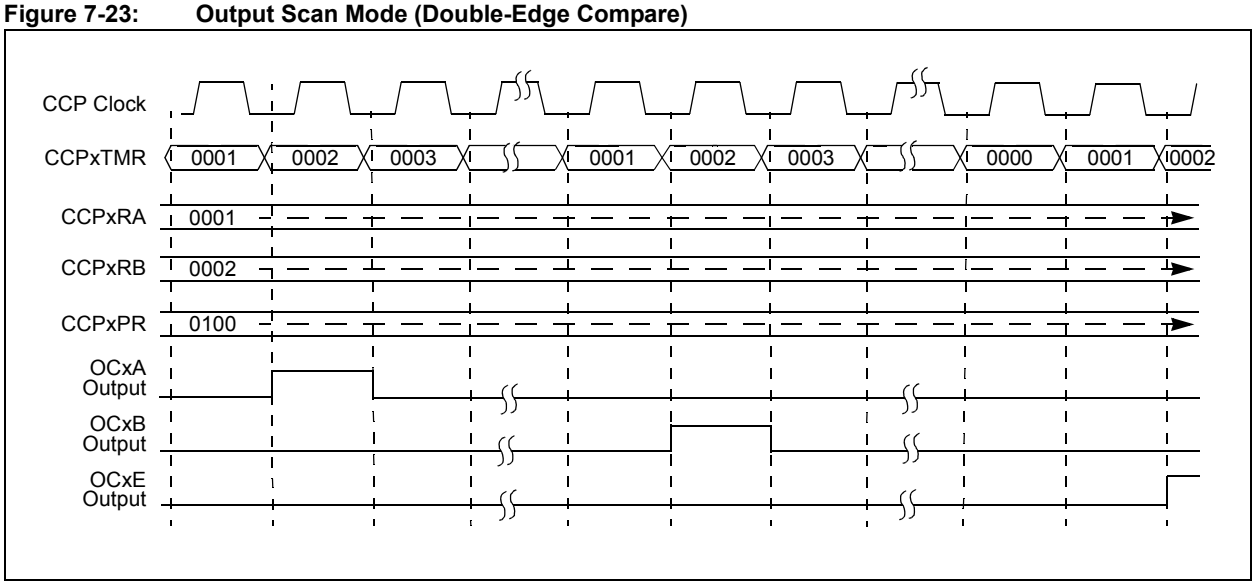
The Output Scan mode (OUTM[2:0] = 110) is similar to the Single Output Steerable mode, except that the Output Compare signal is automatically sequenced among the available OCx pins. The MCCP output pins to be used during Output Scan mode are selected by setting the appropriate OCxEN control bits. For example, if the OCAEN, OCBEN and OCEEN bits are set, the MCCP module will automatically steer the Output Compare signal sequentially between the OCxA, OCxB and OCxE output pins in a continuous pattern.

If the module is disabled (CCPON = 0), the scan sequence logic is reset and will start again on the first enabled pin. When the time base is triggered or reset, the Output Compare signal is moved to the next enabled output in the sequence.

Basic operation of the Output Scan mode is shown in Figure 7-23, using OCxA, OCxB and OCxE. Output Scan mode can also be used with triggered operation, or with One-Shot mode, to produce output sequences with delays between sequences.

Note:	The actual state of the output pin before the module is enabled will depend on the port pin's control logic settings or an enabled peripheral of lower priority

Figure 7-23: Output Scan Mode (Double-Edge Compare)

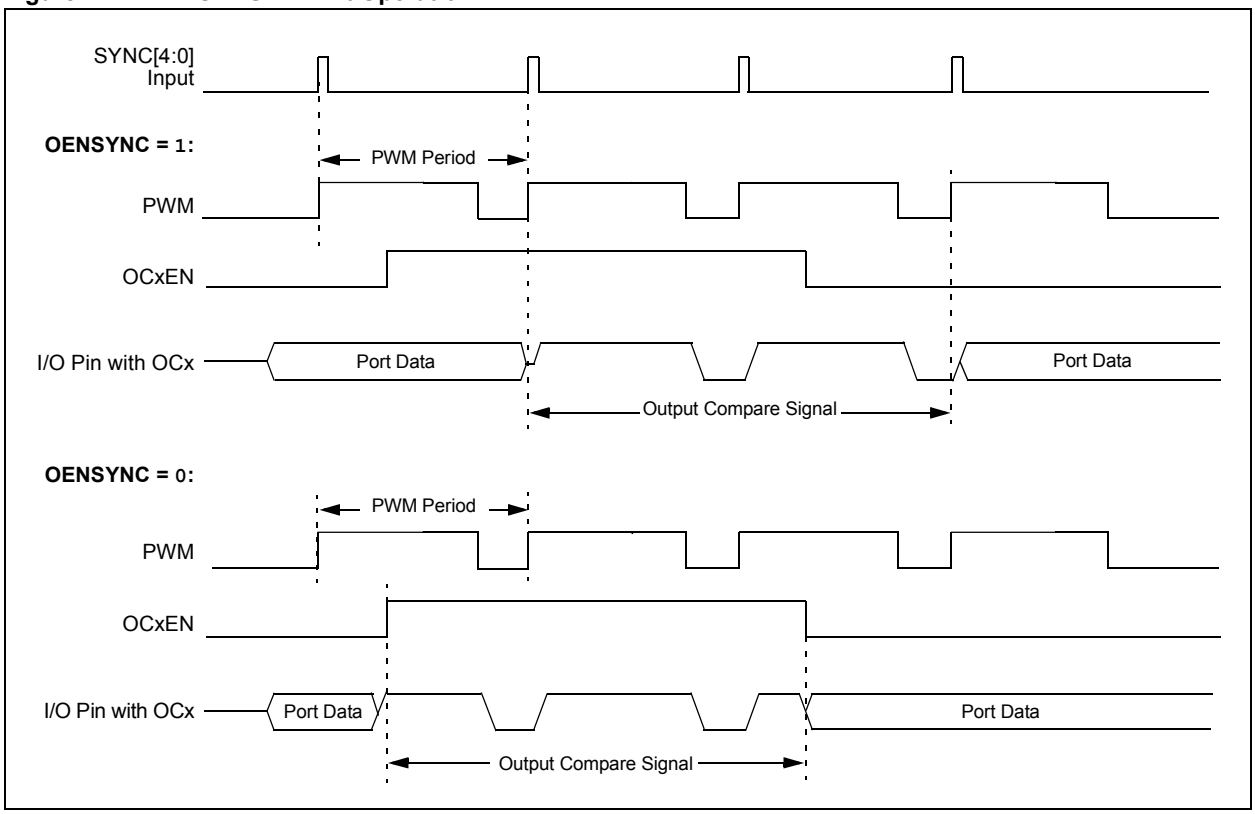


7.6.8 OUTPUT ENABLE SYNCHRONIZATION

Changes to the OCxEN control bits may be optionally synchronized to the timer period, allowing software changes to PWM settings to be synchronized to the PWM period's boundaries. This prevents incomplete output pulses as a result of steering changes.

The OENSYNC control bit (CCPxCON2H[15]) controls the synchronization of the PWM output to period boundaries. When OENSYNC = 1, changes to the OCxEN control bits take effect on a Timer Reset (i.e., the Sync input selected by SYNC[4:0] is asserted). When OENSYNC = 0, changes to the OCxEN control bits take effect immediately. Figure 7-24 shows the effect of the OENSYNC bit on the I/O pin shared by the OCx output.

Figure 7-24: OENSYNC Bit Operation



7.6.9 OUTPUT ENABLE ON TRIGGER

The OETRIG control bit (CCPxCON3H[15]) allows the user to select whether the MCCP output pins are held in a high-impedance state or driven by the module before the timer is triggered. The OETRIG control bit only affects the module operation in Triggered mode (TRIGEN = 1).

The operation of the OETRIG bit function varies depending on the Output mode of the module. For Output Scan mode (OUTM[2:0] = 110), only the currently active output pin enabled in the scan sequence is driven when the time base is triggered. All other pins enabled for the scan sequence are held in a high-impedance state.

For all other settings of the OUTMx bits, all outputs enabled via the OCxEN control bits are driven active when the time base is triggered.

Regardless of the mode, all enabled output pins are held in a high-impedance state when the timer is not triggered (CCPTRIG = 0).

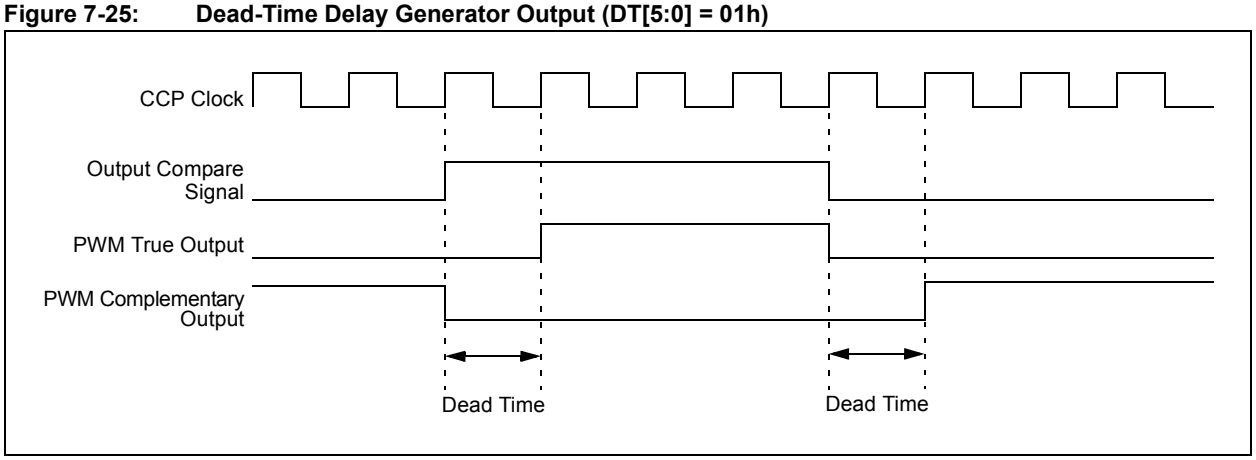
7.6.10 DEAD-TIME DELAY GENERATOR

The dead-time delay generator is used in specific multi-output PWM modes of the module. It creates two output signals from the single output signal of a PWM generator: a “true” signal (matching the polarity of the Output Compare signal) and an inverted “complementary” signal. It also creates a brief delay between the time when one signal is driven inactive and the other signal is driven active.

The generator contains edge detectors to monitor input signal transitions and a digital countdown timer. The rising edges of the output signals are delayed by a number of clock cycles, set by the DT[5:0] bits (CCPxCON3L[5:0]). If the value of the DTx bits is zero, the dead-time delay generator is effectively disabled and complementary output signals are produced with zero delay between the transitions on each output.

A timing diagram for the dead-time generator’s output, showing the relationship between the true and complementary signals, is provided in Figure 7-25.

Figure 7-25: Dead-Time Delay Generator Output (DT[5:0] = 01h)

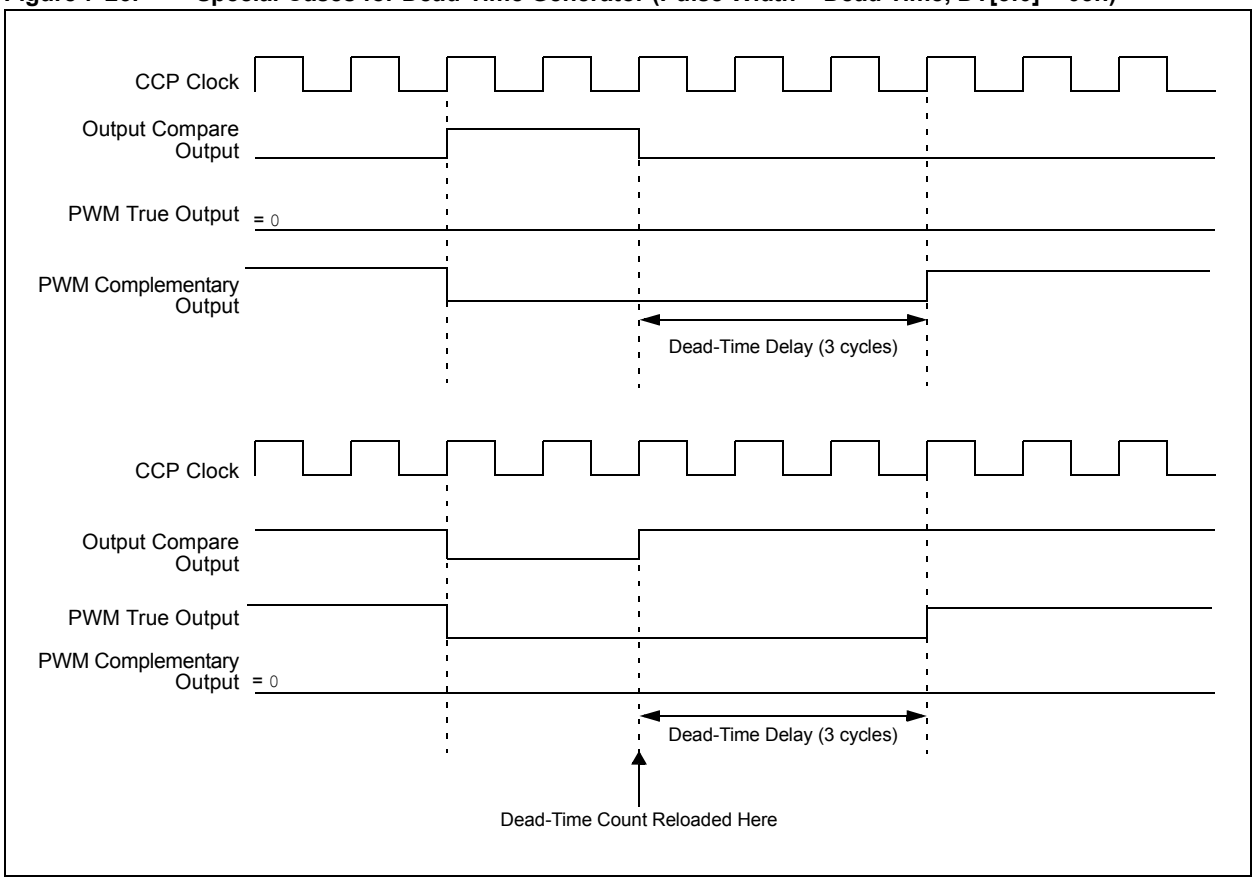


There are three special cases for dead-time generation:

1. When the input signal pulse width is equal to or less than the programmed dead-time value, the desired output results will not be obtained. Figure 7-26 depicts two scenarios where the duty cycle of the input signal is close to 0% and close to 100%.
2. When the input duty cycle is set to 0%, both outputs are driven inactive during the dead-time delay period. There will be no transitions on the input signal. The PWM true output remains low and the PWM complementary signal remains high.
3. When the input duty cycle is set to 100%, both outputs are driven inactive for the dead-time period. There should be no transitions on the input signal. The PWM true output remains high and the PWM complementary signal remains low.

As the input duty cycle approaches 0% or 100%, the dead-band delay time becomes a more significant portion of the input signal pulse width. This effect causes a nonlinear behavior between the requested duty cycle and the actual system response. Systems that are sensitive to this nonlinearity must avoid regions near 0% and 100% duty cycle, or use output feedback to compensate the duty cycle.

Figure 7-26: Special Cases for Dead-Time Generator (Pulse Width < Dead Time, DT[5:0] = 03h)



7.6.10.1 Dead-Time Delay Generation for Half-Bridge Mode

When the module is operated in Half-Bridge mode, the OCxA output pin signal is the noninverted output from the dead-band delay generator (see Figure 7-19). The OCxB output pin signal is the inverted (complementary) output from the dead-band delay generator. Polarity control is provided after the dead-time delay generator block for these two signal outputs.

The output and port control signals for the OCxA/OCxB pin pair are replicated for the OCxC/OCxD and OCxE/OCxF output pins in this Half-Bridge mode. This allows the user to relocate the complementary output signals to another pin pair using the OCxEN bits.

7.6.10.2 Dead-Time Delay Generation for Brush DC Modes

For the Brush DC Operating modes, the dead-time delay generator is used to optionally blank the OCxA, OCxB, OCxC and OCxD output pin signals during a toggle or direction change.

The OCxE and OCxF output pins are not controlled by the module in the Brush DC modes. Their output enable signals should be driven low.

7.6.10.3 Dead-Time Delay Generation for Push-Pull Mode

When the CCP module is operated in Push-Pull mode, the dead-time delay generator is used to optionally blank the OCx output pins at time base period boundaries. Polarity control is provided after the dead-time delay generator block for the six signal outputs.

7.6.10.4 Dead-Time Delay Generation for Output Scan Mode

The dead-time delay generator is not used in Output Scan mode (OUTM[2:0>] = `110`).

7.6.11 AUTO-SHUTDOWN CONTROL

The primary function of the auto-shutdown control logic is to place the module output pins in a safe state when driving external power circuitry. The auto-shutdown function can also be used to place the output pins of the CCP module in a specific state based on an external event.

Auto-shutdown control is implemented as part of the time base gating (see **Section 4.1 "Gating Logic"**). The user must select an input source for the auto-shutdown using the ASDG[7:0] control bits (CCPxCON2L[7:0]). The available sources for auto-shutdown are device-dependent, and typically include such sources as comparator outputs, I/O pins, software control (i.e., the SSDG bit) and so on. With the exception of the SSDG control bit, which is active-high, a low output from the shutdown source places the module OCx pins in the shutdown state. The auto-shutdown event is level-sensitive, not edge-triggered. The comparator output and other shutdown sources are not synchronized to the system clocks to provide an immediate response of the CCP module to the shutdown input signal.

When a shutdown occurs, the selected output states are placed onto the module port pins.

7.6.11.1 Auto-Shutdown Pin State

The state of the output pins is controlled by the PSSACE[1:0] and the PSSBDF[1:0] control bits (CCPxCON3H[3:2,1:0]). The PSSACEx bits affect the states of the OCxA, OCxC and OCxE (high side) output pins. The PSSBDFx bits affect the states of the OCxB, OCxD and OCxF (low side) output pins. These control bits let the user select whether the I/O pin is driven inactive, driven active or put into a high-impedance state.

Note:	An output pin is not affected by auto-shutdown events if the associated steering control bit (OCxEN) is cleared.

7.6.11.2 Software Shutdown

The user application may invoke a shutdown event at any time by setting the SSDG control bit (CCPxCON2L[12]). This bit behaves exactly like an external shutdown source, except that the polarity of the control bit is inverted. A shutdown event will be caused whenever the SSDG bit is set. The module output pins go to their programmed shutdown state and remain in that condition until the SSDG bit is cleared in software. The software shutdown feature may be used by itself or in parallel with an external source.

Note 1:	The user may also need to clear the ASEVT status bit if automatic restarts are not enabled.
2:	Any enabled shutdown source selected by the ASDGx bits and the SSDG software shutdown bit has priority over a software write to the ASEVT bit. The Fault condition cannot be exited unless all shutdown sources are inactive.

7.6.11.3 Auto-Shutdown Status

The ASEVT status bit (CCPxSTATL[4]) indicates the status of a shutdown event. If the ASEVT bit is cleared, the output pins associated with the CCP module will have normal activity.

If the ASEVT bit is set, then the output pins will be driven to their shutdown states or held in a high-impedance state. The ASEVT bit can also be used as a control bit to manually reset the shutdown condition, as described in **Section 7.6.11.4 "Automatic Restart Enable"**.

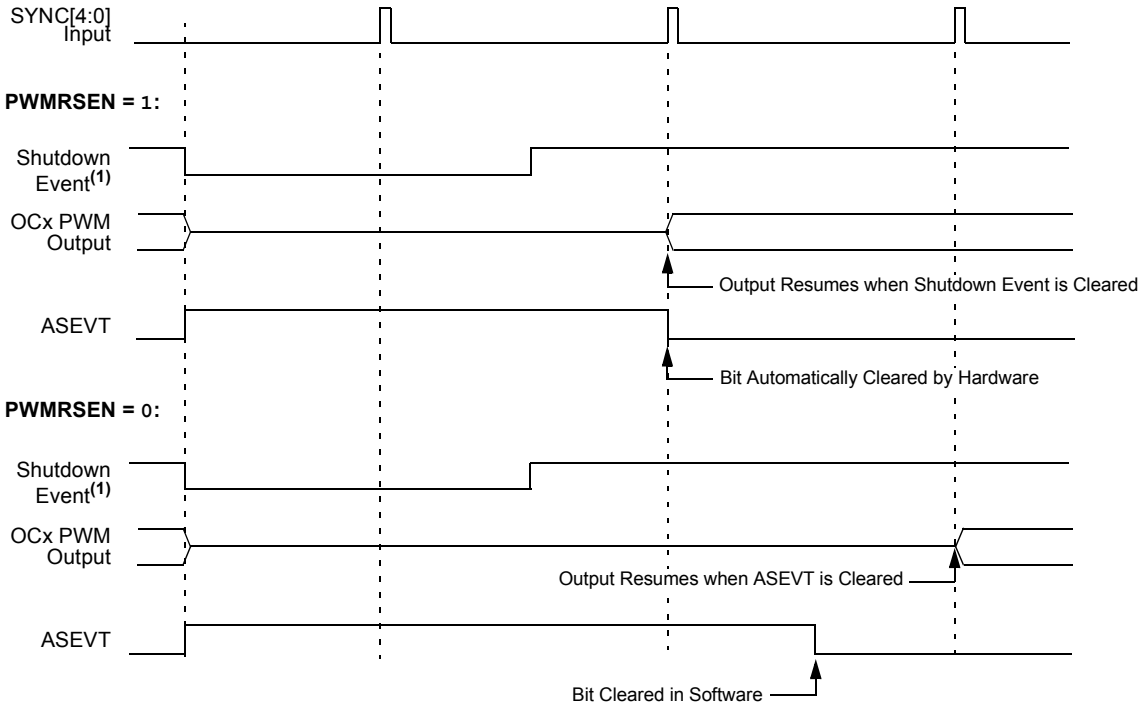
7.6.11.4 Automatic Restart Enable

The PWMRSEN bit (CCPxCON2L[15]) controls how the shutdown state is ended. If PWMRSEN = 0, the module will wait until the ASEVT status bit is cleared in user software. Normal output pin activity can only be resumed when the ASEVT bit is cleared AND the external shutdown source signal is no longer present. If the external shutdown source signal is still active, the user cannot clear the ASEVT bit.

If PWMRSEN = 1, normal output pin activity will automatically resume when the external shutdown source signal is inactive and the next PWM period begins (i.e., when the Sync source selected by SYNC[4:0] is asserted). The ASEVT bit will automatically be cleared in hardware at this time. If the shutdown is still in effect at the time a new cycle begins, that entire cycle is suppressed, thus eliminating narrow, glitch pulses. The PWM outputs are then restarted on the next cycle.

If PWMRSEN = 0, once a shutdown condition occurs, the PWM remains Idle until manually restarted by the user. The module can be restarted by clearing the ASEVT bit in software.

Figure 7-27: Automatic Restart Enable



Note 1: Any device-defined hardware shutdown event when the corresponding ASDG bit is set, or when the SSDG bit is set.

7.6.11.5 Gated Auto-Shutdown Mode

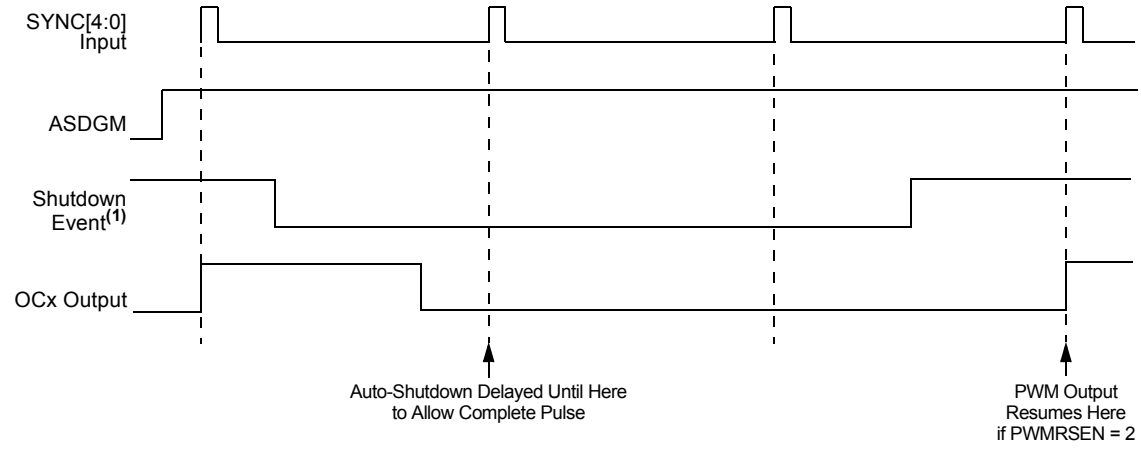
For some types of power control applications, it is useful to delay the effect of the auto-shutdown input. The ASDGM control bit (CCPxCON2L[14]) enables gated shutdown operation. When ASDGM is set, the effect of an auto-shutdown signal input does not take place until the next PWM period boundary. This allows the PWM generator to produce the entire pulse that was programmed for the present cycle.

Pulses are terminated by the hardware beginning on the next cycle. Pulses will resume on the next PWM period after the shutdown event has ended.

Note:	Pulses only resume automatically if PWMRSEN = 1. If PWMRSEN = 0, the ASEVT status bit must be cleared in software for pulses to resume.

The Gated mode allows the Automatic Shutdown mode to be used along with a comparator to implement a 'Pulse Skipping' or 'Gated Oscillator' Switch mode power supply. The inductor is charged for a fixed period of time with each pulse, putting a specific amount of energy into the supply. If the output voltage (current) is high enough, then the comparator gates the pulses.

Figure 7-28: Gated Auto-Shutdown Mode



Note 1: Any device-defined hardware shutdown event when the corresponding ASDGx bit is set, or when the SSDG bit is set.

Note 1:	If automatic restarts are not enabled, the application may also need to clear the ASEVT bit.
2:	Any enabled shutdown source, selected by the ASDGx bits and the SSDG software shutdown bit, takes priority over a software write to the ASEVT bit. The Fault condition cannot be exited unless all shutdown sources are inactive.

7.6.12 OUTPUT POLARITY CONTROL

The polarity of the output pins is controlled by the POLACE and POLBDF control bits (CCPxCON3H[5,4]). The POLACE bit changes the output polarity of the OCxA, OCxC and OCxE pins; the POLBDF bit controls the polarity of the OCxB, OCxD and OCxF pins.

The output polarity control is applied to the output signal after the dead-time control and auto-shutdown logic. The polarity control bits are effective for all Output Compare and PWM modes of the module.

8.0 MODULE SYNC OUTPUTS

By default, the MCCP/SCCP modules generate a CCP Sync signal from the rollover of the CCPxTMR register. This signal is made available to all of the other CCP modules as a Sync source or to trigger another peripheral. The CCP Sync signal is separate from the module's device-level interrupts or other outputs.

There may be circumstances where another event signal may serve as a better basis for the CCP Sync signal or where an additional event output, other than the selected signal, is required. The CCP modules include user configuration options to handle these situations.

8.1 Alternate Sync Out

The ALTSYNC control bit (CCPxCON1H[5]) allows the user to substitute a different synchronization/trigger output in place of the timer rollover for the CCP Sync signal. When ALTSYNC = 0, the CCP Sync output is the default timer rollover signal in all operating modes. When ALTSYNC = 1, the synchronization signal depends on the specific operating mode. Table 8-1 lists the alternate outputs available.

Table 8-1: Alternate Sync Output Signals

ALTSYNC	CCSEL	MOD[3:0]	Output Signal
0	x	All	Standard (default) CCP Sync Output
1	0	0000	Special Event Trigger Output (Timer)
1	0	All except '0000'	Output Compare Interrupt Event (Compare)
1	1	All	Input Capture Event (Capture)

8.2 Auxiliary Output Signal

The MCCP and SCCP modules can also generate a secondary output that is different from the CCP Sync signal (or its alternate version if ALTSYNC is set). The auxiliary output is intended to allow other digital peripherals to access internal CCP module signals, such as:

- Time Base Synchronization
- Peripheral Trigger and Clock Inputs
- Signal Gating

The type of output signal is selected using the AUXOUT[1:0] control bits (CCPxCON2H[4:3]) and is dependent on the module operating mode. More options are available for each mode than with the alternate Sync output, as shown in Table 8-2.

Not all versions of the CCP module have the auxiliary output capability. Refer to the specific device data sheet for details.

Table 8-2: Auxiliary Output Signals

AUXOUT[1:0]	CCSEL	MOD[3:0]	Output Signal
00	x	xxxx	Disabled (no output)
01	0	0000 (Timer modes)	Time Base Period Reset or Rollover
10			Special Event Trigger Output
11			No Output
01	0	'0001' through '1111' (Output Compare modes)	Time Base Period Reset or Rollover
10			Output Compare Event Signal
11			Output Compare Signal
01	1	xxxx (Input Capture modes)	Time Base Period Reset or Rollover
10			Reflects the Value of the ICDIS Bit
11			Input Capture Event Signal

9.0 SYNC AND TRIGGERED OPERATION

Synchronized (“Sync”) and Triggered mode operations can be thought of as Complementary modes that affect the operation of the CCPxTMR registers in most of the module’s major operating modes. Both use the SYNC[4:0] bits (CCPxCON1H[4:0]) to determine the input signal source. The difference is how that signal affects the timer.

In Sync mode operation, the timer counts freely when enabled by the CCPON bit and is reset to zero when the input, selected by SYNC[4:0], is asserted. The timer immediately begins to count again from zero unless it is held for some other reason. Sync operation is used whenever the TRIGEN bit (CCPxCON1H[7]) is cleared.

In Triggered mode operation, the timer is held in Reset until the input selected by SYNC[4:0] is asserted; when this occurs, the timer starts counting and continues to count until the TRCLR bit (CCPxSTATL[5]) is set. Triggered operation is used whenever the TRIGEN bit is set.

Depending on the specific device, the SYNC[4:0] bits allow for the selection of up to 32 internal or external sources. Some implemented sources may be available for triggered operation, but not for Sync operation. In addition, ‘11111’ (free-running counter) is not valid for Sync operation. Refer to the device data sheet for specific details.

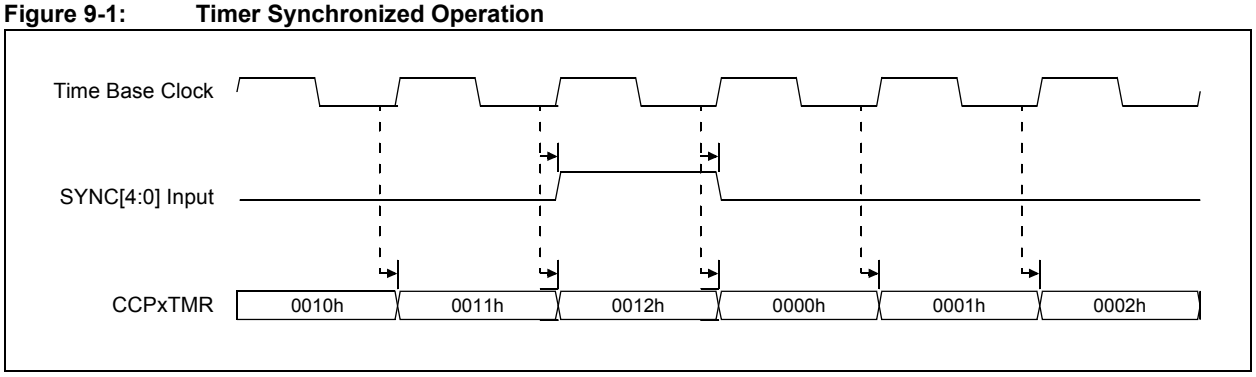
Sync and trigger operations play a major role in the module’s operation in Timer and Output Compare modes by allowing chained, and synchronized operation of multiple modules.

9.1 Timer Synchronized Operation

In Sync operation, the timer can be synchronized with other modules using the synchronization/ trigger inputs selected by SYNC[4:0]. Basic operation is shown in Figure 9-1. Whenever the selected Sync input is asserted (high), the timer rolls over to 0000h on the next positive edge of the time base signal.

The timer functions in Synchronized operation when TRIGEN (CCPxCON1H[7]) is cleared and the SYNC[4:0] bits have any value except ‘11111’. The CCPTRIG bit (CCPxSTATL[7]) has no function.

Figure 9-1: Timer Synchronized Operation



Selecting a SYNCx bits value of '00000' causes the module to run as a periodic timer with automatic rollover to 0000h when the Timer register matches the value of CCPxPR. A value of '11111' rolls over after an overflow from FFFFh.

For values of the SYNC[4:0] bits other than '00000' or '11111', the timer is reset when the input selected by the SYNCx bits is asserted. Refer to the device data sheet for available device-specific inputs.

The procedure for configuring the module for Synchronous operation is shown in Example 9-1.

Example 9-1: Setup for Synchronous Operation (16-Bit Dual Timer Mode)

```
CCP1CON1Hbits.TRIGEN=0;       // Set Sync/Triggered mode (Synchronous Mode)
CCP1CON1Hbits.SYNC = 0;       // rolls over at FFFFh or match
                              // with period register (self sync)
CCP1CON1Lbits.T32=0;          // 16 bit dual timer mode
CCP1CON1Lbits.TMRSYNC = 0;    // Set timebase synchronization (Synchronized)
CCP1CON1Lbits.CLKSEL = 0;     // Set the clock source (Tcy)
CCP1CON1Lbits.TMRPS = 0;      // Set the clock pre-scaler (1:1)
CCP1PRL   =0X0FFF;            // 16 bit MCCP1 low period register
CCP1PRH   =0X0FFF;            // 16 bit MCCP1 high period register
CCP1CON1Lbits.CCPON=1;        // Start the Timer
```

9.1.1 SYNCHRONIZING MULTIPLE MODULES

Each CCP module generates a CCP Sync output signal (see **Section 8.0 "Module Sync Outputs"**) that can be used to synchronize its operation with other modules. This signal is distinct from the module's interrupts or any other output signals. All of the CCP modules have access to each others' Sync signals through the SYNC[4:0] bits; this allows several modules to be chained together for more complex synchronized operations.

A simple example of Synchronized operation is shown in Figure 9-2. In this instance, MCCP2 is being synchronized to MCCP1. Each module has been configured to use the same clock source for their time bases. In addition, both modules use the CCP Sync signal from MCCP1 as their Sync source inputs. CCP1PR now serves as the period register for both MCCP1 and MCCP2.

Figure 9-3 shows the timing relationship between the two modules. When a match between CCP1TMR and CCP1PR occurs, the Sync signal goes active. This causes the timers in both CCP1 and CCP2 to go to 0000h on the next positive timer input clock edge.

When synchronizing modules, there are two important things to keep in mind:

- All synchronized modules are to use the same clock source for their time bases.
- When initializing synchronized modules, the module being used as the synchronization source should be enabled last. This ensures that the timers of all synchronized modules are maintained in a Reset condition until the last module is initialized.

Figure 9-2: Example of Two Synchronized Timers (MCCP2 Synchronized to MCCP1)

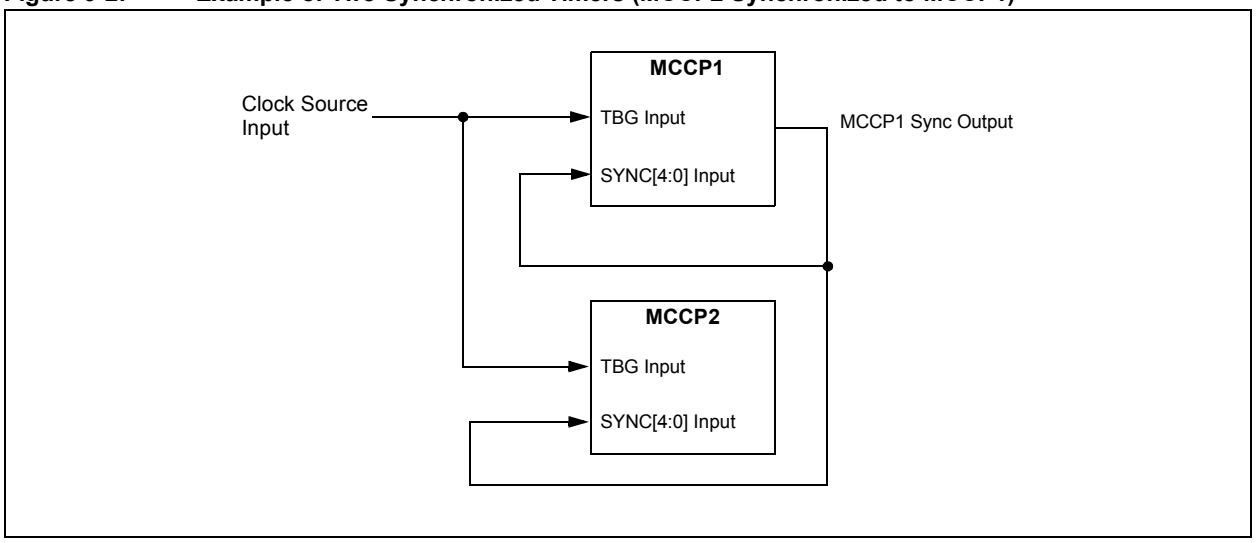
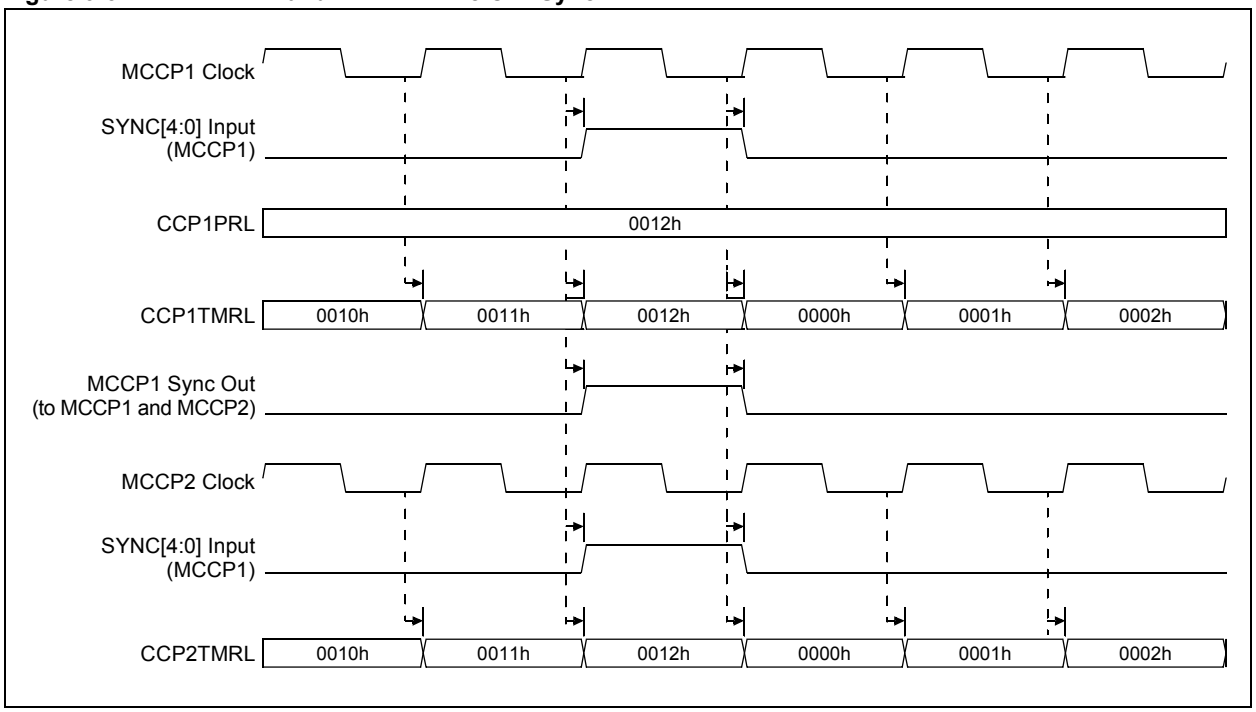


Figure 9-3: MCCP1 and MCCP2 Timers in Sync



9.2 Timer Triggered Operation

Triggered operation of the timer is enabled when TRIGEN = 1. Triggered mode operation is useful in creating time delays. A pulse or edge event can be generated after the delay, depending on the module operating mode.

When configured for triggered operation, the module timer is held in Reset until a trigger event with the source selected by SYNC[4:0] occurs. After the trigger event occurs, the timer begins to count. The timer increments on every positive clock of the time base signal.

If the timer is configured for 16-bit dual timer operation (T32 = 0), only the timer based on CCPxTMRL will function in triggered operation. The timer, based on CCPxTMRH, will operate as a free-running timer.

The CCPTRIG status bit (CCPxSTATL[7]) indicates whether the timer is held in Reset or released to count. When CCPTRIG = 0, the timer is being held in Reset; when CCPTRIG = 1, the timer has been released.

There are two types of trigger conditions when operating in Triggered mode: Hardware/Software and Software-Only. Hardware/software triggered operation is shown in Figure 9-4. When the module is enabled for a triggered response, the timer is held in Reset. It remains in this state until a trigger event is asserted for the SYNC[4:0] input, which sets the CCPTRIG bit within two clock cycles. The trigger signal determines only when the time base starts counting; the CCPxPR register sets the period for the timer. Unlike Sync operation, all trigger sources available through the SYNC[4:0] bits may be used for triggered operation.

CCPTRIG can be manually set at any time and the timer can be released from Reset by writing a '1' to the TRSET bit (CCPxSTATL[6]). The CCPTRIG bit can also be manually cleared in software by writing a '1' to the TRCLR bit (CCPxSTATL[5]).

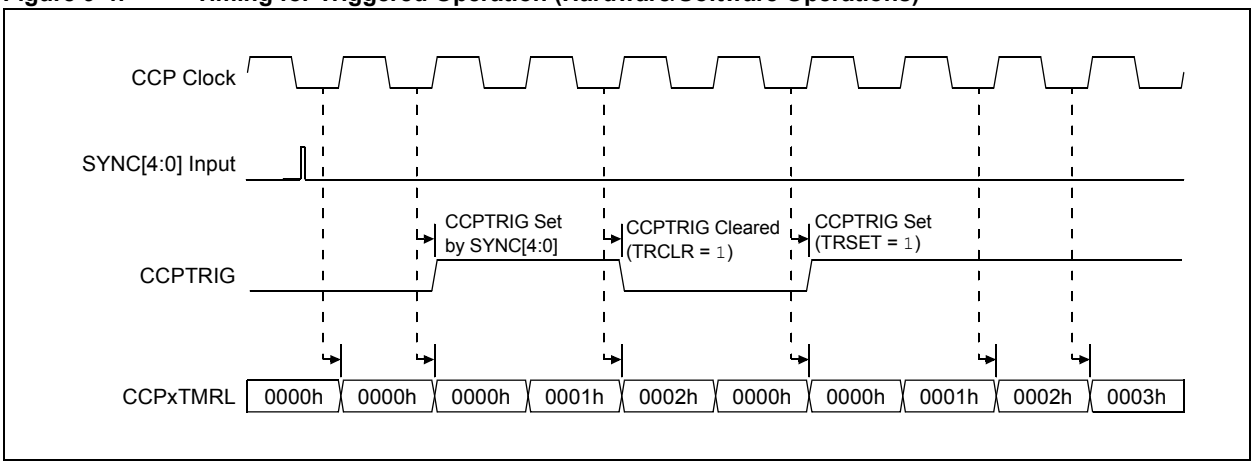
Software-Only operation is selected when SYNC[4:0] = 11111. In this configuration, the only way that the CCPTRIG bit can be set is by a software write to the TRSET bit. This selection effectively disables all external hardware trigger sources.

When the TRIGEN bit is cleared in software, the timer is reset to 0000h on the next timer clock rising edge and is ready for another SYNC[4:0].

Note:	The TRSET and TRCLR bits are write-only bits which always read as '0'. Writing '0' to either location has no effect.

The procedure for configuring the module for triggered operation is shown in Example 9-2.

Figure 9-4: Timing for Triggered Operation (Hardware/Software Operations)



Example 9-2: Setup for Timer Triggered Operation (16-Bit Dual Timer Mode)

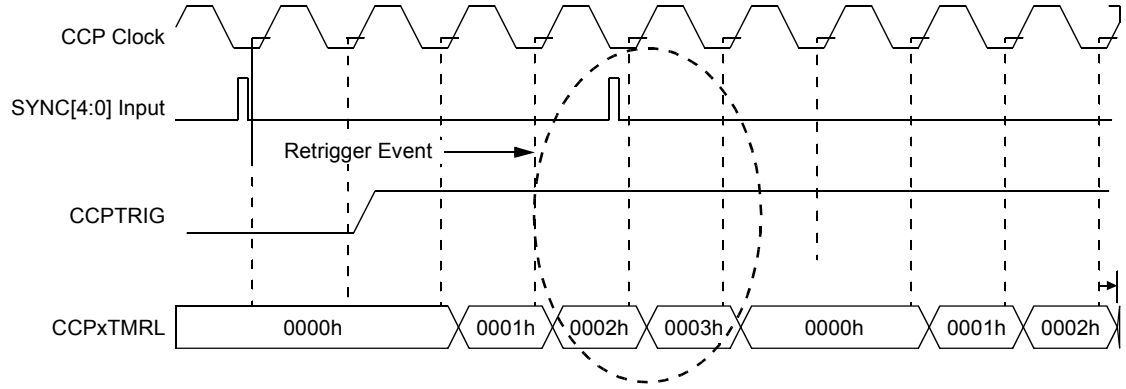
```
CCP1CON1Hbits.TRIGEN=1;        // Set Sync/Triggered mode (Triggered Mode)
CCP1CON1Hbits.SYNC = 0x08;     // INT0 as trigger (verify the data sheet
                               // for Trigger source)
CCP1CON1Lbits.T32=0;           // 16 bit dual timer mode
CCP1CON1Lbits.TMRSYNC = 0;     // Set timebase synchronization (Synchronized)
CCP1CON1Lbits.CLKSEL = 0;      // Set the clock source (Tcy)
CCP1CON1Lbits.TMRPS = 0;       // Set the clock pre-scaler (1:1)
CCP1PRL    =0X0FFF;            // 16-bit MCCP1 low period register
CCP1PRH    =0X0FFF;            // 16-bit MCCP1 high period register
CCP1CON1Lbits.CCPON=1;         // Enable the Timer
```

9.2.1 RETRIGGER OPERATION

The RTRGEN bit (CCPxCON1H[14]) allows the timer to be retriggered while the CCPTRIG bit remains set. When RTRGEN is set, a second trigger event occurring during trigger operation will cause the timer to reset and start counting again. Figure 9-5 shows how the timer restarts counting when the trigger comes again, before the timer overflow happens.

When RTRGEN = 1, multiple trigger pulses occurring within the same time base clock period will not be recognized and will be treated as a single trigger event. If trigger pulses are received on two adjacent timer clock periods, the time base will be held in Reset (0000h) for one additional clock period.

Figure 9-5: Retrigger Operation (RTRGEN = 1)



Note: In the example, if the CCPxPRL is 10h, the timer will reset before the 10h since the retrigger came before the timer reached 10h.

9.2.2 TRIGGERED OPERATION WITH ASYNCHRONOUS CLOCK

The module time base can operate from a variety of clock sources; these may or may not be synchronous to the system clock. In addition, the trigger source may be asynchronous to the module time base clock. To minimize glitches, the incoming trigger signal is latched and synchronized to the module's time base clock source by default.

When the time base clock source is asynchronous to the system clock, there will be a delay of up to two system clock cycles before the trigger state is reflected in the value of the CCPTRIG status bit.

When the time base clock source is asynchronous to the system clock, there will be a delay of up to two time base clock cycles before a trigger set or clear request from software affects the trigger state of the module.

9.2.3 TIMER ROLLOVER IN TRIGGERED OPERATION

When the module is configured for triggered operation, the signal source selected by SYNC[4:0] does not set the time base count period. The primary purpose of the trigger signal is to tell the timer when to start counting, not when to reset (as in Sync mode).

The timer rolls over to 0000h on the next clock after CCPxPRH/L matches CCPxTMRH/L or when CCPxTMRH/L reaches FFFFh (if CCPxPRH/L is not available in the specific operating mode of the module).

There are two values of SYNC[4:0] that are not allowed in triggered operation:

- '00000' (synchronous timer, external triggers are disabled)
- Any value that selects the module's own CCP Sync signal (a trigger must be external)

If the trigger source selected by SYNC[4:0] is initialized and enabled first, there is a chance that the timer will miss trigger events. Therefore, it is recommended the timer be initialized and enabled before the trigger source.

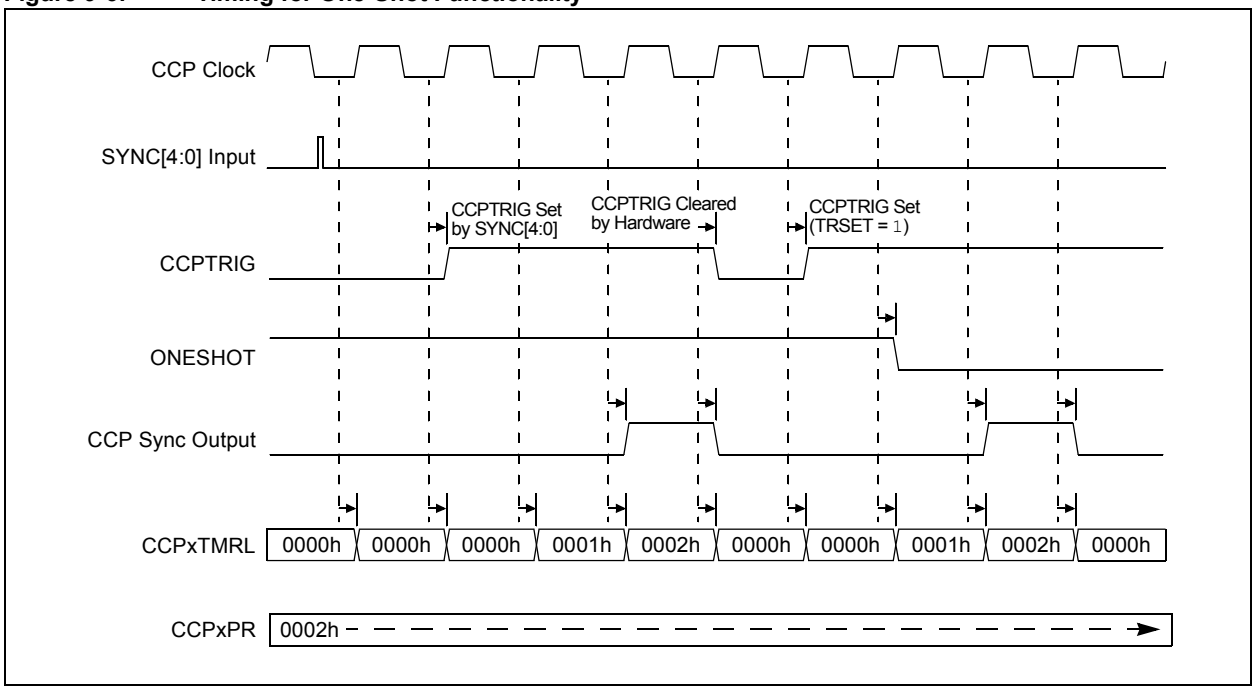
9.2.4 ONE-SHOT FUNCTIONALITY

While in triggered operation, the timer can operate in a One-Shot mode. In this mode, the timer remains in Reset until a hardware or software trigger event occurs. This event sets the CCPTRIG bit and the timer begins to count. When the timer rolls over to 0000h, the CCPTRIG bit is cleared by hardware. This holds the timer in Reset until the next trigger event, creating a one-shot timer.

One-Shot mode is enabled by setting the ONESHOT bit (CCPxCON1H[6]). The OSCNT[2:0] control bits (CCPxCON3H[14:12]) allow a one-shot trigger event to be extended for more than one CCP timer clock cycle. This feature is useful, for example, when the module needs to create more than one pulse at a trigger event.

Note:	Do not modify OSCNT[2:0] while the module is triggered (CCPTRIG = 1); unexpected results may occur.

Figure 9-6: Timing for One-Shot Functionality



10.0 OPERATION DURING SLEEP AND IDLE MODES

10.1 Idle Mode

The behavior of the module in Idle mode is determined by the CCPSIDL bit (CCPxCON1L[13]). If CCPSIDL is cleared, the module will continue to operate in Idle mode. If CCPSIDL is set, the module is disabled when the device enters Idle mode. If the module is performing an operation when Idle mode is invoked, in this case, the results will be similar to those with Sleep mode.

10.2 Sleep Modes

The behavior of the module in Sleep mode is determined by the CCPSLP bit (CCPxCON1L[12]). If CCPSLP is set, the module will continue to operate during Sleep mode, assuming that the selected clock source remains available. The TMRSYNC bit must remain cleared for the module to operate in Sleep mode.

When CCPSLP is cleared and the device enters Sleep mode, the module is disabled. However, if CCPSLP is set and the module is configured for 16-Bit Edge Detect Input Capture mode (MOD[3:0] = 0000, CCSEL = 1), the module can generate an interrupt and wake up the device, as long as the clock source remains active. In this configuration, the Input Capture pin can function like an external interrupt. The corresponding CCP interrupt must also be enabled (CCPxIE = 1).

10.2.1 TRIGGERED OPERATION AND SLEEP MODE

When the module is configured for triggered operation, a trigger signal received from an external source can also wake the module and its time base clock source. The module must request the time base clock source before triggered operation can begin. When the trigger is received from the external source, the CCP module will enable the selected clock source for the time base. When the clock source becomes available, the module will begin triggered operation.

If One-Shot Triggered mode is selected, the time base clock source will be disabled when the CCPTRIG status bit is cleared in hardware. The time base remains disabled until a new trigger signal is received.

The trigger signal can also be generated by an internal source that operates from a low-power clock source.

If Sleep mode operation is enabled, the module will continue to request the configured clock source when the device enters Sleep mode.

11.0 EFFECTS OF A RESET

A device Reset forces all registers to their Reset state; this disables the module and returns it to its default configuration (16-bit timer). All buffer and address registers are initialized to 0000h and all status flags are reset.

By default, the pin associated with OCxA (MCCP modules) or OCx (SCCP modules) resets with the Output Compare function in control of the pin; however, this has no effect when the module is disabled.

12.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 device families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Capture/Compare/PWM/Timer (MCCP and SCCP) are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip website (www.microchip.com) for additional application notes and code examples for the dsPIC33/PIC24 families of devices.

13.0 REVISION HISTORY

Revision A (March 2013)

Original version of this document.

Revision B (February 2019)

Updated **Section 2.0 "Registers"**.

Added Register 3-8, Register 3-9, Register 3-10, Register 3-11, Register 3-12, Register 3-13, Register 3-14 and Register 3-15.

Re-ordered major chapters.

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