Course 3

Running Simulation in GUI mode

Rev. Oct 11, 2012

Applies to Active-HDL 9.2 and later

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Creating workspace and design

Active-HDL allows collecting individual designs along with their resources (source files, output files with simulation results, etc.) into a group of projects referred to as a ***workspace***. A workspace allows working with several projects simultaneously because it acts as a container for Active-HDL designs.

Creating workspace using wizard

- Go to menu **`File | New`** and select **`Workspace`**
- Type the name of the workspace and select the location for where you would like your projects to be saved
- **Check** the **`Add New Design to Workspace`** option, and click OK.

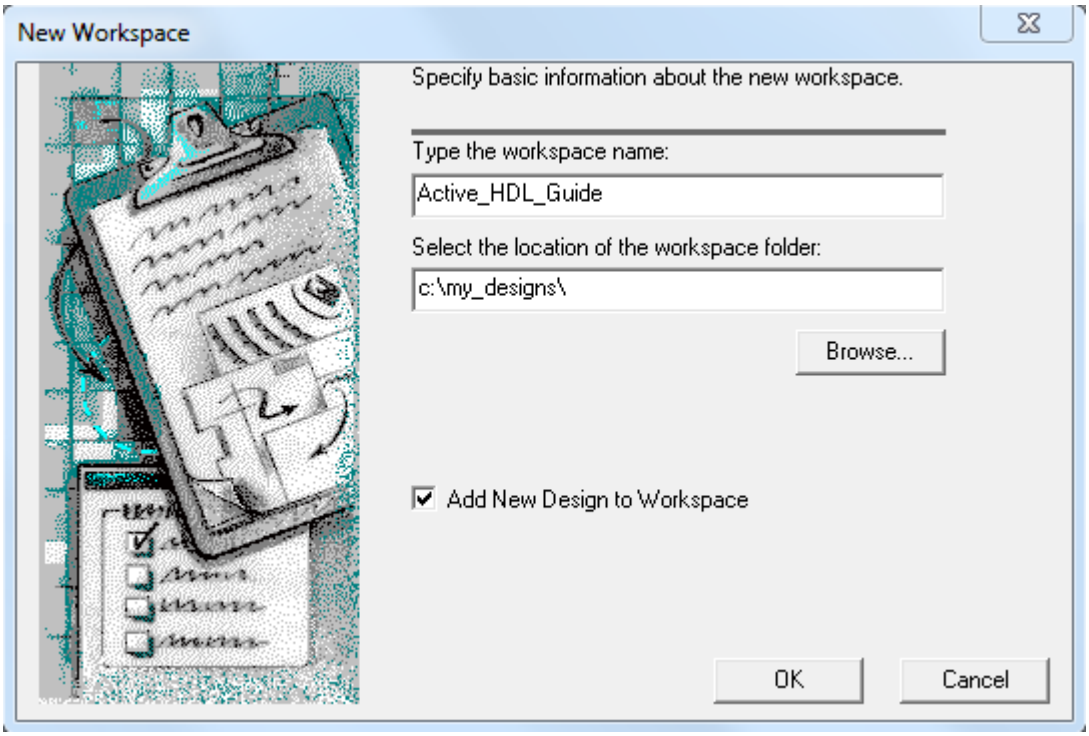

Figure 1 Create new workspace wizard: workspace window

- The **New Design Wizard** window will pop up and give you four options of creating your design:

Create an Empty Design

Creates an empty design with no synthesis or implementation tool set and disables the Design Flow Manager. It allows you to specify the Design Language and Target Technology of the new design.

Create an Empty Design with Design Flow

Creates an empty design and enables the Design Flow Manager. It allows you to specify the Synthesis tool, Implementation tool, Block Diagram Configuration, and Default HDL Language.

Add existing Resource Files

Creates an empty design and enables the Design Flow Manager. It allows you to specify the sources to be added prior to creating the design, as well as specify the Synthesis tool, Implementation tool, Block Diagram Configuration, and Default HDL Language.

Import a Design from Active-CAD

Creates an empty design, imports an Active-CAD project, and enables the Design Flow Manager. It allows you to specify the sources to be added prior to creating the design, as well as specify the Synthesis tool, Implementation tool, Block Diagram Configuration, and Default HDL Language.

Select an option and continue to the next window.

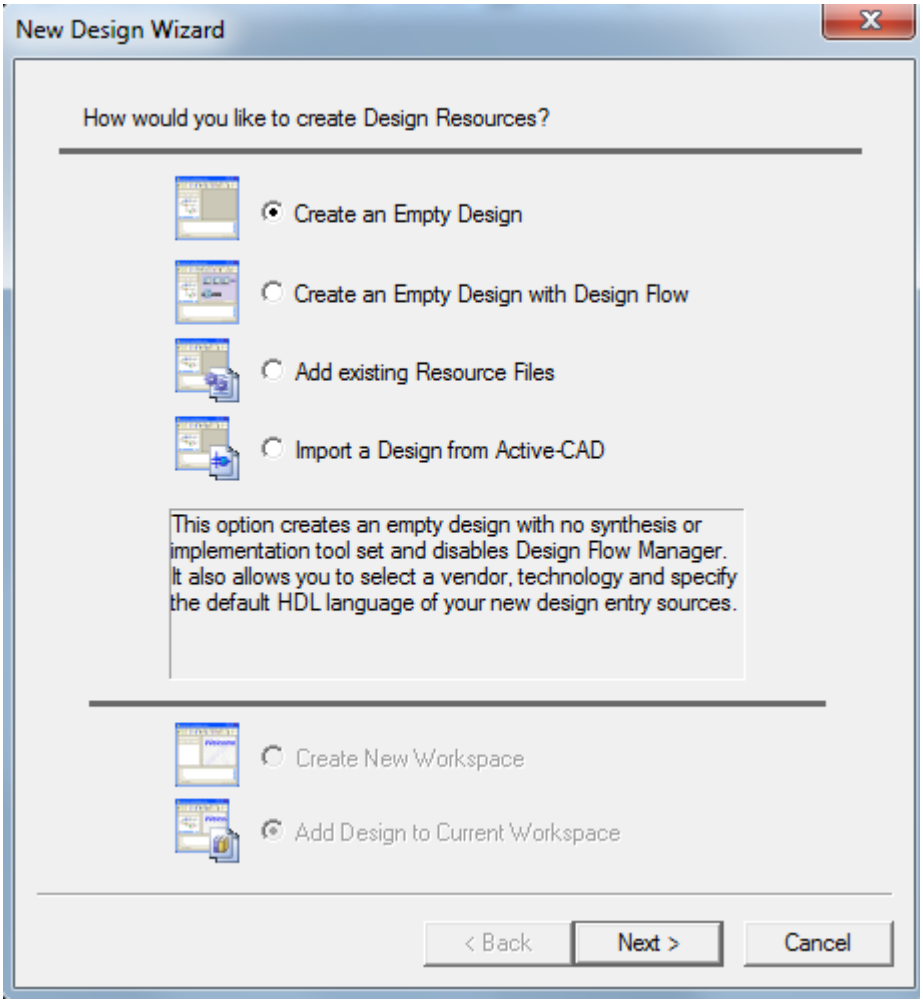

Figure 2 create new workspace wizard: new design

The next window is the **Property Page** which allows you to choose the **Design Language: Block Diagram Configuration** and **Default HDL Language** (Verilog or VHDL). You can then specify the **Target Technology: Vendor** (Lattice, Altera, etc.) and **Technology**. Otherwise, accept the default settings and continue to the next window.

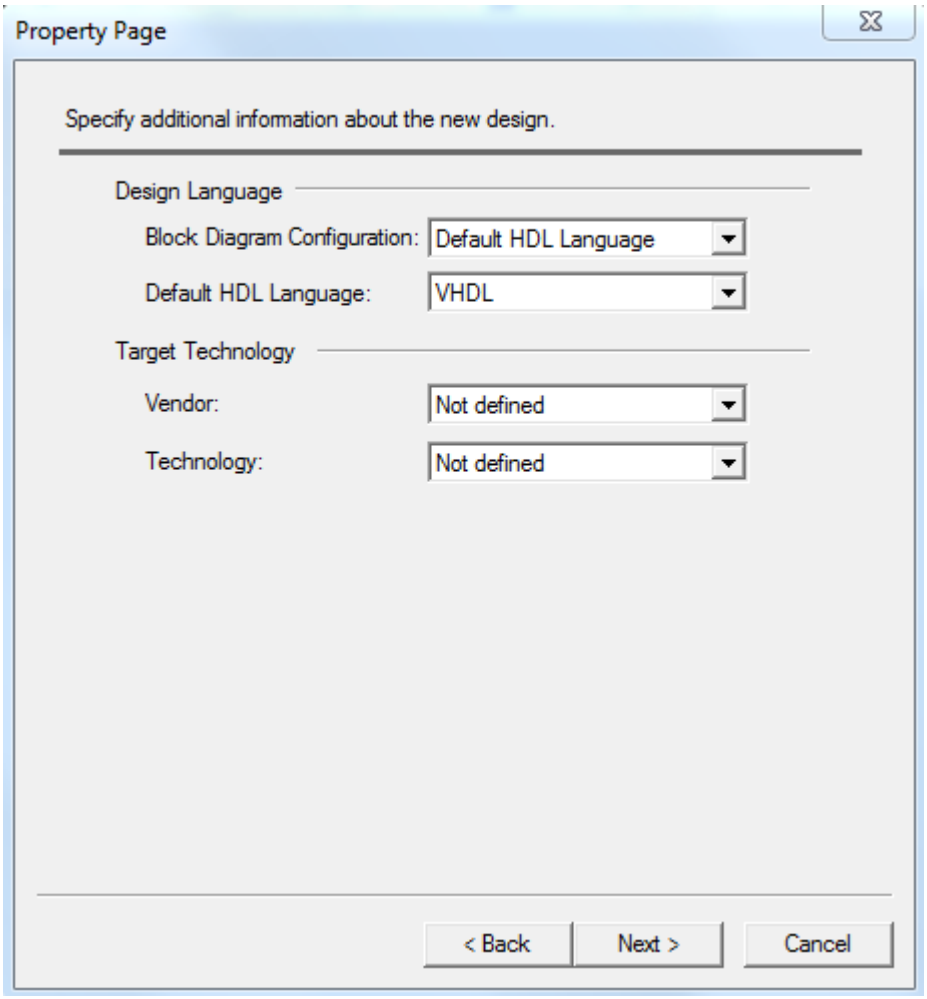

Figure 3 create new workspace wizard: property page

The next window asks to specify the name of the design and the name of the default working library. By default, the name is the same for both.

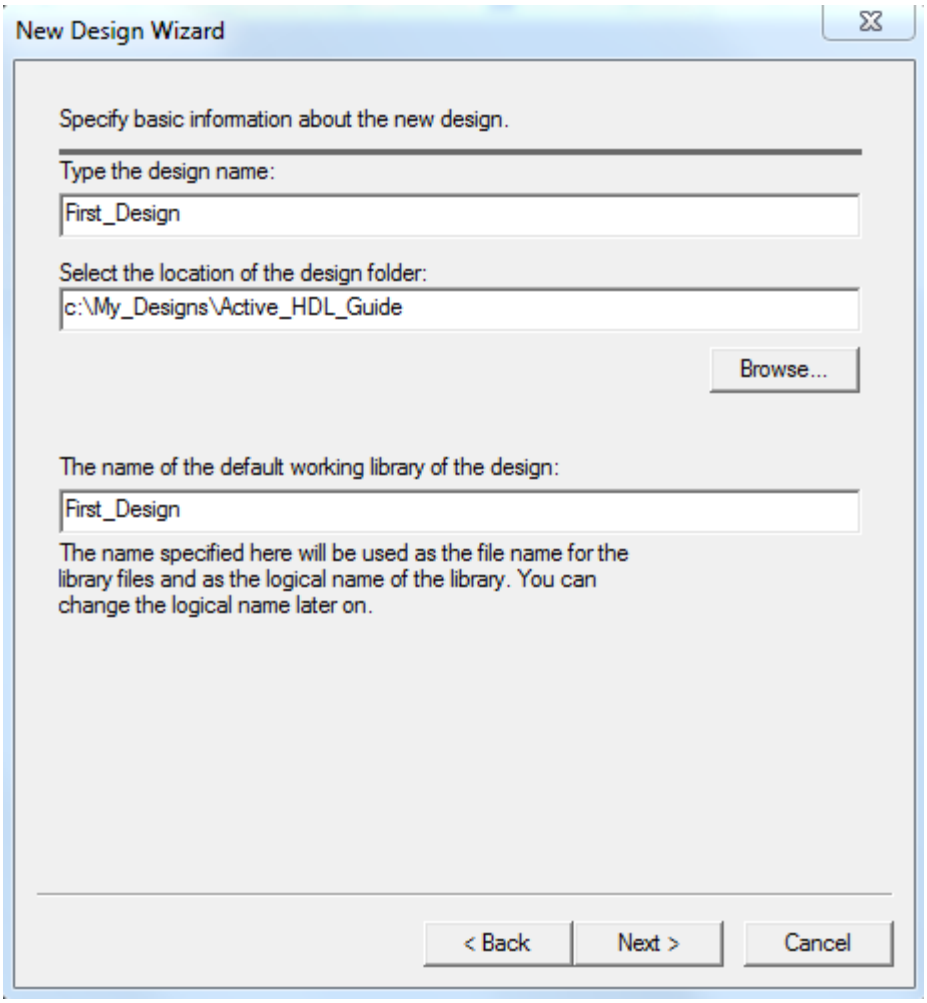

Figure 4 create new workspace wizard: design name

The last window will show you a summary of the design specifications. If you need to change something, click the back button. Otherwise click Finish.

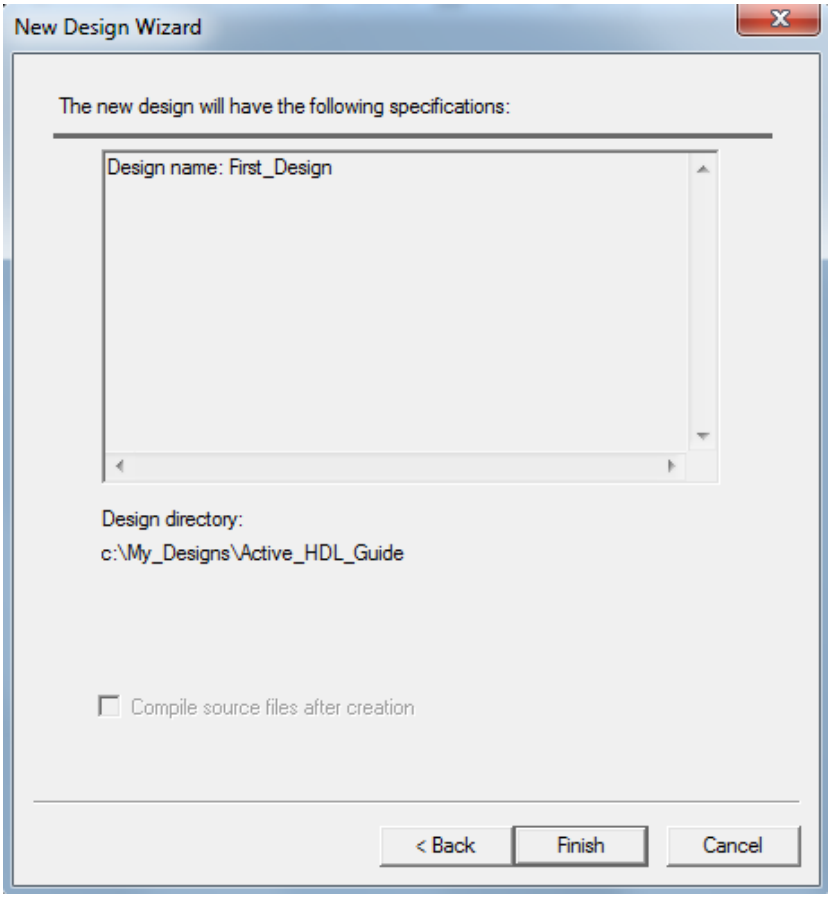

Figure 5 create new workspace wizard: design specifications

- The ***Design Browser*** now shows a workspace name and new design attached with it

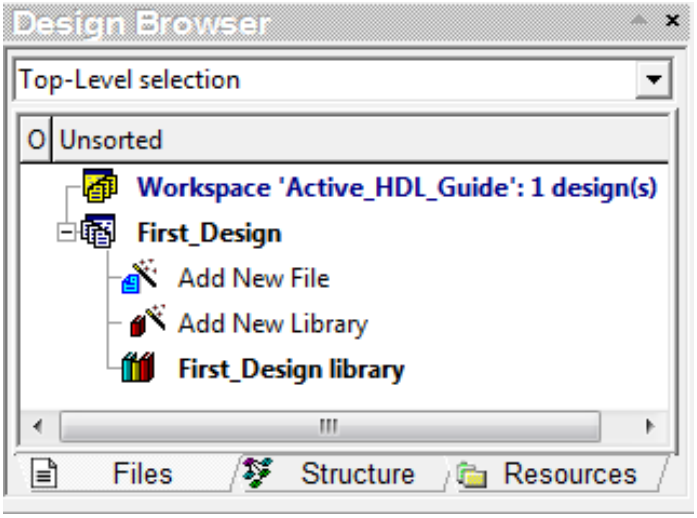

Figure 6 Design manager after workspace and design created

Creating/Adding files to the design

- To create a new file, right click on the “Add New File” option, click on “New” and then select the desired operation.
- To add an existing file, right click on “Add New File” and select “Add Files to Design” option
- You can also use **File | New** menu to open new files and save it to design directory.

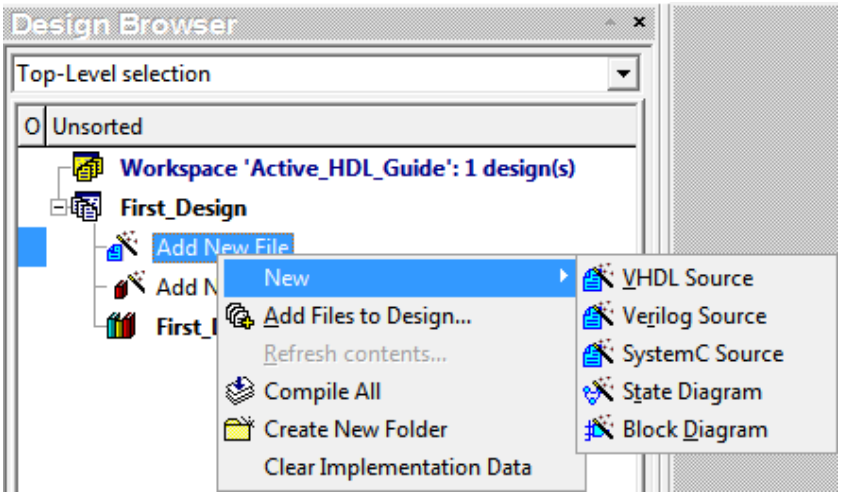

Figure 7 Add new file to design

Compiling files

If you want to compile just one file go the Files tab in the Design Browser, select the file, right click and choose **Compile** from the shortcut menu for a source file.

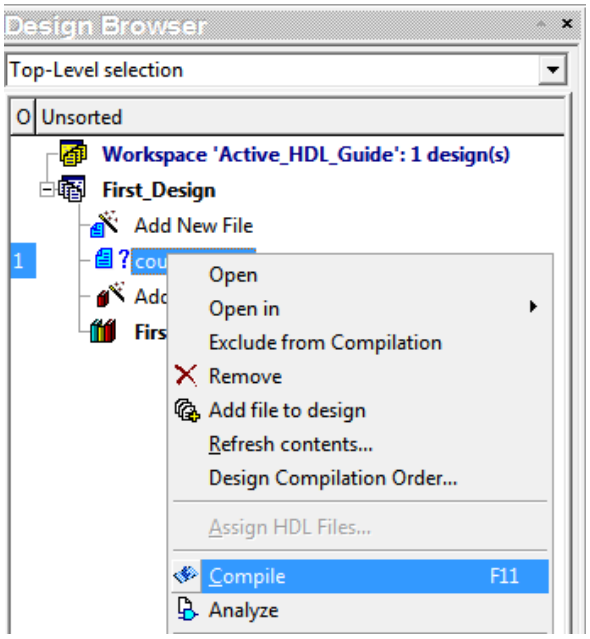

Figure 8 Compile file

If you choose **Compile All** from the **Design** menu for a given design all the files from the design are compiled. Please keep in mind that user is required to order the file manually in design browser. If you select **Compile All With File Reorder**, the compiler automatically reorders source files to ensure proper sequence in which design units are compiled. (Refer Figure 9)

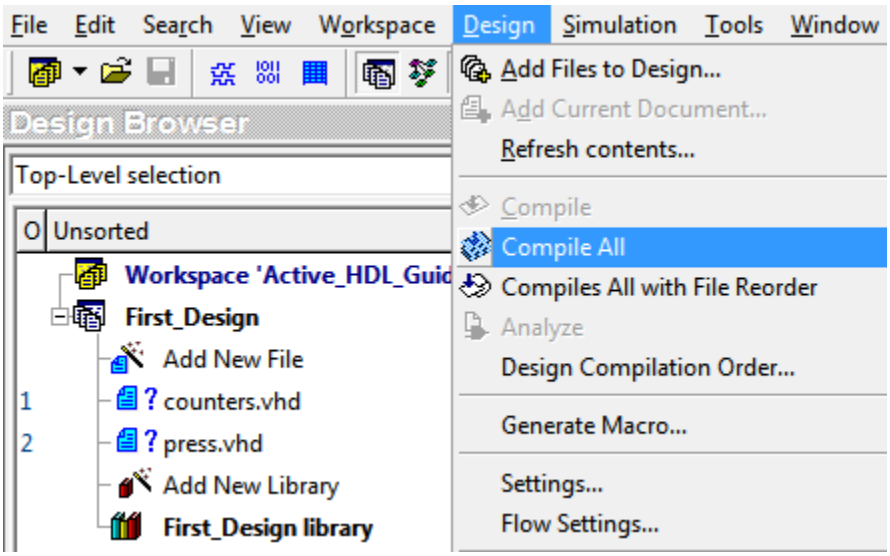

Figure 9 Compile All file option

Initializing the Simulation

Once all needed design units have been successfully compiled, you can initialize the simulation. Before you initialize the simulation, make sure that:

- You have selected the top-level design unit. You can select the top level in three ways:
    1. Select the desired VHDL design entity or configuration, Verilog module, EDIF cell, or SystemC module from the drop-down list located at the very top of the **Design Browser** window

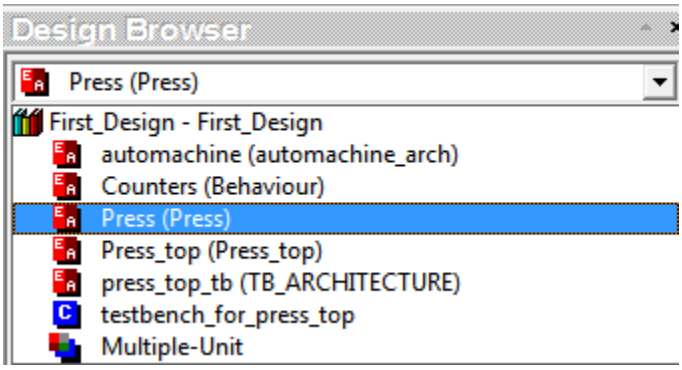

Figure 10 Selecting top level – Drop Down window

2. Expand a structure of a source file (containing a top-level unit) or current working library in the **Files** tab, right-click on the desired design unit and then choose **Set as Top-Level** from the shortcut menu.

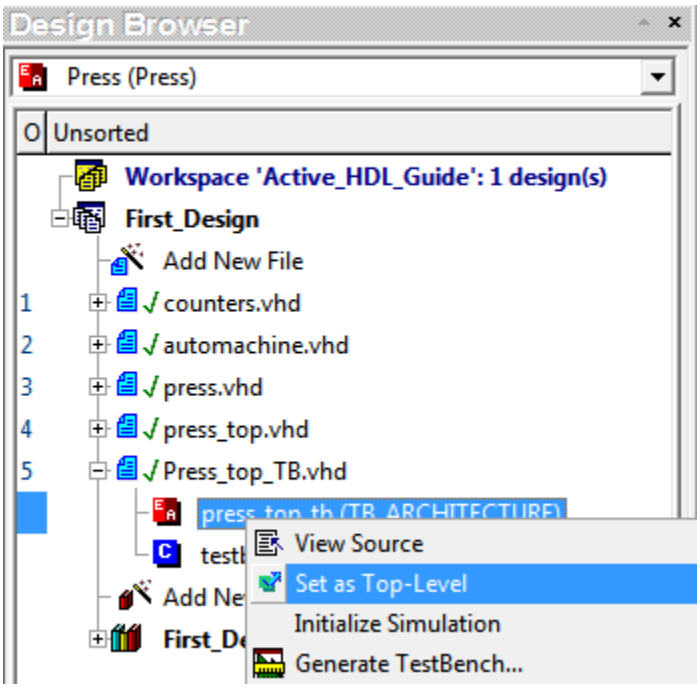

Figure 11 Selecting top level – Expanding the source file

3. Open the **Design Setting Window**. By default, the **General** category is displayed. Go to the Top-level category and select a top-level unit from the list of design units.

To begin simulation, you must choose **Initialize Simulation** from the **Simulation** menu. This will launch the elaboration and initialization of the simulation model. During elaboration, the simulator loads design units, and builds the simulation model in the computer memory. During the initialization, all objects in the model (signals, variables, etc.) acquire their initial values (either default or explicitly specified) and all concurrent processes are executed once until their suspension.

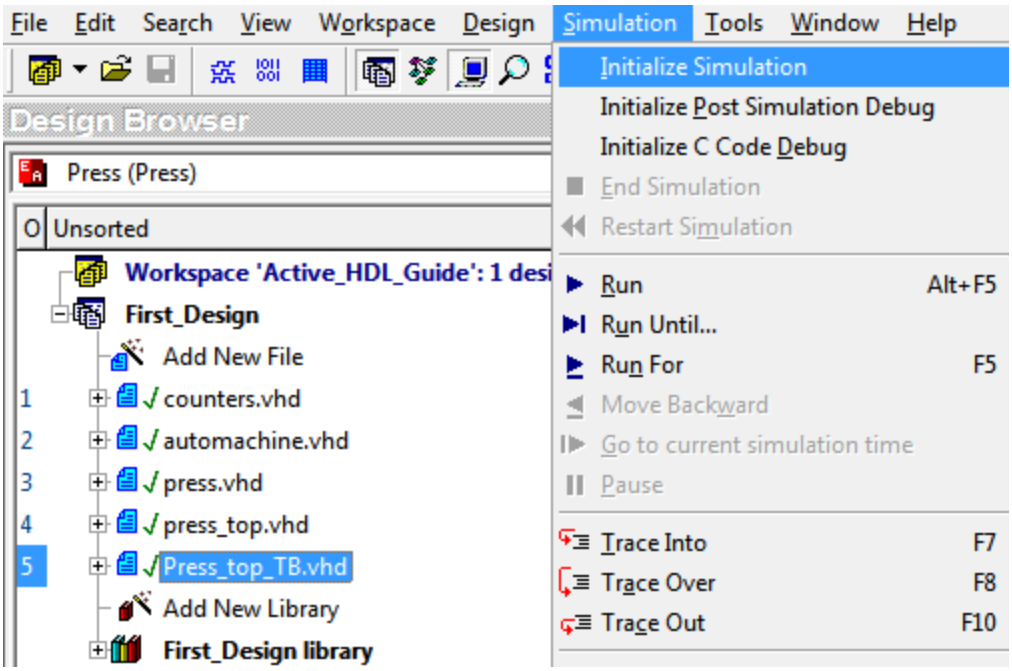

Figure 12 Initializing the simulation

Running the Simulation

After simulation has been initialized, design can be run using **Run** from the **Simulation** menu.

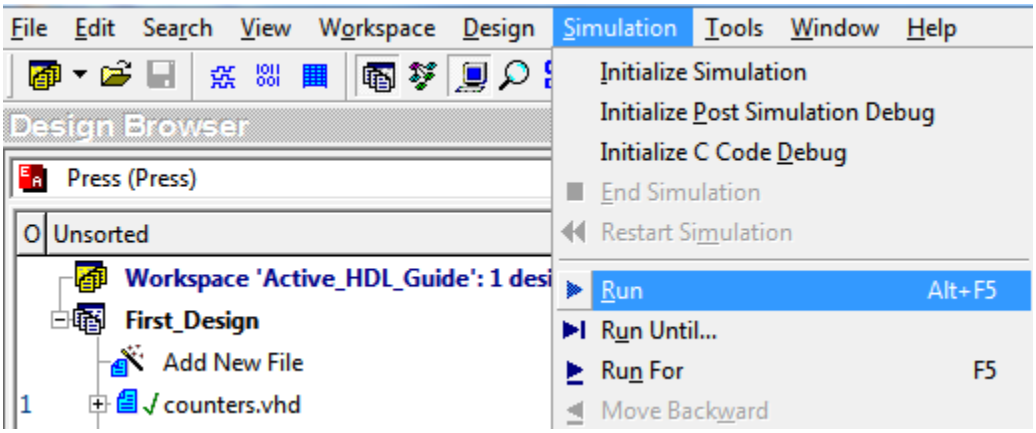

Figure 13 Running Simulation