Course 2

Running Simulation in Batch mode

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Introduction

This document describes running an HDL simulation using Active-HDL in the batch mode. It has been tested on Active-HDL 9.2. If you have any questions about compatibility, please contact support@aldec.com

Tool Operation Modes

Active-HDL can operate in three different modes as described in the table below.

Table 1. Modes of Operation

Mode	Description	How To Invoke
GUI	Interactive graphical interface: windows, menus, push-buttons, and Command Line in the Console window.	Desktop icon or the following command from the OS command shell prompt: `> avhdl.exe`
Interactive Command Line	Interactive Command Line, no GUI.	Desktop icon or the following command from the OS command shell prompt: `> vsimsa`
Batch	Non-interactive batch execution, no GUI or Interactive Command Line.	Command from the OS command shell prompt: `> vsim <arguments>`

To compile and simulate a design in the batch mode you can either run Active-HDL commands in the tool shell, or you can execute Active-HDL commands directly in the OS console.

Running Active-HDL in the Tool Shell Mode

You can start Active-HDL in the shell mode by running the **vsimsa** file located in */BIN* folder in the Active-HDL installation directory. It forces the execution of the configuration files that set all necessary system variables and then starts the **vsimsa** batch mode simulator.

Note. All paths in this document are relative to the installation directory of Active-HDL.

When the **vsimsa** shell starts, you can start manually entering Active-HDL commands in the command prompt as shown below.

```
$alib work
ALIB: Library `work' attached.
work = C:\tester\my_designs\counter\work\work.lib
$set worklib work
VSIMSA: 'work' is now working library.
```

Note. '$' indicates the **vsimsa** shell prompt

Alternatively you can put Active-HDL commands in the macro file with .do or .tcl extension and execute them in the batch:

```
$do runsim.do
```

The *runsim.do* macro script can contain the following commands:

```
#creating library
alib work
#setting work library as the default target for all commands
set worklib work
#compiling verilog source files
alog file1.v file2.v file3.v
#starting simulation with tb_top as the top level module
asim tb_top
#running the simulation
run –all
#closing the simulation
endsim
```

Note. For VHDL compilation you have to use **`acom`** command:

```
acom file1.vhd file2.vhd …
```

The vsimsa command prompt will return when the execution of the vsimsa with macro is completed without errors. If you want the vsimsa shell to be closed upon the script completion end your macro script with the *`quit`* command.

If the macro execution errors out, vsimsa will exit the macro to allow you to read all the messages and examine the source of the problem. If you want vsimsa to continue macro execution after it reports an error, add the following entry to your macro file:

```
onerror {
  resume
}
```

For complete syntax of the above Active-HDL commands please refer to the HTML help file <Active-HDL Installation Dir>/BOOKS/Avhdl.chm

Running Active-HDL Commands in the OS shell

The most important Active-HDL commands are available as standalone executables and can be invoked directly from the operating system shell. All external commands are located in the *BIN/* subdirectory of the Active-HDL installation directory. External commands can be used for library management, compilation, simulation, etc.

For complete syntax and description please refer to the HTML help file <Active-HDL Installation Dir>/BOOKS/Avhdl.chm

Below you can find the list of most frequently used Active-HDL commands.

Library Management Commands

- `vlib` (creates a new library)
- `vlist` (lists libraries visible from the current directory)
- `vdir` (lists library contents)
- `vdel` (removes compiled units from a library)
- `vmap` (adds or removes library mappings)

Compilation Commands

- `vcom` (compiles VHDL files)
- `vlog` (compiles Verilog files)
- `ccomp` (compiles SystemC files)
- `addsc` (imports SystemC modules from a shared object library or a dynamic-link library)

Simulation Commands

- `vsim` (elaborates the design and runs simulation)

ASDB Manipulation

- `asdbcompare` (compares two ASDB files and generates a text report)
- asdb conversion utilities (`asdb2ctf, asdb2ctv, asdb2lst, asdb2macro, asdb2vcd, vcd2asdb`)

Below you can see a complete example of the shell script that calls external Active-HDL commands to compile and simulate the design.

```
# create library v_bjack
vlib v_bjack

# compile source files
# working library is specified with –work switch
vlog -work bjack src/*.v

# initialize simulation
vsim -lib bjack V_BJACK_tb –do run.do
```

The vsim command in the example above calls **run.do** macro file that contains two commands:

```
run –all
quit
```

Please refer to the Waveform Viewer course to see how to enable signal values dumping in Active-HDL.