Design Flow Manager

Learn how to use Design Flow Manager

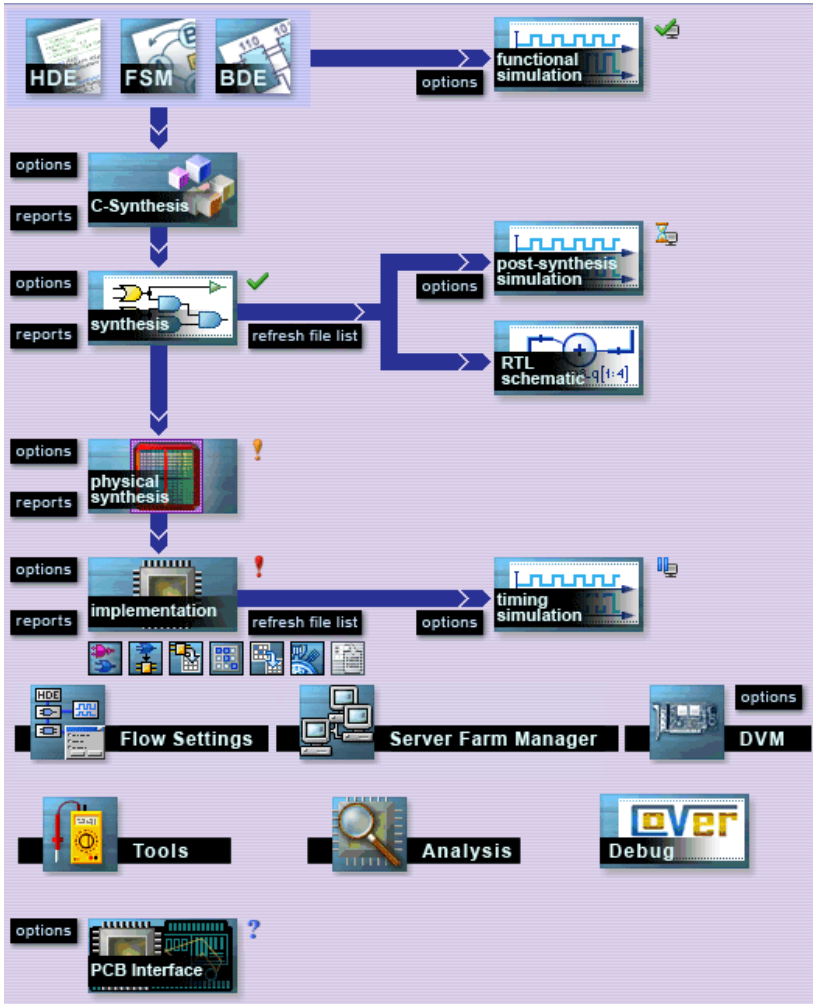
Outline

- Overview
- Design Entry
  - HDE, BDE, FSM
- Functional Simulation
- Synthesis
  - C, HDL, Physical
- Post-synthesis Simulation
- Implementation
- Timing Simulation
- Tools & Analysis
- PCB Tools

Overview

- The **Design Flow Manager** is a tool implemented in Active-HDL that is designed to automate and simplify the design, synthesis, and implementation processes.

- The interface of the of the **Design Flow Manager** takes the form of *design flowcharts* which show the design path in graphical form.



Overview (cont.)

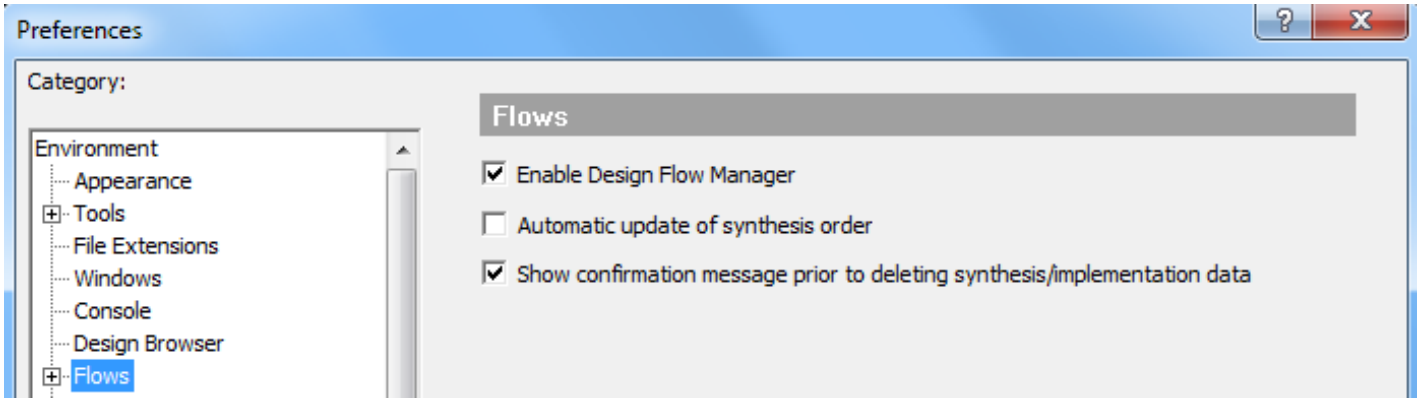
- The main functions of the **Design Flow Manager** are:
- Handling bi-directional communication between the Active-HDL environment and external third-party tools used for C/HDL *synthesis* and *implementation*
- Specifying and customizing synthesis and implementation settings for individual vendor tools and design processes.
- Providing a graphical user interface that allows controlling external third-party C/HDL/physical synthesis and implementation tools from the Active-HDL environment.
- Version/Revision control: compares dates of the design files and library units' modifications at all stages of the design processing to ensure all changes introduced into the source files propagate through the entire design path.
- Initializing and running *functional, post-synthesis, and timing* simulations.
- Launching additional vendor-specific flow tools through built-in interfaces.

Overview (cont.)

- The benefit of having the **Design Flow Manager** in the form of graphical *design flowcharts*:
  - Allows running a C/HDL/physical synthesis and implementation process in the GUI or batch mode using scripts.
  - Interactive buttons that invoke applications used to process the design which allows the user to perform everything in one tool rather than switching back and forth between multiple tools.
  - Displays synthesis and implementation status information
  - Provides access to synthesis, implementation, and simulation options.
  - Provides access to additional flow tools provided by EDA vendors
  - Allows exporting/importing pin assignments between third-party synthesis and implementation tools selected in the Design Flow Manager and external PCB tools

Overview (cont.)

- To enable the **Design Flow Manager**:
- Go to the **Preferences** dialog box, **Environment|Flows** and select the **Enable Design Flow Manager** check box.



- To view your design flow:
- In your Active-HDL toolbar, select the **View Flow** icon 

Overview (cont.)

- A typical design flow has three phases which are each followed by a simulation
- **Design Entry**
  - HDE
  - BDE
  - FSM
- **Synthesis**
  - C
  - HDL
  - Physical
- **Implementation**

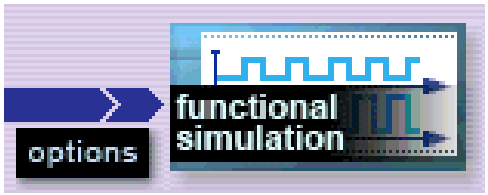
Design Entry

- The **Design Entry** phase of the **Design Flow Manager** is where you create your design that consists of:
- HDL source files
- Finite State Machines
- Block Diagrams

- After these files are created, you can simulate them using **Functional Simulation**.

Functional Simulation

- You can customize your simulation using the *options* button.

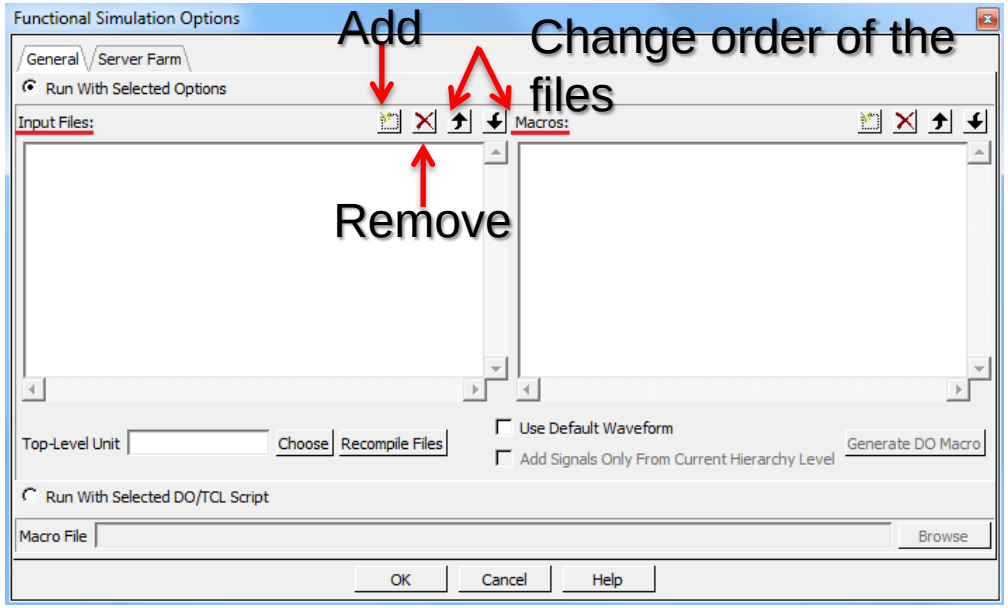


- There are two ways to run the simulation:
- **Run with Selected Options**
  - The simulation initialized from the flowchart window will be run based on the settings specified under this dialog box.
- **Run With Selected DO/TCL Script**
  - The simulation initialized from the flowchart window will be run based on the settings defined within the macro specified in the **Macro File** box.

Functional Simulation (cont.)

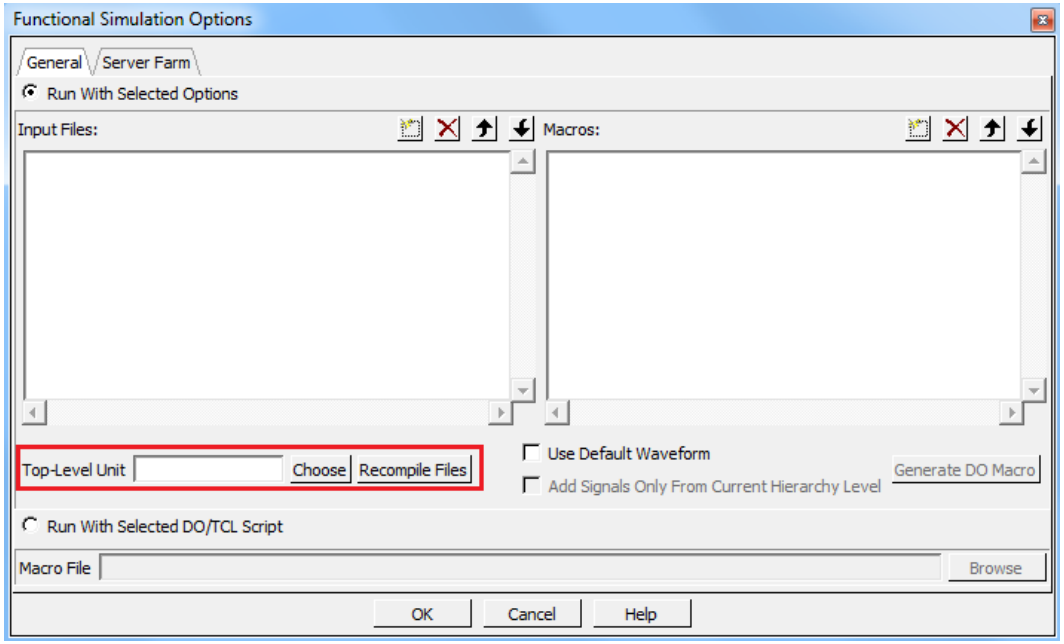
- Using **Run With Selected Options**, allows the user to specify which source files to simulate.

- You can choose to add:
- Input Files
  - Files that need to be compiled before simulation is performed
- Macros
  - Macros and scripts that will be executed after the initialization of simulation.



Functional Simulation (cont.)

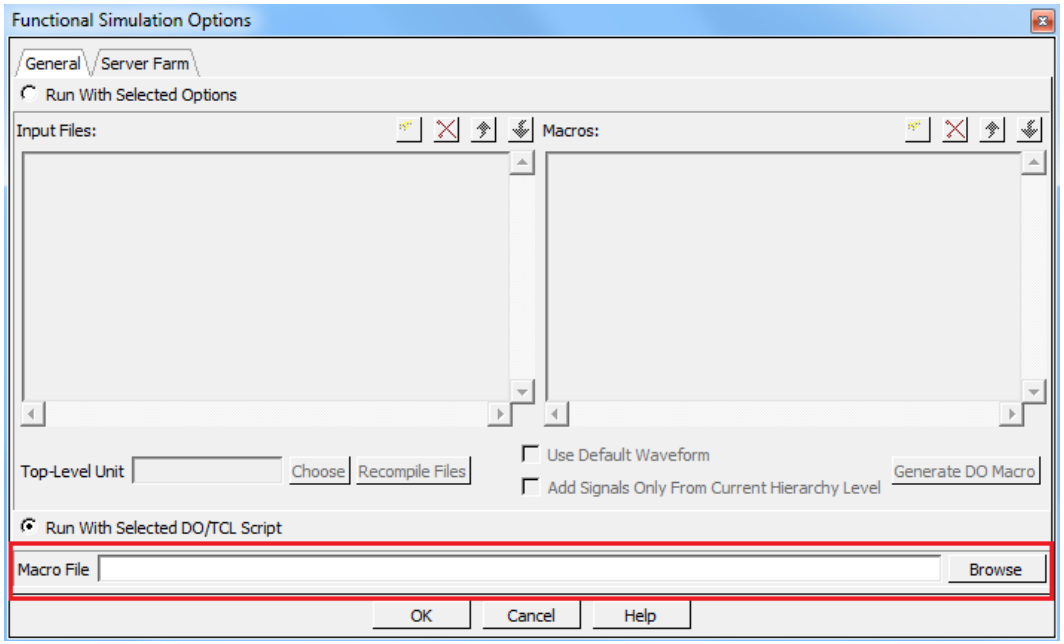
- You can choose your top-level unit two ways:
- Type the name of the unit
- Press the **Choose** button to select a unit in the **top-level unit(s)** window.
- Press **Recompile Files** to recompile all specified input files before running the simulation.



Functional Simulation (cont.)

- Using **Run With Selected DO/TCL Script** ignores ALL of the specified settings and will run simulation based on the defined macro or script.

- Press **Browse** to select the macro (*.do) or script (*.tcl) file that will be executed when you press the **Functional Simulation** button.



Functional Simulation (cont.)

- After the options are defined, press the **Functional Simulation** button to run the simulation. The status of each phase will be marked next to each button.

Overall status of the running process

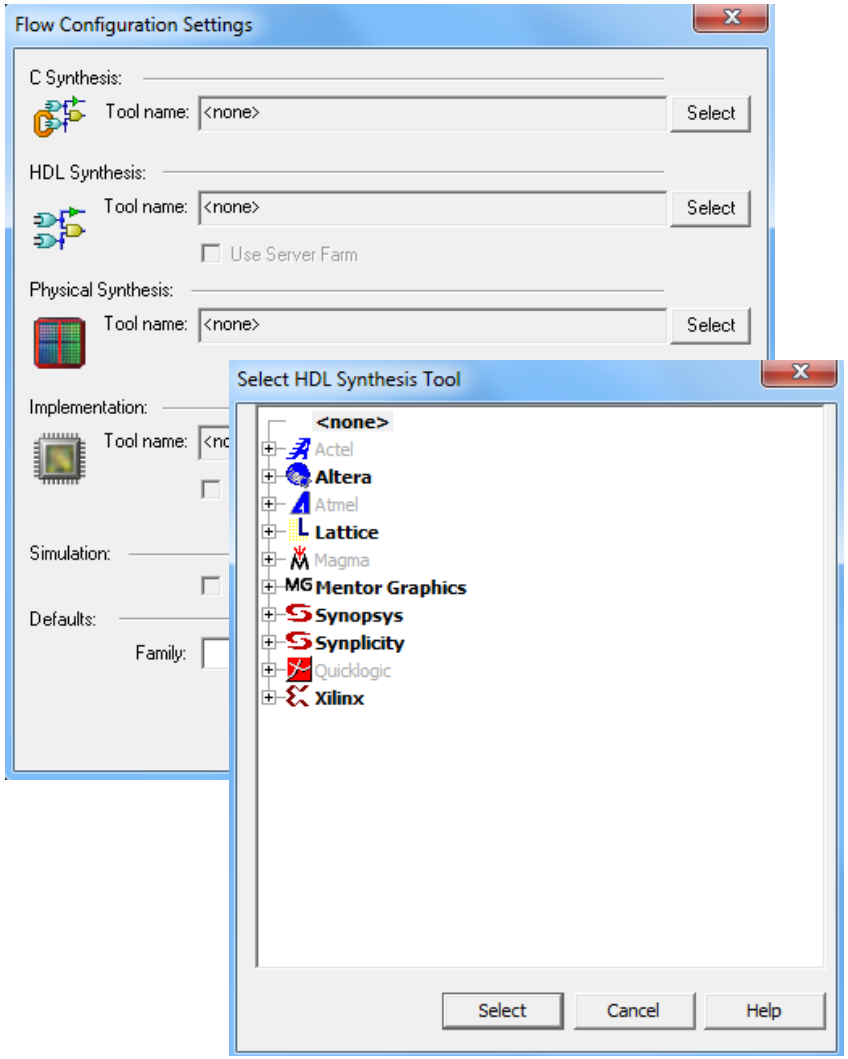
Icon	Description
	OK Status The process has completed successfully.
	Error Status The process has completed with errors.
	Warning The process has completed with warnings.
	Unknown Status The process has not been performed yet or some files/settings have changed since the last execution.

Icon	Description
	Waiting Status The task is being prepared or sent to the Server Farm.
	Run Status The task is currently executed.
	Finished Status The task execution has been completed successfully.
	Killed Status The task execution has been terminated or failed.
	Paused Status The task execution has been paused.
	Unknown Status The task has not been executed yet or some files/settings have changed since the last execution.

Status of the tasks scheduled to execute

Synthesis

- The **Synthesis** phase has three different tools:
  - C-Synthesis
  - HDL Synthesis
  - Physical Synthesis
- Each Synthesis tool is specified in the **Flow Configuration Settings.**
- When you hit the **Select** button for each synthesis tool, the available external third-party tools are denoted in bold.



Synthesis (cont.)

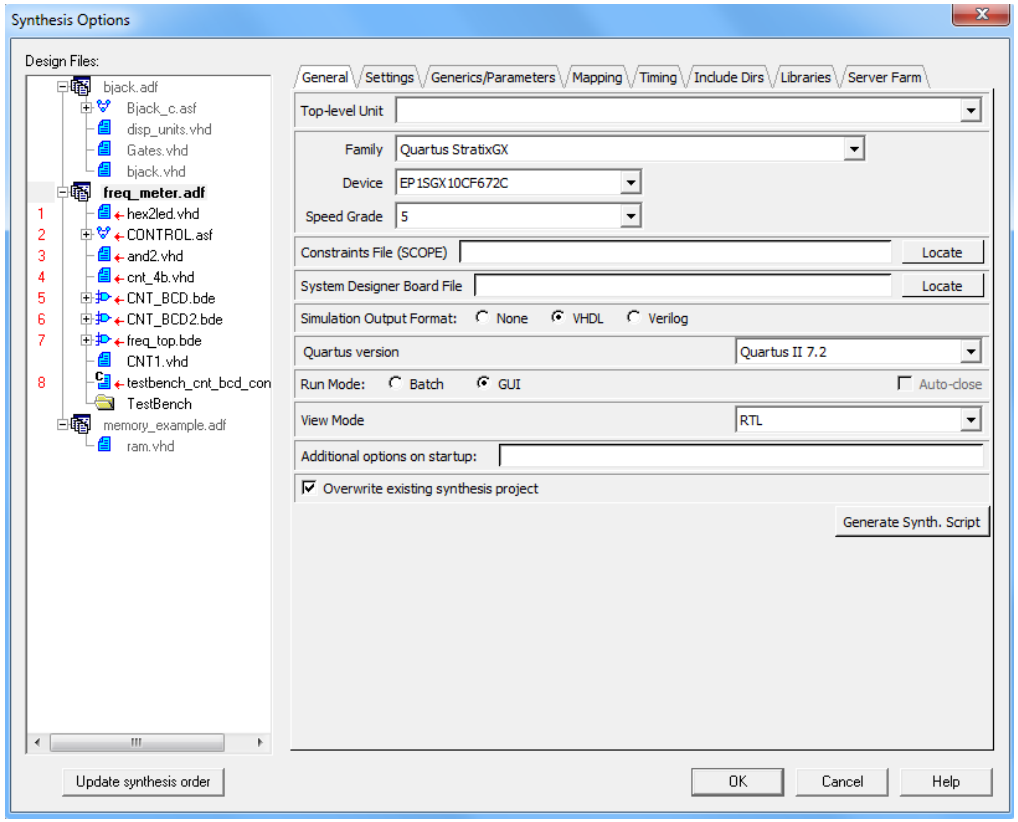
- Select the *options* button to define the settings for the specified synthesis tools.

- Every design that is within your workspace will be displayed in the **Design Files** pane. However, the synthesis options can only be set for the active design (denoted in bold).
- Resources from the inactive designs can be used as a synthesis library for the active design.

- **Note:** The *reports* button opens a window with links to the synthesis log files.

Synthesis (cont.)

- When you click on the active design, a number of tabs will be available to define your synthesis settings.

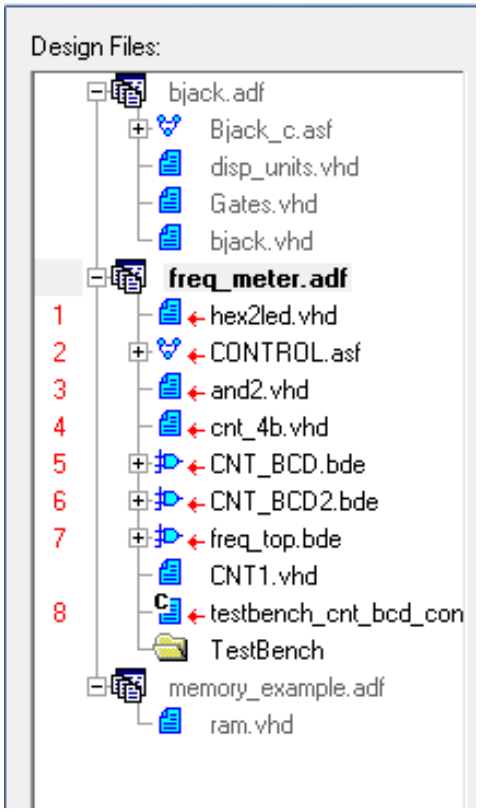


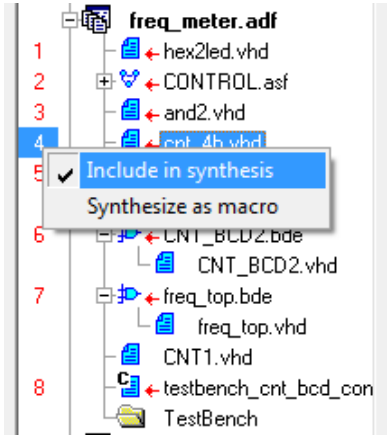
- **Note:** Except for the **General, Settings,** and **Libraries** tabs, the option tabs will vary from design to design depending on which synthesis tools you specify.

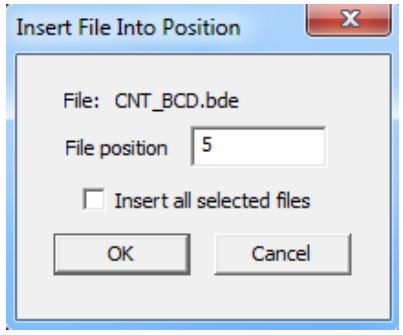
Synthesis (cont.)

- The red numbers listed next to your active design denote the order in which the design files will be processed during synthesis.

- If you need to change the order:
  - Right-click the design file
  - Uncheck **Include in synthesis**
  - Re-check **Include in synthesis**
  - The **Insert File Into Position** window will open and you can specify which file position you would like your design file to be in.

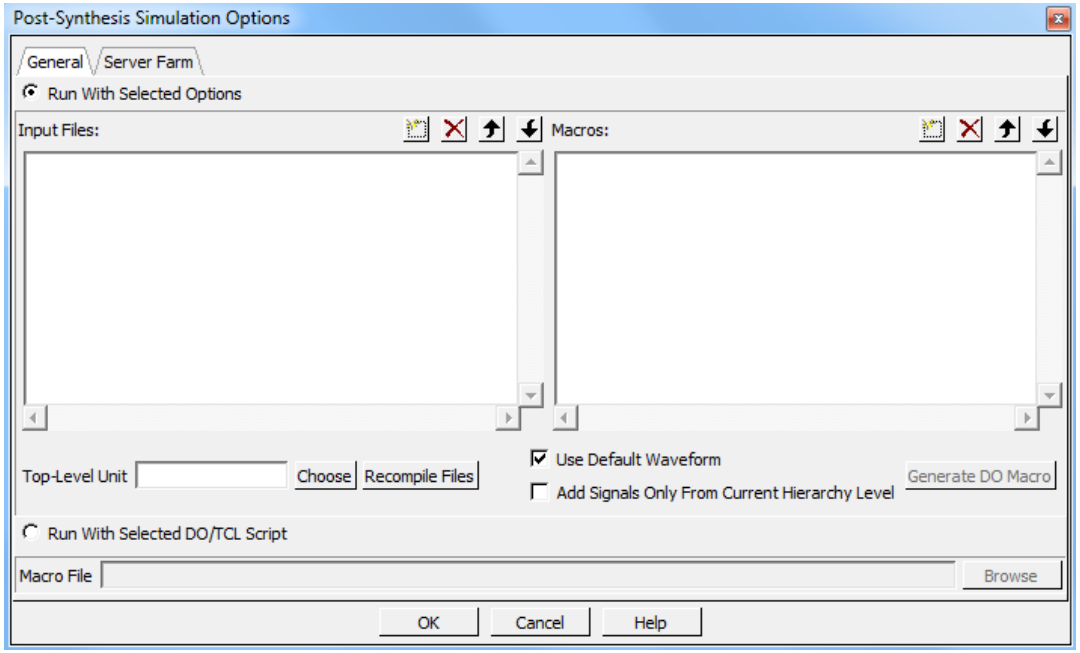






Post-Synthesis Simulation

- The *options* for **Post-Synthesis Simulation** is the same as **Functional Simulation**:
- Run with Selected Options
- Run With Selected DO/TCL Script

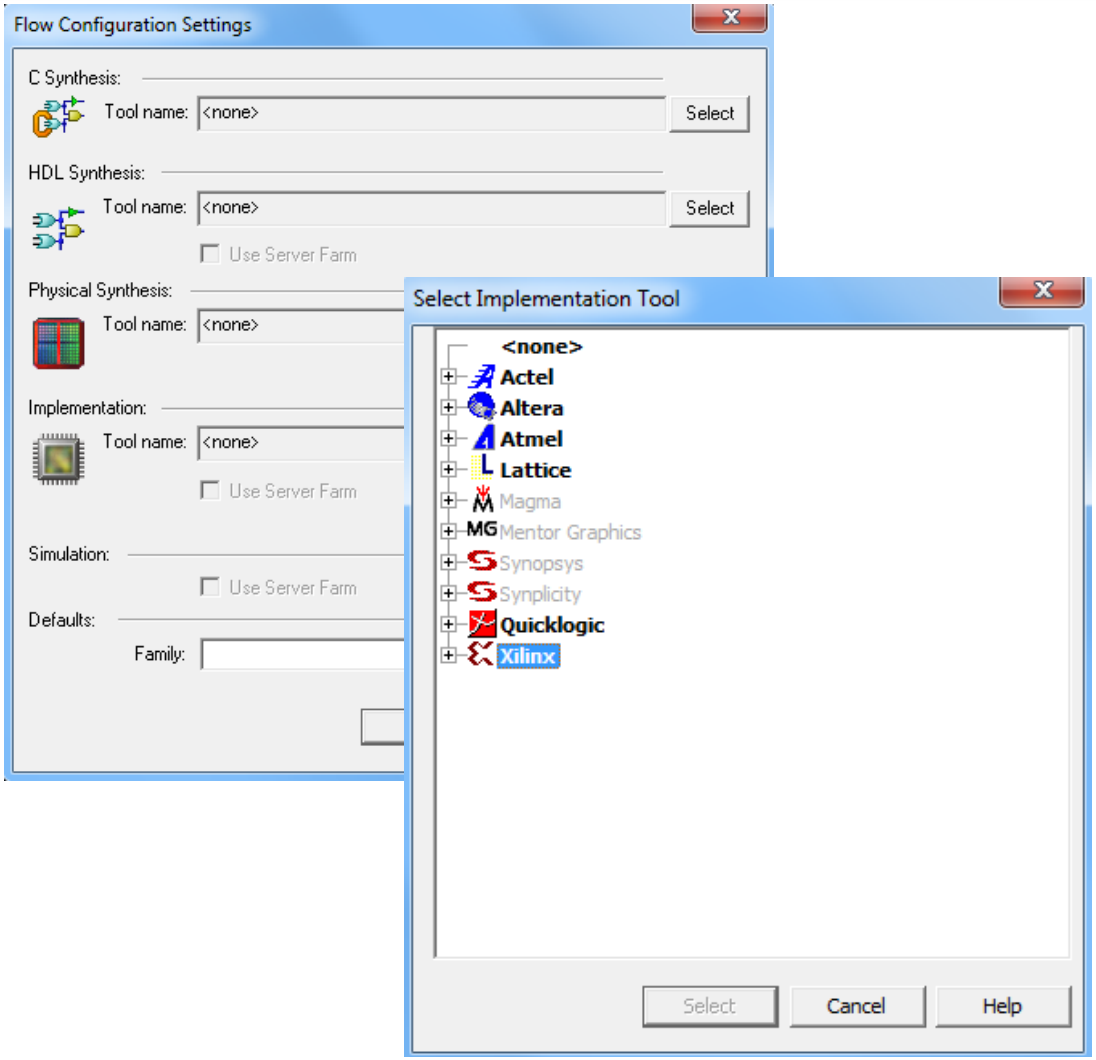


Post-Synthesis Simulation (cont.)

- When you press the **Post-Synthesis Simulation** button, it initiates the following sequence of operations:
- Depending on the synthesis options, the synthesis tool generates either a VHDL or Verilog source files. These file are compiled into the **Post-Synthesis** library.
- The top-level design unit is automatically selected for simulation based on the specified top-level unit in the **Post-Synthesis Options**. If you want to simulate more than one top-level, all specified units will be added to the **Multiple-Unit** pseudo-unit.
- The simulation is initialized for the selected top-level unit(s).
- The waveform viewer window is opened

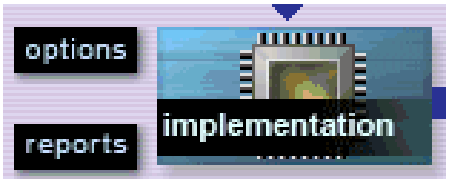
Implementation

- Similar to **Synthesis, Implementation** tools are specified in the **Flow Configuration Settings.**
- When you hit the **Select** button for each synthesis tool, the available external third-party tools are denoted in bold.



Implementation

- The *options* for the **Implementation** tool are vendor-specific. The implementation options can be specified for the following tools:
- Actel Designer™
- Altera® Max+PlusII®
- Altera® Quartus® II
- Atmel Figaro IDS
- Lattice ispLEVER®
- QuickLogic QuickWorks®
- Xilinx® Foundation & Alliance
- Xilinx® ISE/WebPack

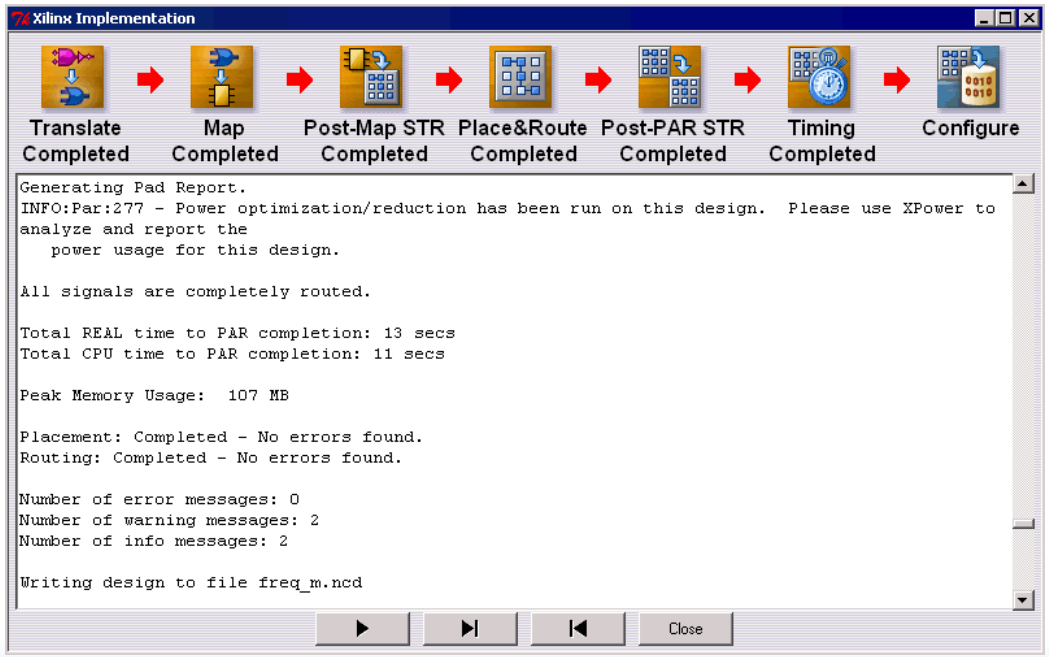


Note: The *reports* button opens a window with links to the implementation log files.

Implementation (cont.)

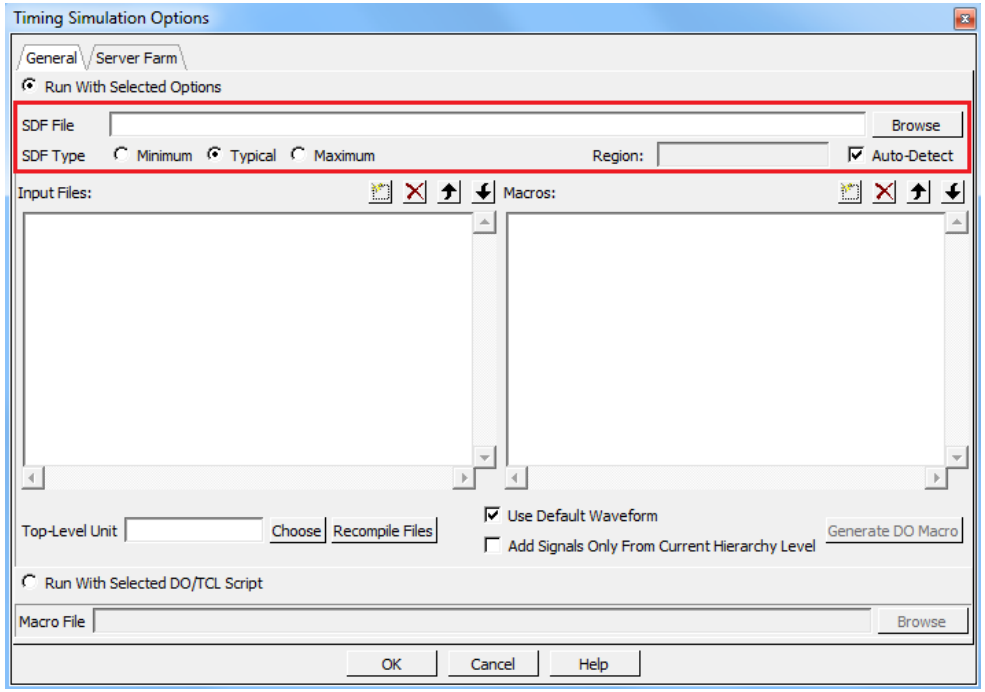
- When you press the **Implementation** button, it runs as an independent Windows task. The engine window shows icons representing subsequent processes taking place during implementation. The number and type of process depends on the target device (CPLD or FPGA) along with implementation options.

- For Example:



Timing Simulation

- The option settings for **Timing Simulation** is the same as **Post-Synthesis Simulation** and **Functional Simulation**:
- Run with Selected Options
- Run With Selected DO/TCL Script
- However, the **Timing Simulation** differs from the other simulation tools by containing SDF file settings.



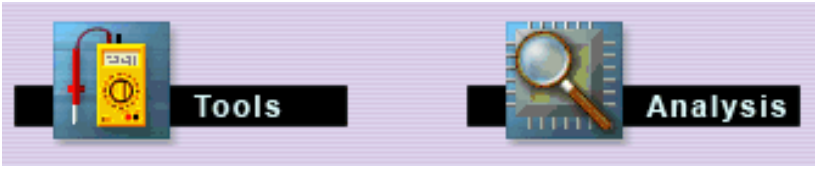
Timing Simulation (cont.)

- When you press the **Timing Simulation** button, it initiates similar operations to **Post-Synthesis** except for:

- The generated implementation output file is either VHDL, Verilog, or an EDIF netlist. This file is compiled into the timing library.
- If the simulation output format is VHDL or Verilog, an SDF file may be read and loaded into memory.

Tools & Analysis

- The **Tools** and **Analysis** buttons are additional flow tools from the following vendors:
- Actel
- Altera
- Lattice
- QuickLogic
- Xilinx

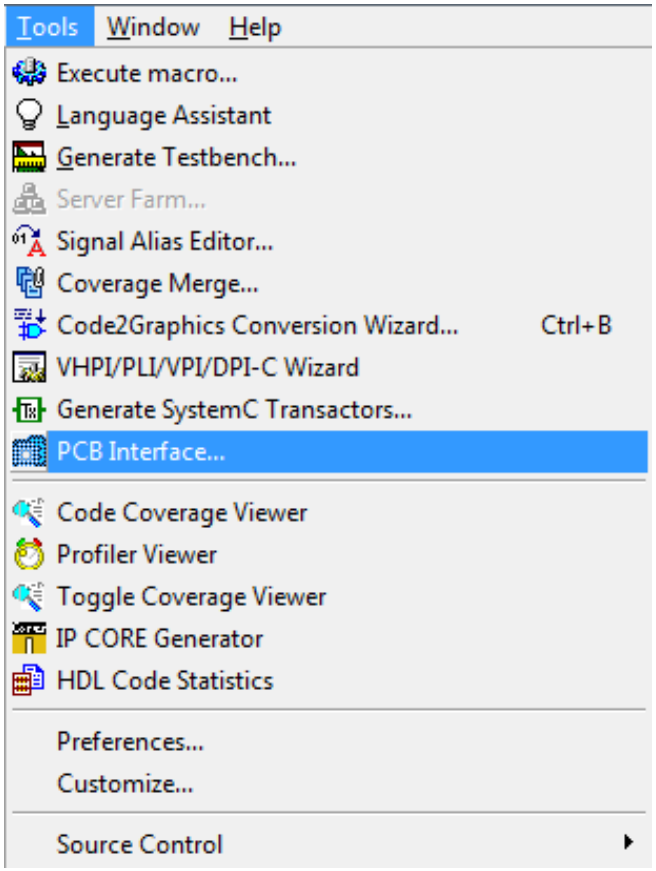


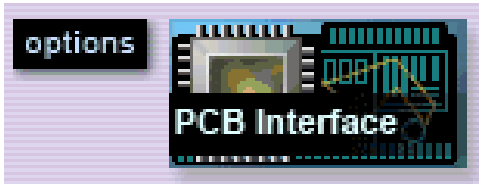
- These flow tools invoke auxiliary applications available in:
- Designer
- Quartus II
- ispLEVER
- QuickWorks
- Foundation, Alliance, WebPack, ISE packages

PCB Tools

- The options for the **PCB Interface** tool all exchanging constraints (pin assignments) produced by third-party synthesis or implementation tools, and third-party PCB tools.

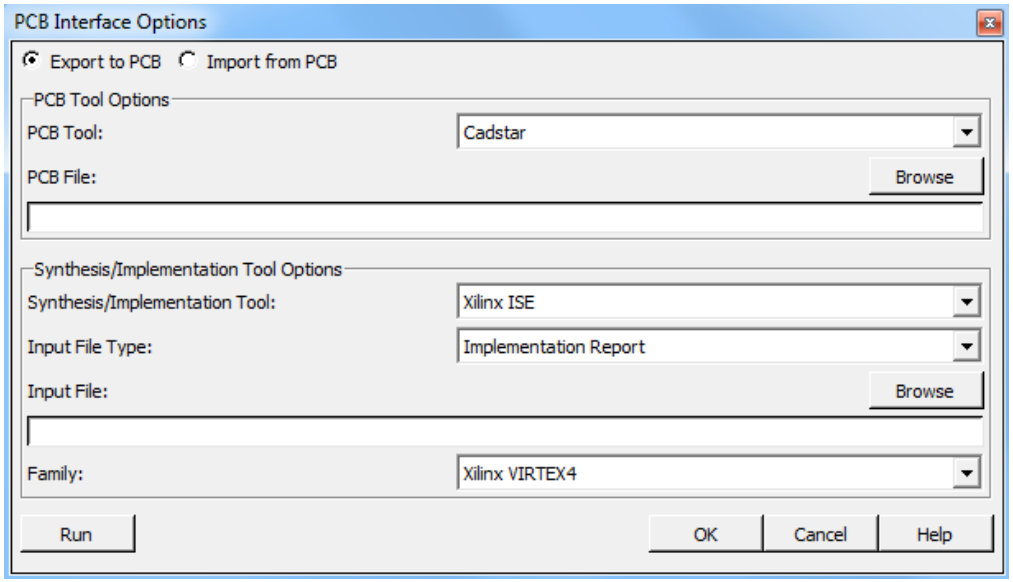
- There are two ways to open the **PCB Interface** options:
- Select the options button in the **Design Flow Manager**
- If you did not use the **Design Flow Manager**, go to the Tools menu and select **PCB Interface…**





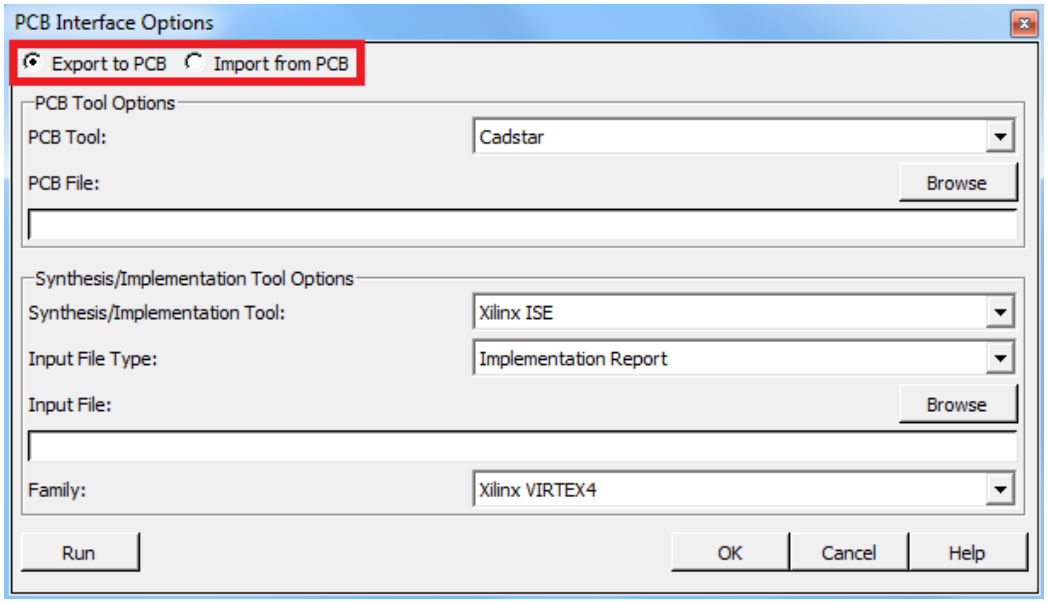
PCB Tools (cont.)

- The **PCB Interface** options allow you to specify:
- Export to PCB
- Import from PCB
- PCB Tool options
- Synthesis/Implementation Tool Options



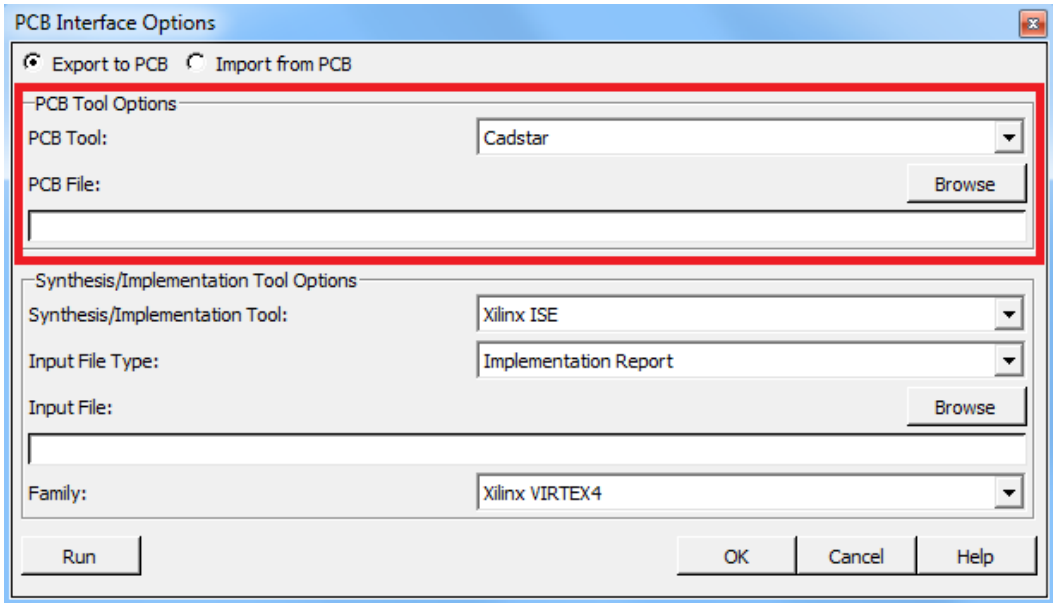
PCB Tools (cont.)

- Export to PCB
  - Exports the constraints stored in the **Input File** to the specified **PCB File**
- Import from PCB
  - Imports the constraints stored in the specified **PCB File** to the specified **Input File**.



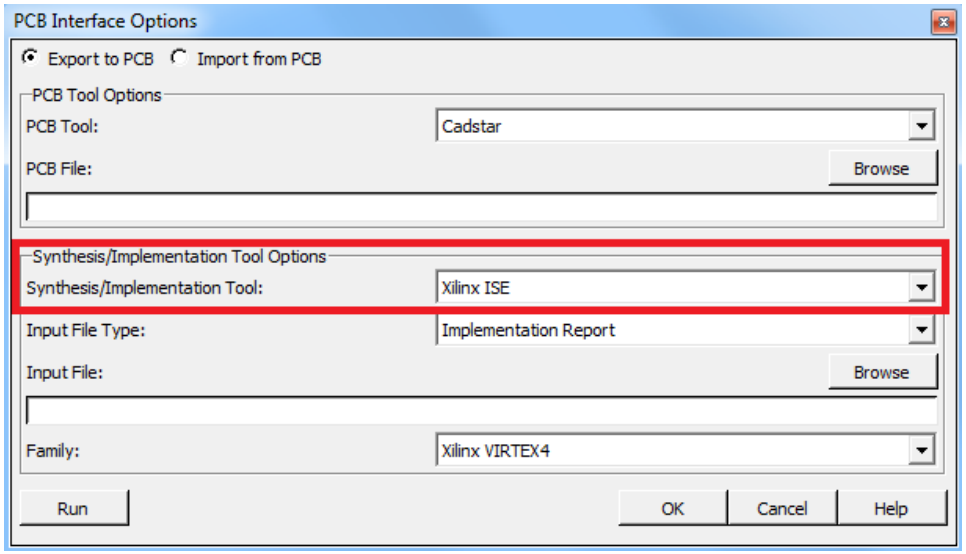
PCB Tools (cont.)

- PCB Tool
  - This version of the interface only support the CADSTAR PCB editor
- PCB File
  - **Export:** File is updated by Active-HDL after pin assignment data is extracted from the **Input File**
  - **Import:** The interface reads the constraints stored in this file, converts them, and saves to the **Output File**



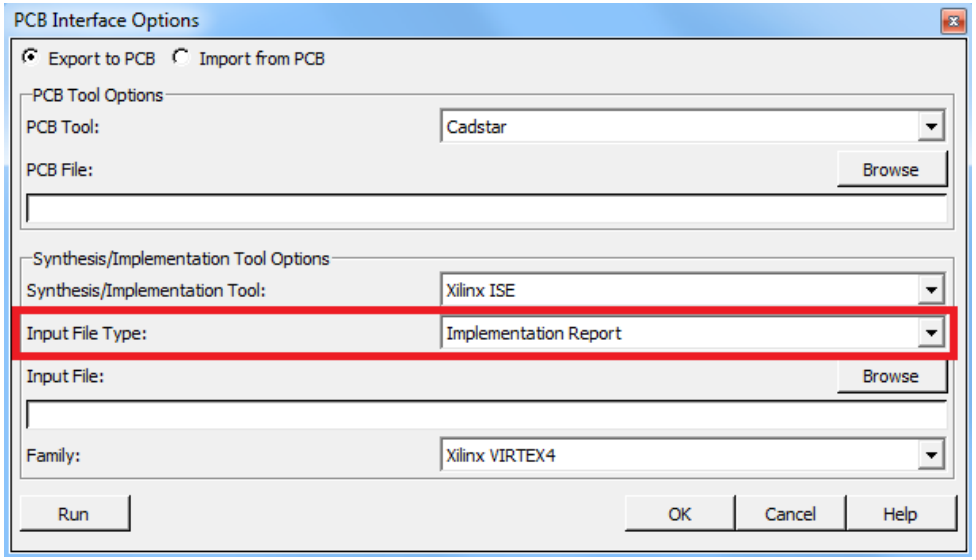
PCB Tools (cont.)

- Synthesis/Implementation Tool
  - The tool for which synthesis or implementation constraints will be exported or imported.
  - **Synthesis:**
    - Mentor Graphics Precision RTL
    - Synplicity Synplify
    - Xilinx ISE
  - **Implementation:**
    - Actel Designer
    - Altera Quuartus II
    - Lattice ispLEVER
    - Xilinx ISE



PCB Tools (cont.)

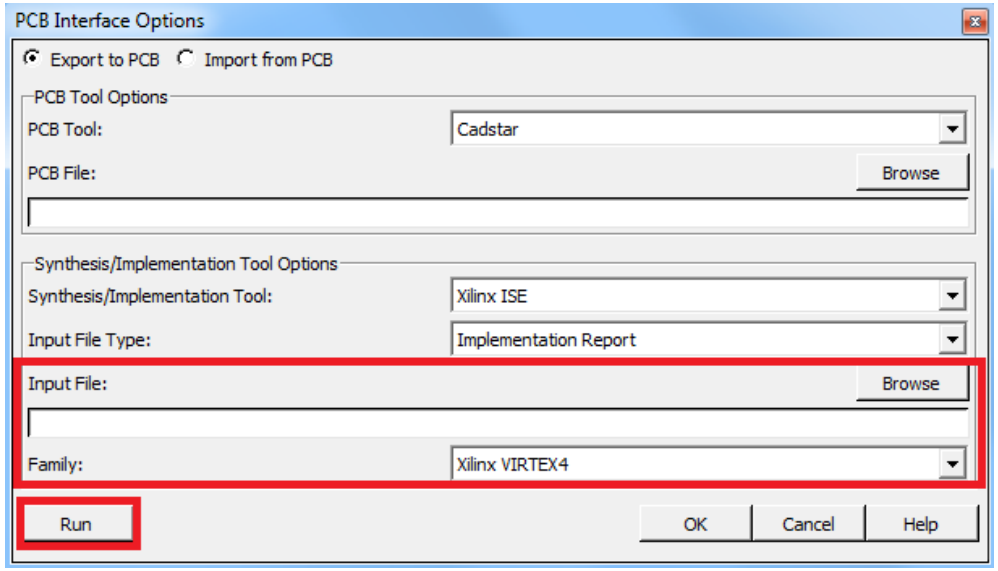
- Input/Output File Type
  - Input => Export Process
    - Synthesis Constraints
    - Implementation Constraints
    - Implementation Report
  - Output => Import Process
    - Synthesis Constraints
    - Implementation Constraints



- **Note**: The type of constraint depends on the tool selected from the **Synthesis/Implementation Tool** field.

PCB Tools (cont.)

- Input/Output File
  - Specifies the path and name of the file storing constraints for a PCB or synthesis/implementation tool.
- Family
  - Select the device family used in your project
- Run
  - Runs the import or export process if you did not use the **Design Flow Manager**. Otherwise, press the **PCB Interface** button.



PCB Tools (cont.)

- Pressing the **PCB Interface** button starts the export/import of the constraints.
- After the conversion is started, the entire process is divided into two phases:
  - Reading and processing input data by the interface
  - Writing output data for either a PCB tool or synthesis/implementation tool
- The process of constraints conversion can be monitored in the **Console** window. When the conversion is complete, you will see the following message:
  - # Import from <input_data> file finished successfully.
  - # Export to <output_data> file finished successfully.