Course 6

Verilog Performance Optimizations

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Verilog Performance Optimization in Batch mode

This section explains what compilation and simulation options (switches) must be used to achieve the ultimate Verilog simulation performance. Note that the Verilog simulation switches (to the vsim command) could be mixed with VHDL switches in case of the mixed language simulation.

Compilation Options

Perform the following steps in order to optimize design compilation:

- To shorten the compilation time specify multiple source files in a single vlog command:

  Instead of:

  ```
  > vlog gates.v
  > vlog disp_units.v
  > vlog bin2bcd.v
  > vlog bcd2led.v
  ```

  Use:

  ```
  > vlog gates.v disp_units.v bin2bcd.v bcd2led.v
  ```

  If the number of files is large, you can store the file list in a text file and specify the file as an argument for the compiler. Assuming that all files are stored in file **files.txt**, use the following command:

  ```
  > vlog –f files.txt
  ```

  Arguments stored in a file can be combined with a regular command-line, for example:

  ```
  > vlog –work mylib –f files.txt
  ```

- Make sure the debug mode is ***not*** enabled (**`-dbg`** switch is ***not*** used in vlog command), for example:

  Optimized:

  ```
  > vlog top.v
  ```

  Not Optimized:

  ```
  > vlog –dbg top.v
  ```

- Limit the compiler output to errors and warnings only (use `–quiet` option). For example:

  ```
  > vlog –quiet –f files.txt
  ```

Simulation Options

In the batch mode, simulation is initialized with the **`vsim`** command. When the GUI is used, Active-HDL reads the simulation settings and prints them in console window. When simulating in the batch mode you need to take care of providing the appropriate arguments. To speed-up the simulation, use the options described in the table below.

Simulation Options	Tip	Comments
`-t <resolution>`	Make sure not to use simulation resolution higher than necessary. An unnecessarily fine-grained resolution will slow down the simulator.	The default value is 1ps (Auto). If the design includes Verilog modules compiled with the `timescale directives, the smallest time unit implied by the `timescale

		directives is chosen.

`+nosdfwarn`
or
`-sdfnowarn`
	Disable warnings from the SDF file reader.	

`+no_pulse_msg`	Disable messages on pulse errors.	This option is related to messages about errors on path pulses (PATHPULSE$).
`+no_tchk_msg`	Disables generation of warning messages about violation of timing constraints.	Applies to Verilog timing check tasks.

In the batch mode you should not invoke the simulator with debugging options that may be useful in GUI but are usually irrelevant to the batch simulation. This is important, especially when you start regression tests after using Active-HDL GUI for debugging. You should make sure that **no** unnecessary options (see the table below) are left in the command line.

Simulation Options	Tip	Comments
`+access`	Do not let debugging tools and PLI applications access all design structure unless you are planning to log design signals.	Enable access to design objects or modules.
`-advdataflow`	Do not enable data for Advanced Dataflow.	Turns on data generation for the **Advanced Dataflow** window. Using this option increases memory allocation.
`-ses`	Do not enable Show Event Source feature.	This option is never useful in command line simulations; in GUI it allows to jump to assignments that cause events shown in the Waveform Viewer.

Verilog Performance Optimization in GUI

This section explains what compilation and simulation options must be used to achieve the ultimate Verilog simulation performance. Note that the Verilog simulation options (to the vsim command) could be mixed with VHDL switches in case of the mixed language simulation.

Compilation Options

Follow the guidance below to achieve the shortest compilation time and generate the most optimized code for the simulation.

- Compile multiple source files using **`Compile`** option instead of compiling them individually. For instance, select all the files you want to compile together then right click select compile.

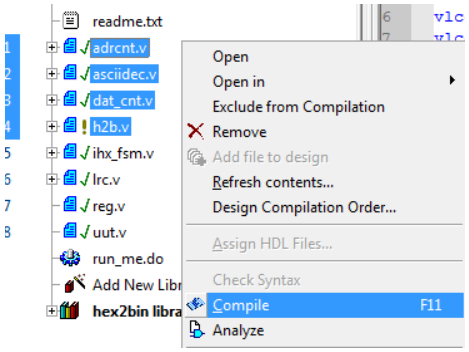

Figure 1 Compile files together

- Uncheck the Generate debug information option located in the preferences area of Active-HDL. It is located under **`Design`** | **`Settings`** | **`Compilation`** | **`Verilog`** category

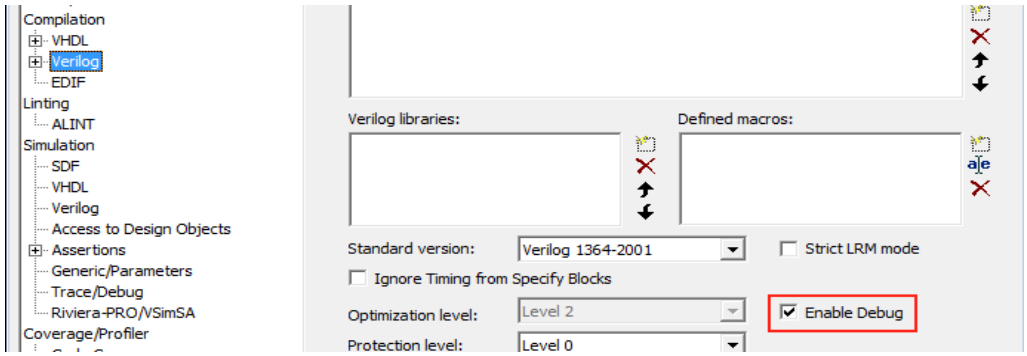

Figure 2 Debugging option

- Limit the compiler output to the errors and warnings only by selecting Severity level Errors + Warnings under **`Design`** | **`Settings`** | **`Compilation`** | **`Verilog`** category.

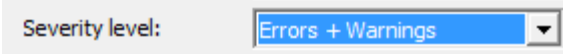

Figure 3 Option for printing warning and errors only

Simulation Options

When the GUI is used, Active-HDL reads the simulation settings from the **Design Settings** window and prints them in console window. Setting the proper options in the **Design Settings** window allows Active-HDL to optimize the performance. Make sure that below options are set properly,

Simulation Options	Action	Settings Location
Resolution	Make sure not to use simulation resolution higher than necessary. An unnecessarily fine-grained resolution will slow down the simulator.	Design | Settings | Simulation Default is set to AUTO
SDF warnings	Disable warnings from the SDF reader.	Design | Settings | Simulation | SDF
Pulse errors and warnings	Disable messages on pulse errors and Warnings. This option is related to messages about errors on path pulses (PATHPULSE$).	Design | Settings | Simulation | Verilog
Timing check messages	Disable generation of warning messages about violation of timing constraints.	Design | Settings | Simulation
Accessing design structure	Do not let debugging tools and PLI applications access all design structure unless you are planning to log design signals.	Design | Settings | Simulation | Access to Design Objects
Advanced Dataflow	Do not enable data for Advanced Dataflow.	Design | Settings | Simulation
Show event source	Do not enable Show Event Source.	Design | Settings | Simulation | Trace/Debug