Course 5

VHDL Performance Optimizations

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VHDL Performance Optimization in Batch mode

This section explains what compilation and simulation options (switches) must be used to achieve the ultimate VHDL simulation performance. Note that the VHDL simulation switches (to the vsim command) could be mixed with Verilog switches in case of the mixed language simulation.

Compilation Options

Follow the guidance below to achieve the shortest compilation time and generate the most optimized code for the simulation.

- Compile multiple source files using single line compilation command. For instance,

  instead of:

  ```
  > vcom gates.vhd
  > vcom disp_units.vhd
  > vcom bin2bcd.vhd
  > vcom bcd2led.vhd
  ```

  use:

  ```
  > vcom gates.vhd disp_units.vhd bin2bcd.vhd bcd2led.vhd
  ```

  If the number of files is large, you can store the file list along with the arguments in a text file and specify such file as an argument for the compiler. Assuming that all files are stored in file **files.txt**, use the following command:

  ```
  > vcom –f files.txt
  ```

  Arguments stored in a file can be combined with a regular command-line, for example:

  ```
  > vcom –work my_lib –f files.txt
  ```

- Make sure the debug mode is ***not*** enabled. The `–dbg` switch disables optimizations.

  Optimized

  ```
  > vcom top.vhd
  ```

  Not Optimized

  ```
  > vcom –dbg top.vhd
  ```

- Limit the compiler output to the errors and warnings only (use `–quiet` option). For example:

  ```
  > vcom –quiet –f files.txt
  ```

Simulation Options

In the batch mode, simulation is initialized with the **`vsim`** command. When the GUI is used, Active-HDL reads the simulation settings and prints them in the console window. When simulating in the batch mode you need to take care of providing the appropriate arguments. To speed-up the simulation use the options described in the table below.

Simulation Options	Tip	Comments
`-t <resolution>`	Make sure not to use simulation resolution higher than necessary. An unnecessarily fine-grained resolution will slow down the	The default resolution for VHDL designs is 1 ps

	simulator.	
+nosdfwarn **or** -sdfnowarn	Disables warnings from the SDF file reader.	
-ieee_nowarn	Disables warnings generation from the IEEE libraries.	Disables IEEE warnings such as: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
+no_tchk_msg	Disables generation of warning messages about violation of timing constraints.	Applies to timing check functions from the VITAL package.
+no_glitch_msg **or** -noglitch	Disables generation of VITAL glitch messages.	This option is related to the glitch errors detected by routines from the VITAL package.

In the batch mode you should not invoke the simulator with the debugging options that may be very useful in GUI but are irrelevant in the batch simulations. This is important, especially when you start regression tests after using the Active-HDL GUI for debugging. You should make sure that **no** unnecessary options are left in the command line (see the table below).

Simulation Options	Tip	Comments
+access	Do not let debugging tools and PLI applications access all design structure unless you are planning to log design signals.	Enables access to design objects or modules.
-advdataflow	Do not enable data for Advanced Dataflow.	Turns on data generation for the **Advanced Dataflow** window. Using this option increases memory allocation.
-ses	Do not enable Show Event Source.	This option is never useful in command line simulations; in GUI it allows to jump to assignments that cause events shown in the Waveform Viewer.

VHDL Performance Optimization in GUI

This section explains what compilation and simulation options must be used to achieve the ultimate VHDL simulation performance.

Compilation Options

Follow the guidance below to achieve the shortest compilation time and generate the most optimized code for the simulation.

- Compile multiple source files by right clicking a folder or the design icon and select **`Compile All.`**

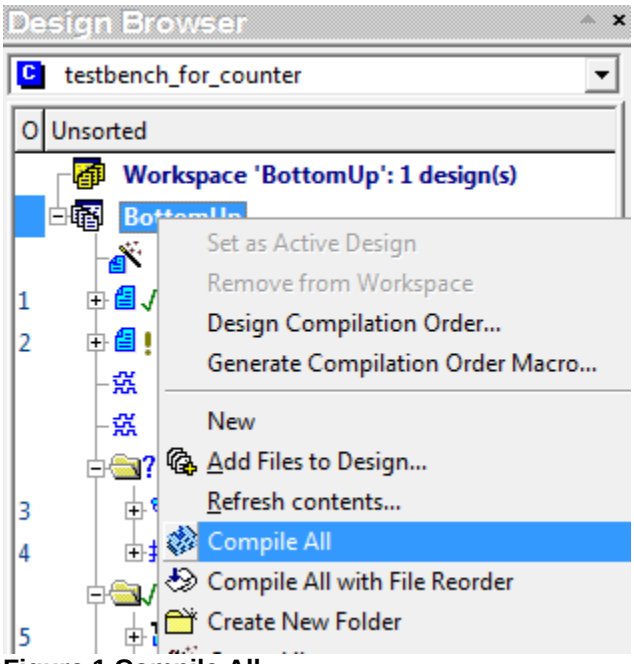

Figure 1 Compile All

- Uncheck the Generate debug information option located in the preferences area of Active-HDL. It is located under **`Design | Settings | Compilation | VHDL Compiler.`**

Figure 2 Debugging option

- Limit the compiler output to display only error and warning messages under **`Design | Settings | Compilation | VHDL | Advanced.`**

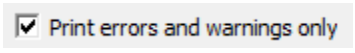

Figure 3 Option to print error and warning messages only

Simulation Options

When the GUI is used, Active-HDL reads the simulation settings from the **`Design | Settings`** window and prints them in the Console window. Setting the proper options in the preferences window enables Active-HDL to optimize the performance. Make sure that below options are set properly,

Simulation Options	Action	Settings Location
`Resolution`	Make sure not to use simulation resolution higher than necessary. An unnecessarily fine-grained resolution will slow down the simulator.	Design | Settings | Simulation Default is set to AUTO
`SDF warnings`	Disable warnings from the SDF file reader.	Design | Settings | Simulation | SDF
`IEEE warnings`	Disable warnings generation from the IEEE libraries.	Design | Settings | Simulation | VHDL
`Timing check messages`	Disable generation of warning messages about violation of timing constraints.	Design | Settings | Simulation
`VITAL glitch messages`	Disable generation of VITAL glitch messages.	Design | Settings | Simulation | VHDL
`Advanced Dataflow`	Do not enable data for Advanced Dataflow.	Design | Settings | Simulation
`Show event source`	Do not enable Show Event Source.	Design | Settings | Simulation | Assertions | Trace/Debug