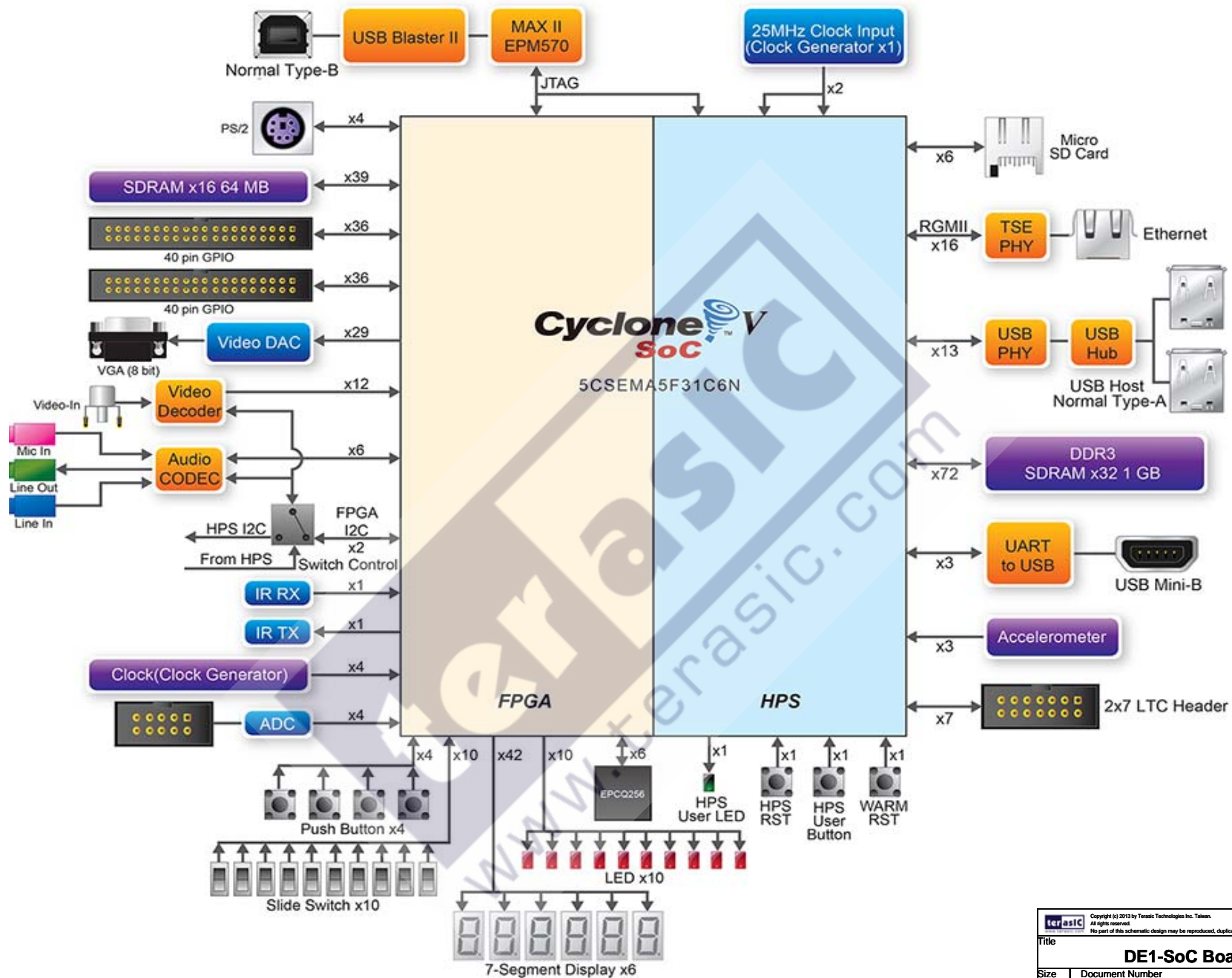


ALTERA Cyclone V SoC Development & Education Board (DE1-SoC)

PAGE	CONTENT	PAGE	CONTENT
1	Cover Page	16	ADV7123 VGA
2	Block Diagram	17	ADV7180 Video Decoder
3	FPGA BANK 3, BANK 4	18	Audio CODEC
4	FPGA BANK 5, BANK 6	19	7-Segment Display, LED
5	FPGA BANK 7, BANK 8	20	FPGA BUTTON, Switch
6	FPGA Clocks, GND	21	ADC, PS2, IR Tx, IR Rx
7	FPGA Configuration	22	2-port USB Host
8	FPGA Decoupling	23	1 Gigabit Ethernet
9	FPGA Power	24	UART to USB, SD CARD
10	USB Blaster II	25	Accelerometer, LTC Connector
11	JTAG Chain	26	I2C Multiplexer, HPS BUTTON, HPS LED
12	GPIO 0	27	Power - 1.1V
13	GPIO 1	28	Power - 5V, 3.3V
14	SDRAM, HPS QSPI Flash	29	Power - 9V, 2.5V, 1.5V
15	HPS DDR3 SDRAM	30	Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT



SW[9..0] 7,20
USB_B2_DATA[7..0] 7,10

DRAM_ADDR[12..0] 6,14
DRAM_DQ[15..0] 14
KEY[3..0] 6,20

GPIO_0[35..0] 6,12
GPIO_1[35..0] 6,13

LEDR[9..0] 4,19

U20-9

Bank 3 VCCIO = 3.3V

Bank 3A

Bank 3B

AG10 DRAM DQ5
AH9 DRAM DQ11
AF11 14 DRAM CAS_N
AG11 14 DRAM CS_N
AA13 14 DRAM WE_N
AB13 14 DRAM LDQM
AK2 21 ADC SCLK
AK3 21 ADC DOUT
AJ4 21 ADC CS_N
AK4 21 ADC DIN
AE13 14 DRAM RAS_N
AF13 14 DRAM BA0
AD14 DRAM ADDR6
AE14 DRAM ADDR3
AJ5 DRAM DQ15
AK6 DRAM DQ0
AJ6 DRAM DQ14
AJ7 DRAM DQ1
AG12 DRAM ADDR10
AG13 DRAM ADDR9
AB15 DRAM ADDR4
AC14 DRAM ADDR5
AK7 DRAM DQ2
AK8 DRAM DQ3
AJ9 DRAM DQ10
AK9 DRAM DQ4
AH13 DRAM ADDR11
AH14 DRAM ADDR1
AH7 DRAM DQ13
AH8 DRAM DQ12
AH10 DRAM DQ8
AJ10 DRAM DQ9
AJ11 DRAM DQ7
AK11 DRAM DQ6
AA14 KEY0
AA15 KEY1
AK12 14 DRAM UDQM
AK13 14 DRAM CKE
AG15 DRAM ADDR2
AH15 DRAM ADDR8
AJ14 DRAM ADDR12
AK14 DRAM ADDR0

GPIO_012 AG16
GPIO_015 AG17
GPIO_018 AE17
GPIO_032 AF18
LEDR0 V16
LEDR1 W16
GPIO_013 AE16
GPIO_014 AF16
GPIO_09 AJ16
GPIO_04 AK16
GPIO_031 AG21
GPIO_022 AH20
GPIO_011 AH17
GPIO_010 AH18
GPIO_034 AG18
GPIO_020 AH19
GPIO_08 AJ17
GPIO_05 AK18
LEDR2 V17
LEDR4 W17
GPIO_07 AJ19
GPIO_06 AK19
GPIO_021 AJ20
GPIO_035 AJ21
GPIO_030 AF19
GPIO_033 AG20
GPIO_123 AG23
GPIO_111 AH24
GPIO_129 AG22
GPIO_126 AH22
GPIO_028 AE18
GPIO_027 AE19
GPIO_01 Y17
GPIO_016 AA18
GPIO_023 AK21
GPIO_126 AK22
GPIO_125 AH23
GPIO_127 AJ22

U20-10

Bank 4A VCCIO = 3.3V


IO_4A/DIFFIO_TX_B41P/DQ6B/B_DQ_2
IO_4A/RZQ_0/DIFFIO_TX_B41N
IO_4A/DIFFIO_RX_B42P/DQ6B/B_DQ_1
IO_4A/DIFFIO_RX_B42N/DQ6B/B_DQ_0
IO_4A/DIFFIO_RX_B43P/DQ6B/B_DQ_5
IO_4A/DIFFIO_RX_B43N/DQ6B/B_DQ_0
IO_4A/DIFFIO_TX_B44P/B_ODT_0
IO_4A/DIFFIO_TX_B44N/DQ6B/B_DQ_3
IO_4A/DIFFIO_TX_B45P/DQ6B/B_DQ_6
IO_4A/DIFFIO_TX_B45N/DQ6B/B_ODT_1
IO_4A/DIFFIO_RX_B46P/DQ6B/B_DQ_5
IO_4A/DIFFIO_RX_B46N/DQ6B/B_DQ_4
IO_4A/DIFFIO_TX_B48P/DQ6B/B_DM_0
IO_4A/DIFFIO_TX_B48N/DQ6B/B_DQ_7
IO_4A/DIFFIO_TX_B49P/DQ7B/B_DQ_10
IO_4A/DIFFIO_TX_B49N/GND
IO_4A/DIFFIO_RX_B50P/DQ7B/B_DQ_9
IO_4A/DIFFIO_RX_B50N/DQ7B/B_DQ_8
IO_4A/DIFFIO_RX_B51P/DQ7B/B_DQ_5
IO_4A/DIFFIO_RX_B51N/DQ5N7B/B_DQSN_1
IO_4A/DIFFIO_TX_B52P/B_CKE_1
IO_4A/DIFFIO_TX_B52N/DQ7B/B_DQ_11
IO_4A/DIFFIO_TX_B53P/DQ7B/B_DQ_14
IO_4A/DIFFIO_TX_B53N/DQ7B/B_CKE_0
IO_4A/DIFFIO_RX_B54P/DQ7B/B_DQ_13
IO_4A/DIFFIO_RX_B54N/DQ7B/B_DQ_12
IO_4A/DIFFIO_TX_B56P/DQ7B/B_DM_1
IO_4A/DIFFIO_TX_B56N/DQ7B/B_DQ_15
IO_4A/DIFFIO_TX_B57P/DQ8B/B_DQ_18
IO_4A/DIFFIO_TX_B57N/GND
IO_4A/DIFFIO_TX_B57N/GND
IO_4A/DIFFIO_RX_B58P/DQ8B/B_DQ_17
IO_4A/DIFFIO_RX_B58N/DQ8B/B_DQ_16
IO_4A/DIFFIO_RX_B59P/DQ8B/B_DQ_2
IO_4A/DIFFIO_RX_B59N/DQ8B/B_DQSN_2
IO_4A/DIFFIO_TX_B60P/B_RESETN
IO_4A/DIFFIO_TX_B60N/DQ8B/B_DQ_19
IO_4A/DIFFIO_TX_B61P/DQ8B/B_DQ_22
IO_4A/DIFFIO_TX_B61N/DQ8B/B_DQ_22

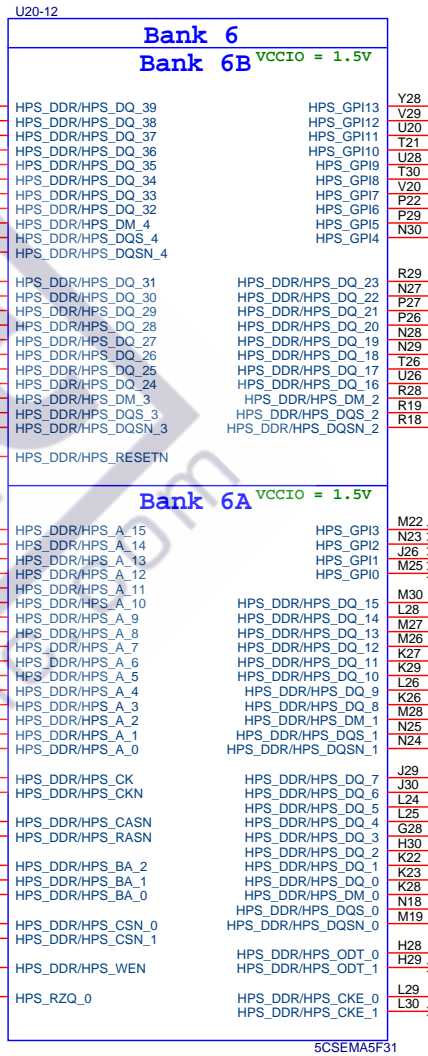
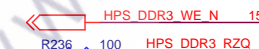
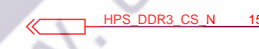
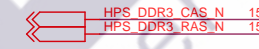
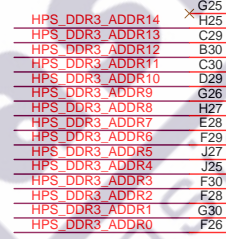
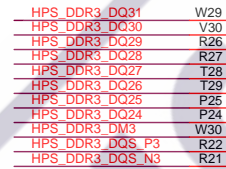
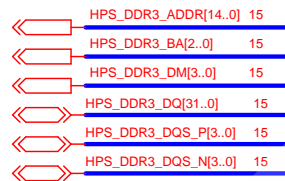
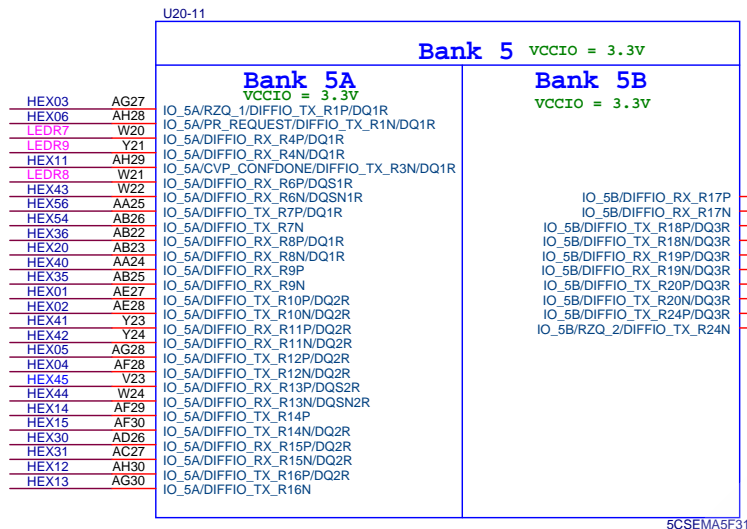
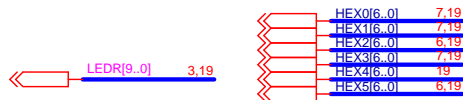
IO_4A/DIFFIO_RX_B62P/DQ8B/B_DQ_21
IO_4A/DIFFIO_RX_B62N/DQ8B/B_DQ_20
IO_4A/DIFFIO_RX_B63P/GND
IO_4A/DIFFIO_RX_B63N/GND
IO_4A/DIFFIO_TX_B64P/DQ8B/B_DM_2
IO_4A/DIFFIO_TX_B64N/DQ8B/B_DQ_23
IO_4A/DIFFIO_TX_B65P/DQ8B/B_DQ_26
IO_4A/DIFFIO_TX_B65N/GND
IO_4A/DIFFIO_RX_B66P/DQ8B/B_DQ_25
IO_4A/DIFFIO_RX_B66N/DQ8B/B_DQ_24
IO_4A/DIFFIO_RX_B67P/DQ8B/B_DQ_3
IO_4A/DIFFIO_RX_B67N/DQ8B/B_DQSN_3
IO_4A/DIFFIO_TX_B68P/GND
IO_4A/DIFFIO_TX_B68N/DQ8B/B_DQ_27
IO_4A/DIFFIO_TX_B69P/DQ8B/B_DQ_30
IO_4A/DIFFIO_TX_B69N/DQ8B/B_DQSN_4
IO_4A/DIFFIO_RX_B70P/DQ8B/B_DQ_29
IO_4A/DIFFIO_RX_B70N/DQ8B/B_DQ_28
IO_4A/DIFFIO_RX_B71P/GND
IO_4A/DIFFIO_RX_B71N/GND
IO_4A/DIFFIO_TX_B72P/DQ8B/B_DM_3
IO_4A/DIFFIO_TX_B72N/DQ8B/B_DQ_11
IO_4A/DIFFIO_TX_B73P/DQ10B/B_DQ_34
IO_4A/DIFFIO_TX_B73N/GND
IO_4A/DIFFIO_RX_B74P/DQ10B/B_DQ_33
IO_4A/DIFFIO_RX_B74N/DQ10B/B_DQ_32
IO_4A/DIFFIO_RX_B75P/DQ10B/B_DQ_5
IO_4A/DIFFIO_RX_B75N/DQSN10B/B_DQSN_4
IO_4A/DIFFIO_TX_B76P/GND
IO_4A/DIFFIO_TX_B76N/DQ10B/B_DQ_35
IO_4A/DIFFIO_TX_B77P/DQ10B/B_DQ_38
IO_4A/DIFFIO_TX_B77N/DQ10B/GND
IO_4A/DIFFIO_RX_B78P/DQ10B/B_DQ_37
IO_4A/DIFFIO_RX_B78N/DQ10B/B_DQ_36
IO_4A/DIFFIO_RX_B79P/GND
IO_4A/DIFFIO_RX_B79N/GND
IO_4A/DIFFIO_TX_B80P/DQ10B/B_DM_4
IO_4A/DIFFIO_TX_B80N/DQ10B/B_DQ_39

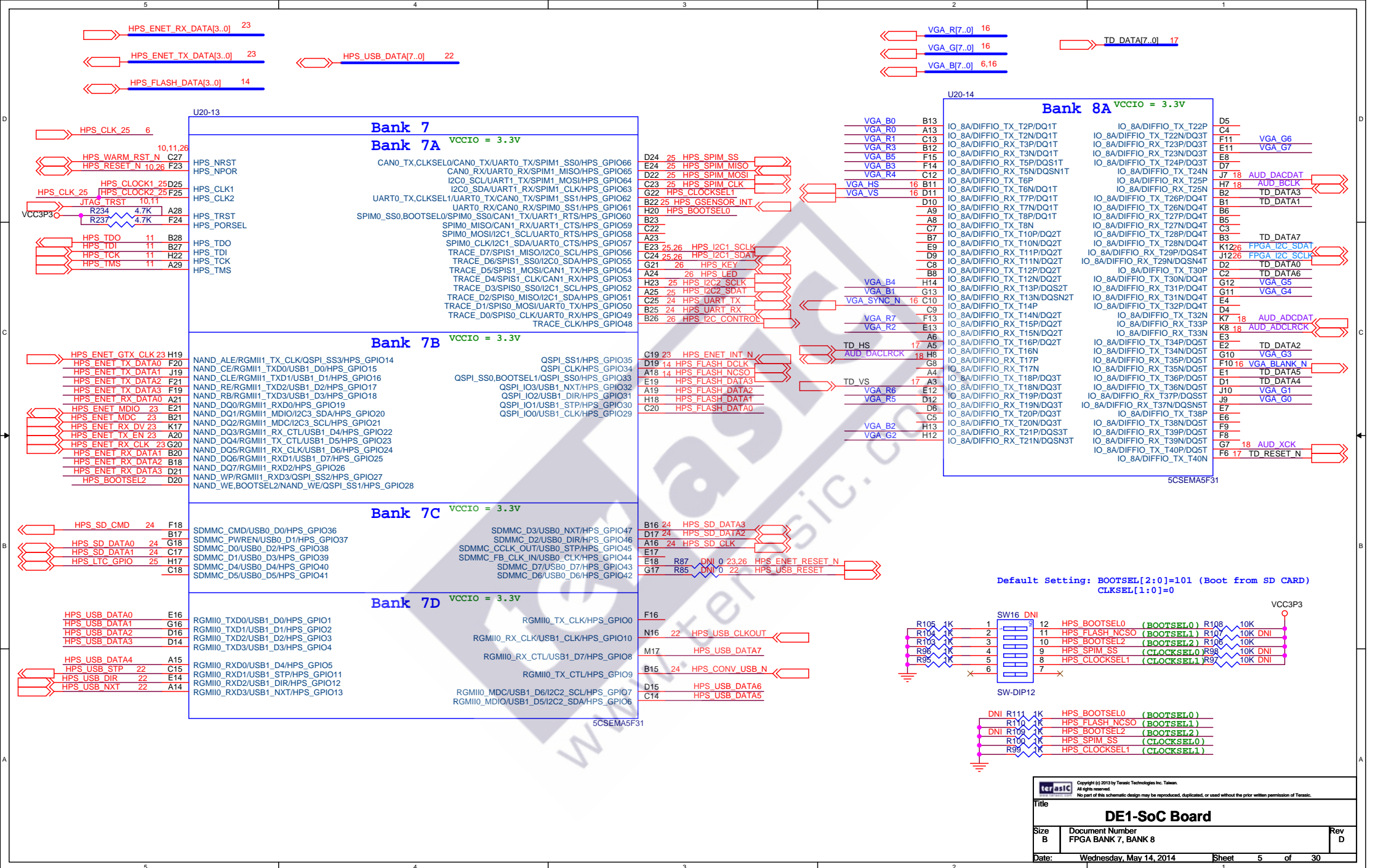
AF20 GPIO_028
AF21 GPIO_029
Y18 GPIO_03
AA19 GPIO_017
AK23 GPIO_124
AK24 GPIO_122
AJ24 GPIO_121
AF23 GPIO_131
AF24 GPIO_130
AC20 GPIO_019
AD19 GPIO_024
AJ26 GPIO_117
AK26 GPIO_118
AG25 GPIO_19
AH25 GPIO_119
AE22 GPIO_132
AE23 GPIO_15
V18 LEDR3
W19 LEDR5
AJ27 GPIO_113
AK27 GPIO_116
AK28 GPIO_115
AK29 GPIO_114
AD20 GPIO_025
AD21 GPIO_133
Y19 LEDR6
AA20 GPIO_134
AG26 GPIO_110
AH27 GPIO_112
AF25 GPIO_17
AF26 GPIO_18
AC22 GPIO_135
AC23 GPIO_13
AA21 GPIO_11
AB21 GPIO_12
AD24 GPIO_14
AE24 GPIO_16

5CSEMA5F31

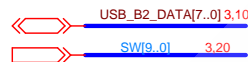
5CSEMA5F31

 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	FPGA BANK 3, BANK 4	D
Date:	Wednesday, May 14, 2014	Sheet 3 of 30

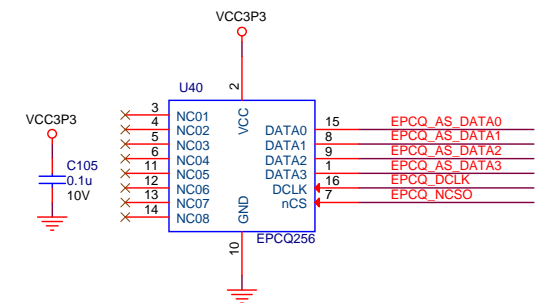
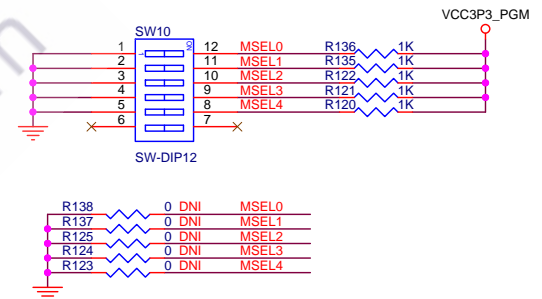
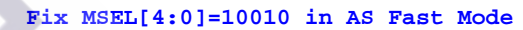


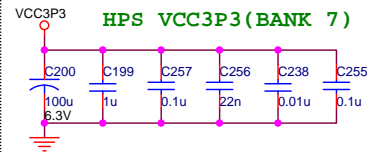
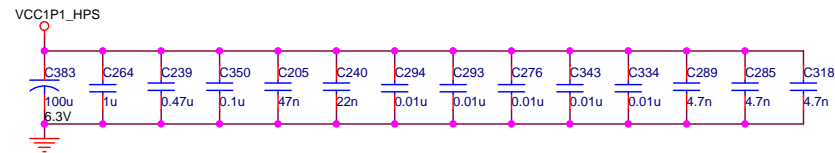
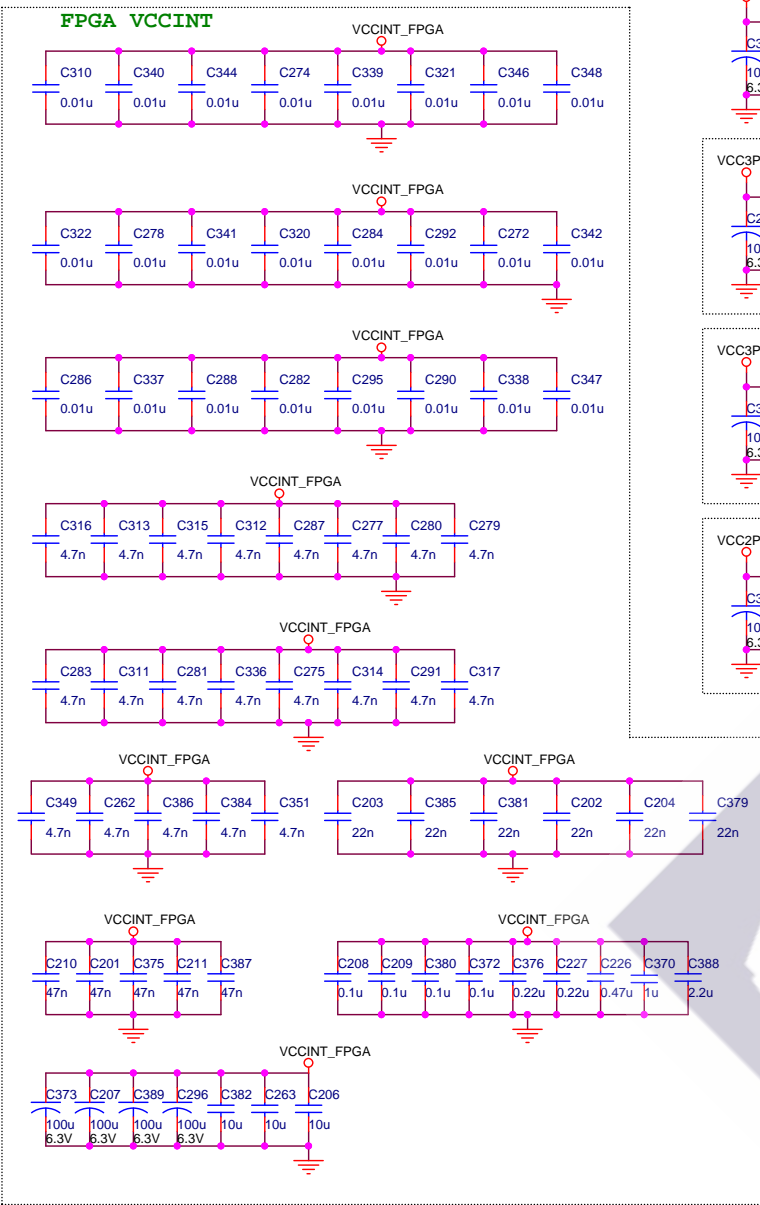


	FPGA_TDI	11
	JTAG_TMS	11
	JTAG_TCK	11
	FPGA_TDO	11



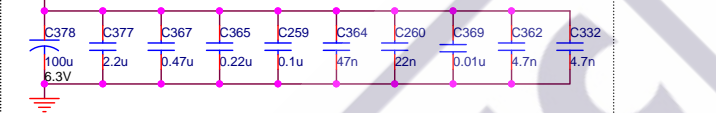
AD25	HEX32
AC25	HEX33
AE26	HEX00
AJ29	HEX10
AD27	HEX16



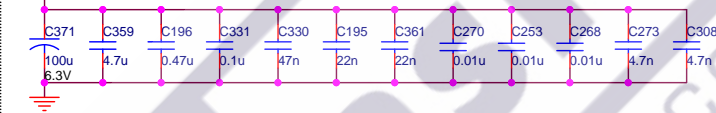


Place C394 close to J20/G23 pin

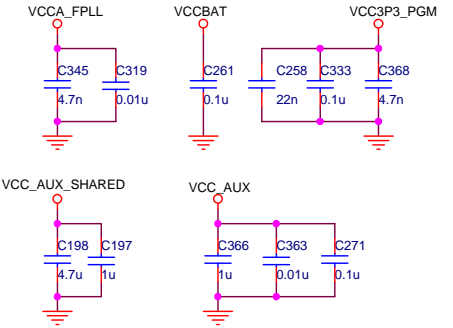
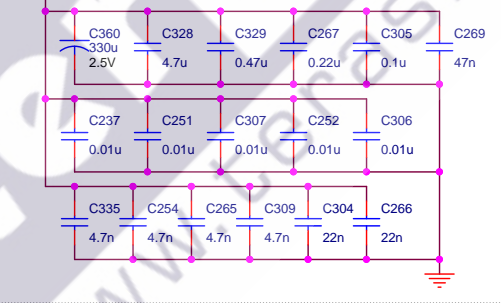
VCC3P3 **FPGA VCC3P3(BANK 3, 4, 5, 8)**

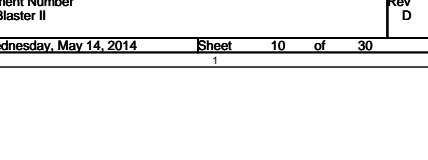
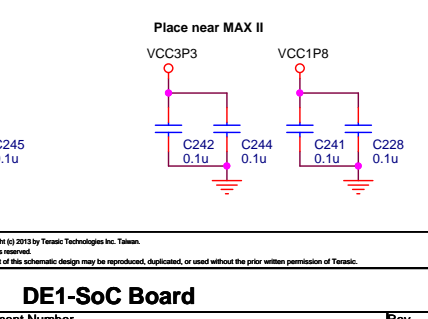
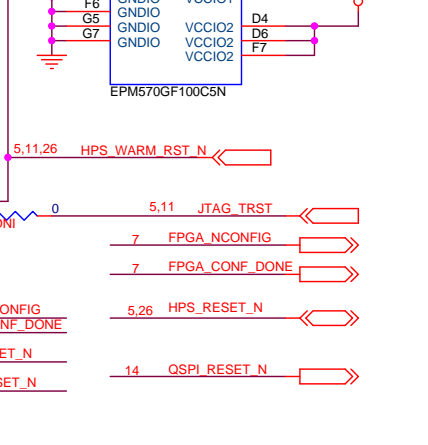
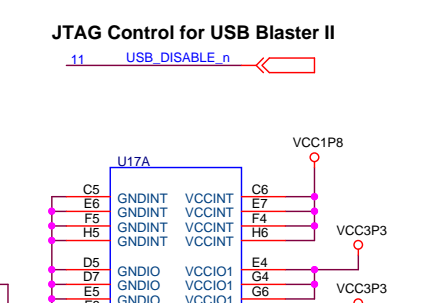
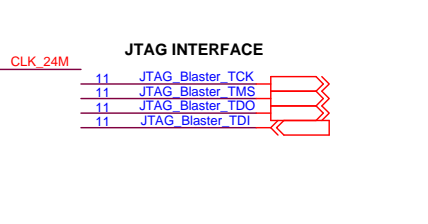
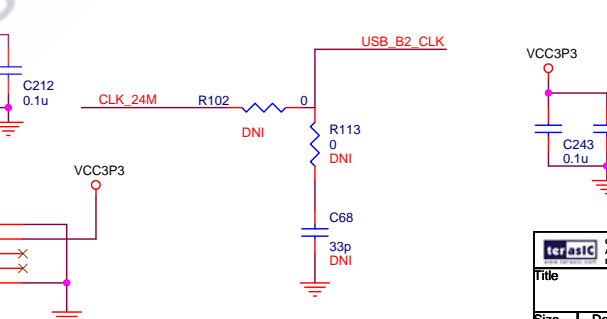
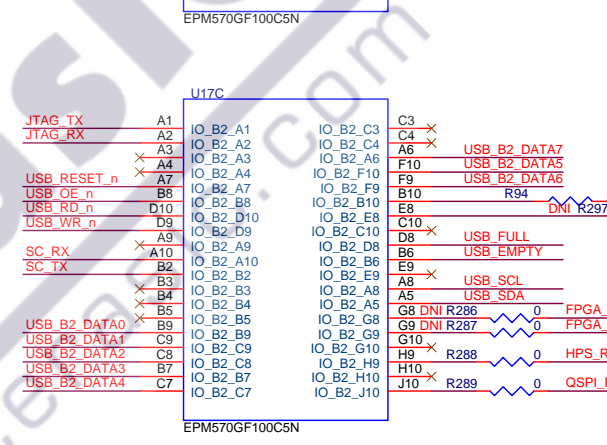
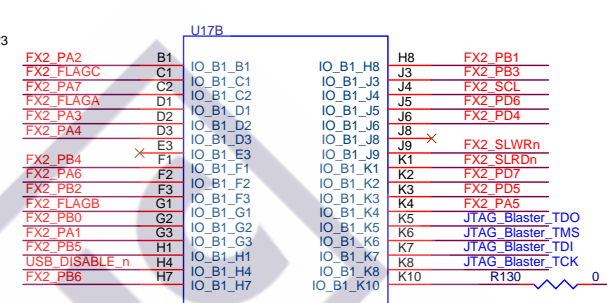
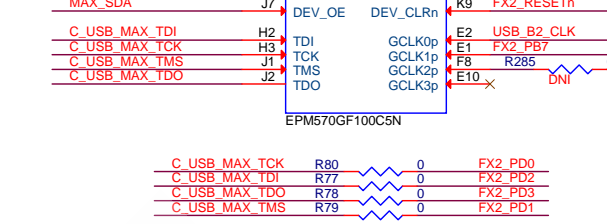
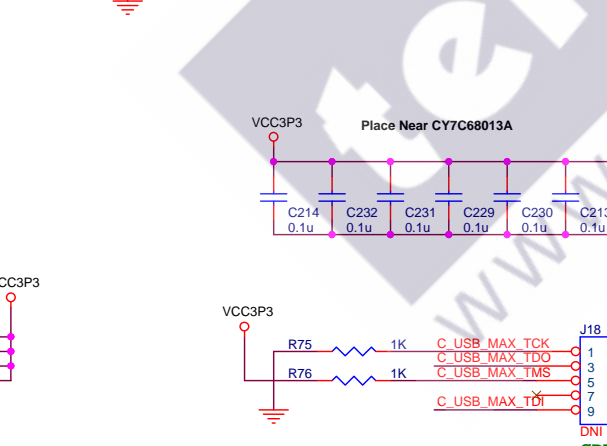
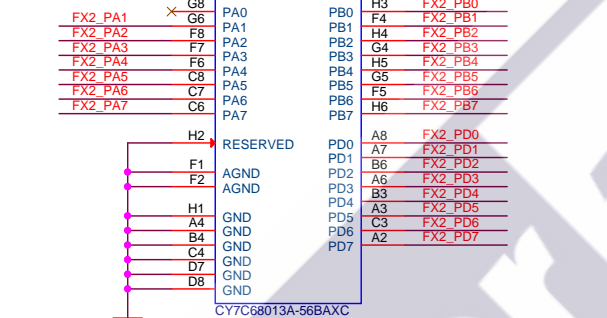
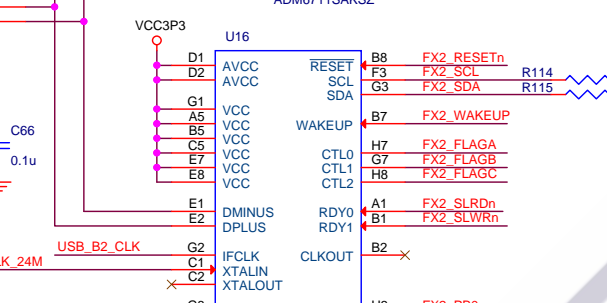
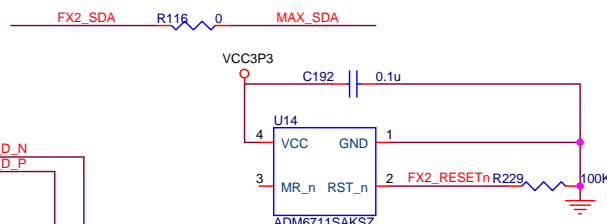
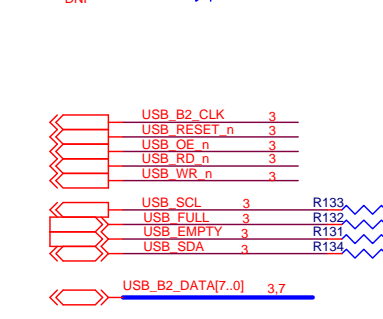
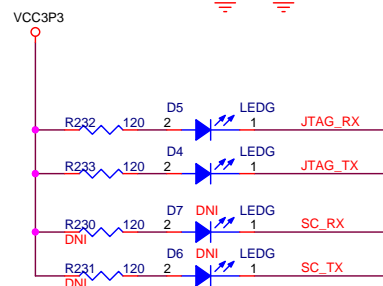
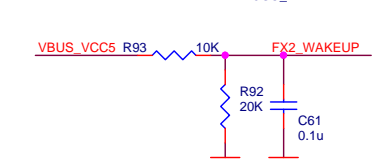
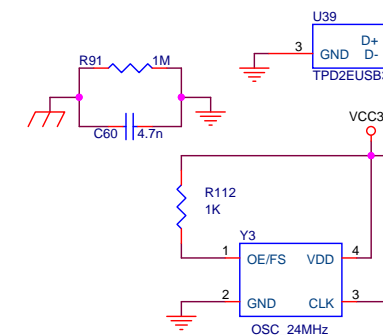
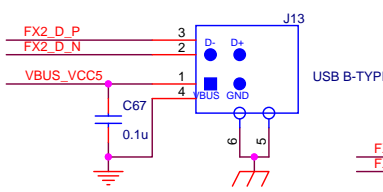


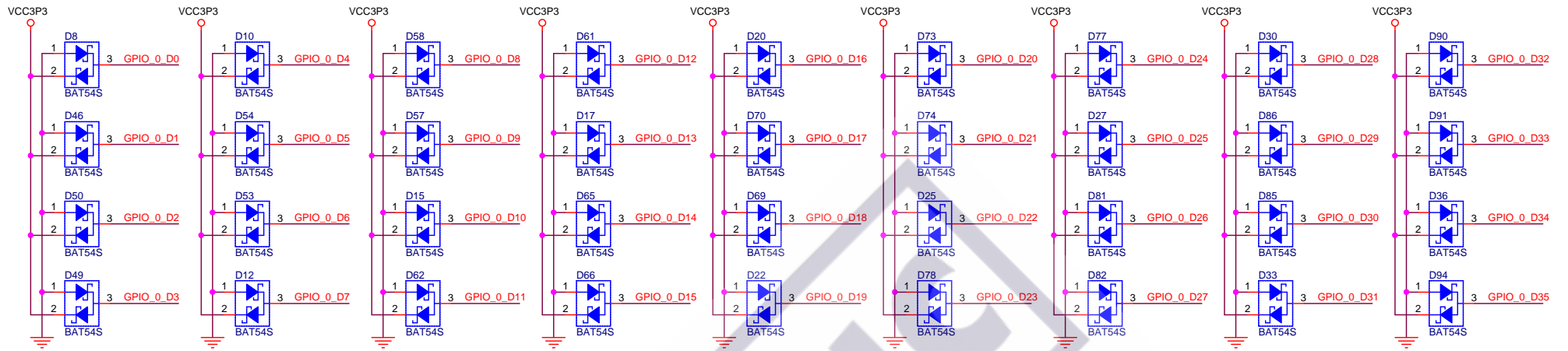
VCC2P5 **HPS VCC2P5(BANK 6)**



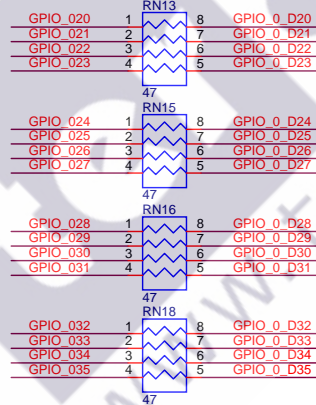
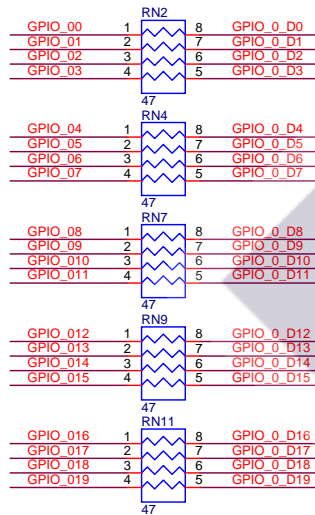
VCC1P5_DDR3 **HPS 1.5V(BANK 6)**



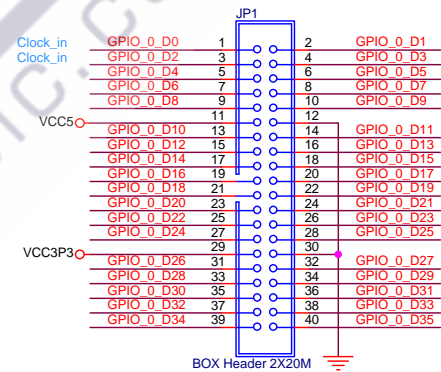




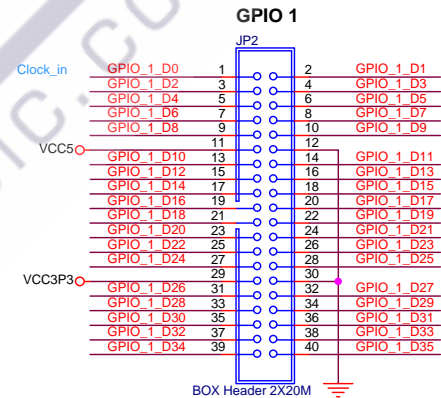
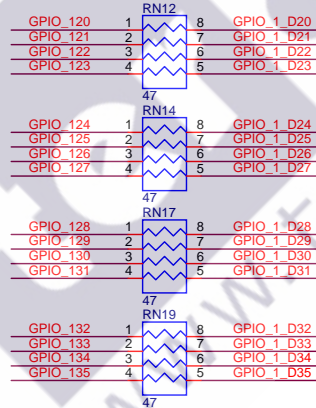
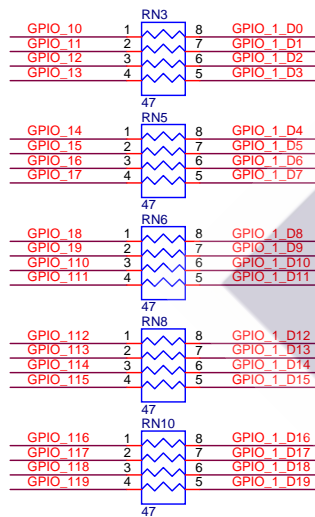
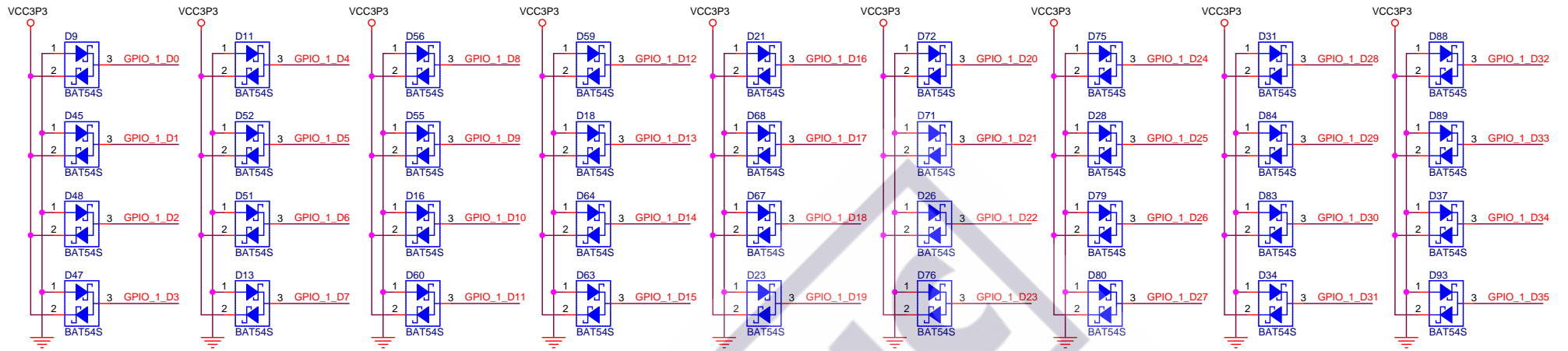
GPIO 0



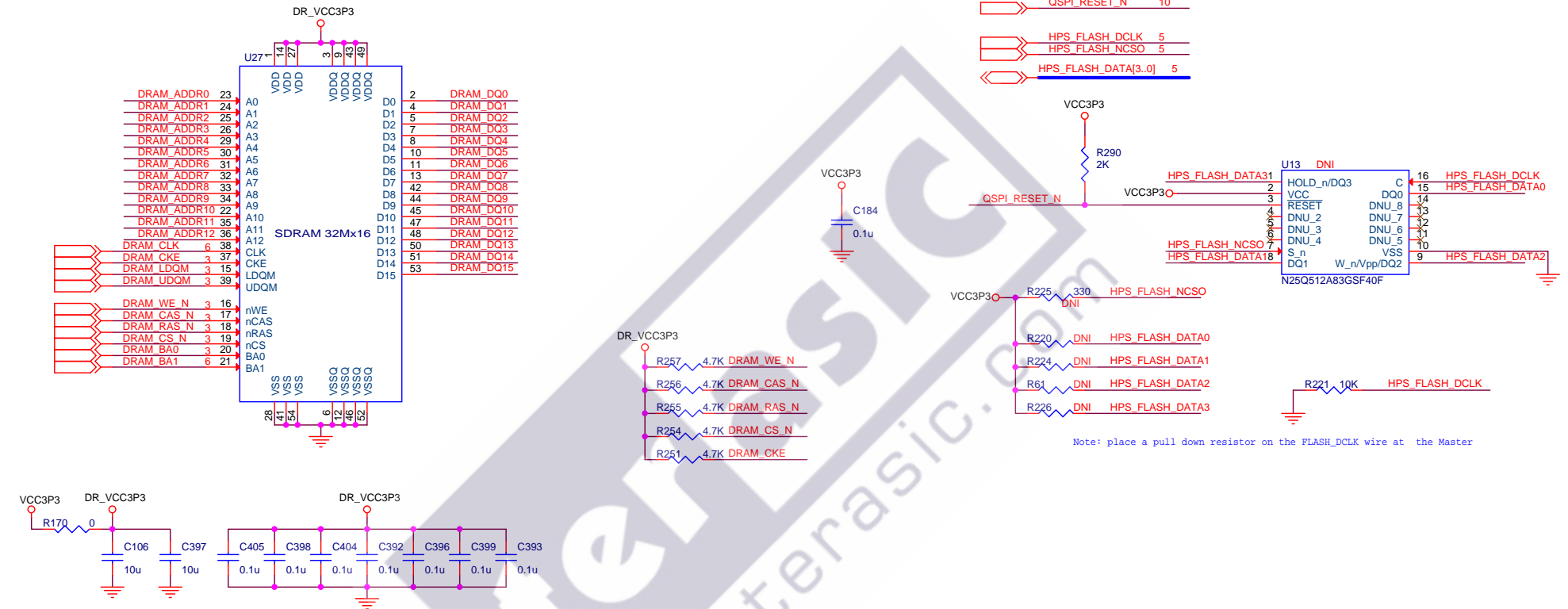
GPIO 0

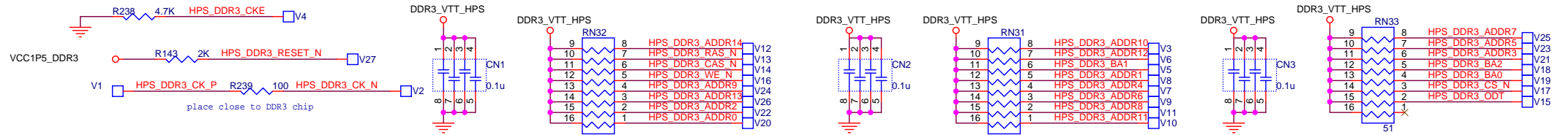


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	GPIO 0	D
Date:	Wednesday, May 14, 2014	Sheet 12 of 30

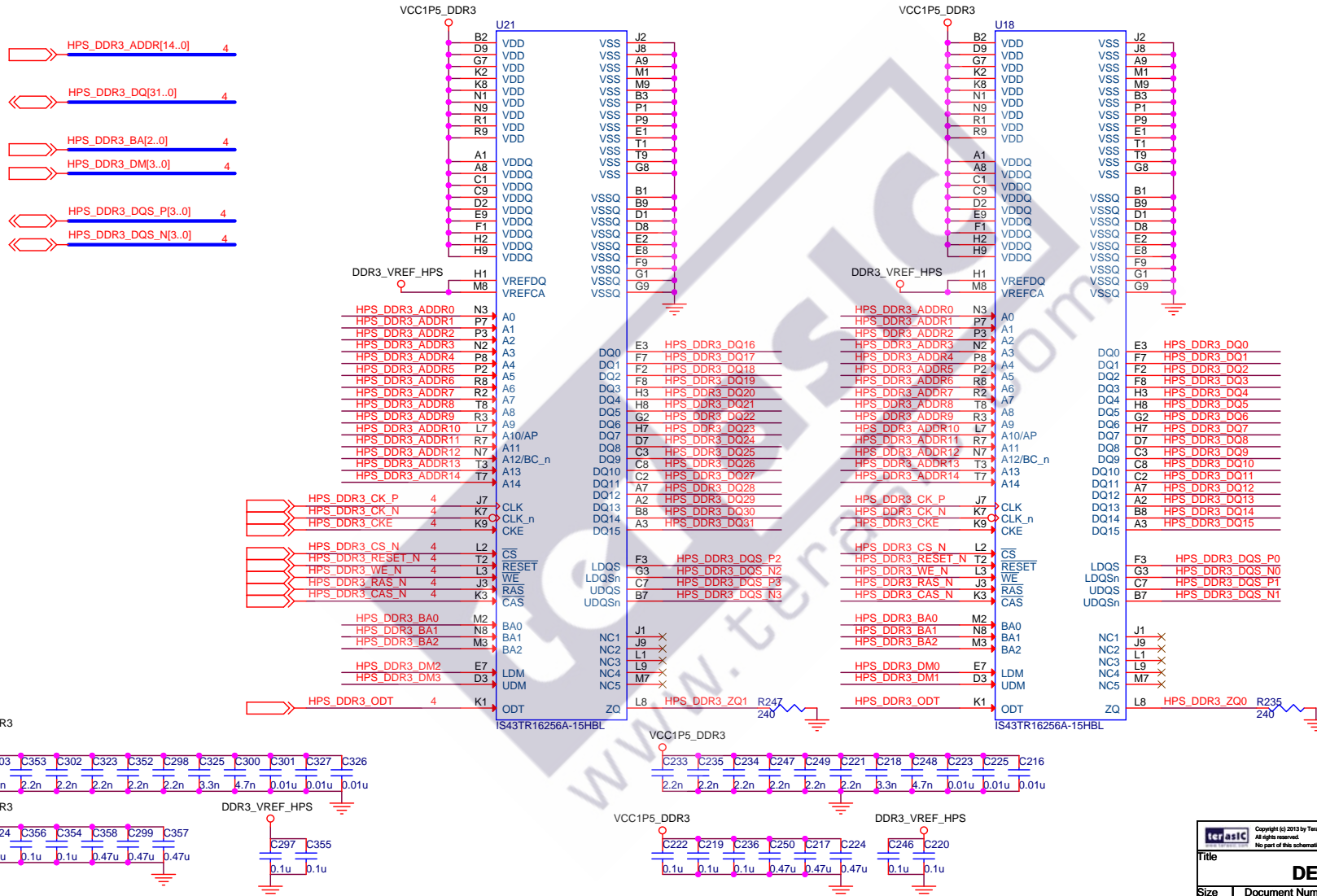


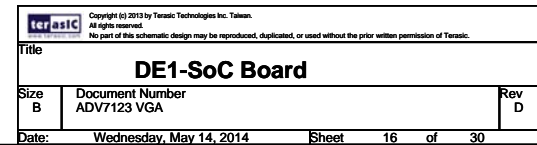
DRAM_DQ[15..0] 3
DRAM_ADDR[12..0] 3,6

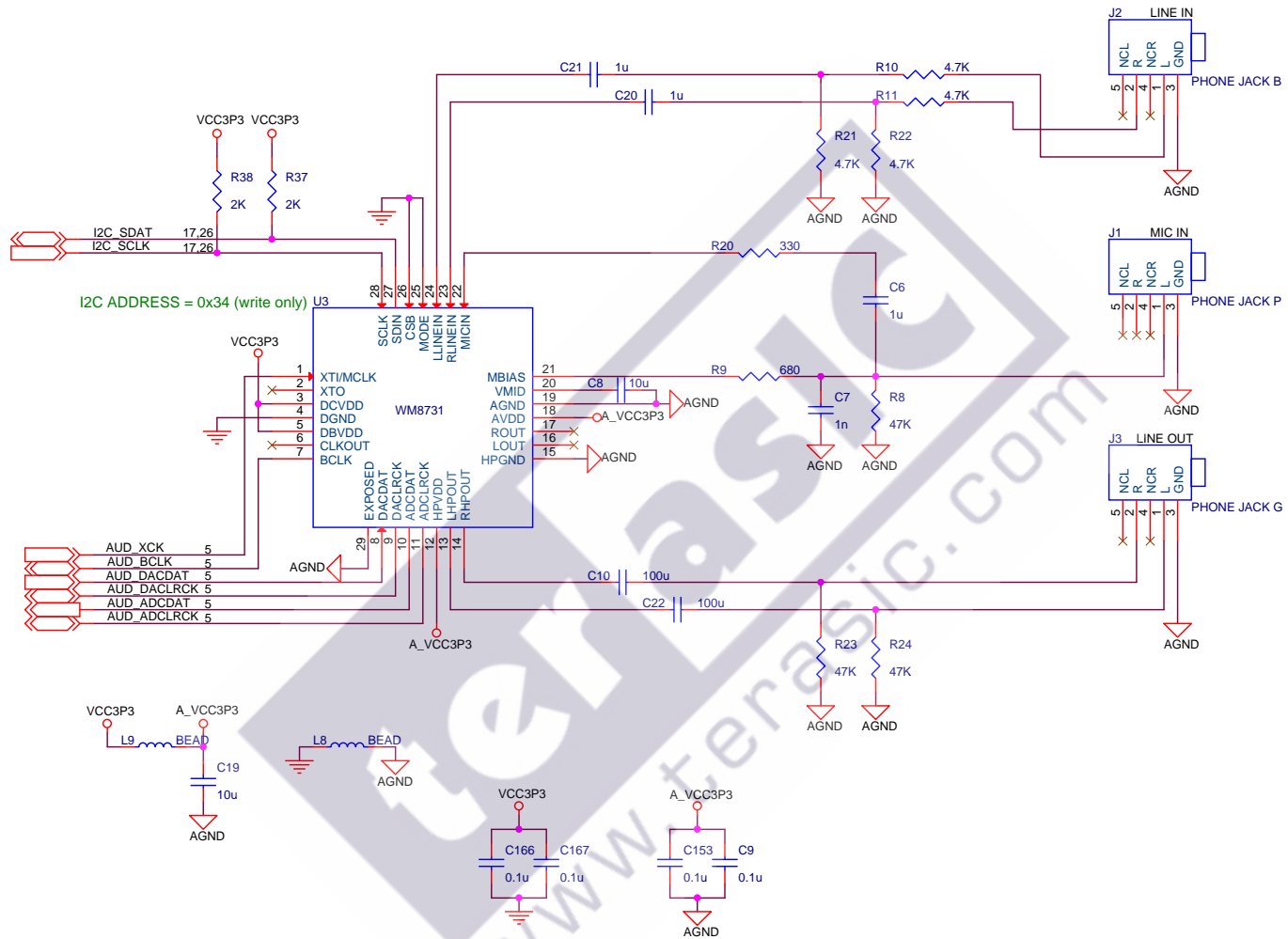


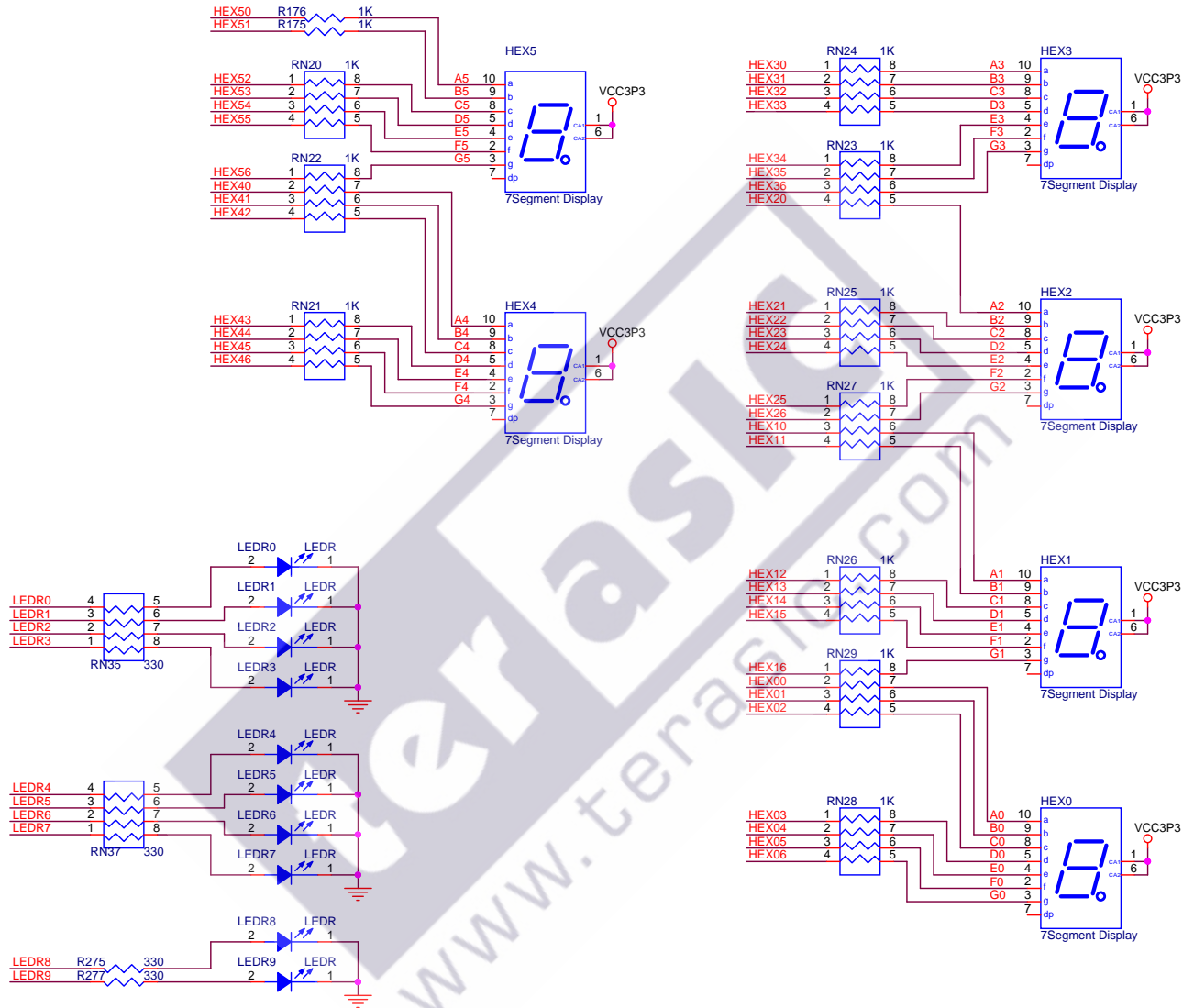
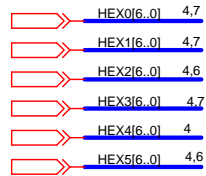


Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note: you can swap the signals on the OCT resistor array(include NC pin)

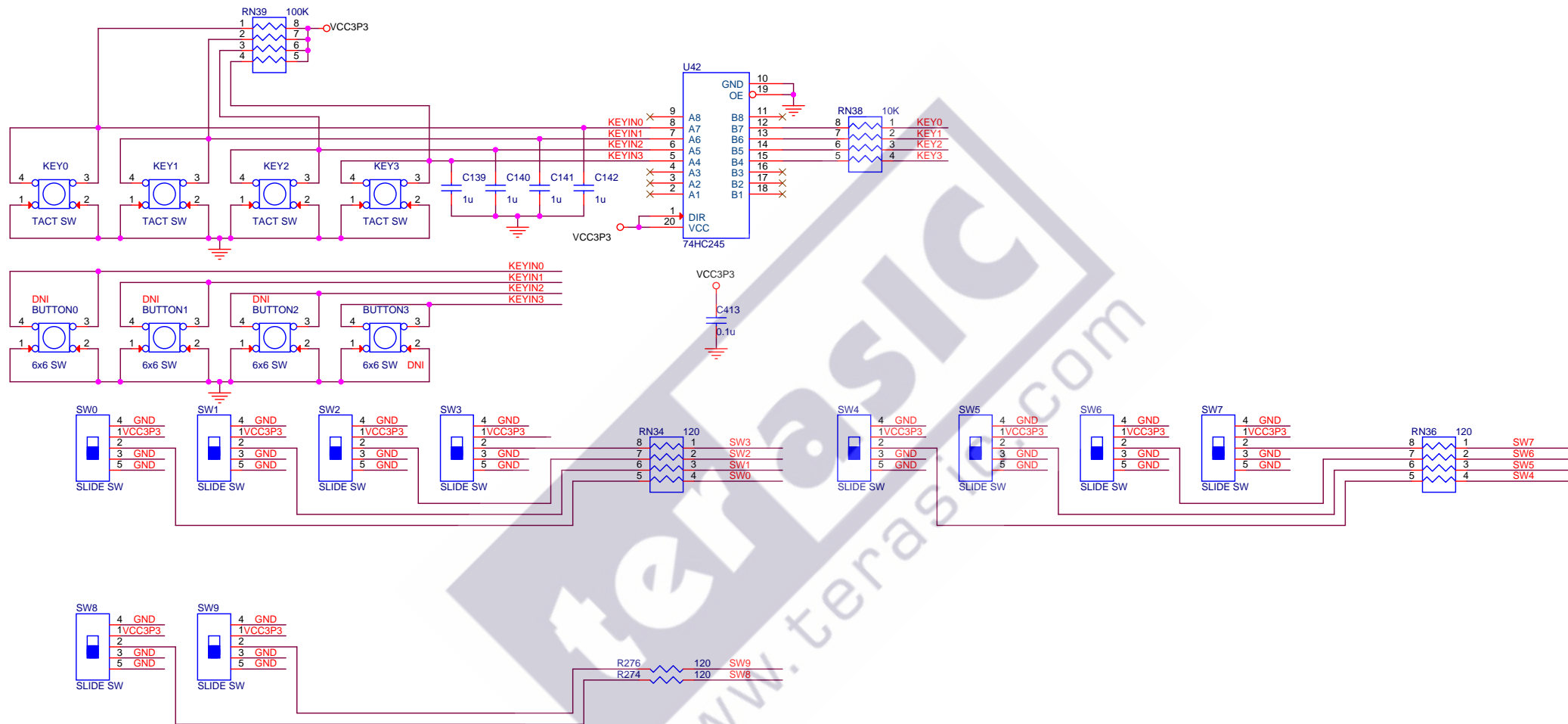


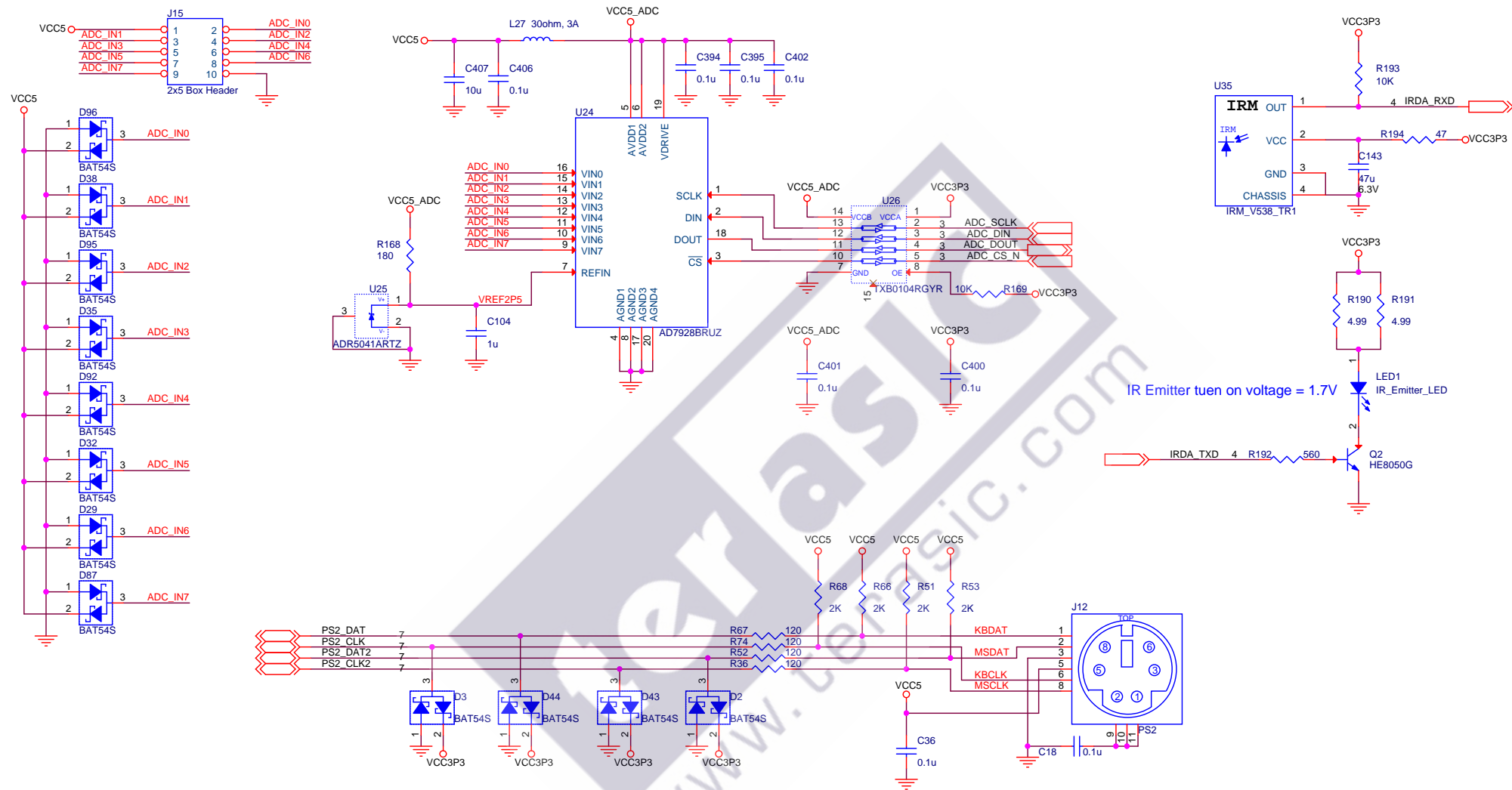


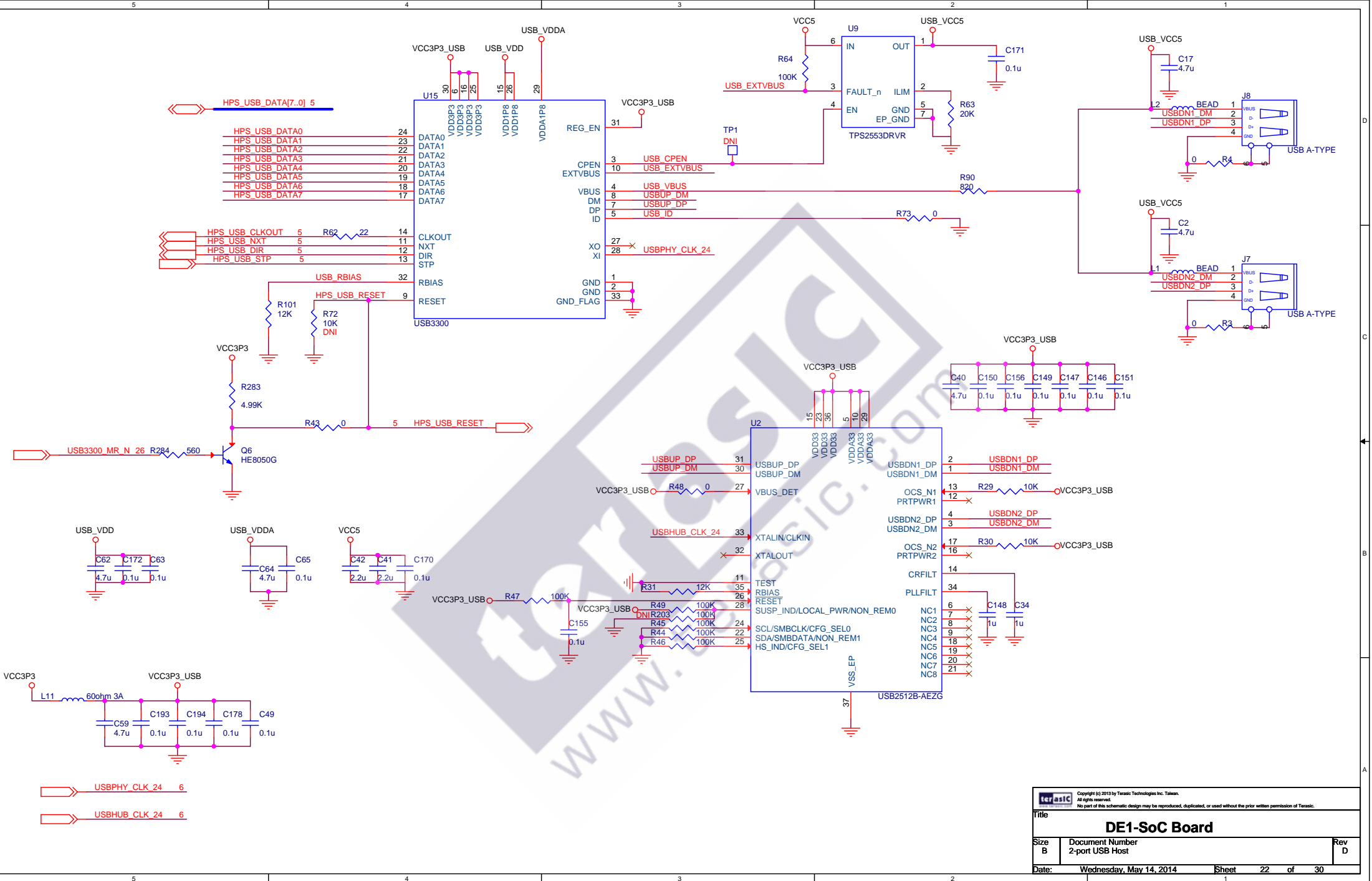


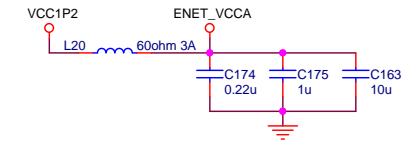
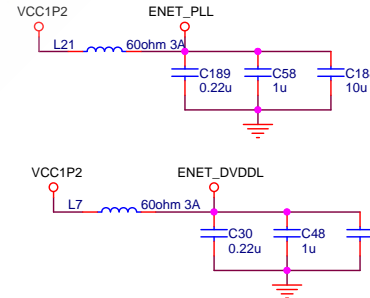
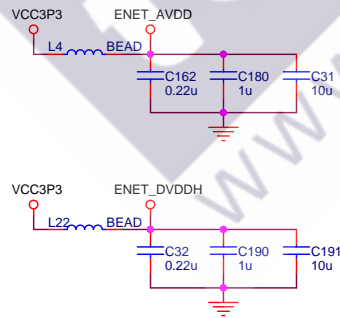
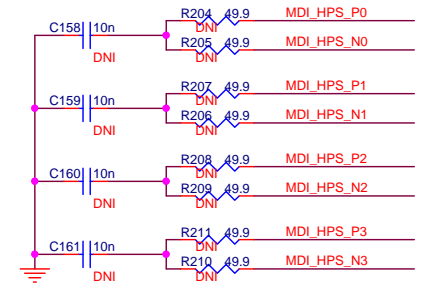
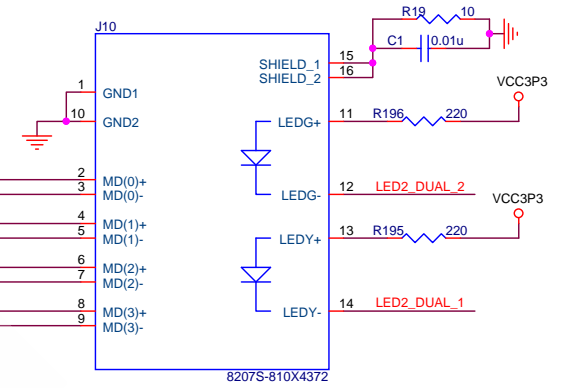
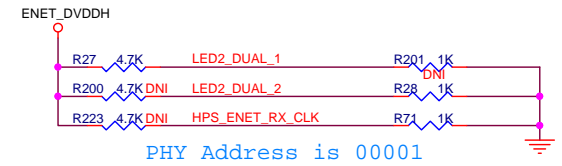
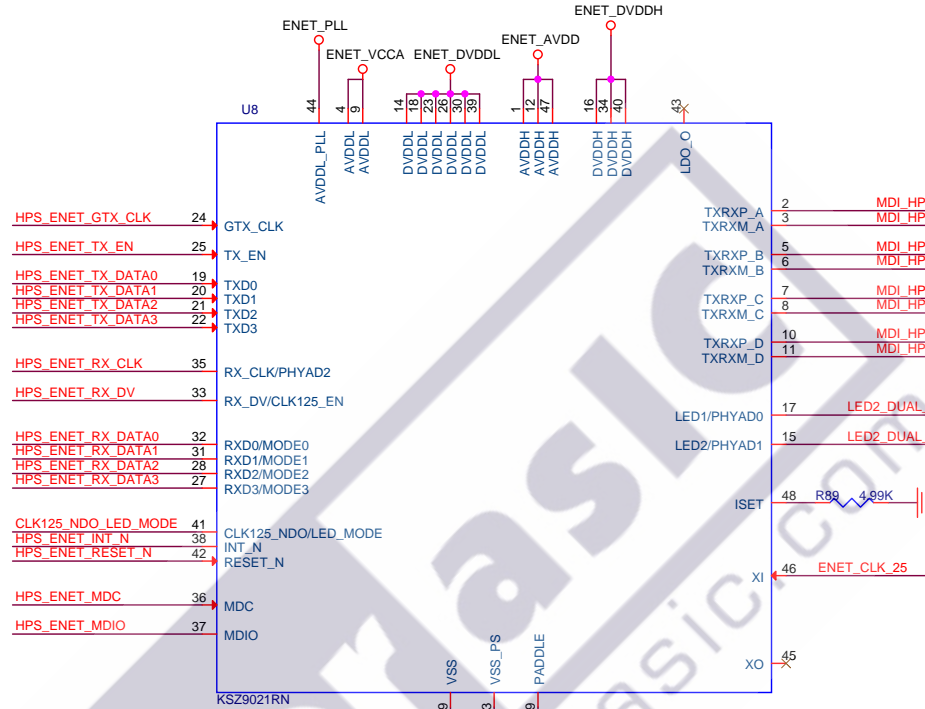
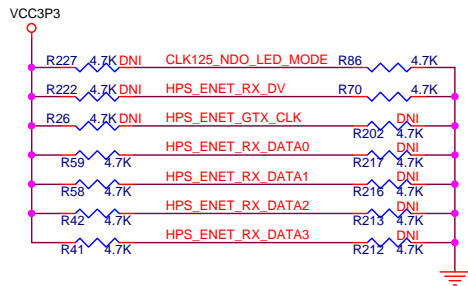
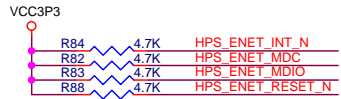
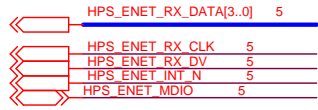
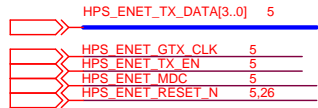



KEY[3..0] 3.6
SW[9..0] 3.7

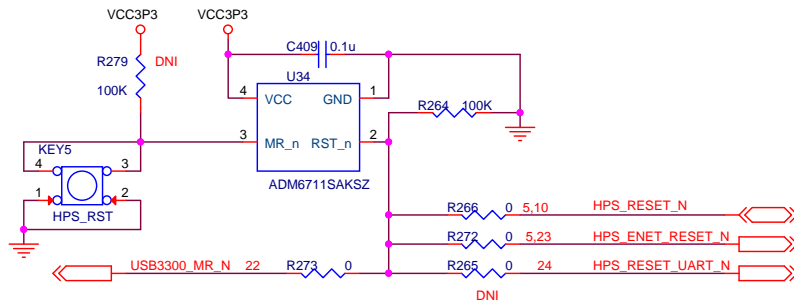






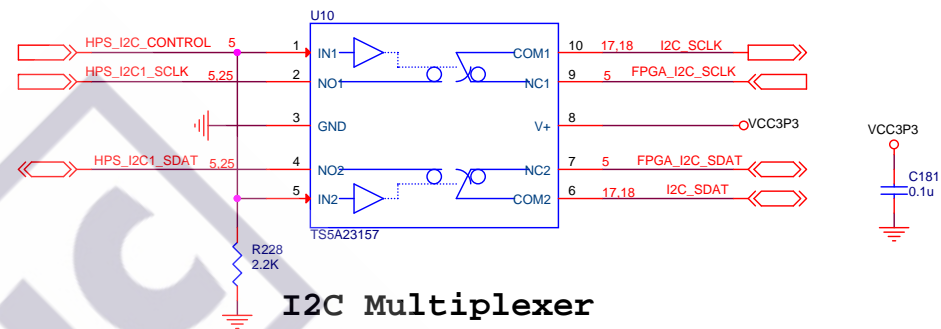


		Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title			
DE1-SoC Board			
Size B	Document Number 1 Ggabit Ethernet		Rev D
Date:	Wednesday, May 14, 2014		Sheet 23 of 30

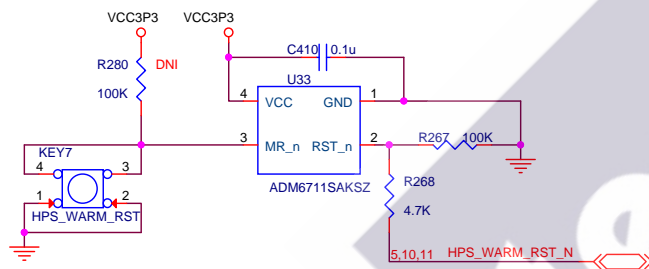


HPS Cold Reset

LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON



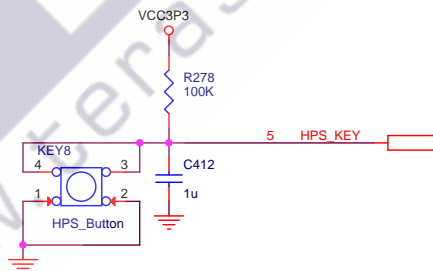
I2C Multiplexer



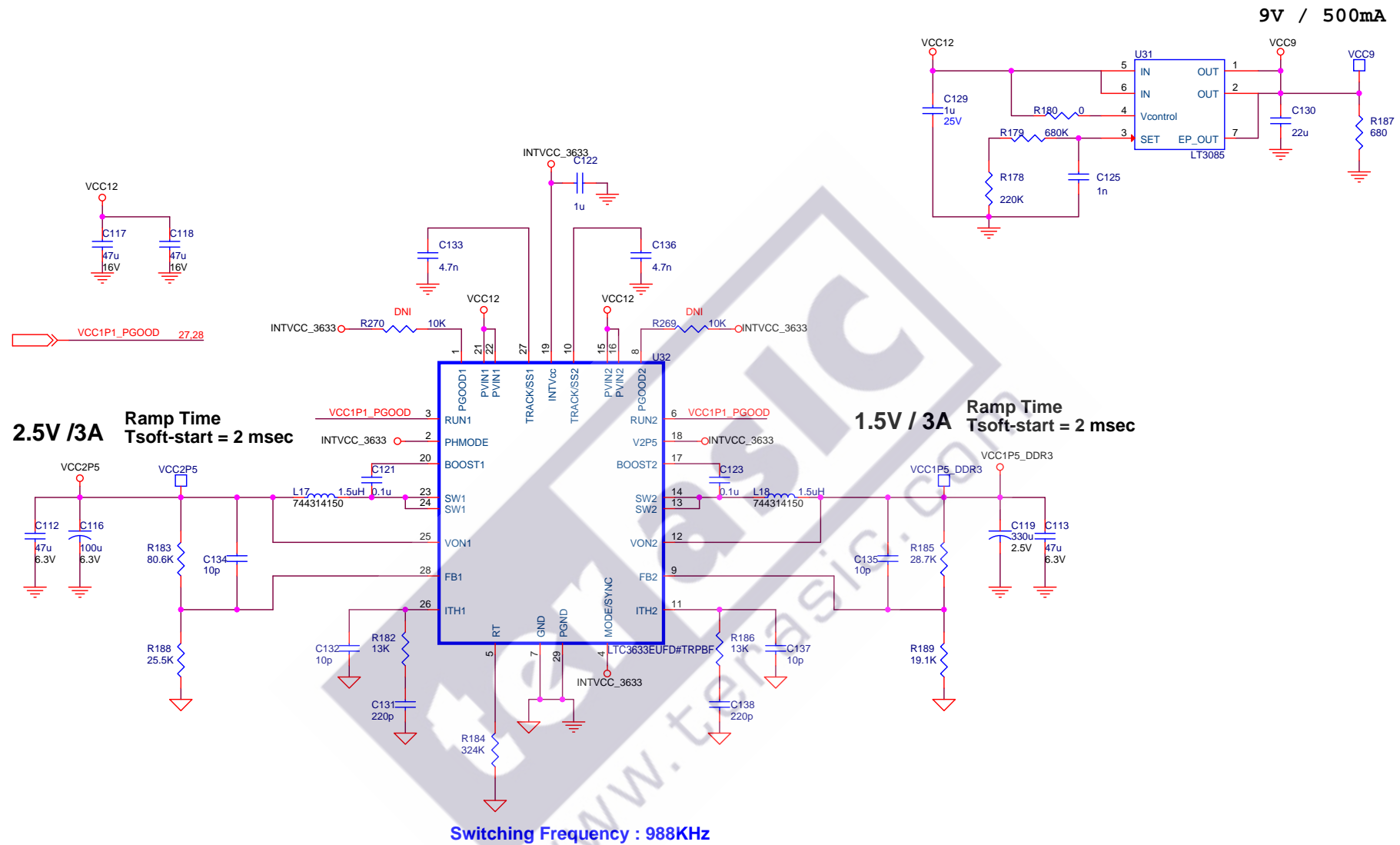
HPS Warm Reset



HPS User LED

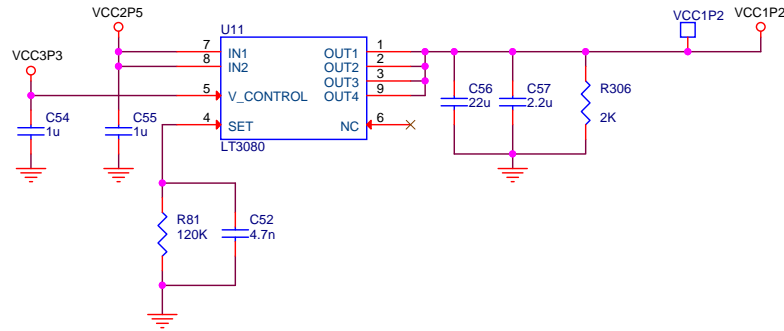


HPS User Button

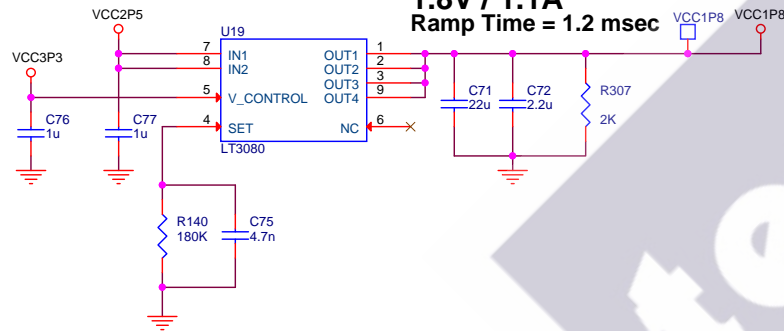


<div> <div>terasic</div> <div>Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div>		
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Power - 9V, 2.5V, 1.5V	D
Date:	Wednesday, May 14, 2014	Sheet 29 of 30

1.2V / 1.1A
Ramp Time = 0.8msec



1.8V / 1.1A
Ramp Time = 1.2 msec



DDR3 VTT, VREF

