# ModelSim Product Comparison

| Feature | ModelSim PE<br>*Block/Small System Simulation, Windows* | ModelSim DE<br>*Block/Small System Simulation, Windows/Linux* | ModelSim SE<br>*Large Block/System Simulation, All Platforms* |
|---|---|---|---|
| **General** | | | |
| Licensing - Floating License | Option | Option | ■ |
| Language Neutral License | | | Option |
| ASIC Sign-Off | | | ■ |
| HDL Editor | ■ | ■ | ■ |
| Integrated Project Manager | ■ | ■ | ■ |
| Source Code Templates and Wizards | ■ | ■ | ■ |
| Platform-Independent Compiled Database | ■ | ■ | ■ |
| Native-Compiled Architecture | ■ | ■ | ■ |
| Incremental Compilation | ■ | ■ | ■ |
| 32/64-Bit Cross-Compatability | | | ■ |
| **Languages** | | | |
| VHDL | ■ | ■ | ■ |
| Verilog | ■ | ■ | ■ |
| VHDL Plus Verilog Dual Language | Option | Option | Option |
| Verilog 2001, 2005 | ■ | ■ | ■ |
| SystemVerilog Design | ■ | ■ | ■ |
| SystemVerilog and PSL IEEE 1850 Assertions | | ■ | |
| SystemC 2.2 | Option | Option | Option |
| Analog/Mixed Signal (Questa AMS Product) | | | Option |
| Verilog PLI/VPI | ■ | ■ | ■ |
| SystemVerilog Direct Programming Interface | ■ | ■ | ■ |
| VHDL FLI | | | ■ |
| **Debug** | | | |
| Interactive Debug | ■ | ■ | ■ |
| Post-Simulation Debug | | | ■ |
| Enhanced Dataflow Window | Option | ■ | ■ |
| Source Annotation | Option[1] | ■ | ■ |
| Hyperlinked Navigation | ■ | ■ | ■ |
| Assertion Thread Debug | | ■ | ■ |
| Advanced FSM Debug | | | ■ |
| C Debugger | Option[2] | Option[2] | ■ |
| Memory Window | ■ | ■ | ■ |
| Extra Standalone Viewer | Option | Option | Option |
| Multiple Waveform Windows | | | ■ |
| Waveform Compare | Option | ■ | ■ |
| Transaction Viewing (SystemC) | Option[2] | Option[2] | Option[2] |
| JobSpy | | | ■ |
| SignalSpy | ■ | ■ | ■ |
| User-Customizable GUI (via Tk) | | | ■ |
| Cross Referencing between Windows | ■ | ■ | ■ |
| **Coverage** | | | |
| Code Coverage (with Toggle Coverage) | Option | ■ | ■ |
| Unified Coverage DataBase (UCDB) | ■[4] | ■ | ■ |
| Coverage Viewer | ■[4] | ■ | ■ |
| Test Ranking | ■[4] | ■ | ■ |
| HTML Reporting | ■[4] | ■ | ■ |
| **Simulation** | | | |
| Single-Kernel Simulation Engine | ■ | ■ | ■ |
| Verilog RTL & Gate Performance Optimizations | | | ■ |
| VHDL RTL & VITAL Performance Optimizations | | | ■ |
| Performance and Memory Profiler | Option | Option | ■ |
| Separate Elaboration | | | ■ |
| Waveform Management Tool Set | ■ | ■ | ■ |
| VCD and Extended VCD Support | ■ | ■ | ■ |
| VCD Re-Simulation | ■ | ■ | ■ |
| Batch Mode Simulation | ■ | ■ | ■ |
| Integrated Sim Farm Support (via JobSpy) | | | ■ |
| Interactive Simulation | ■ | ■ | ■ |
| Black Box Regression Suite Throughput | | | ■ |
| Checkpoint & Restore | | | ■ |
| VHDL 2008 Encryption | ■ | ■ | ■ |
| Verilog 2005 Encryption | ■ | ■ | ■ |
| SWIFT Interface / SmartModels | Option | Option | ■ |
| SecureIP | Option[3] | ■ | ■ |
| Synopsys Hardware Modeler Support | | | ■ |
| **Platform Support** | | | |
| 32-Bit OS Support | Windows XP/Vista | Windows XP/Vista/Linux | Linux, Solaris, Windows XP/Vista |
| 64-Bit OS Support | | | Linux x86-64, Solaris 64 |

1 - Included in Enhanced Dataflow Option

2 - Included in SystemC Option

3 - Option for use with VHDL

4 - Data generated with code coverage option

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