



Intel® Stratix® 10 Analog to Digital Converter User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.1**



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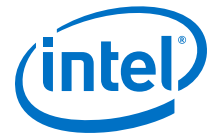
UG-S10ADC | 2018.11.05

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Contents

1. Intel® Stratix® 10 ADC Overview.....	3
2. Intel Stratix 10 ADC Architecture and Features.....	4
2.1. Intel Stratix 10 Voltage Sensor.....	4
2.1.1. Voltage Conversion.....	5
2.2. Intel Stratix 10 Temperature Sensing Diodes.....	5
2.2.1. Internal Temperature Sensor.....	6
2.2.2. External Temperature Sensor.....	7
2.2.3. Temperature Sensor Channels and Locations.....	7
3. Intel Stratix 10 ADC Design Considerations.....	10
3.1. Guidelines: Using External Temperature Sensors.....	10
4. Intel Stratix 10 ADC Implementation Guides.....	11
4.1. Sampling the Intel Stratix 10 Voltage Sensor Channels.....	11
4.2. Reading the Intel Stratix 10 Internal Temperature Sensing Diodes.....	13
5. Intel Stratix 10 ADC IP Core References.....	15
5.1. Voltage Sensor Intel Stratix 10 FPGA IP Digital Signals.....	15
5.2. Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals.....	16
6. Intel Stratix 10 Analog to Digital Converter User Guide Archives.....	19
7. Document Revision History for the Intel Stratix 10 Analog to Digital Converter User Guide.....	20



1. Intel® Stratix® 10 ADC Overview

The analog-to-digital converters (ADCs) in Intel® Stratix® 10 devices provide built-in capability for converting external analog voltage signals and monitoring on-die temperature.

Intel Stratix 10 devices contain two types of on-die sensors:

- Voltage sensor—provides digital voltage readings.
 - You can use the voltage sensor to perform live monitoring of critical on-chip supply voltages and external analog signals.
 - You can access the voltage readout using the Voltage Sensor Intel Stratix 10 FPGA IP.
- Temperature sensor—provides on-die temperature readings.
 - The internal digital temperature sensor consists of internal temperature sensing diodes (TSD) and built-in ADC.
 - You can monitor the on-die temperature through the internal digital temperature sensor in the Intel Stratix 10 core fabric and transceiver tiles.
 - You can use the Temperature Sensor Intel Stratix 10 FPGA IP to read the digital temperature in Celsius.
 - You can also access on-die TSDs using external third-party temperature sensors.
 - If you want temperature reading correlation, you can use both internal and external temperature sensors simultaneously.

Related Information

- [Intel Stratix 10 Analog to Digital Converter User Guide Archives](#) on page 19
Provides a list of user guides for previous versions of the Intel Stratix 10 ADC IP core.
- [Secure Device Manager](#)
- [Stratix 10 Device Datasheet](#)
- [Stratix 10 Power Management User Guide](#)

2. Intel Stratix 10 ADC Architecture and Features

In Intel Stratix 10 devices, the SDM connects to the voltage and internal temperature sensors. The devices feature internal temperature sensors and external temperature sensing diodes (TSDs) in select locations.

To access the voltage or internal TSD readouts, use the Voltage Sensor Intel Stratix 10 FPGA IP or Temperature Sensor Intel Stratix 10 FPGA IP. To use an external temperature sensor, connect the sensor to the Intel Stratix 10 external TSD pins.

2.1. Intel Stratix 10 Voltage Sensor

The on-chip voltage sensor in Intel Stratix 10 is an 8-bit full differential ADC.

The voltage sensor monitors two external differential inputs and five internal power supplies. To read the voltage values through the SDM, use the Voltage Sensor IP core.

Figure 1. Intel Stratix 10 Voltage Sensor

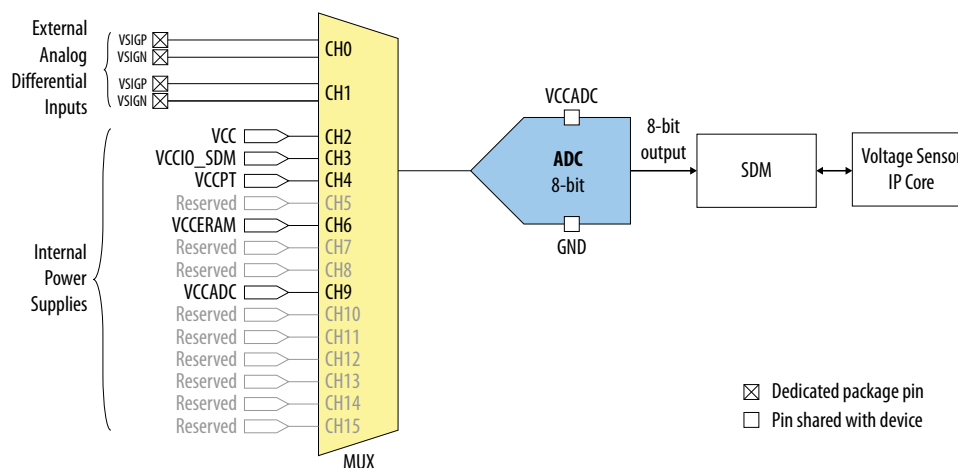
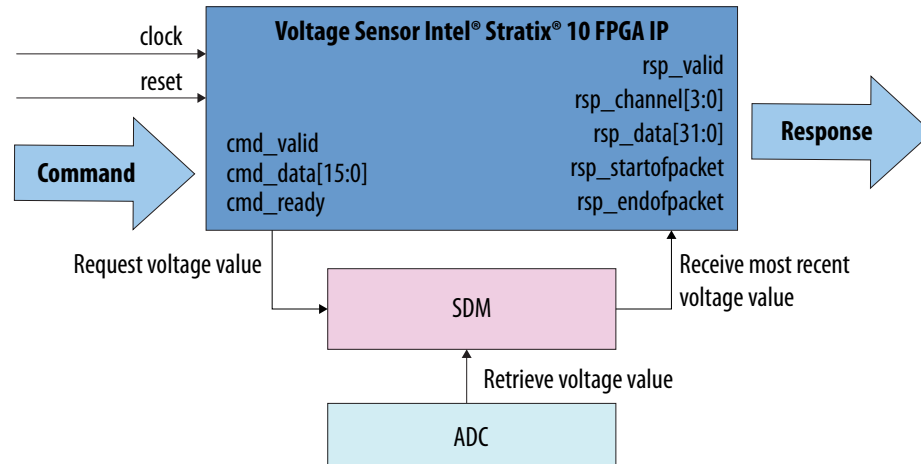




Figure 2. Voltage Sensor IP Core Block Diagram



The ADC samples the voltage at regular intervals. When the Voltage Sensor IP core sends voltage sampling request to the SDM, the SDM returns the most recently read voltage value. The IP core then returns the observed voltage value as an unsigned 32-bit fixed point binary number.

The maximum value of the external analog signal (differential scale) is 1.24 V.

Related Information

- [Sampling the Intel Stratix 10 Voltage Sensor Channels](#) on page 11
Provides the steps to read the voltage values and the timing diagram.
- [Voltage Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 15
Provides more information about the command and response signals of the Voltage Sensor IP core.

2.1.1. Voltage Conversion

The Voltage Sensor IP core returns the sampled voltage in unsigned 32-bit fixed point binary format, with 16 bits below binary point.

For example, if the returned value is 0x0000C000, the voltage value is 0.75 V.

2.2. Intel Stratix 10 Temperature Sensing Diodes

For system-level power supply management, the Intel Stratix 10 device provides internal and external TSDs. You can use both internal and external TSDs simultaneously.

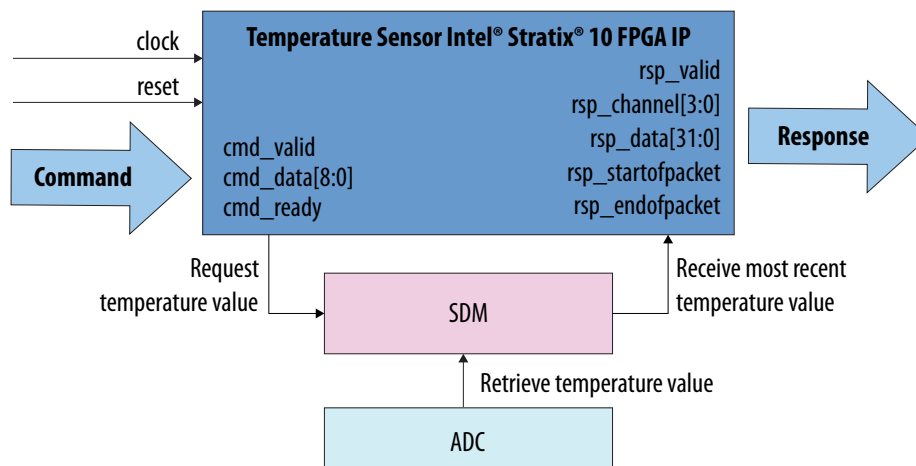
- The internal TSDs allow you to monitor the device's on-die temperature using the on-chip digital temperature sensing circuitry. The internal TSDs are available in the core fabric, transceiver tiles, and high-bandwidth DRAM memory (HBM2) stacks.
- The external TSDs allow you to monitor the device's on-die temperature using external temperature sensors. The external TSDs are available in the core fabric and transceiver tiles.

When a transceiver tile is powered down, the tile's internal TSD is not available. However, you can still sample the tile's temperature through its external TSD.

2.2.1. Internal Temperature Sensor

The SDM reads the temperature value from the internal TSDs. To sample the on-die temperature value through the SDM, use the Temperature Sensor IP core.

Figure 3. Temperature Sensor IP Core Block Diagram



The ADC samples the temperature at a regular interval. When the Temperature Sensor IP core sends temperature sampling request to the SDM, the SDM returns the most recently read temperature value. The IP core then returns the observed temperature value in Celsius as a signed 32-bit fixed point binary number.

Note: You can use any clock source to clock the Temperature Sensor IP core. However, you must always ensure that your design closes timing.

Related Information

- [Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 16
Provides more information about the command and response signals of the Temperature Sensor IP core.
- [Reading the Intel Stratix 10 Internal Temperature Sensing Diodes](#) on page 13
Provides the steps to read the temperature values and the timing diagram.
- [Temperature Sensor Channels and Locations](#) on page 7

2.2.1.1. Temperature Calculation for the Internal Temperature Sensor

The Temperature Sensor IP core returns the Celsius temperature value in signed 32-bit fixed point binary format, with eight bits below binary point.

To convert the returned value into decimal, use two's complement operation on the signed integer portion. Then, add the decimal number to the unsigned 8-bit fraction (bit value $\times 2^{-1} + \text{bit value} \times 2^{-2} + \dots + \text{bit value} \times 2^{-8}$). For example, if the returned value is 0xFFFFE1C0, the temperature value is -30.25°C.

The unsigned 8-bit fraction is always zero for the temperature values returned by the transceiver tiles.

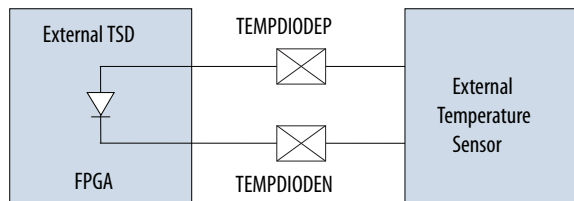


2.2.2. External Temperature Sensor

You can monitor the Intel Stratix 10 device's die temperature by connecting an external temperature sensor to the Intel Stratix 10 external TSD.

The external TSD requires two pins for voltage reference. If you do not use the external TSD pins, leave the pins unconnected.

Figure 4. External Temperature Sensor Connection to Intel Stratix 10 External TSD



Related Information

- [Temperature Sensor Channels and Locations](#) on page 7
- [Guidelines: Using External Temperature Sensors](#) on page 10

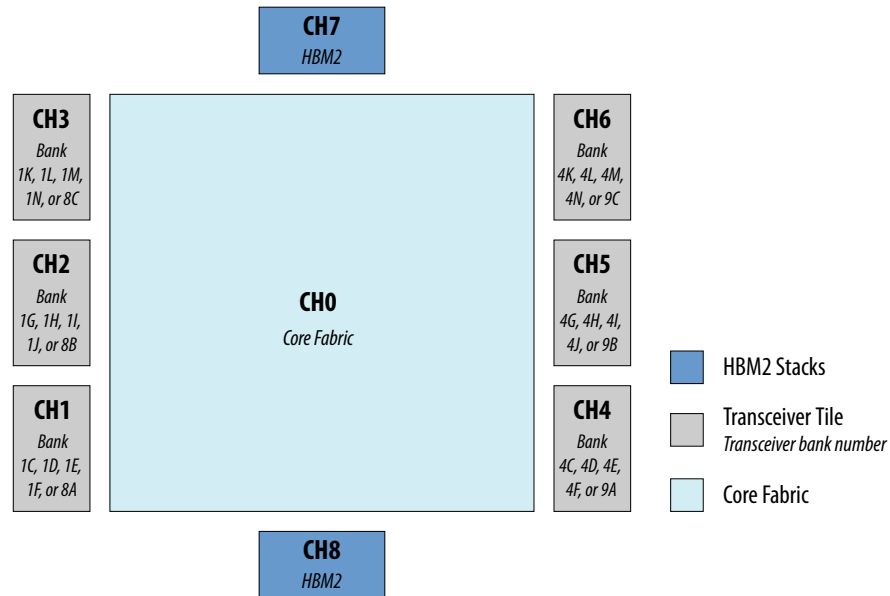
2.2.3. Temperature Sensor Channels and Locations

The Intel Stratix 10 internal TSDs are located in the core fabric, transceiver tiles, and HBM2 stacks. The external TSDs are available in the core fabric and transceiver tiles.

- To read the internal TSDs, specify the channels to sample in the `cmd_data` signal to the Temperature Sensor IP core.
- To read the external TSDs, connect external temperature sensors to the designated TEMPDIODE pin.

Figure 5. Locations and Channel Numbers of Intel Stratix 10 TSDs

This diagram shows the temperature sensor channel locations from a package bottom view. Each transceiver tile in the diagram is labeled using the bank number of one of its transceiver banks.



Note: The availability of the transceiver tiles and HBM2 stacks varies among Intel Stratix 10 devices. To identify the location—and availability—of a transceiver tile, find the location of one of its transceiver banks in the Intel Quartus® Prime Pin Planner.

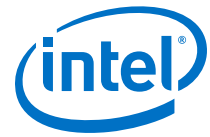
Table 1. Internal TSD Channels and External TSD Pins

Internal TSD Channel	External TSD	
	Pin	Device and Package Support
CH0	TEMPDIODEp[0] TEMPDIODEn[0]	All Intel Stratix 10 devices and packages.
CH1	TEMPDIODEp[1] TEMPDIODEn[1]	All Intel Stratix 10 devices and packages.
CH2	TEMPDIODEp[2] TEMPDIODEn[2]	Support of these external TSDs depends on availability of the transceiver tile. However, regardless of transceiver tile availability, these external TSDs are not supported in the NF43, UF50, and HF55 packages of the following devices: <ul style="list-style-type: none"> GX 850 and SX 850 GX 1100 and SX 1100 GX 1650 and SX 1650 GX 2100 and SX 2100 GX 2500 and SX 2500 GX 2800 and SX 2800 GX 4500 and SX 4500 GX 5500 and SX 5500 For the listed devices, use the Temperature Sensor IP core to read the internal TSD channels.
CH3	TEMPDIODEp[3] TEMPDIODEn[3]	
CH4	TEMPDIODEp[4] TEMPDIODEn[4]	
CH5	TEMPDIODEp[5] TEMPDIODEn[5]	
CH6	TEMPDIODEp[6] TEMPDIODEn[6]	
CH7	—	The high-bandwidth DRAM memory (HBM2) stacks do not feature external TSDs. Use the internal TSD channels.
CH8	—	



Related Information

- [Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 16
Provides more information about the command and response signals of the Temperature Sensor IP core.
- [Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 16
- [Internal Temperature Sensor](#) on page 6
- [External Temperature Sensor](#) on page 7



3. Intel Stratix 10 ADC Design Considerations

There are several considerations that require your attention to ensure the success of your designs. Unless noted otherwise, these design guidelines apply to all variants of this device family.

3.1. Guidelines: Using External Temperature Sensors

Noise coupled from board traces or from within the Intel Stratix 10 device package can influence the sensitive TSD circuit. The signal from the device to the external temperature sensor is based on millivolts (mV) of difference at the external TSD pins. Switching the I/O near the external TSD pins can affect the temperature reading.

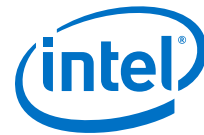
Intel recommends that you sample the temperature when the device is inactive or use the internal temperature sensor with the internal TSD.

You can use both internal and external temperature sensors simultaneously.

Board Connection Guidelines for the Traces to the External TSD Pins

- Keep the trace lengths to the $TEMPDIODE_P$ or $TEMPDIODE_N$ pins less than eight inches.
- Route both traces in parallel and place them close to each other with grounded guard tracks on each side.
- Intel recommends a 10-mils width and space for both traces.
- Route both traces through the most minimum number of vias and crossunders possible to minimize the thermocouple effects.
- Ensure that the number of vias for both traces are the same.
- Ensure that both traces are approximately the same length.
- To avoid coupling, insert a GND plane between the external TSD pins traces and high-frequency toggling signals, such as clocks and I/O signals.
- To filter high-frequency noise, place an external capacitor between the traces close to the external sensors. For Maxim* temperature sensors, use an external capacitor between 2200 pF and 3300 pF.
- Place a 0.1 μ F bypass capacitor close to the external temperature sensor.
- If you use only the internal TSD, you can leave the $TEMPDIODE_P$ and $TEMPDIODE_N$ pins unconnected.

For details about device specifications and connection guidelines, refer to the external temperature sensor manufacturer's datasheet.



4. Intel Stratix 10 ADC Implementation Guides

The Voltage Sensor and Temperature Sensor IP cores are soft controllers for the ADC hard IP blocks. With these IP cores, you can read sampling values from the different ADC channels through the SDM.

- To sample external or internal voltages, use the Voltage Sensor Intel Stratix 10 FPGA IP.
- To sample the on-die temperature using the internal TSDs, use the Temperature Sensor Intel Stratix 10 FPGA IP.

The Voltage Sensor or Temperature Sensor IP core does not have configurable options in the Intel Quartus Prime parameter editor. To use the IP core, instantiate an instance of it in your design and use the digital signal interface of the IP core to access the voltage or temperature readouts.

The command and response interfaces of the Voltage Sensor and Temperature Sensor IP cores are Avalon® Streaming (Avalon-ST) interfaces with ready latency of 0.

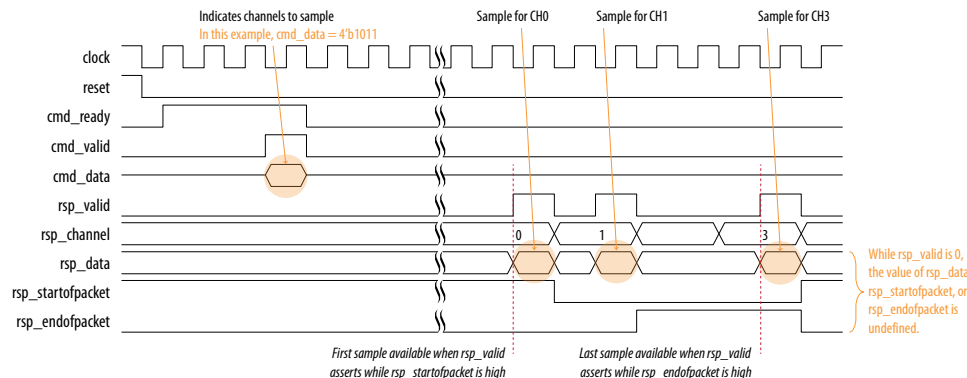
Related Information

- [Secure Device Manager](#)
- [Voltage Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 15
Provides more information about the command and response signals of the Voltage Sensor IP core.
- [Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 16
Provides more information about the command and response signals of the Temperature Sensor IP core.

4.1. Sampling the Intel Stratix 10 Voltage Sensor Channels

To sample a single or multiple voltage sensor channels, specify which channels to sample in the Voltage Sensor IP core.

Figure 6. Waveform Example: Sampling Voltage Values from Channels 0, 1, and 3



Note: Set only valid bits in the **cmd_data** word. Otherwise, the response from the voltage sensor is undefined.

- During device initialization, before the device enters user mode:
 - Assert the **reset** port of the Voltage Sensor IP core to keep it in reset mode.
 - Keep the **cmd_valid** and **cmd_data** signal at "0".
- After the device enters user mode, simultaneously assert a logic high to the **cmd_valid** signal and send the **cmd_data** value. For each sampling, assert **cmd_valid** for a period of only one to three clock cycles. When you are not acquiring the voltage sensor readout, deassert **cmd_valid**.

The **cmd_data** signal is a 16-bit bitmask that specifies from which channel to sample the voltage. The SDM samples the voltages approximately every 1 ms ⁽¹⁾.

When you assert **cmd_valid** while **cmd_ready** is high, the IP core requests from the SDM the most recent voltage values of the channels you specify in **cmd_data**. After sending the request, the IP core drives **cmd_ready** low and waits for response from the SDM.

- Each time the **rsp_valid** signal goes high, indicating that the voltage value is ready, read the **rsp_data** and **rsp_channel** response signals.

The **rsp_valid** signal goes high once for each bit in the **cmd_data** word. The first valid data in the cycle is available when **rsp_valid** asserts while the **rsp_startofpacket** signal is high. The last valid data in the cycle is available when **rsp_valid** asserts while the **rsp_endofpacket** signal is high. In each valid response, the **rsp_data** signal provides the voltage value while the **rsp_channel** signal indicates from which channel the voltage was sampled.

The value in **rsp_data** is an unsigned 32-bit fixed point binary number, with 16 bits below the binary point.

Related Information

- [Voltage Conversion](#) on page 5

⁽¹⁾ If the SDM processor is busy, the response time may be longer.

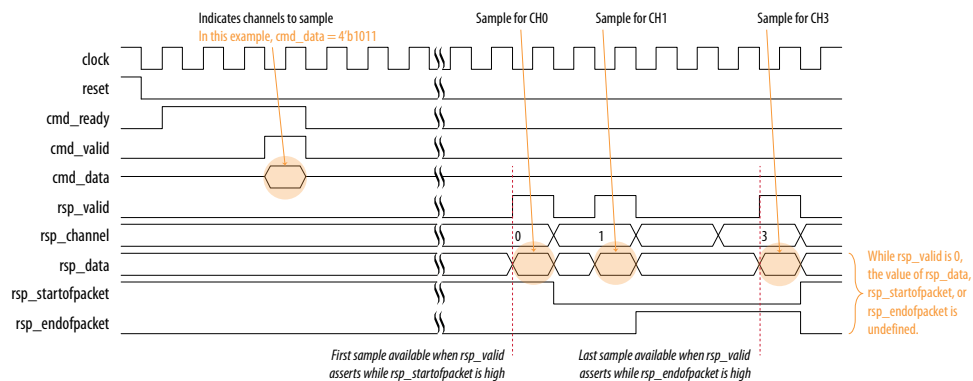


- [Voltage Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 15
Provides the list of voltage sensor signals and descriptions.
- [Intel Stratix 10 Voltage Sensor](#) on page 4
- [Voltage Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 15
Provides more information about the command and response signals of the Voltage Sensor IP core.

4.2. Reading the Intel Stratix 10 Internal Temperature Sensing Diodes

To sample the Intel Stratix 10 die temperature using the internal TSDs of the core fabric, transceiver tiles, and HBM2 stacks, use the Temperature Sensor IP core.

Figure 7. Waveform Example: Sampling Temperature from Channels 0, 1, and 3



Note: Set only valid bits in the `cmd_data` word. Otherwise, the response from the temperature sensor is undefined.

1. During device initialization, before the device enters user mode:
 - Assert the `reset` port of the Temperature Sensor IP core to keep it in reset mode.
 - Keep the `cmd_valid` and `cmd_data` signal at "0".

2. After the device enters user mode, simultaneously assert a logic high to the `cmd_valid` signal and send the `cmd_data` value. For each sampling, assert `cmd_valid` for a period of only one to three clock cycles. When you are not acquiring the temperature sensor readout, deassert `cmd_valid`.

The `cmd_data` signal is a 9-bit bitmask that specifies from which channel to sample the temperature.

When you assert `cmd_valid` while `cmd_ready` is high, the IP core requests from the SDM the most recent temperature values of the channels you specify in `cmd_data`. After sending the request, the IP core drives `cmd_ready` low and waits for response from the SDM.

3. Each time the `rsp_valid` signal goes high, indicating that the temperature value is ready, read the `rsp_data` and `rsp_channel` response signals.

The `rsp_valid` signal goes high once for each bit in the `cmd_data` word. The first valid data in the cycle is available when `rsp_valid` asserts while the `rsp_startofpacket` signal is high. The last valid data in the cycle is available when `rsp_valid` asserts while the `rsp_endofpacket` signal is high. For each valid response, the `rsp_data` signal provides the temperature value while the `rsp_channel` signal indicates from which channel the temperature was sampled.

The value in `rsp_data` is a signed 32-bit fixed point binary number, with 8 bits below the binary point.

Related Information

- [Temperature Calculation for the Internal Temperature Sensor](#) on page 6
- [Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 16
Provides more information about the command and response signals of the Temperature Sensor IP core.
- [Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals](#) on page 16
Provides the list of temperature sensor signals and descriptions.
- [Internal Temperature Sensor](#) on page 6

5. Intel Stratix 10 ADC IP Core References

The Voltage Sensor or Temperature Sensor IP core does not have configurable parameter options. After you generate and add the IP core to your design, use the digital signal interface of the IP core to access the voltage or temperature readouts.

5.1. Voltage Sensor Intel Stratix 10 FPGA IP Digital Signals

These signals are the operational signals of the Voltage Sensor IP core. The command and response interfaces are Avalon Streaming (Avalon-ST) interfaces with ready latency of 0.

Figure 8. Voltage Sensor IP Core

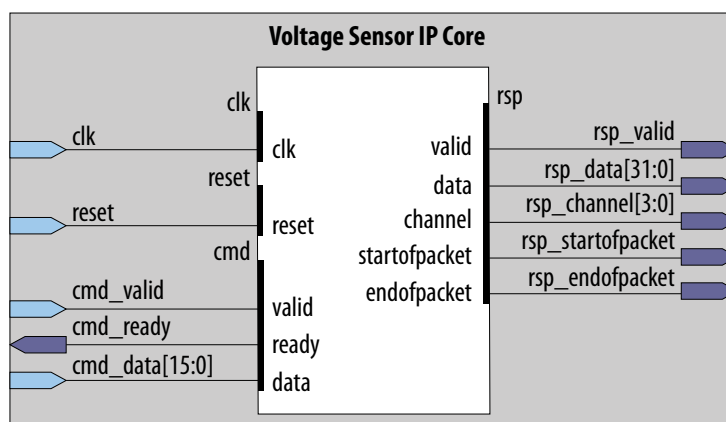


Table 2. Clock and Reset Signals

Signal	Width (Bit)	Type	Description
clk	1	Input	All signals in the IP core is synchronous to this clock. The frequency supported for this clock is from 10 MHz to 100 MHz.
reset	1	Input	Active high reset. Deassert this signal synchronous to the clock.

Table 3. Command Signals

Signal	Width (Bit)	Type	Description
cmd_valid	1	Input	Assert this signal high to send voltage sampling request to the IP core.
cmd_ready	1	Output	The IP core drives this signal high to indicate that the IP core is ready to receive command.
cmd_data	16	Input	<p>Bitmask to indicate from which channel to return the voltage value. Send this data signal together with the cmd_valid signal.</p> <ul style="list-style-type: none"> Bit 0 to 1—sample the external voltage values from the specified analog input channels. Bits 2 to 15—sample the internal voltage values from the specified channels. <p>For example, 0000001000010001 signals the IP core to sample the voltage values from channels 0, 4, and 9. Set only valid bits in the cmd_data word. Otherwise, the response from the voltage sensor is undefined.</p>

Table 4. Response Signals

Signal	Width (Bit)	Type	Description
rsp_valid	1	Output	Indication from the IP core that the voltage value is ready.
rsp_channel	4	Output	Indicates the channel of the voltage value sampled from the analog inputs or internal supplies.
rsp_data	32	Output	The voltage value in a signed 32-bit fixed-point binary format, with 16 bits below the binary point.
rsp_startofpacket	1	Output	Indicates that the current transfer is the start of packet.
rsp_endofpacket	1	Output	Indicates that the current transfer is the end of packet.

Related Information

- [Voltage Conversion](#) on page 5
- [Sampling the Intel Stratix 10 Voltage Sensor Channels](#) on page 11
Provides the steps to read the voltage values and the timing diagram.
- [Intel Stratix 10 Voltage Sensor](#) on page 4
Provides a list of channel numbers and the supply voltages the ADC monitors.

5.2. Temperature Sensor Intel Stratix 10 FPGA IP Digital Signals

These signals are the operational signals of the Temperature Sensor IP core. The command and response interfaces are Avalon Streaming (Avalon-ST) interfaces with ready latency of 0.



Figure 9. Temperature Sensor IP Core

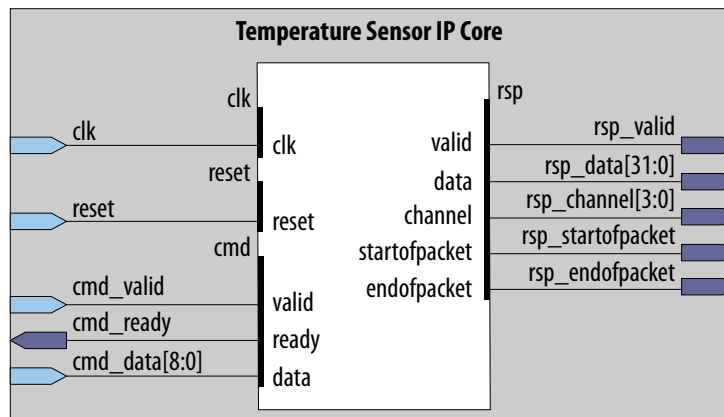
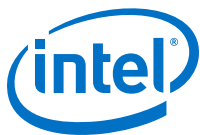


Table 5. Clock and Reset Signals

Signal	Width (Bit)	Type	Description
clk	1	Input	All signals in the IP core is synchronous to this clock. The frequency supported for this clock is from 10 MHz to 100 MHz.
reset	1	Input	Active high reset. Deassert this signal synchronous to the clock.

Table 6. Command Signals

Signal	Width (Bit)	Type	Description
cmd_valid	1	Input	Assert this signal high to send temperature sampling request to the IP core.
cmd_ready	1	Output	The IP core drives this signal high to indicate that the IP core is ready to receive command.
cmd_data	9	Input	<p>Bitmask to indicate from which channel to return the temperature. Send this data signal together with the cmd_valid signal.</p> <ul style="list-style-type: none"> Bit 0—sample the temperature value from the internal TSD in the core fabric. Bits 1 to 6—sample the temperature values from internal TSDs in the transceiver tiles. Bits 7 and 8—sample the temperature values from internal TSDs in the HBM2 stacks. <p>For example, 0000101 signals the IP core to sample the temperature values from channel 0 (core fabric) and channel 2 (bank 6B).</p> <p>For the designated temperature sensor channel number of each transceiver tile and HBM2 stacks, refer to the related information.</p> <p>Set only valid bits in the cmd_data word. Otherwise, the response from the temperature sensor is undefined.</p> <p><i>Note:</i> The availability of the internal TSD channels varies among Intel Stratix 10 devices and packages.</p>

**Table 7. Response Signals**

Signal	Width (Bit)	Type	Description
rsp_valid	1	Output	Indication from the IP core that the temperature value is ready.
rsp_channel	4	Output	Indicates the channel of the temperature value sampled from the core fabric or transceiver tile.
rsp_data	32	Output	The temperature value in a signed 32-bit fixed-point binary format, with 8 bits below the binary point. A value of 0x80000000 indicates invalid data.
rsp_startofpacket	1	Output	Indicates that the current transfer is the start of packet.
rsp_endofpacket	1	Output	Indicates that the current transfer is the end of packet.

Related Information

- [Temperature Calculation for the Internal Temperature Sensor](#) on page 6
- [Reading the Intel Stratix 10 Internal Temperature Sensing Diodes](#) on page 13
Provides the steps to read the temperature values and the timing diagram.
- [Temperature Sensor Channels and Locations](#) on page 7



6. Intel Stratix 10 Analog to Digital Converter User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.0	Intel Stratix 10 Analog to Digital Converter User Guide
17.1	Intel Stratix 10 Analog to Digital Converter User Guide

7. Document Revision History for the Intel Stratix 10 Analog to Digital Converter User Guide

Document Version	Intel Quartus Prime Version	Changes
2018.11.05	18.1	<ul style="list-style-type: none"> Updated the topic about the Intel Stratix 10 ADC architecture and features to improve clarity. Removed external V_{REF} support for the Intel Stratix 10 voltage sensor: <ul style="list-style-type: none"> Removed the <code>VREFP_ADC</code> and <code>VREFN_ADC</code> pins from the Intel Stratix 10 voltage sensor diagram. Removed the guideline topic about connecting external voltage reference to the Intel Stratix 10 ADC voltage reference pins. Updated the Intel Stratix 10 voltage sensor diagram: <ul style="list-style-type: none"> Updated communication between the blocks labeled "SDM" and "Voltage Sensor IP Core" to bidirectional. Updated the legend for the shared pin to clarify that the pin is shared with the device, not the GPIO. Updated the topic about the Intel Stratix 10 voltage sensor: <ul style="list-style-type: none"> Specified that the ADC samples the voltage at regular intervals. Updated the maximum value of the external analog signal from 1.25 V to 1.24 V. Updated the topic about the Intel Stratix 10 internal temperature sensor to specify that the ADC samples the voltage at regular intervals. Updated the topic that lists the temperature sensor channels and locations to clarify that you specify the internal TSD channels to sample through the <code>cmd_data</code> signal. Updated the ADC implementation guides topic to clarify that you only need to instantiate one instance of the IP core and interact with it using its digital signal interface.
2018.07.19	18.0	<ul style="list-style-type: none"> Removed the word "speed" from the note about the clock source to the Temperature Sensor IP core in the topic about the internal temperature sensor. You can use any clock source between 10 MHz to 100 MHz. Updated the steps for sampling the voltage sensor and reading the internal temperature sensor. The updated steps clarify that you must keep the Voltage Sensor or Temperature Sensor IP core in reset mode during device initialization until the device enters user mode.
2018.05.07	18.0	<ul style="list-style-type: none"> Updated the IP names from "Intel FPGA S10 Voltage Sensor" and "Intel FPGA S10 Temperature Sensor" to "Voltage Sensor Intel® Stratix 10 FPGA IP" and "Temperature Sensor Intel® Stratix 10 FPGA IP". Added information about transceiver tile's internal and external TSD availability when the tile is powered down. Added support for temperature sensors in the HBM2 stacks. Updated the diagram and description to identify the location and availability of the TSDs by using transceiver bank numbers instead of 3 V I/O bank numbers. Updated the table listing the internal TSD channels and external TSD pins to improve clarity.
continued...		



Document Version	Intel Quartus Prime Version	Changes
		<ul style="list-style-type: none"> Updated the topics describing the steps to access the voltage and temperature sensor readouts: <ul style="list-style-type: none"> Added steps to perform during device initialization. Removed mentions of "continuous sampling" and specified that you must assert <code>cmd_valid</code> only for one to three clock cycles. Updated the introduction for the Intel Stratix 10 ADC IP core reference section. Updated the frequency supported by the <code>clk</code> signal of the ADC IP cores from 250 MHz to a range of 10 MHz to 100 MHz. Added the <code>rsp_data</code> response value that indicates invalid data.

Date	Version	Changes
November 2017	2017.11.06	<ul style="list-style-type: none"> Added support for external temperature sensors. Restructured the document, updated content, and added topics to support the external temperature sensors feature. Added board design guidelines for connecting external voltage reference sources to the ADC V_{REF} pins. Updated the waveform examples to improve clarity.
May 2017	2017.05.08	<ul style="list-style-type: none"> Updated the topic about the voltage sensor to specify that the voltage sensor monitors two external voltages and only five internal power supplies. Updated the timing diagrams and descriptions in the topics about sampling the voltage and temperature sensors to improve clarity. Updated <code>cmd_data</code> width in the Temperature Sensor IP core block diagram from 6 bits to 7 bits. Updated the description of <code>cmd_data</code> to specify that invalid bits cause undefined response data from the sensors. Updated the temperature sensor channels location figure with 3 V I/O bank numbers to identify in which transceiver tile the sensor is located.
February 2017	2017.02.13	<ul style="list-style-type: none"> Updated the Voltage Sensor and Temperature Sensor IP cores block diagrams to improve clarity. Updated the topic about temperature calculation to clarify about the values returned by the temperature sensors in the transceiver tiles. Updated the topics about sampling the voltage sensor and temperature sensor channels to improve clarity. Updated the temperature sensor <code>cmd_data</code> bitmask signal from 6 bits to 7 bits. Updated the maximum supported frequency of the Temperature Sensor and Voltage Sensor IP cores clock input to be equivalent to the system clock. Added a topic showing the temperature sensor locations and channel numbers. Updated the topics listing the Voltage Sensor and Temperature Sensor IP cores signals.
December 2016	2016.12.05	Updated the tables listing the clock and reset signals for the Voltage Sensor and Temperature Sensor IP cores.
October 2016	2016.10.31	Initial release.