Stratix 10 SoC FPGA Development Kit Board

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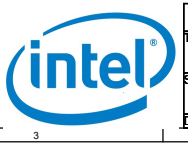
REV	DATE	PAGES	DESCRIPTION
0.1		All	INITIAL REVISION A RELEASE
A.0 release		All	Power/SI/Mechanical Test Board Release
A.1 release		25	Add FGPA dedicated I2C port to Optical Module
		21,22	Move signal FALAP17 to FPGA clock input pin
		7	Add Header to select USB blaster code
		25	Move signal FBLAP17 to FPGA clock input pin
		28	SWAP byte assignment of FGPA DDR ports.
		15	C185 to 1uf
		35	R851 value is changed to 17.4K. Wrong connection of C1614
		27	Change C249 decoupling to VDD
			Add more Power test pins
		28	Change Memory IO connection for I J K L
		10,11	Sepearte case gnd and signa gnd
		10,11	Change R63, R87 to 4.7K
		12	Update U13 Symbol
		15	ADD U18 I2C Address
		21	Fix Signal PN connections
		22	Fix Signal PN connections, add dedicated I2C ports for clock cleaner and QSFP+ ports
		25	Add dedicated I2C ports for Video and SFP ports
		30	Change JTAG_RESET to DC Power good
		31	Add pull down resistor
		36	Change AC coupling cap from 4.7uf to 0.1uf
		42	Fix Signal PN connections. Change J56 from 2-pin to 3-pin
		46	Short A-GND to Signal GND



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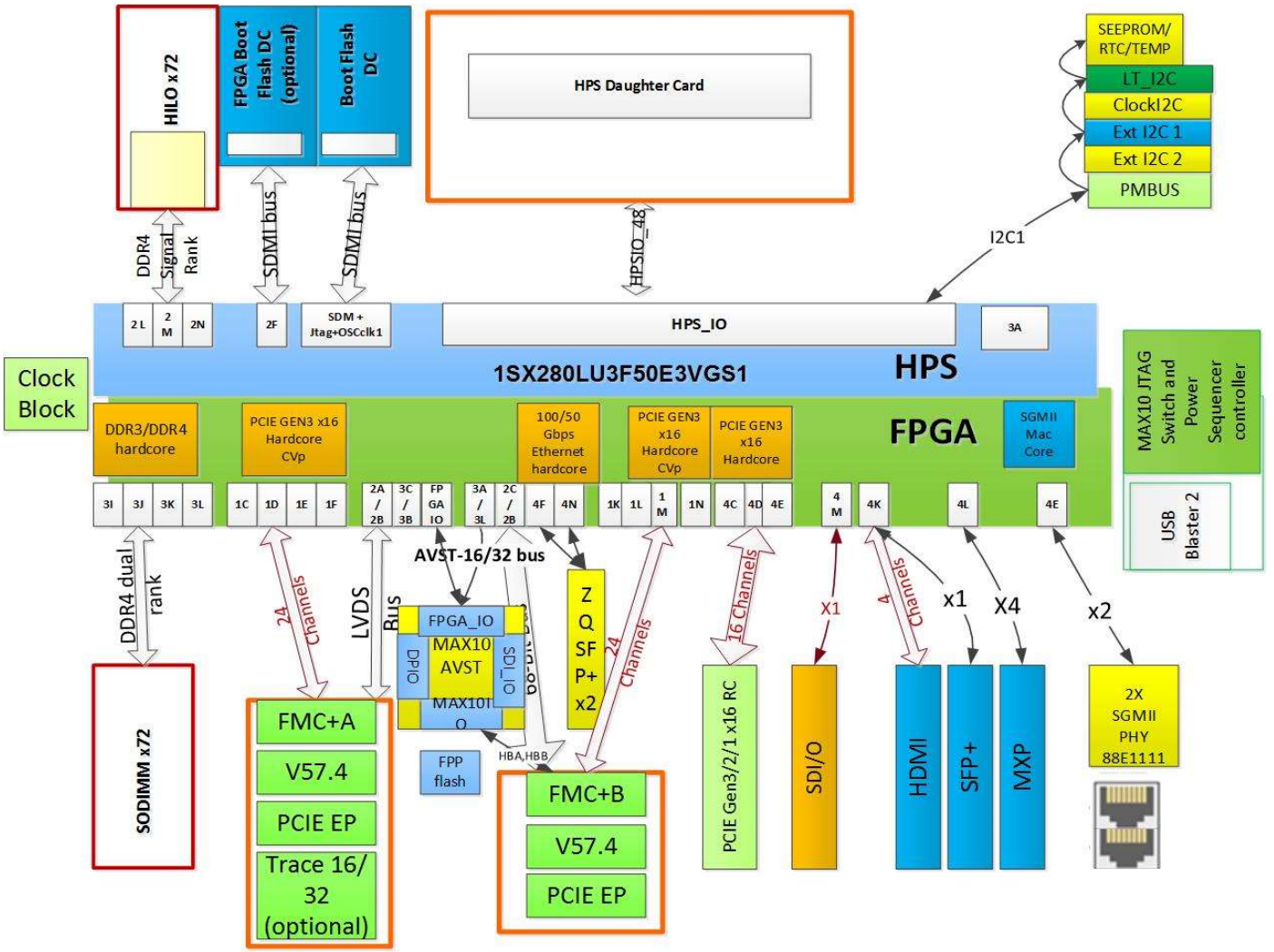
Stratix 10 Dev Kit Block Diagram



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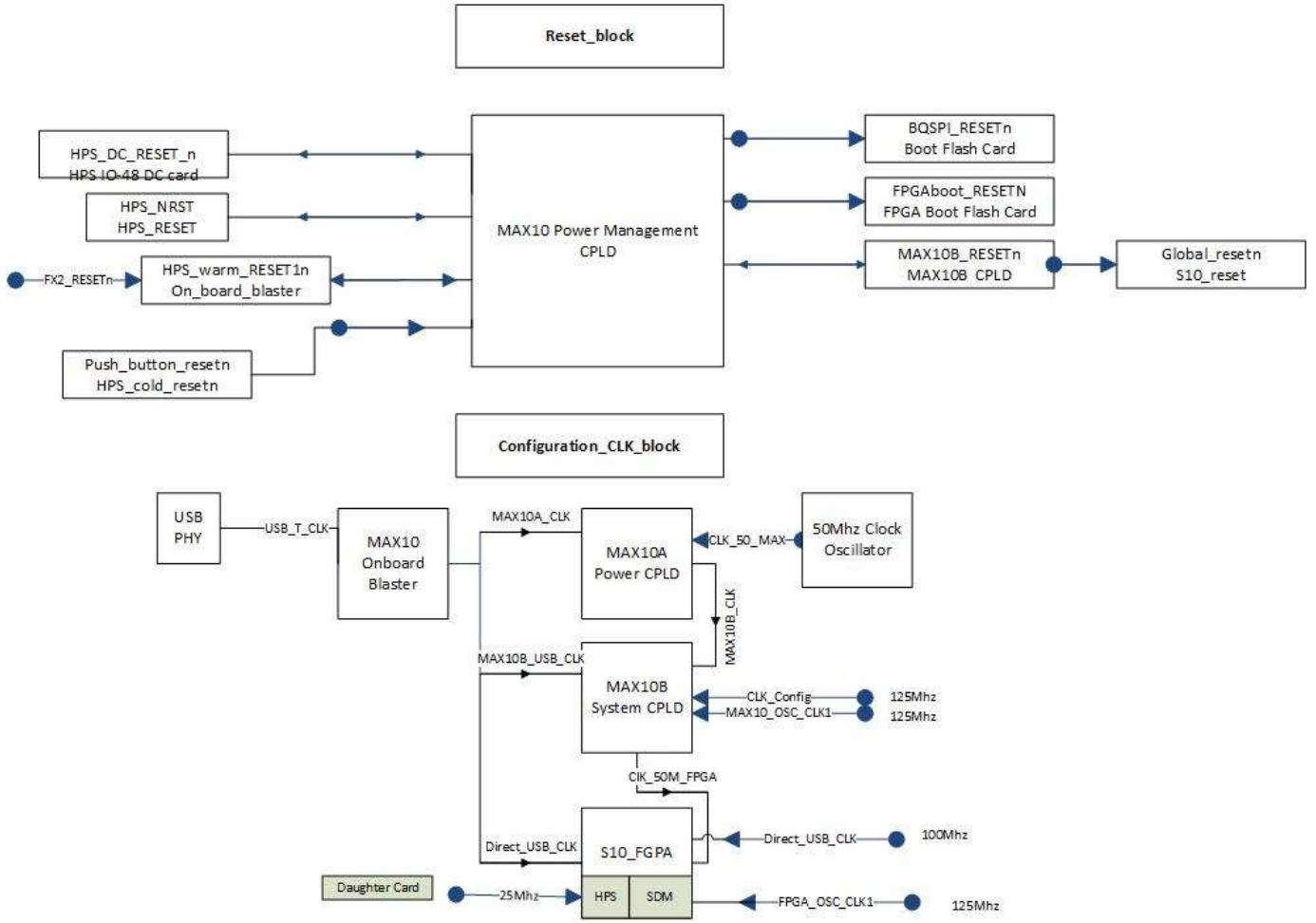
S10soc Dev Kit Reset Block



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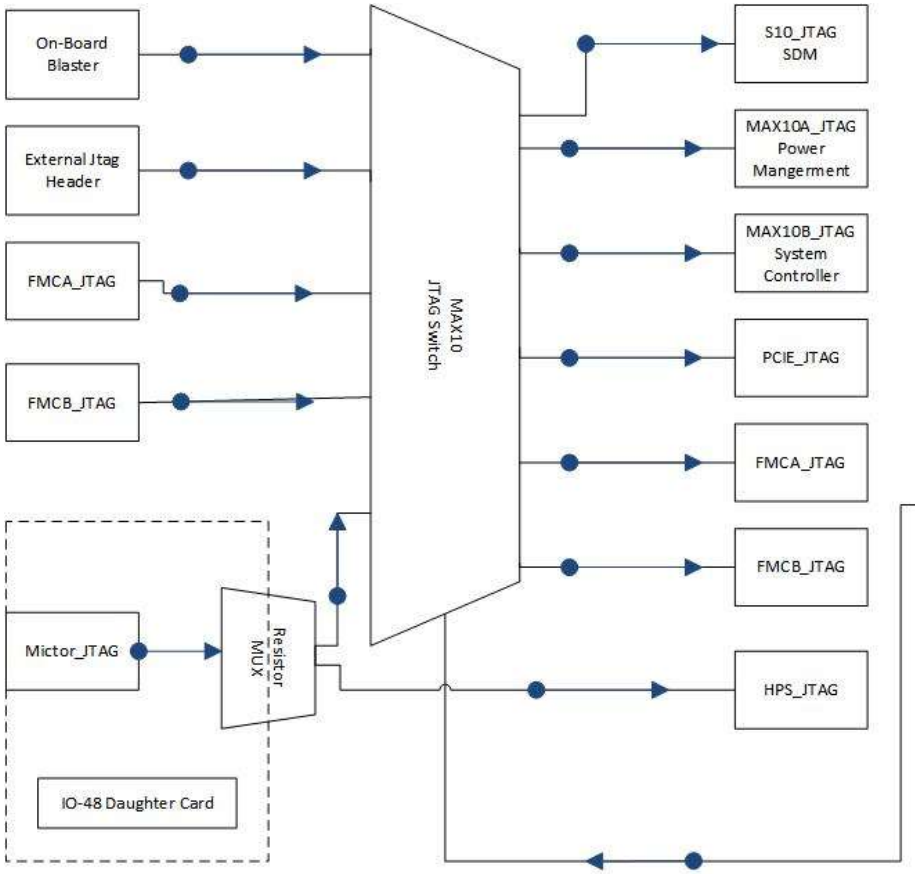
JTAG Connection Diagram



JTAG Selection Switch

8-bit	Dipswitch
Bit 1:	S10_Bypass
Bit 2:	M10B_Bypass
Bit 3:	FMCA_Bypass
Bit 4:	FMCB_Bypass
Bit5:	PCIE_Bypass
Bit6:	MSTR0
Bit7:	MSTR1
Bit8:	MSTR2

MSTR2, MSTR1,MSTR0	Mod
ON, ON, ON	Boot
OFF ON ON	FMCA Master
ON OFF ON	FMCB Master
OFF OFF ON	Reserved
ON ON OFF	Reserved
OFF ON OFF	GUI Test
ON OFF OFF	MAX10A program
OFF OFF OFF	On board Blaster

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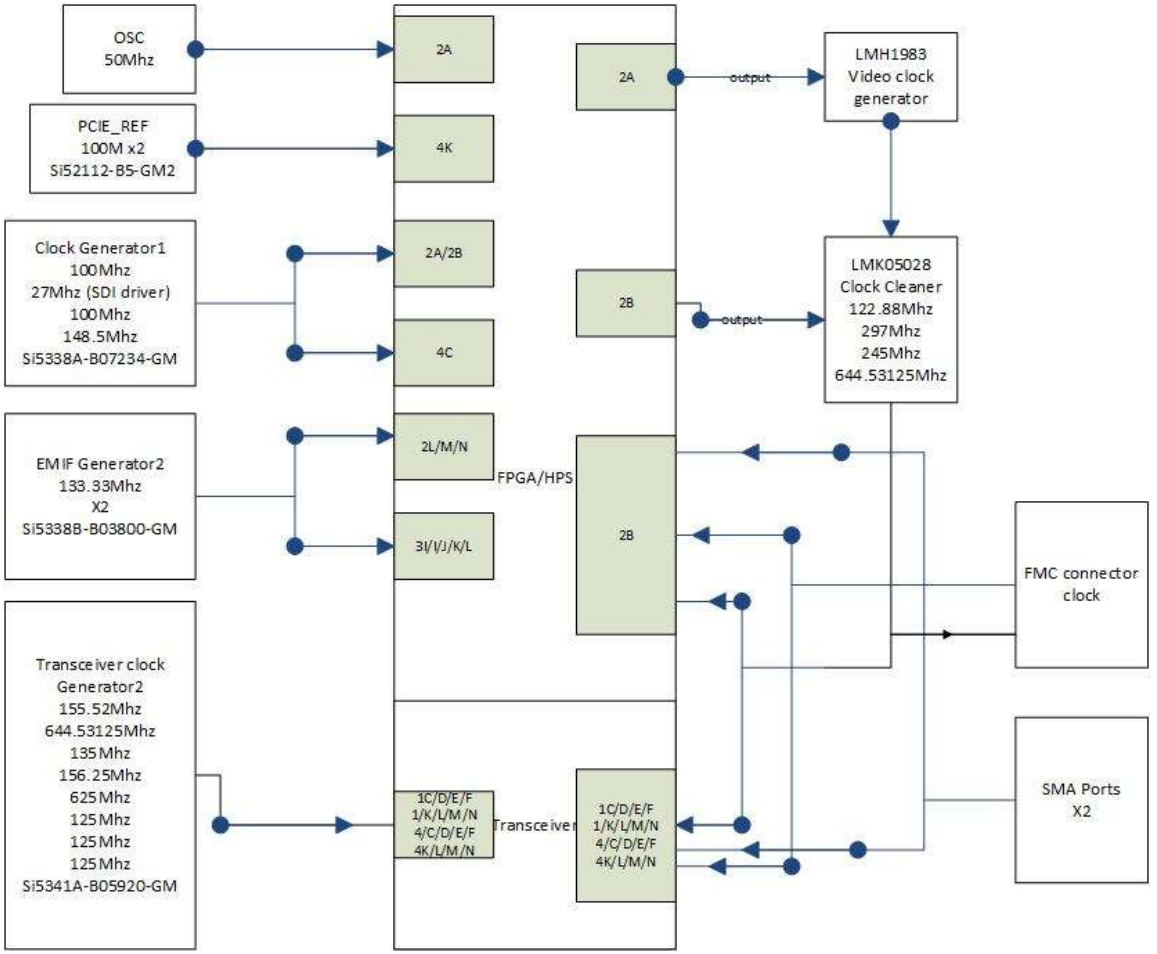
Stratix 10 Dev Kit Clock Connection



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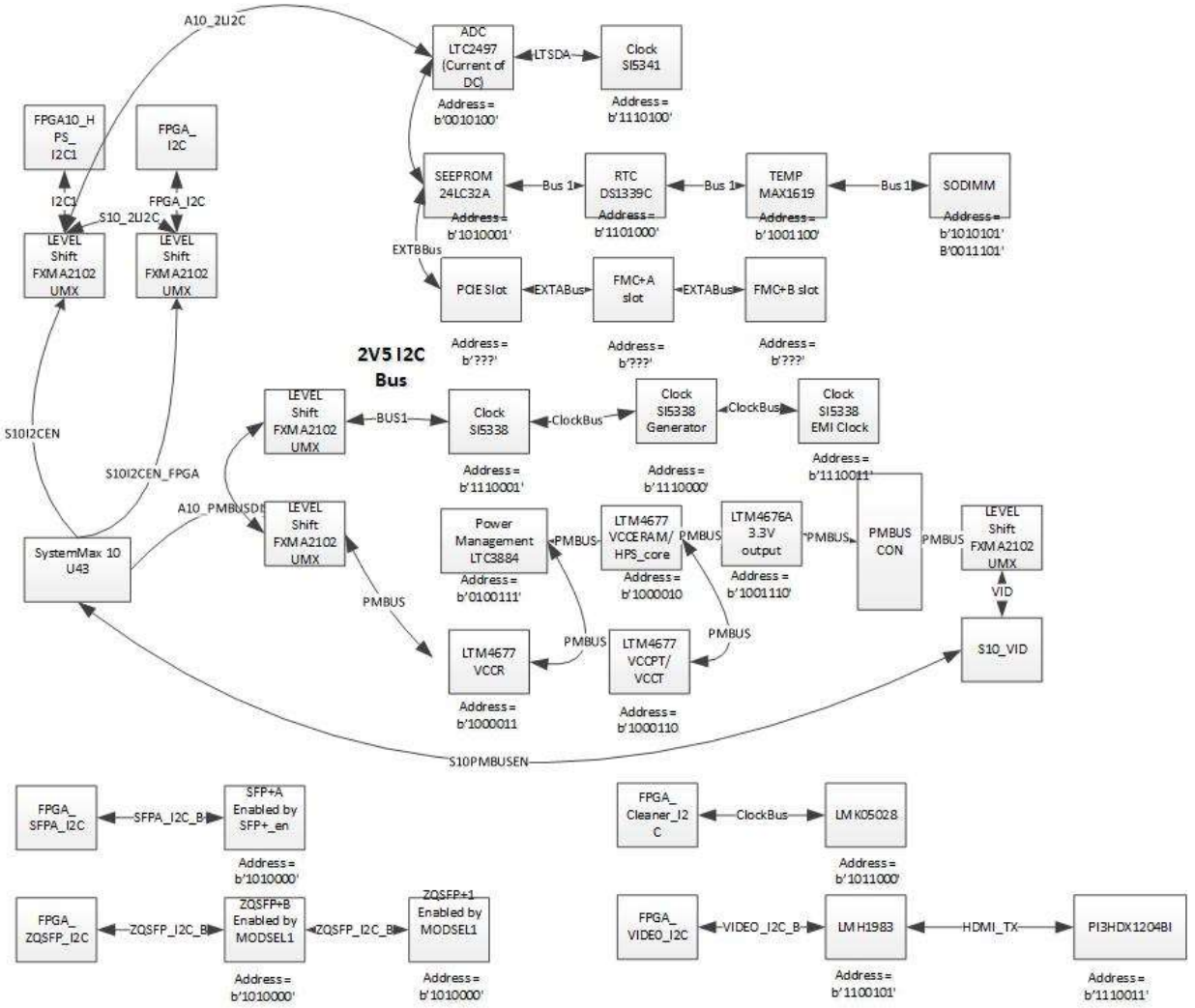
Stratix 10 Dev Kit I2C bus Connection



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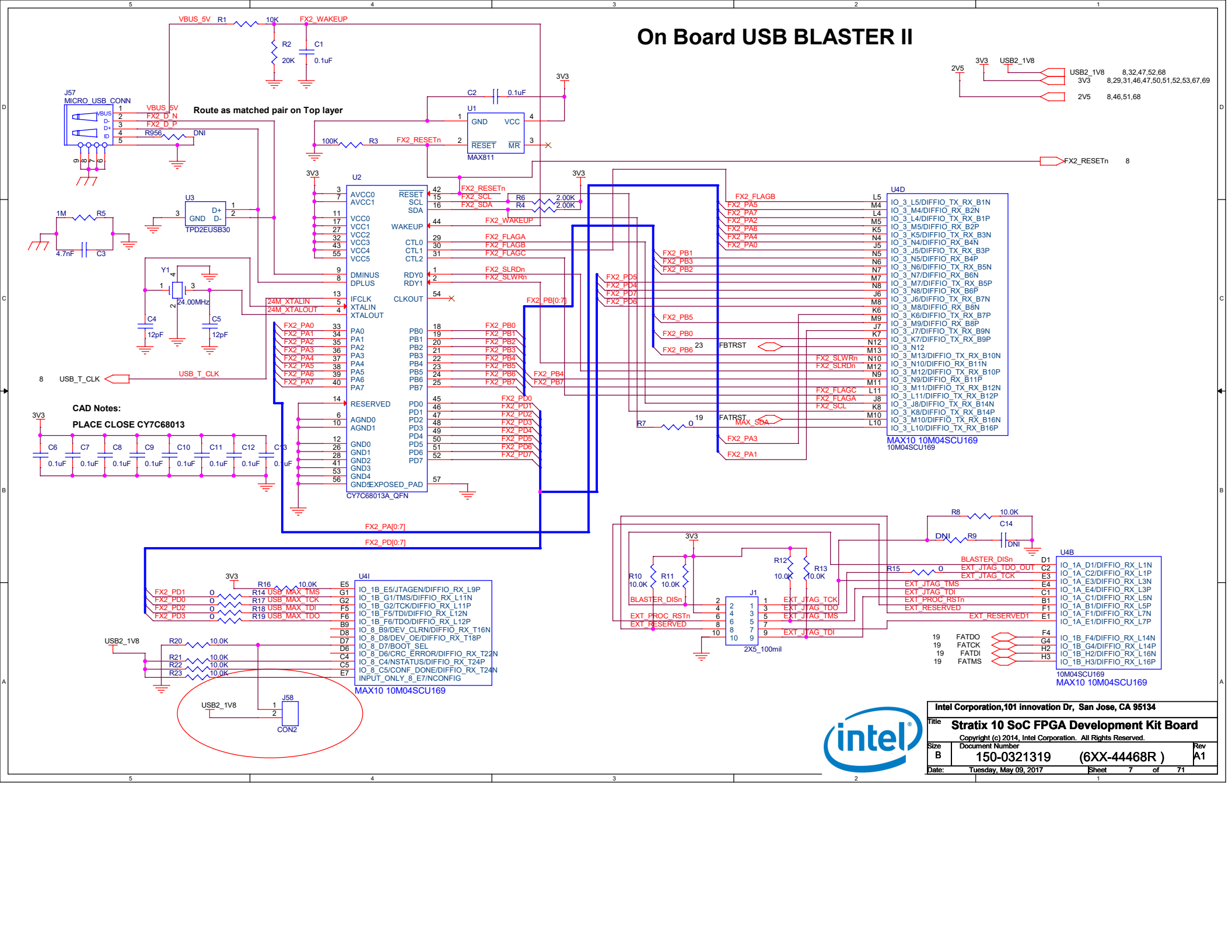
On Board USB BLASTER II



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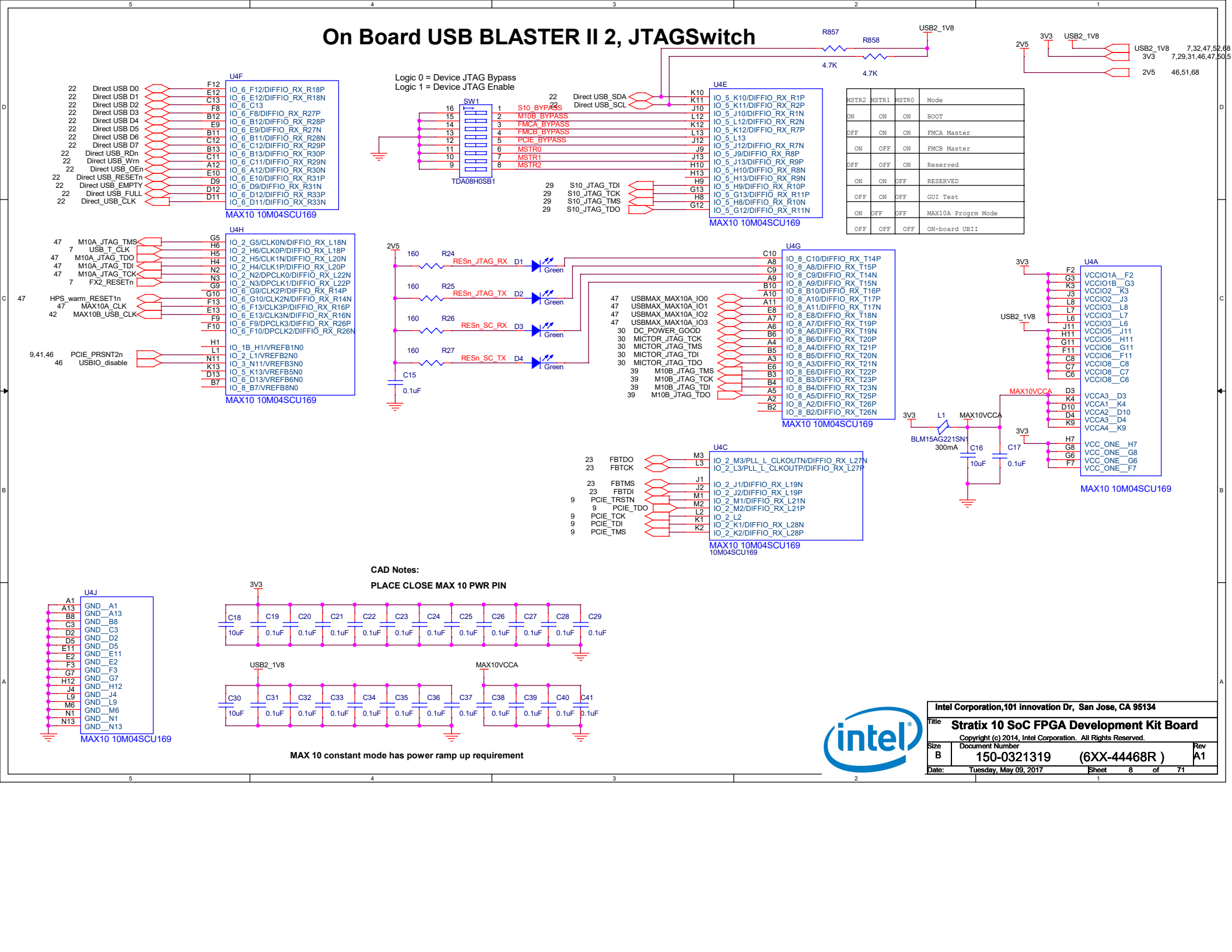
On Board USB BLASTER II 2, JTAGSwitch



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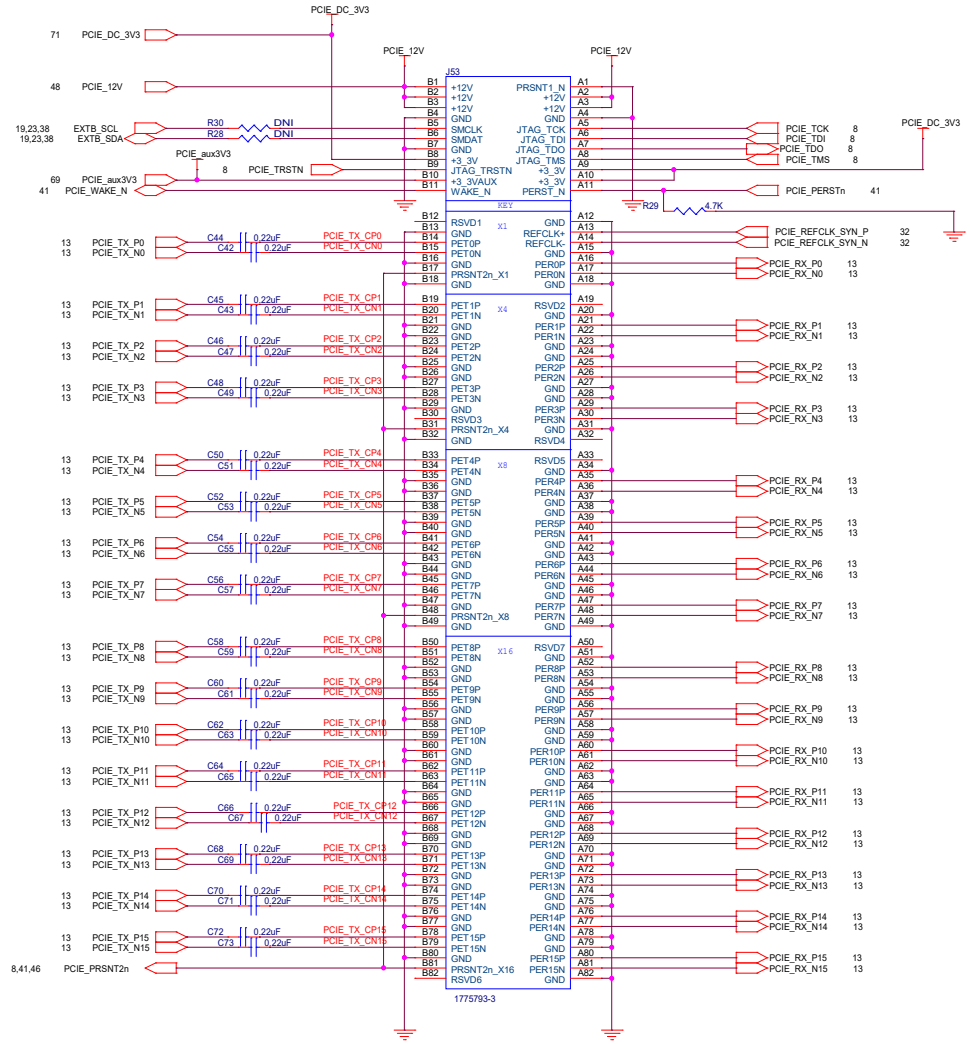
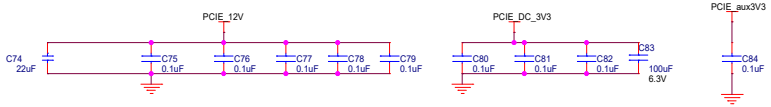
PCI Express GEN3 X 16 Connector



75-ohm to 100-ohm XCVR traces.



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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

DVDD = 1.0V
DVDD = 1.2V

ENET_DVDD = 1.0V/0.207A

SGMII Mode (default)

Place near 88E1111 PHY

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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
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CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

SGMII Mode (default)

Place near 88E1111 PHY

DVDD = 1.0V
DVDD = 1.2V

ENET_DVDD = 1.0V/0.207A

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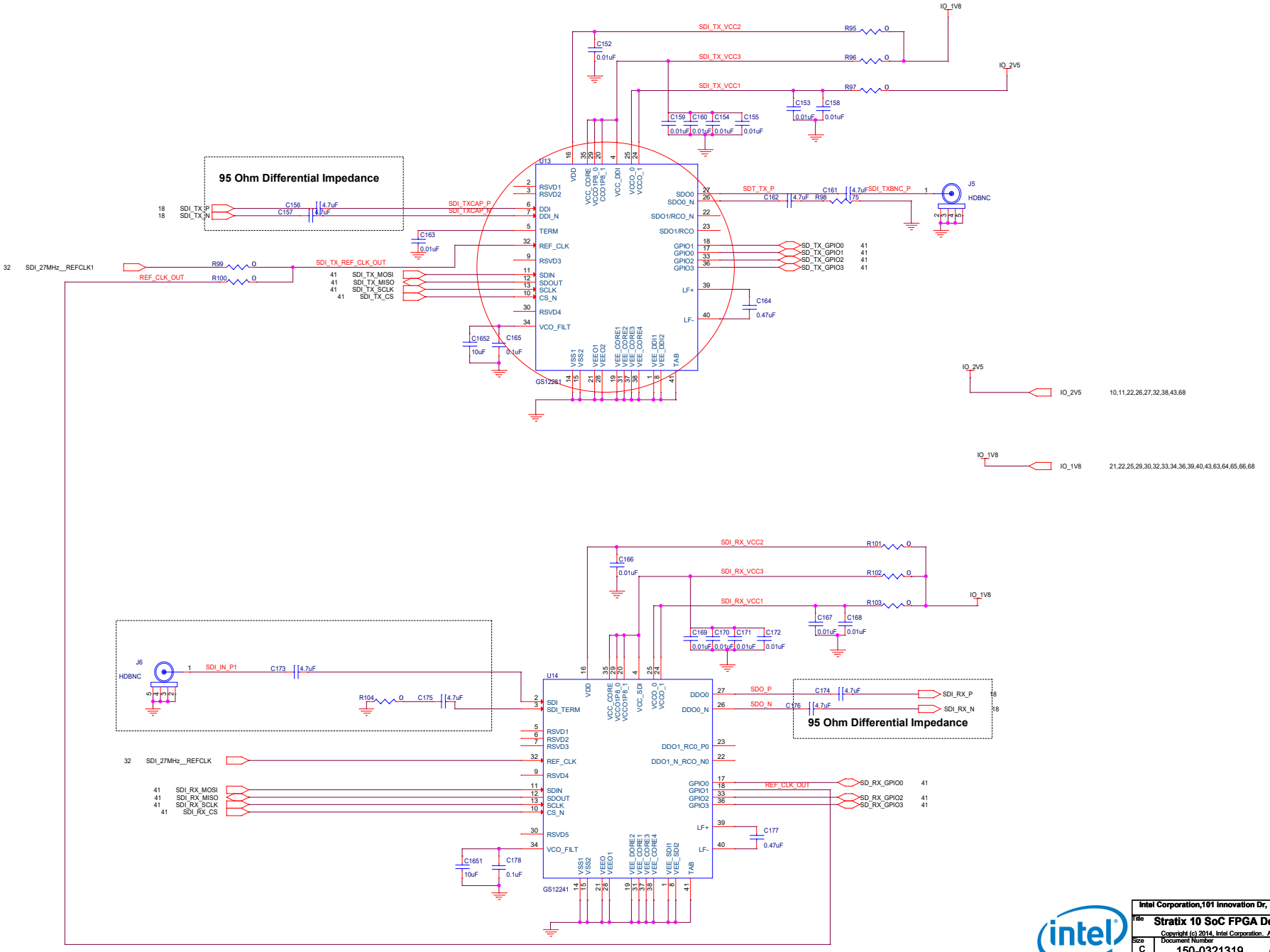
SDI Cable Driver, Equalizer, and SMB



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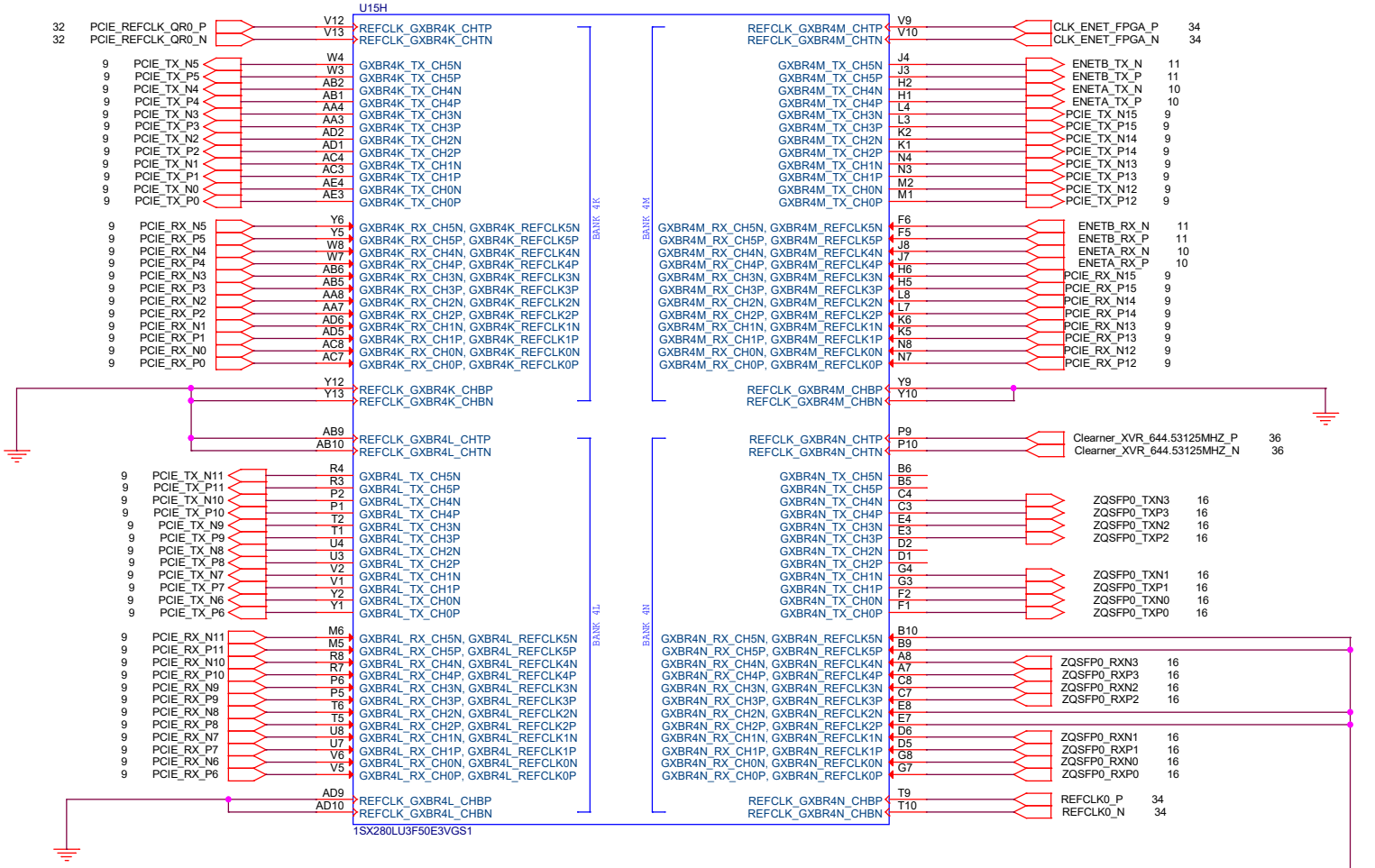
Stratix 10 XCVR Banks - 4K/L/M/N



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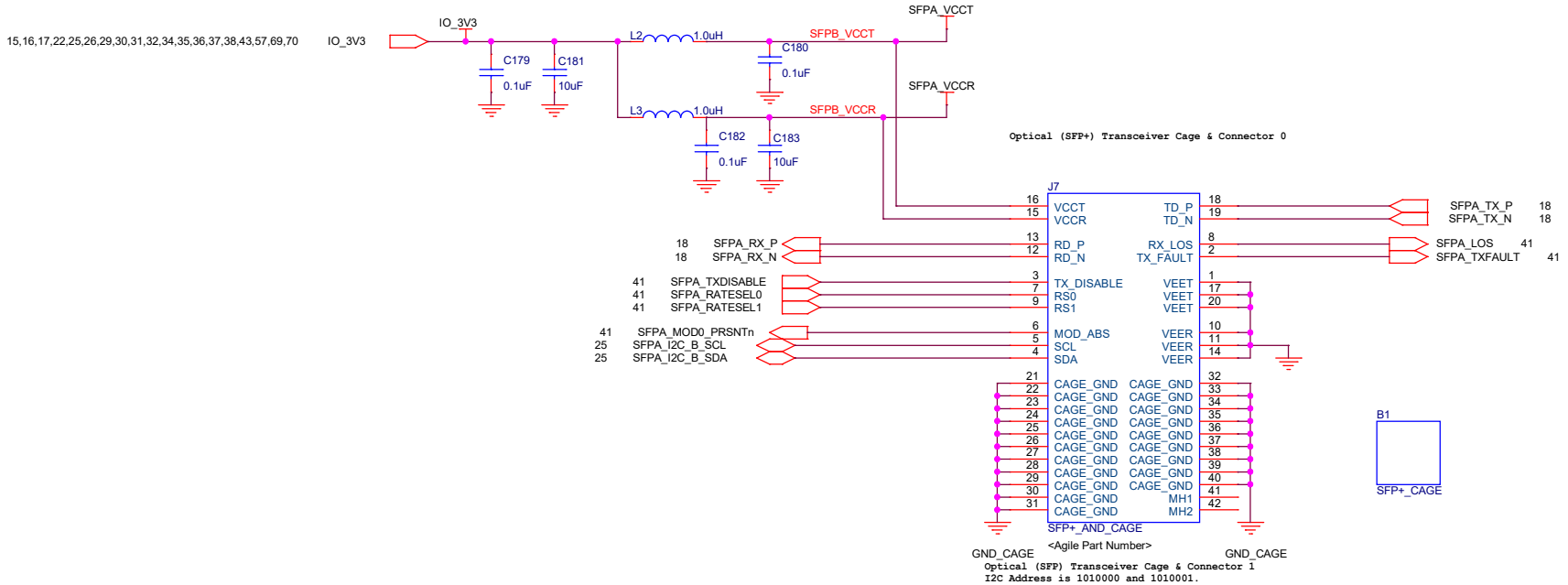
Small Form Factor Pluggable Plus (SFP+) Port A



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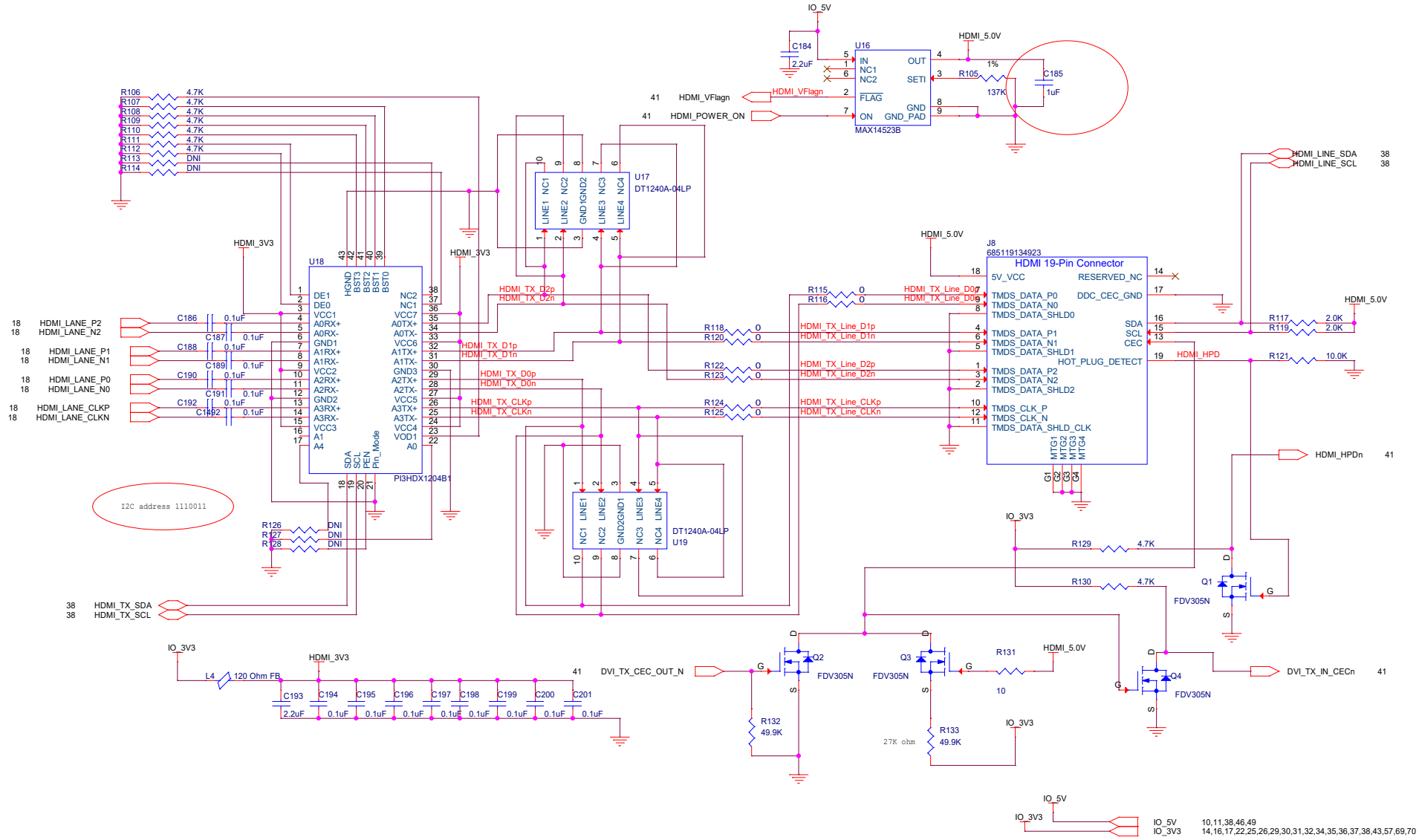
HDMI (VIDEO ONLY)



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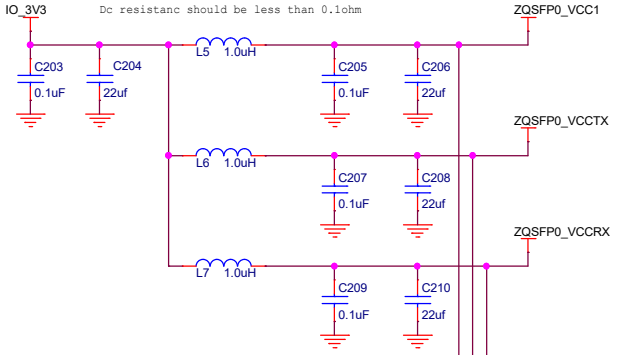
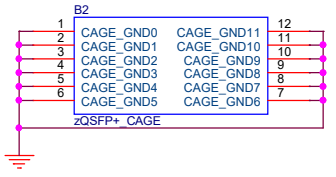
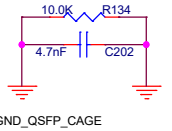
QSFP28 Interface 0 & MXP Cable connection

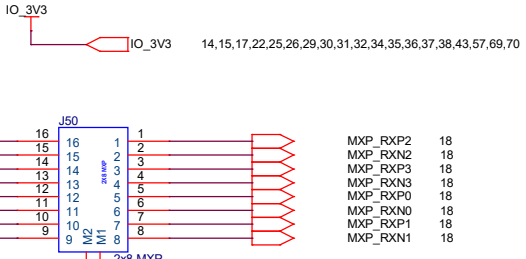


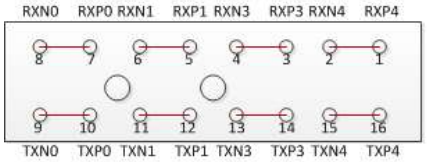
P and N can be swapped for better SI performance



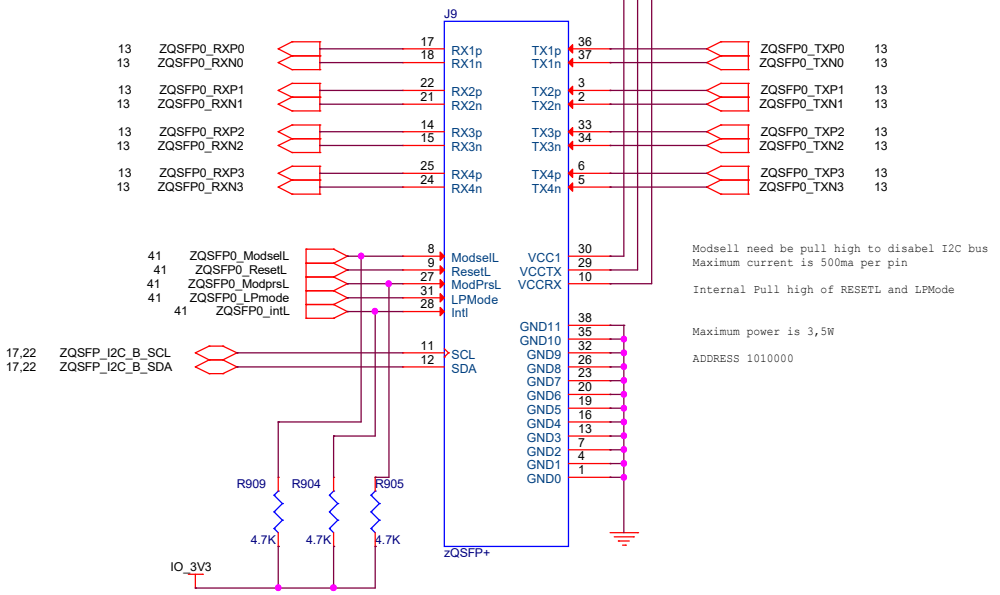


Cage GND on top layer





QSFP28 Interface



Modsell need be pull high to disabel I2C bus
Maximum current is 500ma per pin

Internal Pull high of RESETL and LPMode

Maximum power is 3,5W

ADDRESS 1010000

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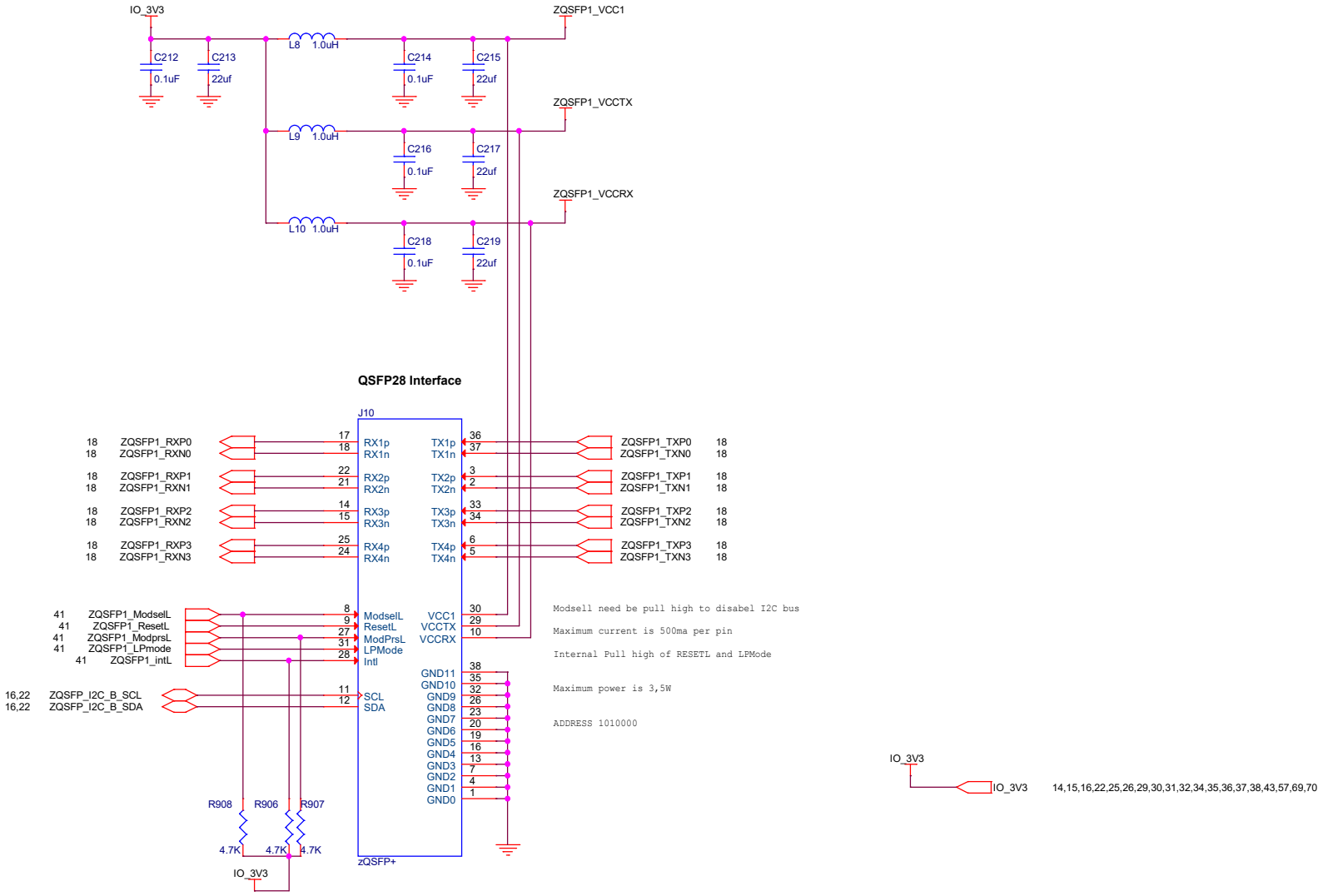
QSFP28 Interface 1

Dc resistanc should be less than 0.1ohm



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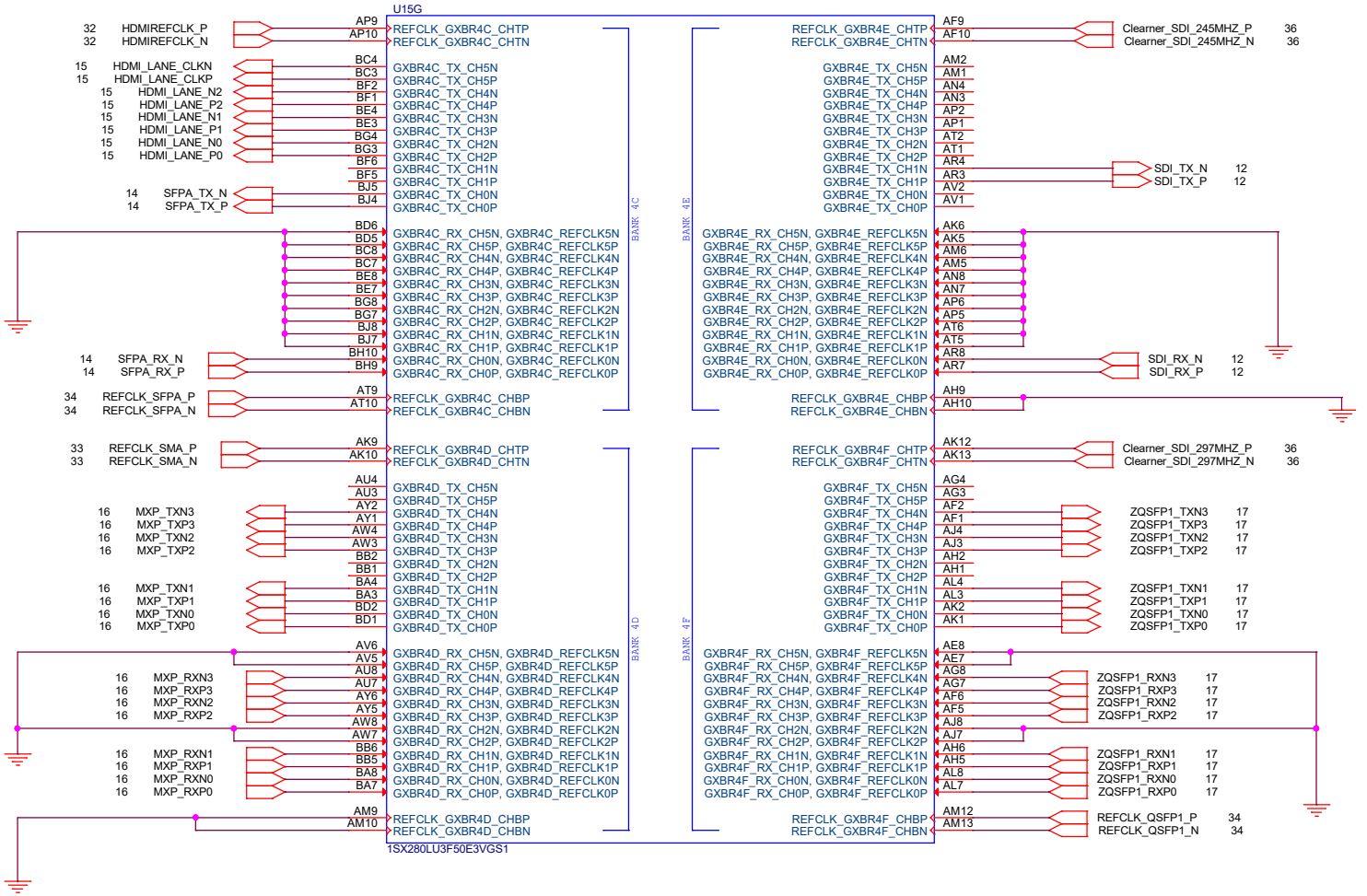
S10 XCVR Banks - 4C/D/E/F



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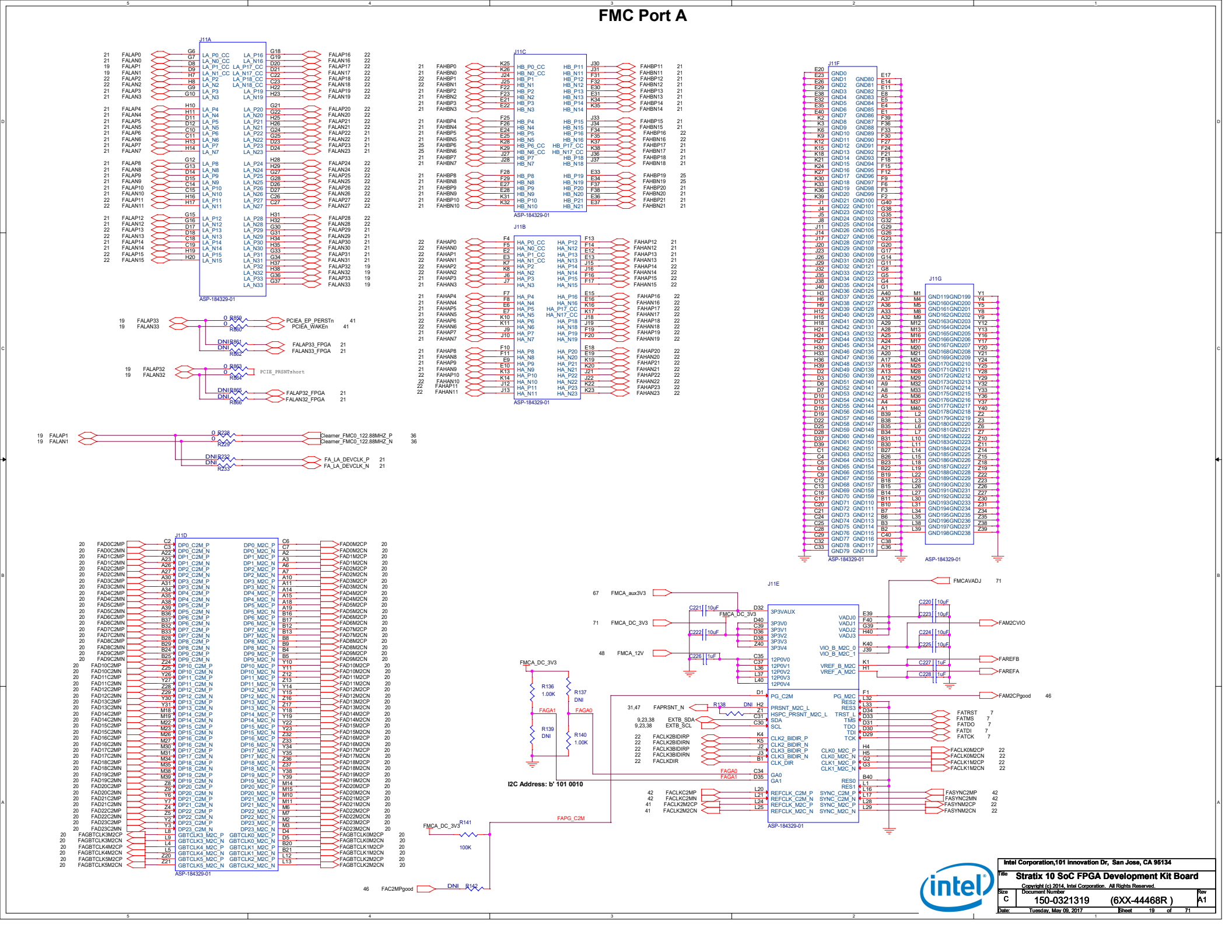
FMC Port A


J11A
ASP-184329-01
J11C
ASP-184329-01
J11B
ASP-184329-01
J11F
ASP-184329-01
J11G
ASP-184329-01
J11D
ASP-184329-01
J11E
ASP-184329-01
I2C Address: b' 101 0010
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Size C
Document Number 150-0321319 (6XX-44668R)
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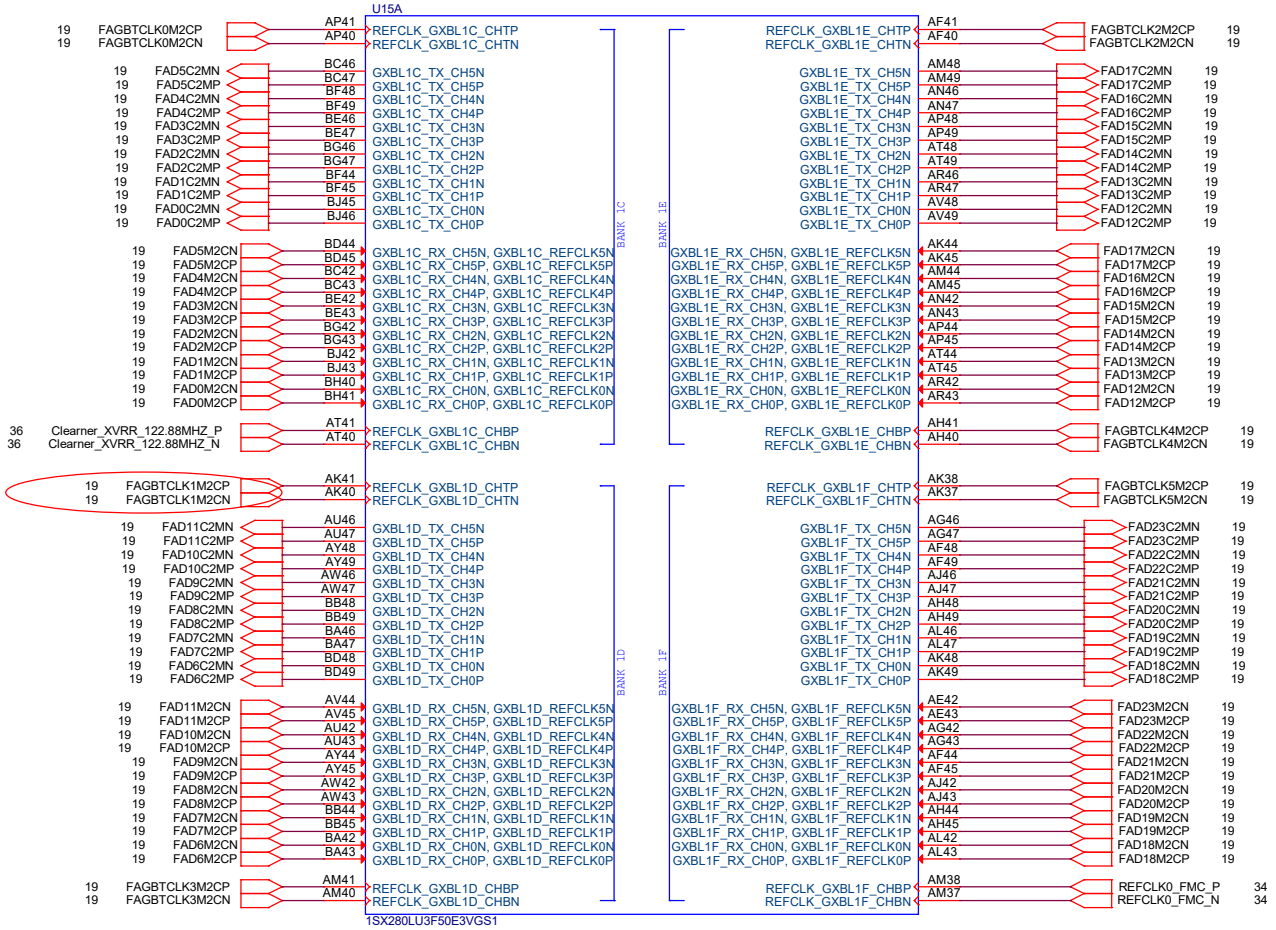
Stratix 10 XCVR Banks - 1C/D/E/F



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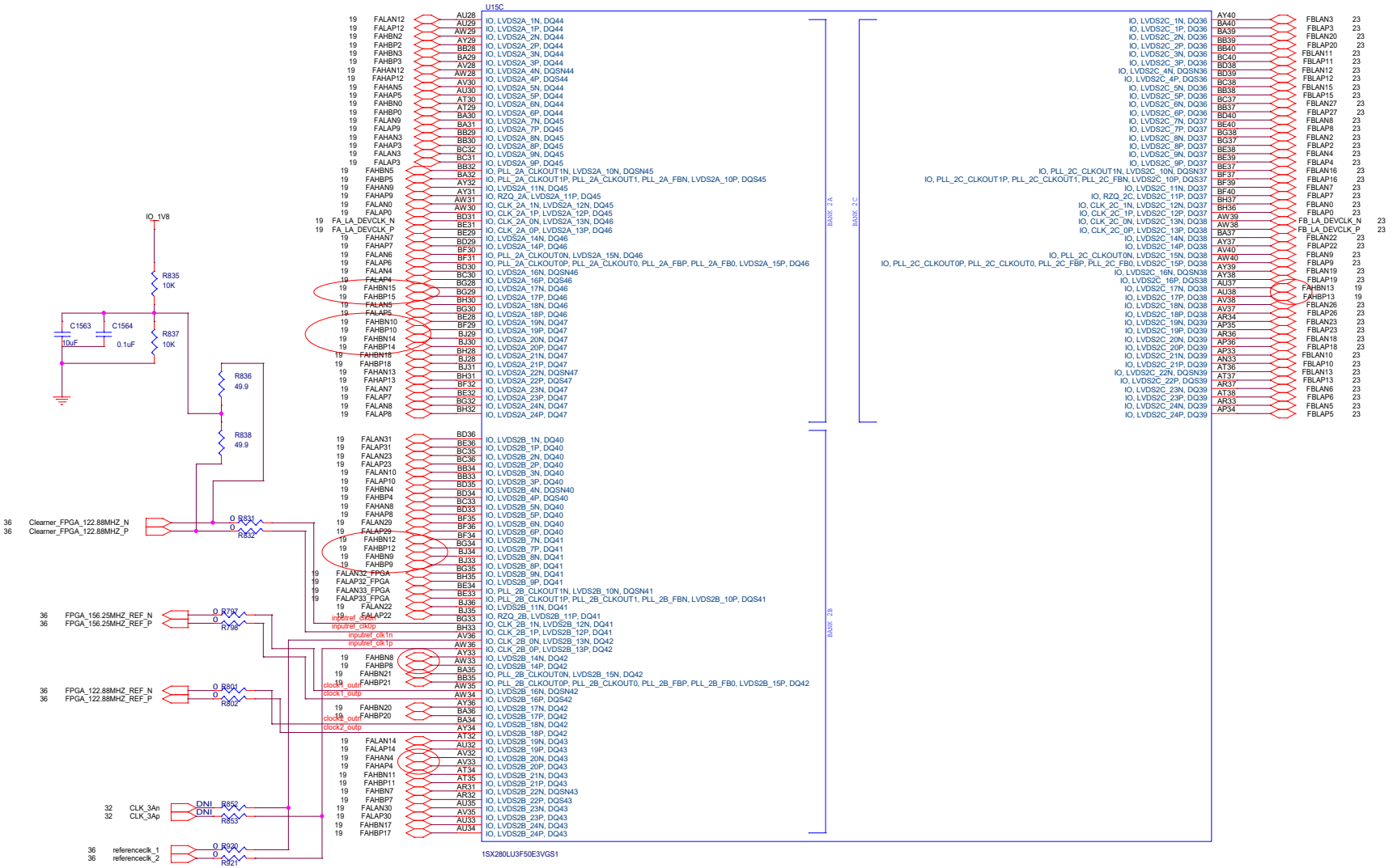
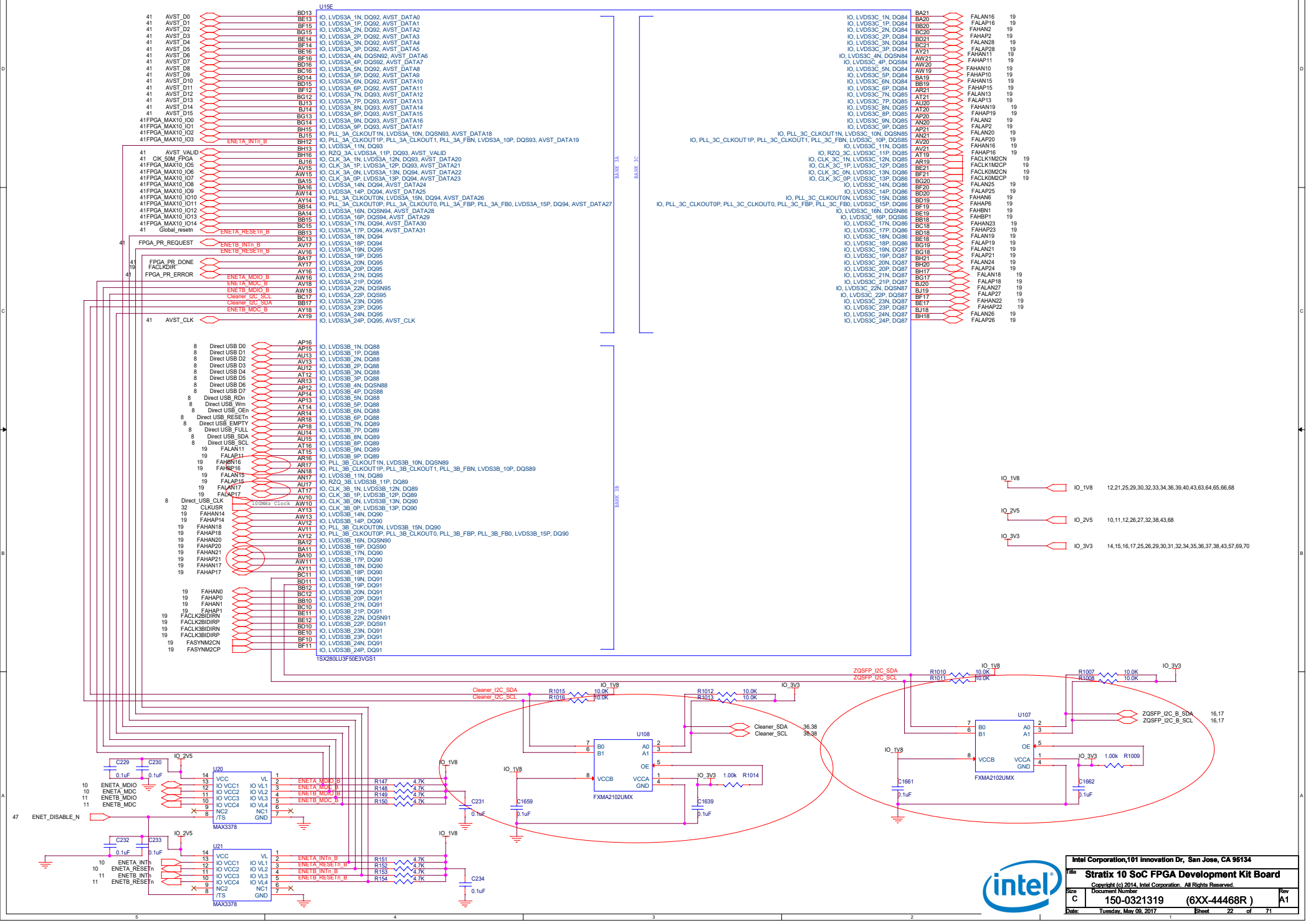
Stratix 10 Banks 2 A/B/C



Stratix 10 Banks - 3 A/B/C



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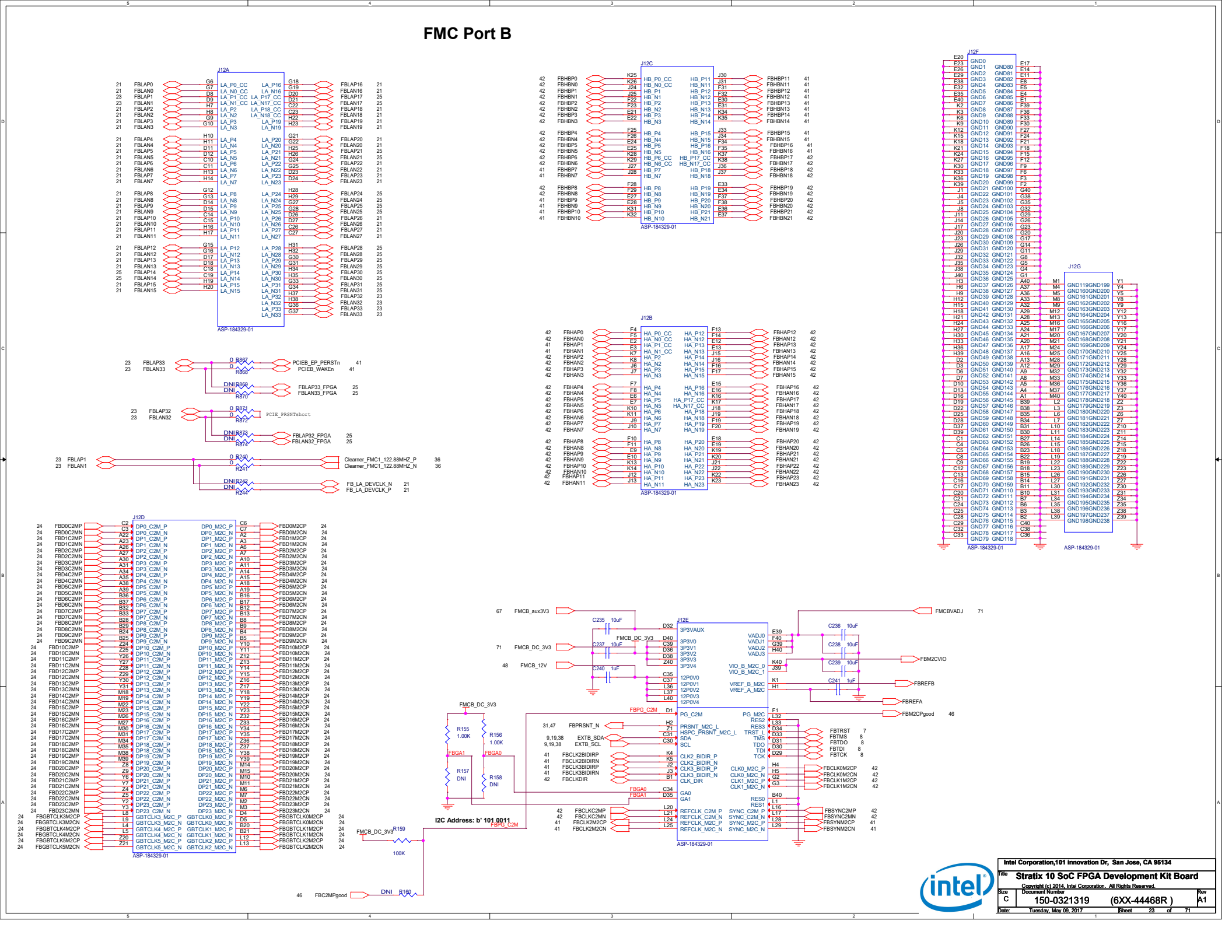
FMC Port B


J12A
J12C
J12F
J12B
J12G
J12D
J12E
ASP-184329-01
I2C Address: b' 101 0011
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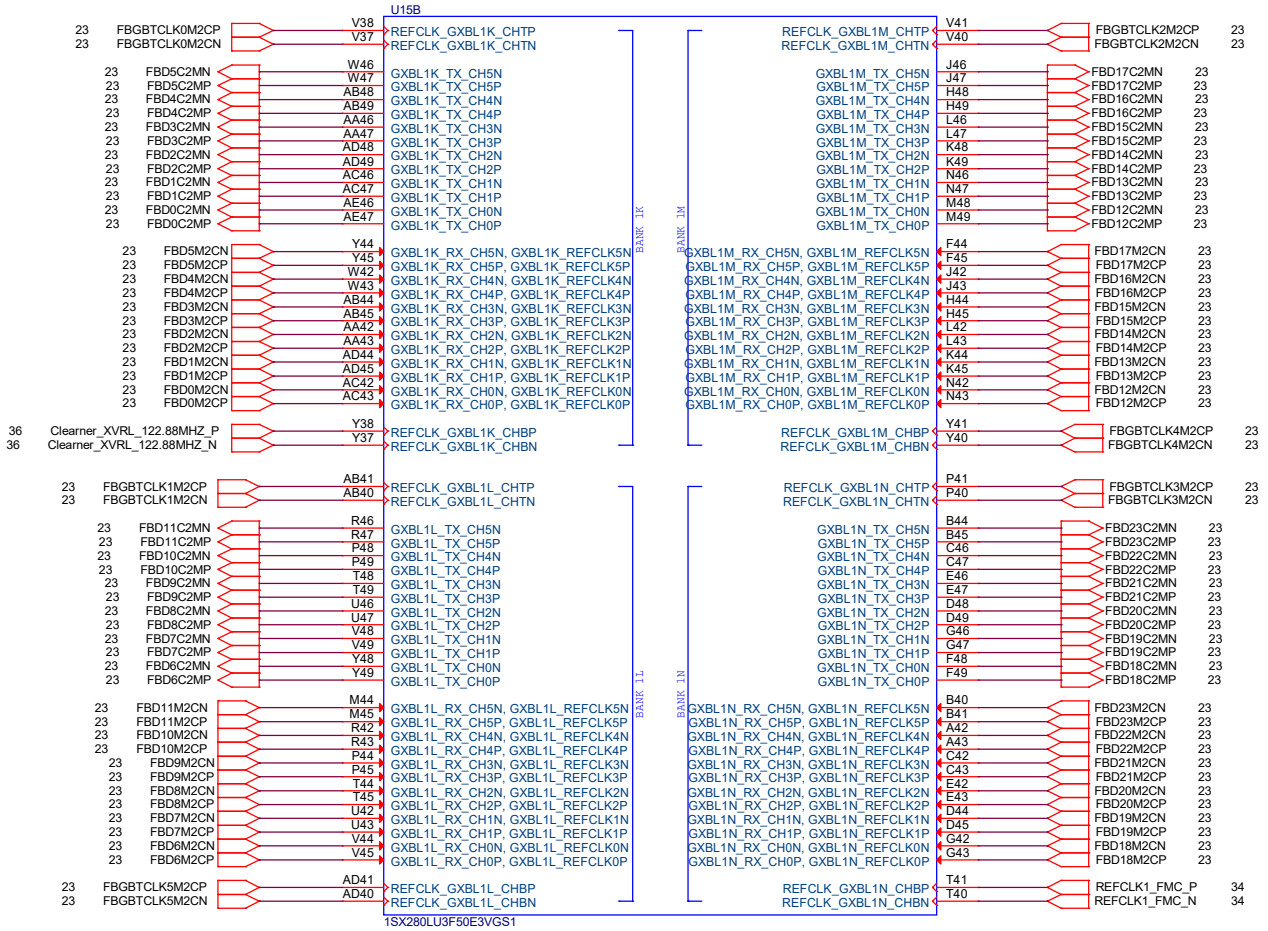
Stratix 10 XCVR Banks - 1K/L/M/N



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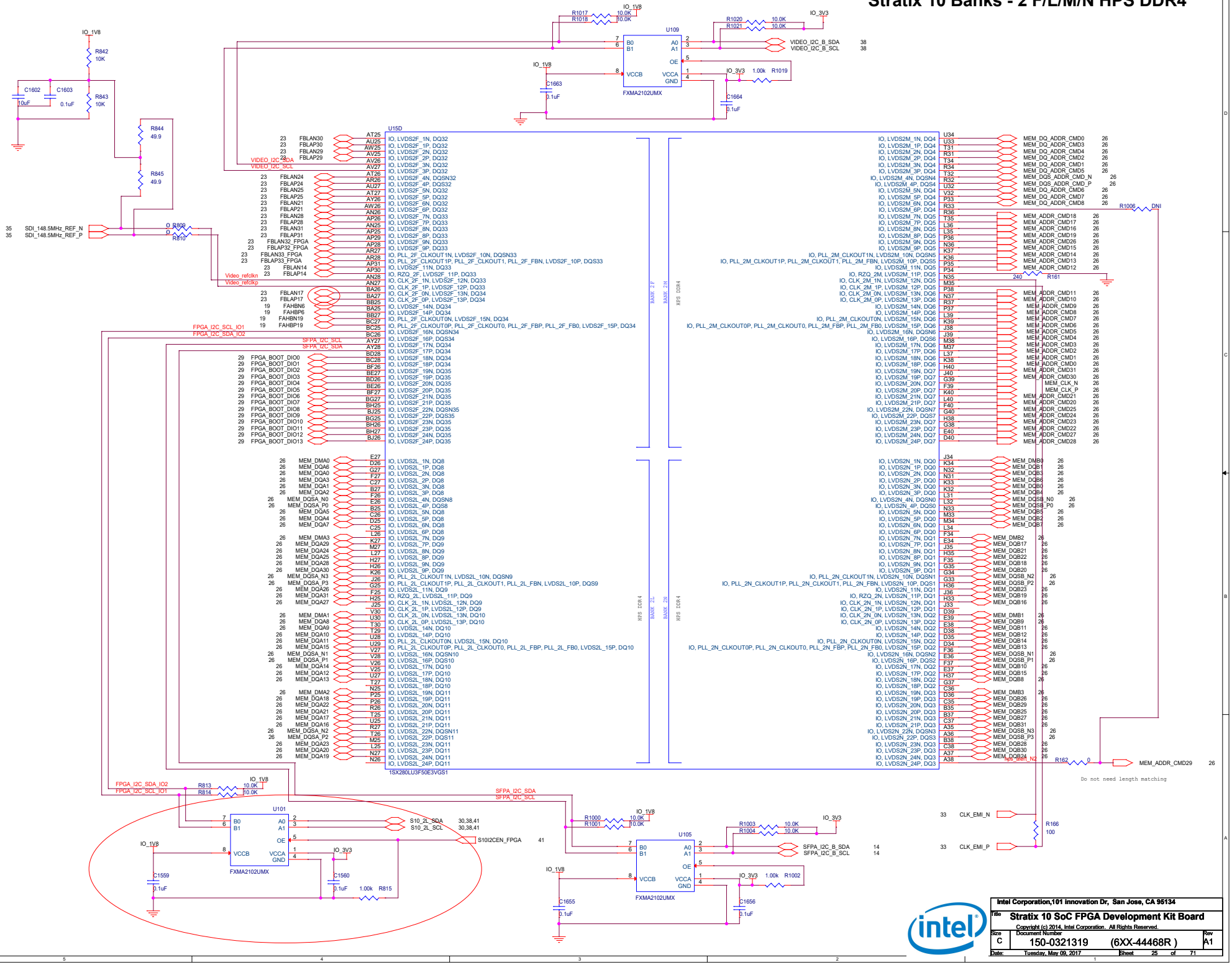
Stratix 10 Banks - 2 F/L/M/N HPS DDR4



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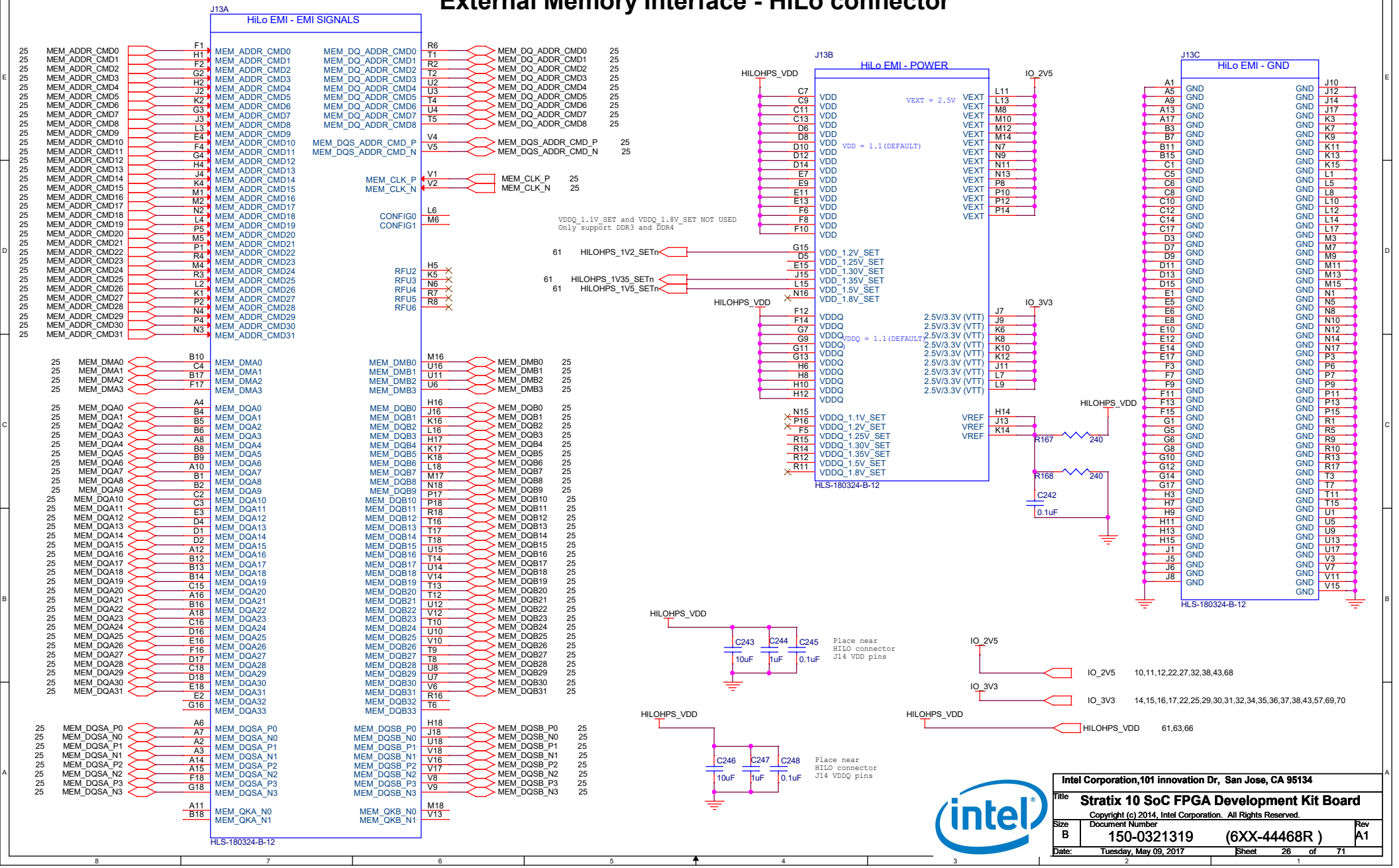
External Memory Interface - HiLo connector



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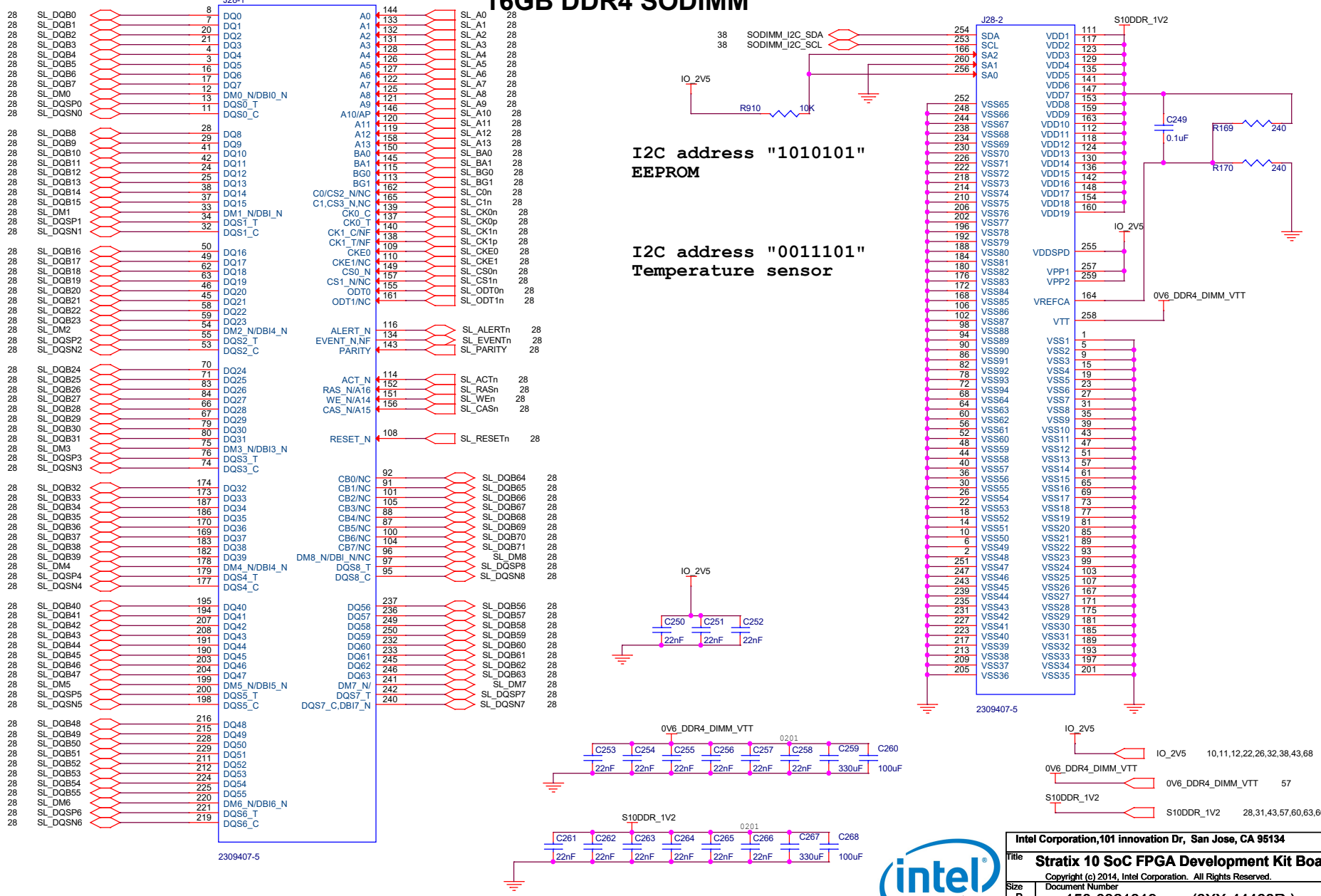
16GB DDR4 SODIMM



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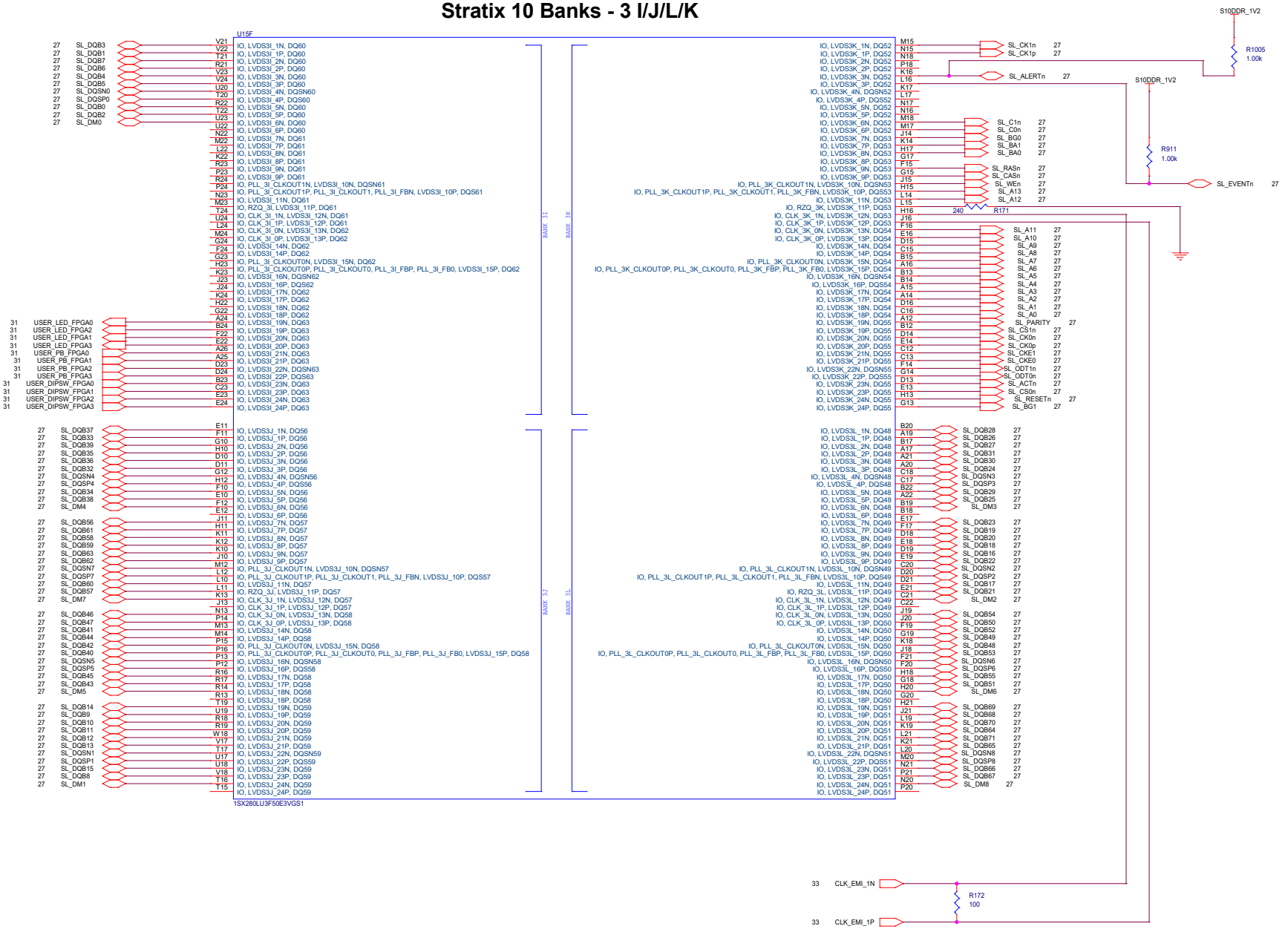
Stratix 10 Banks - 3 I/J/L/K



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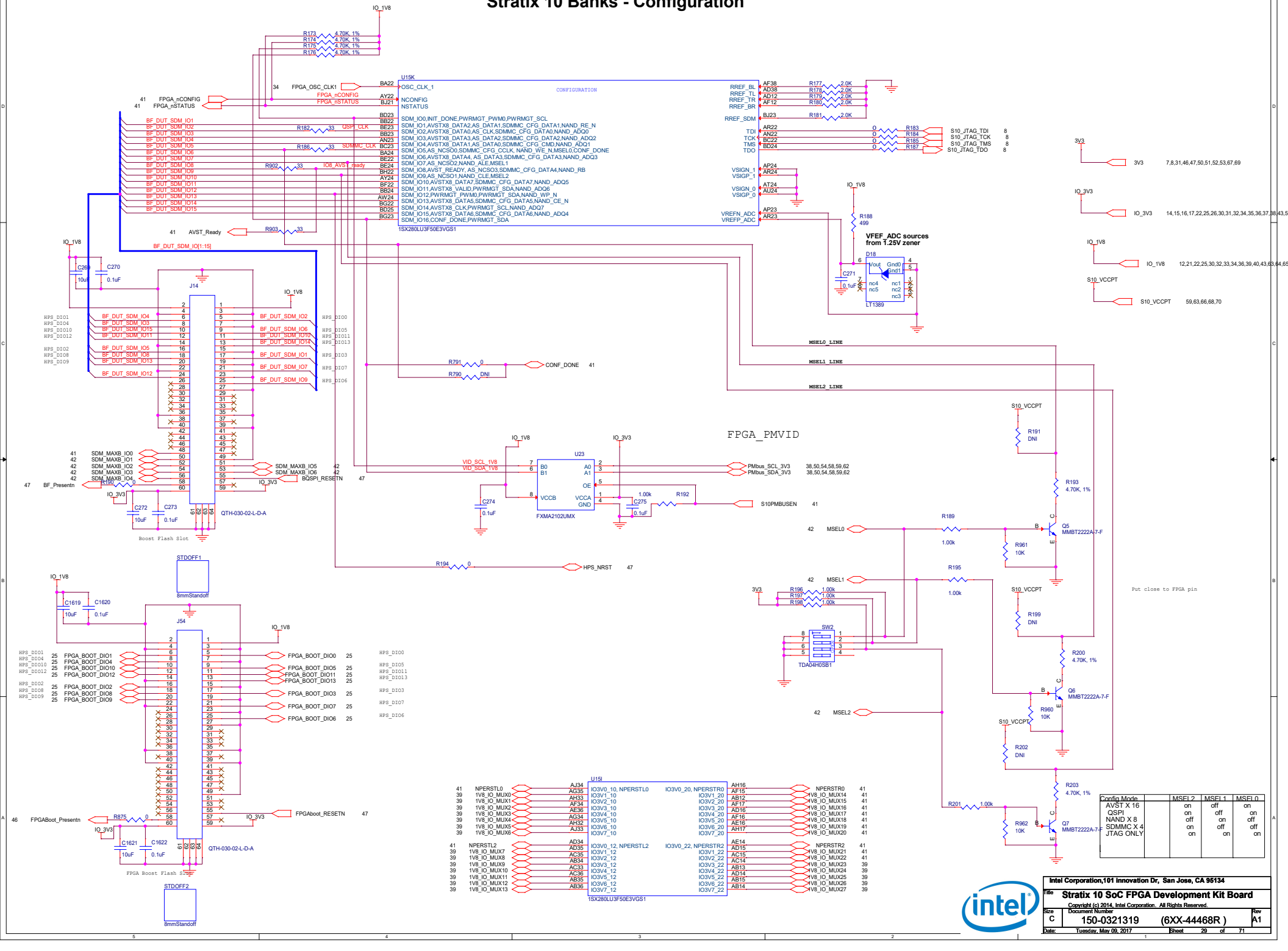
Stratix 10 Banks - Configuration



Config Mode	MSEL 2	MSEL 1	MSEL 0
AVST X 16	on	off	on
QSPI	on	off	on
NAND X 8	off	on	off
SDMMC X 4	on	off	off
JTAG ONLY	on	on	on

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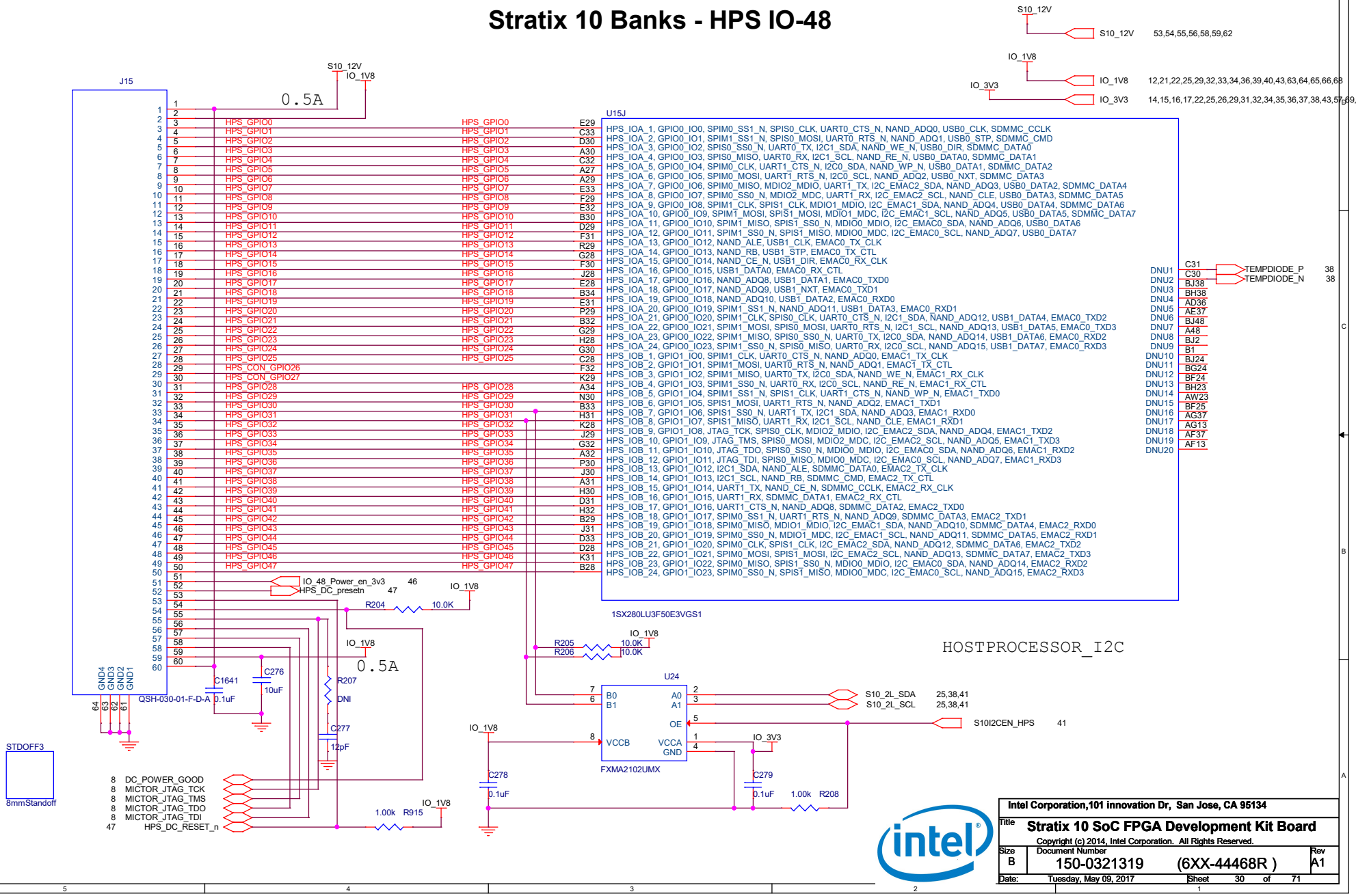
Stratix 10 Banks - HPS IO-48



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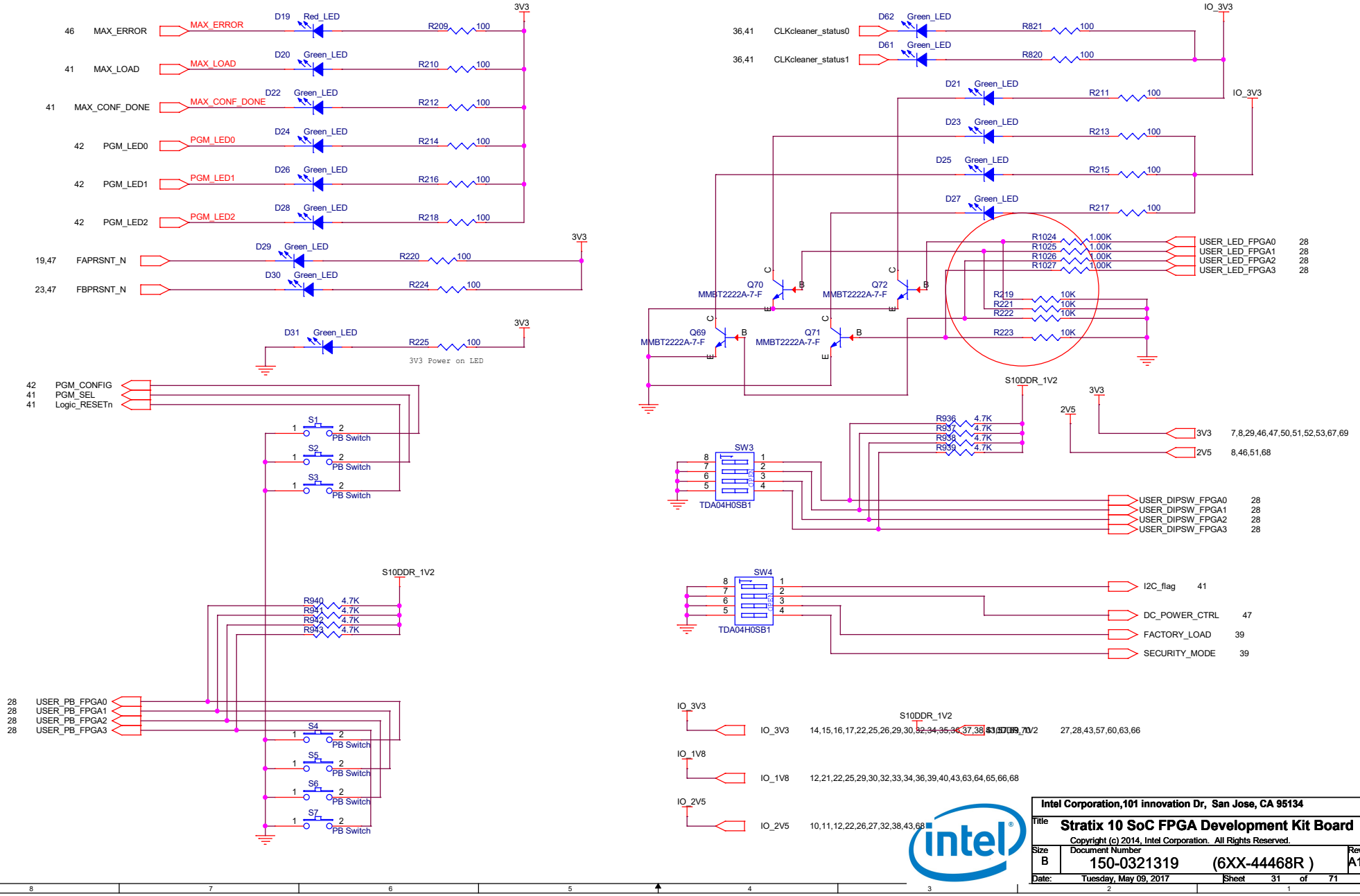
User I/O



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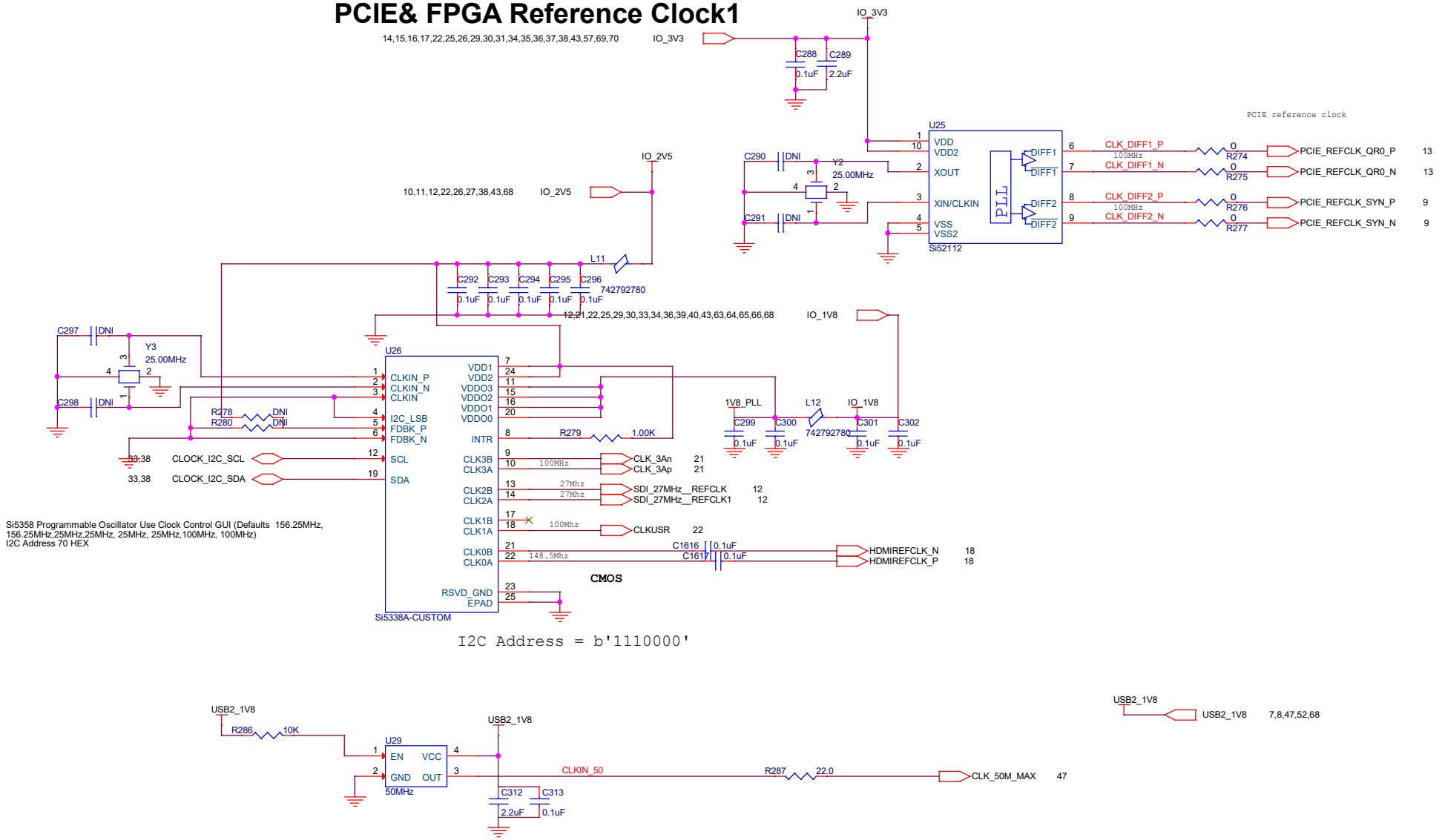
PCIE& FPGA Reference Clock1



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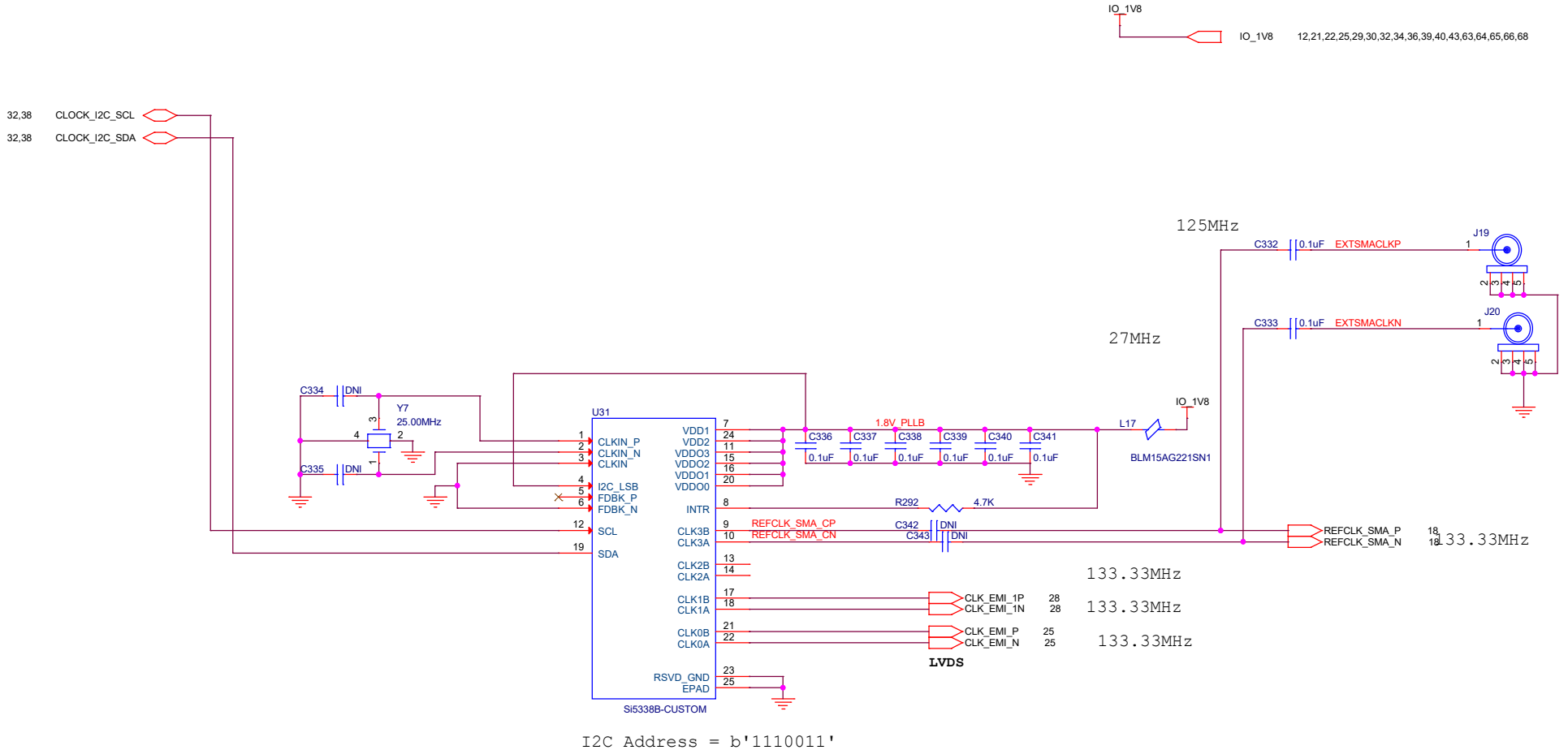
FPGA Memomory Reference clock



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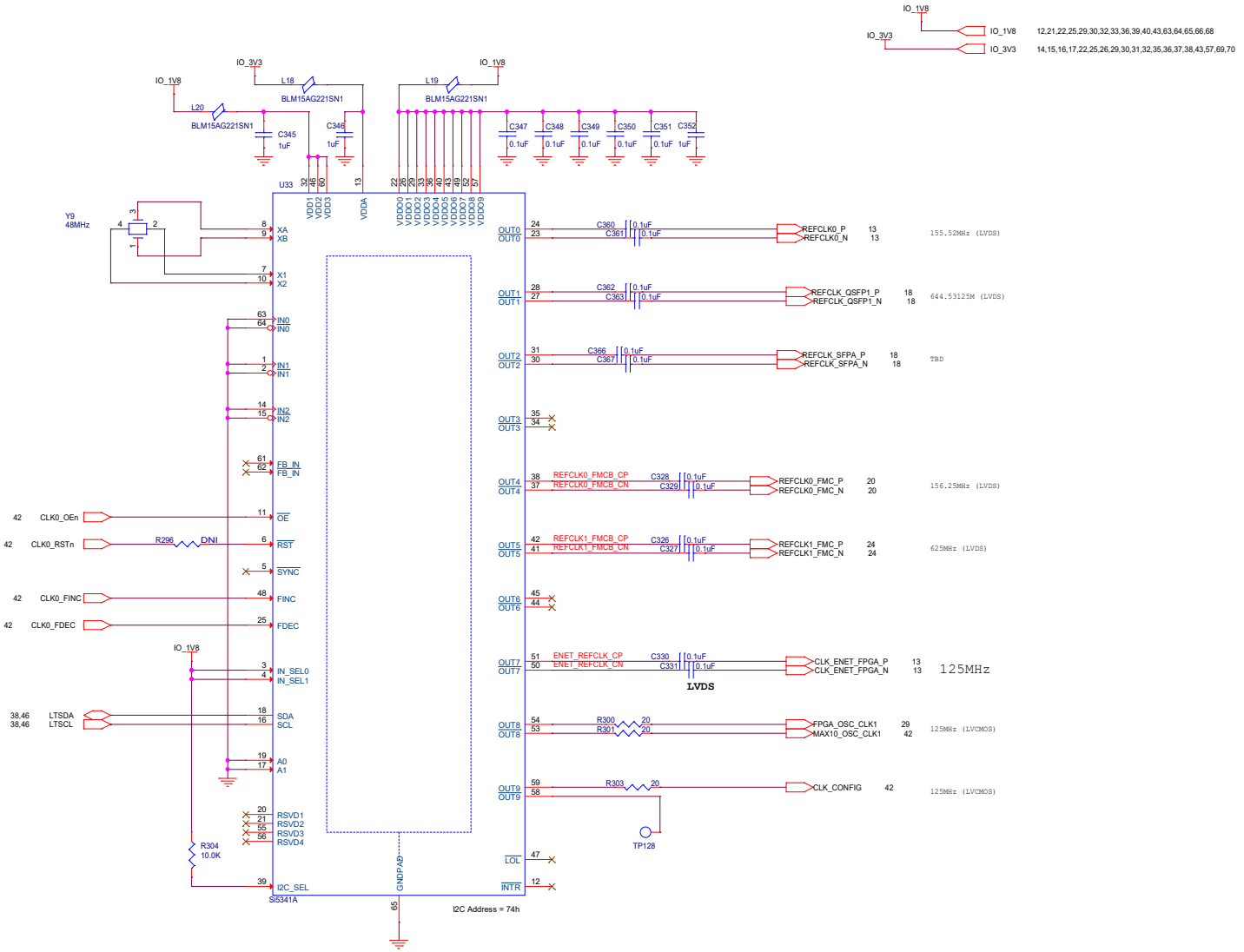
FPGA Transceiver reference Clocks



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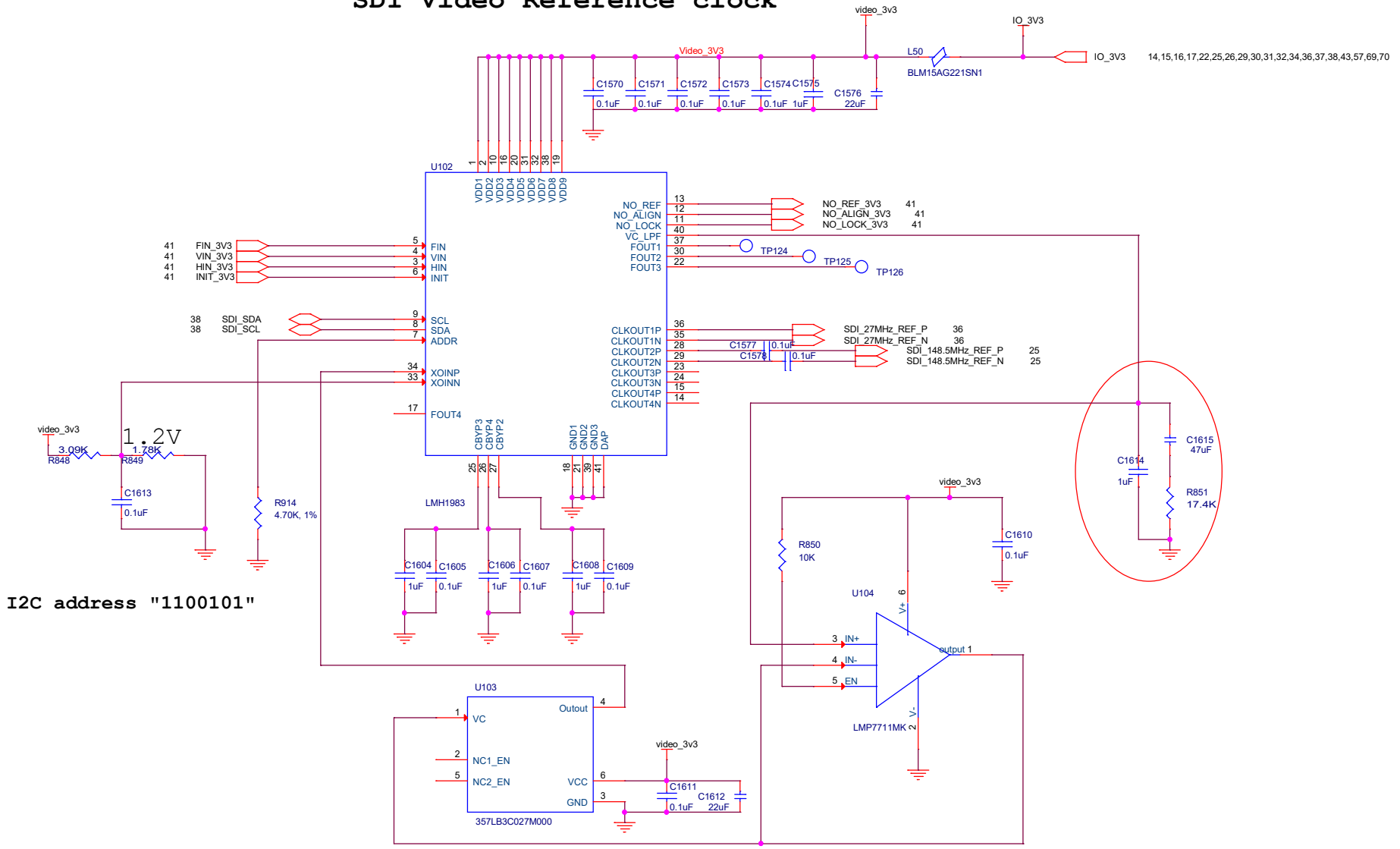
SDI Video Reference clock



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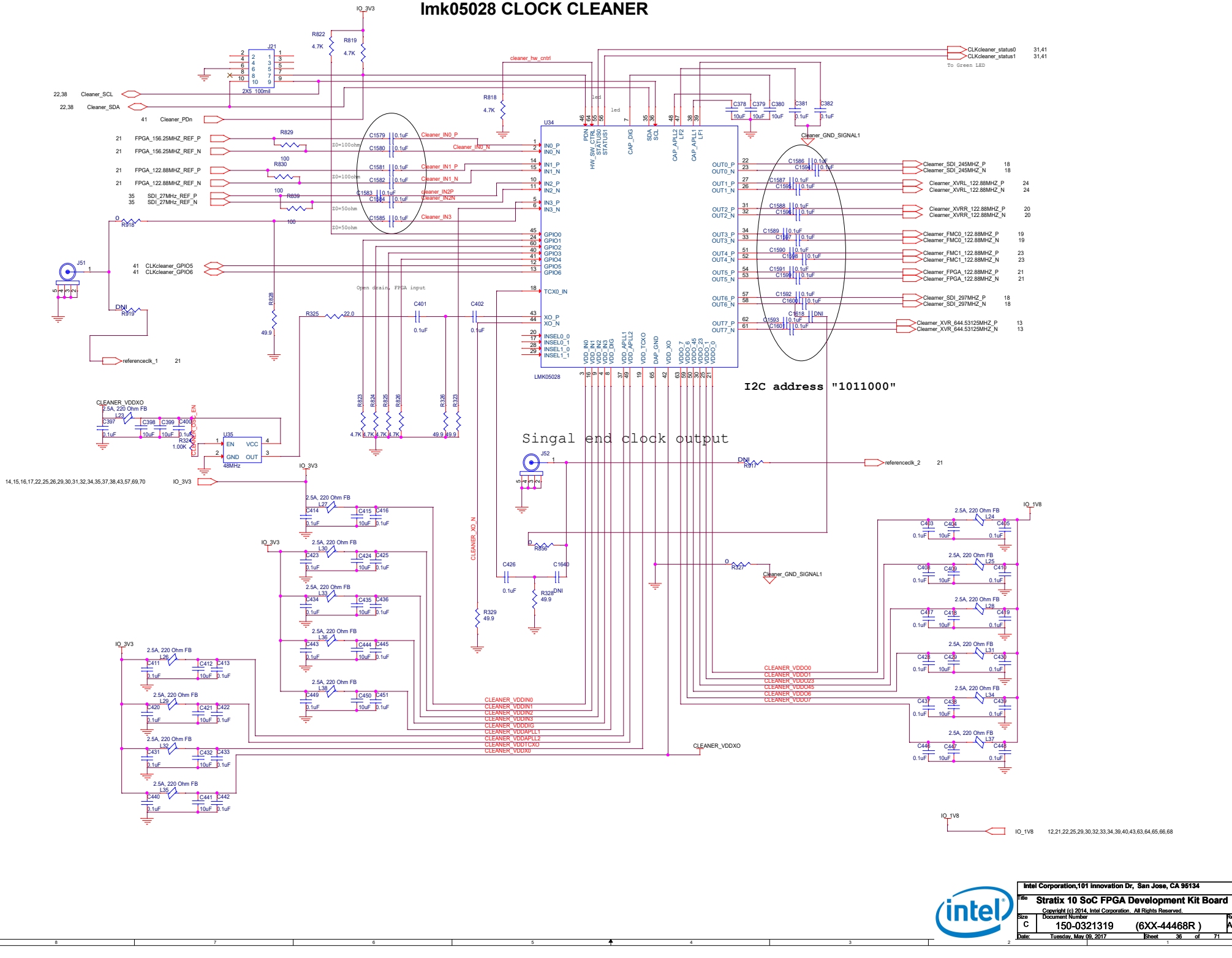
lmk05028 CLOCK CLEANER



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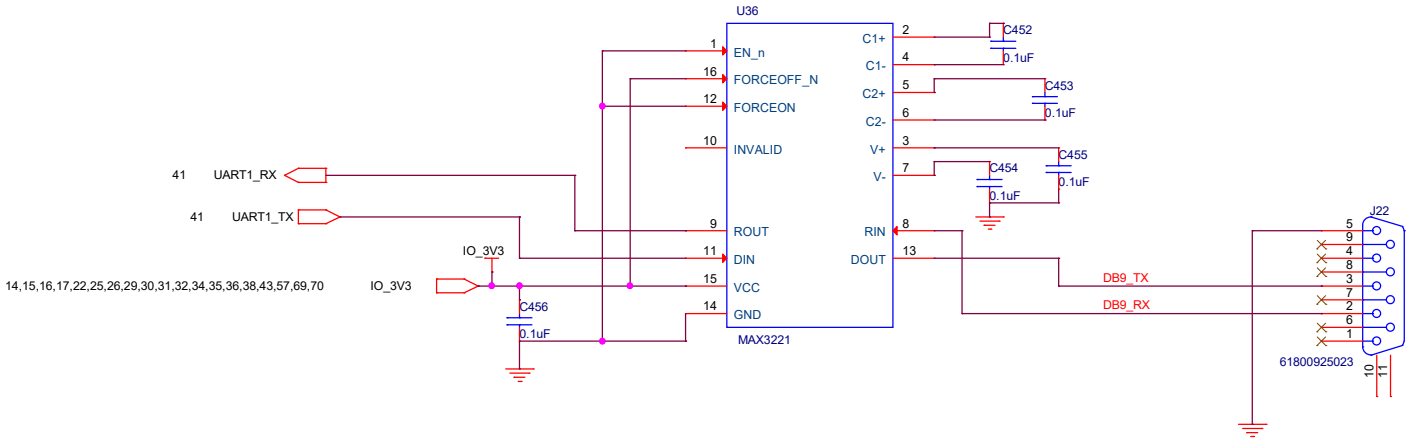
UART Port B



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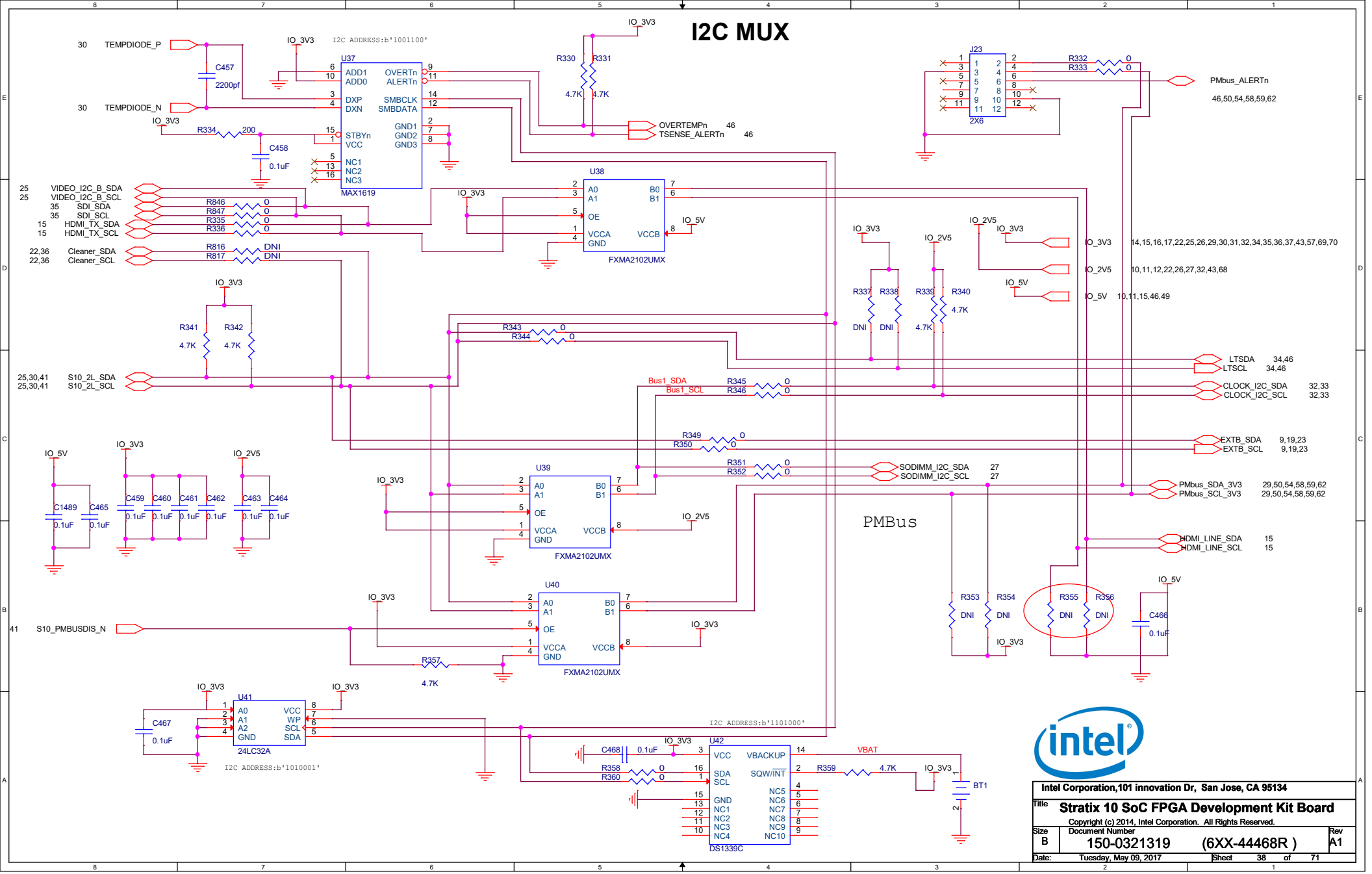
I2C MUX



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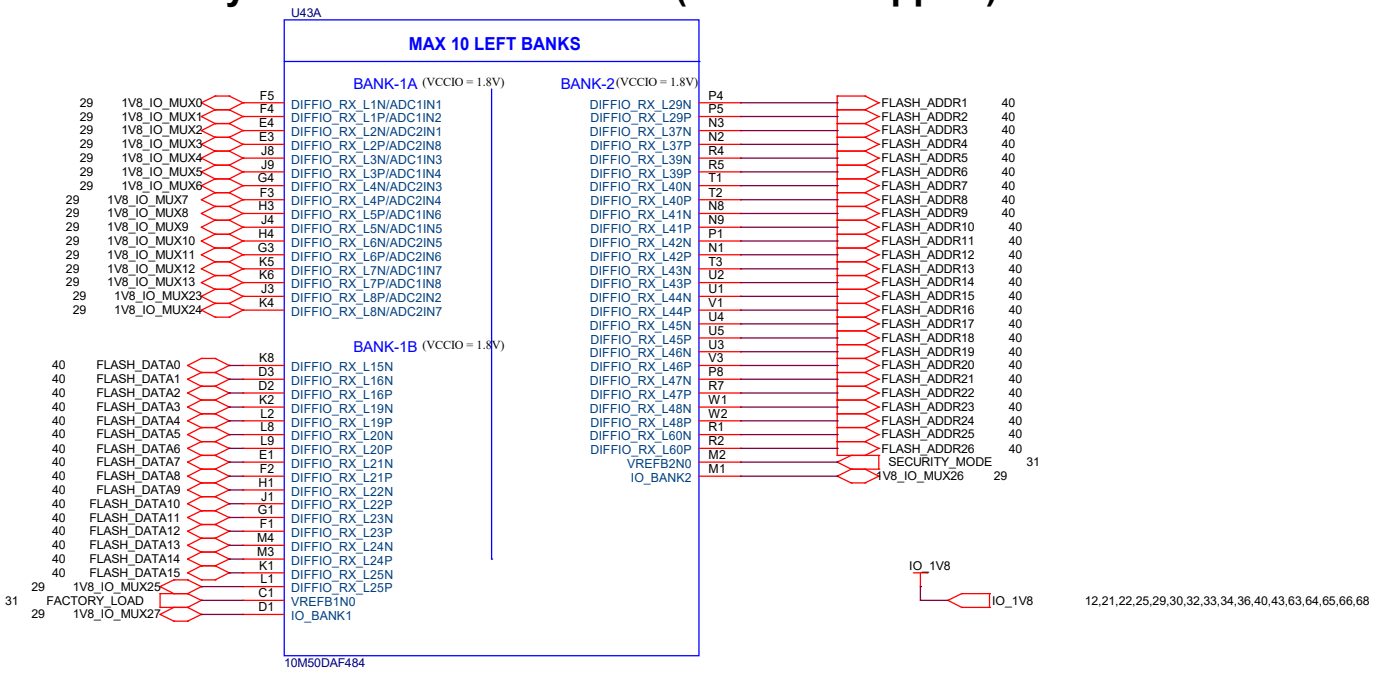
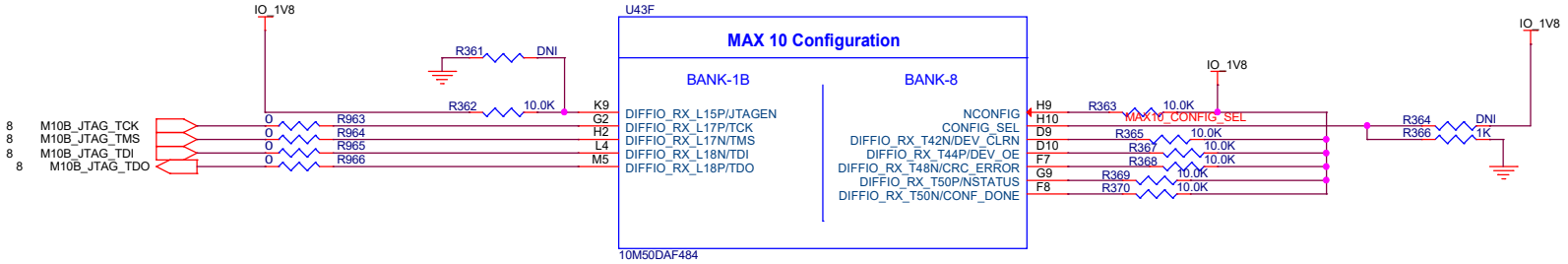
System MAX10 Controller (NO ADC Support)





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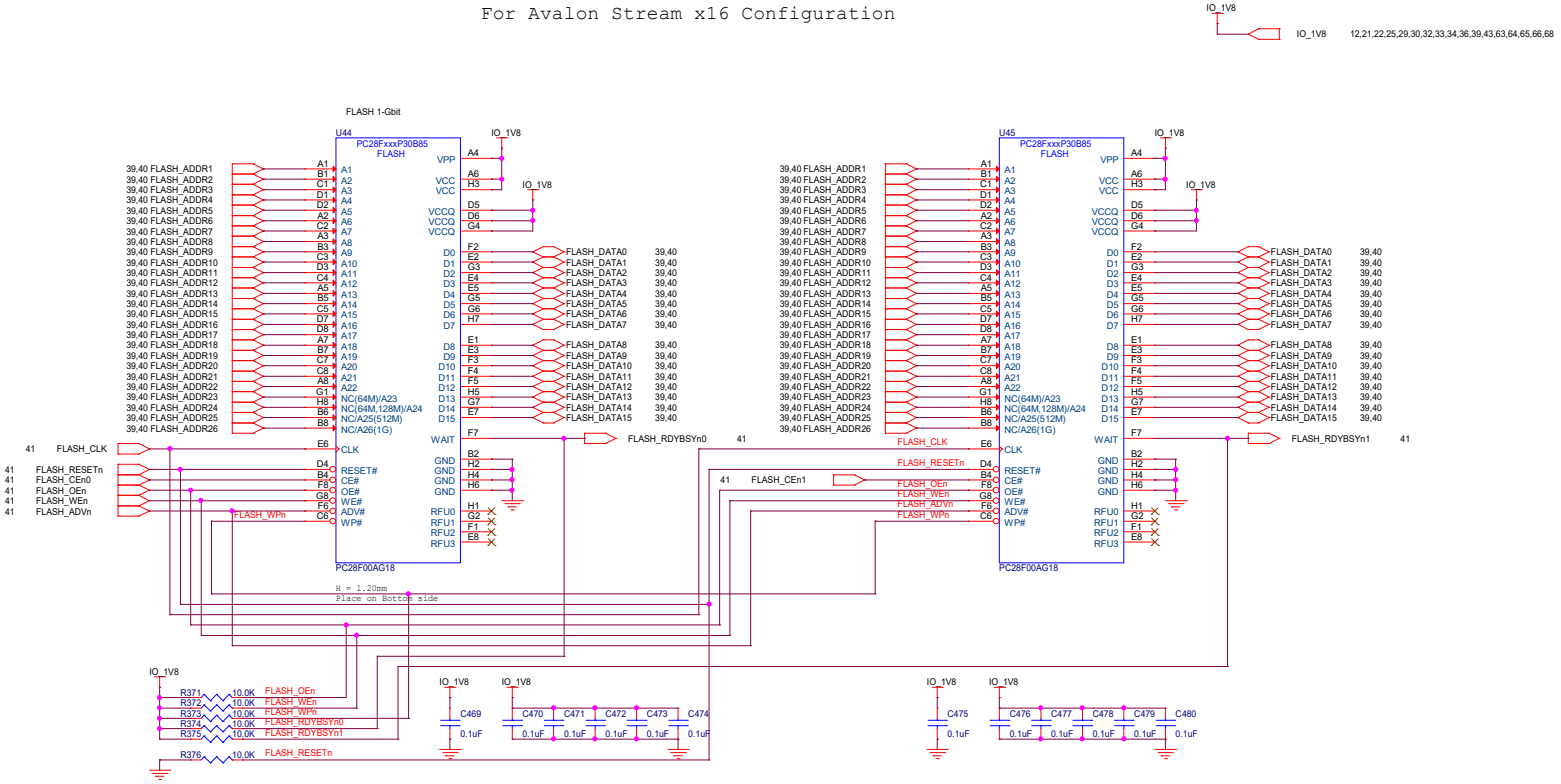
Flash Memory

For Avalon Stream x16 Configuration



- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.

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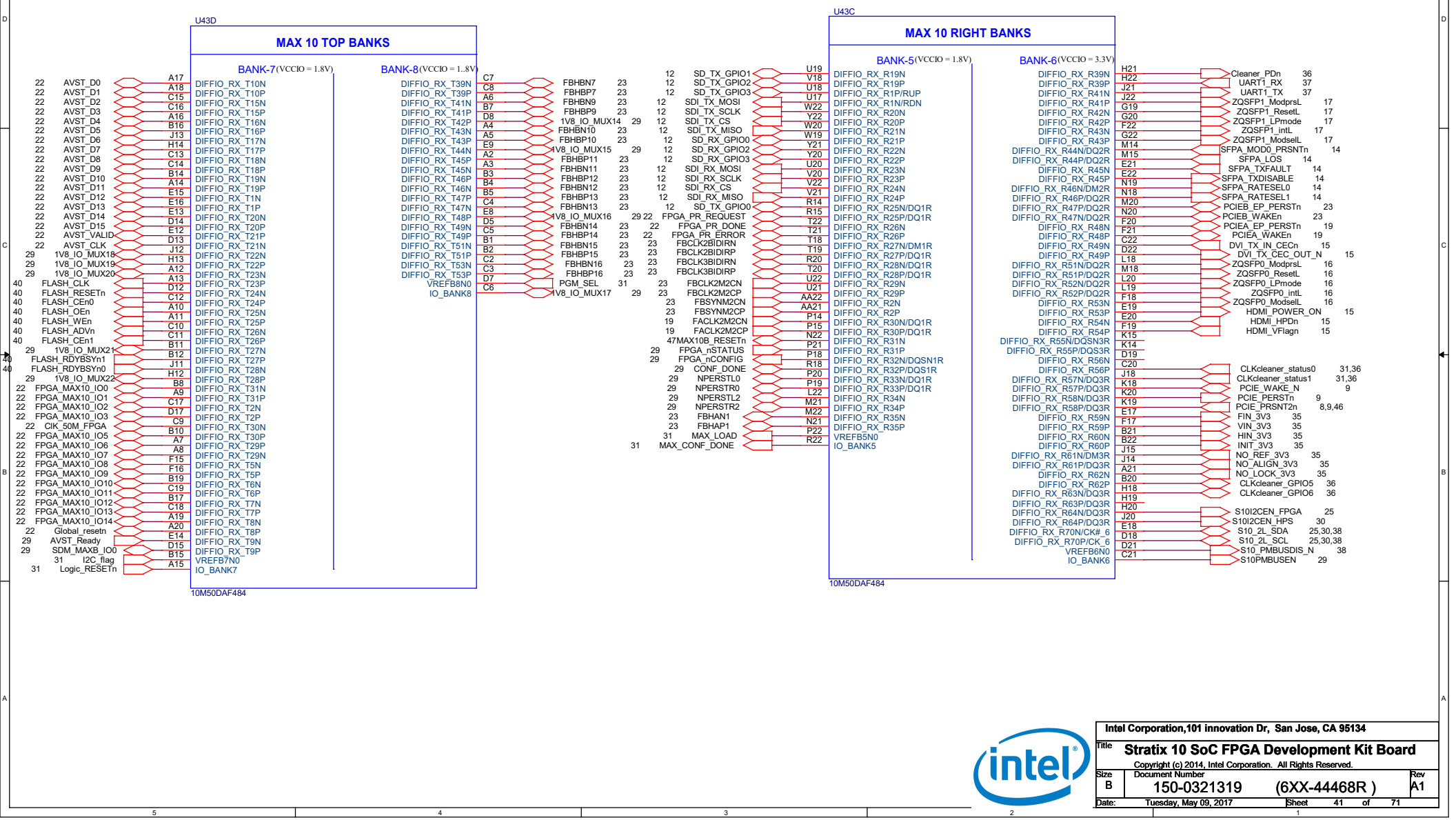
System MAX10 Controller 2



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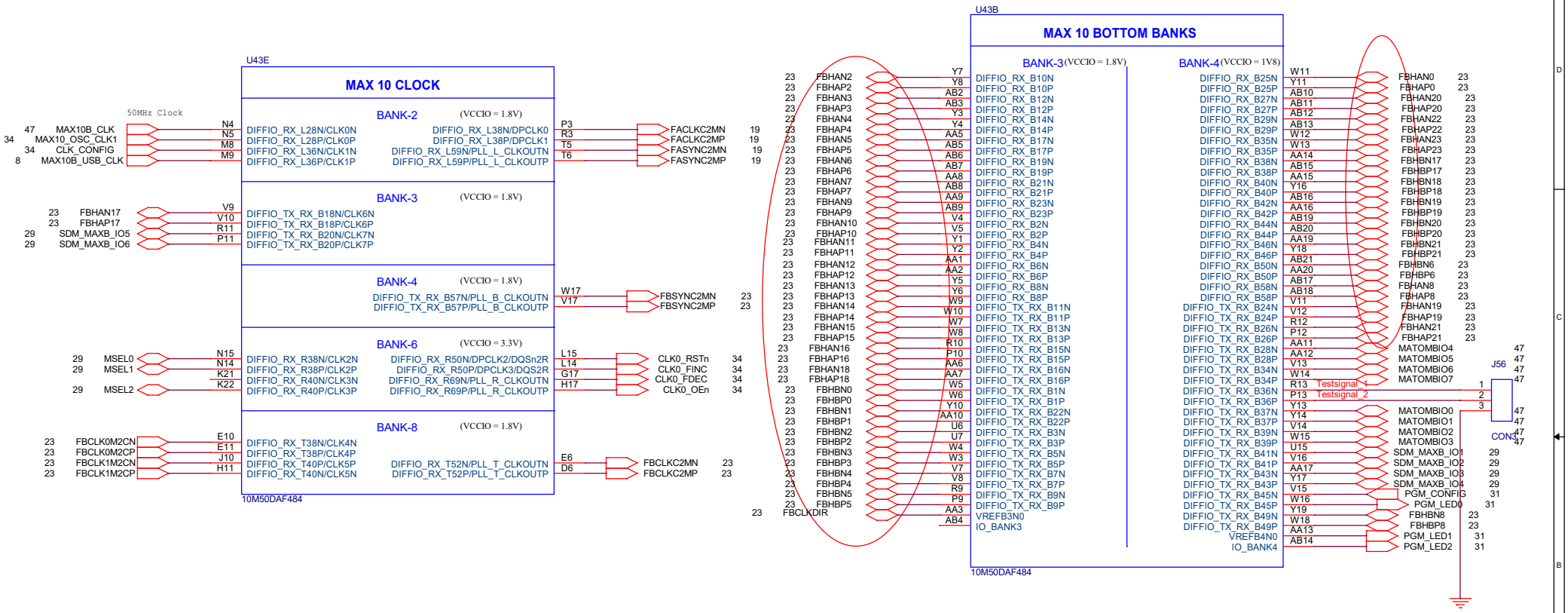
System MAX10 Controller 3



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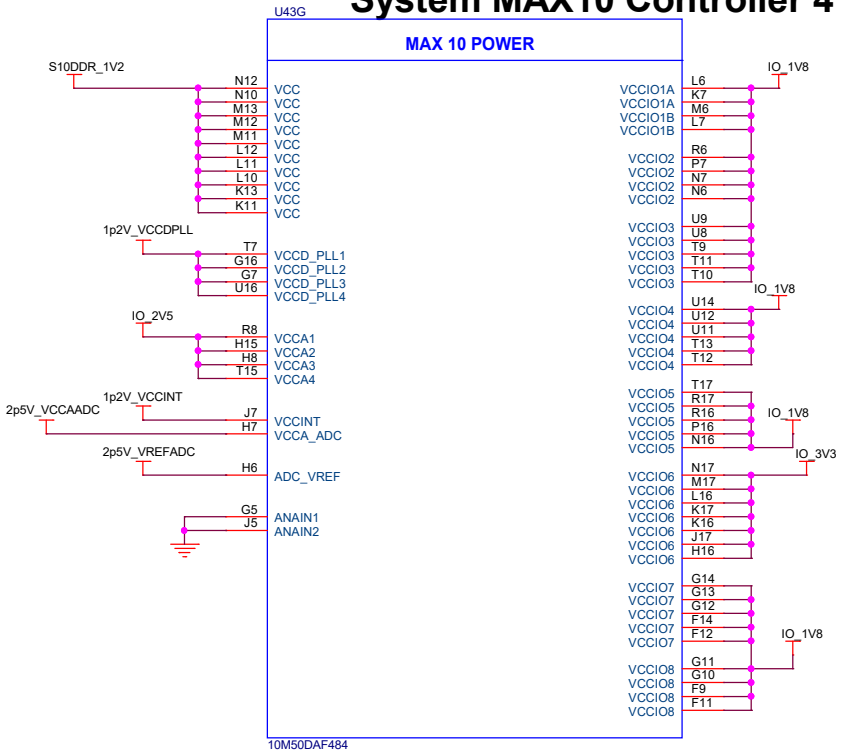
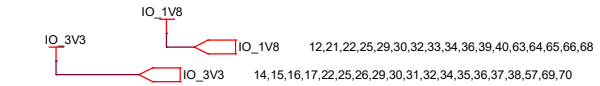
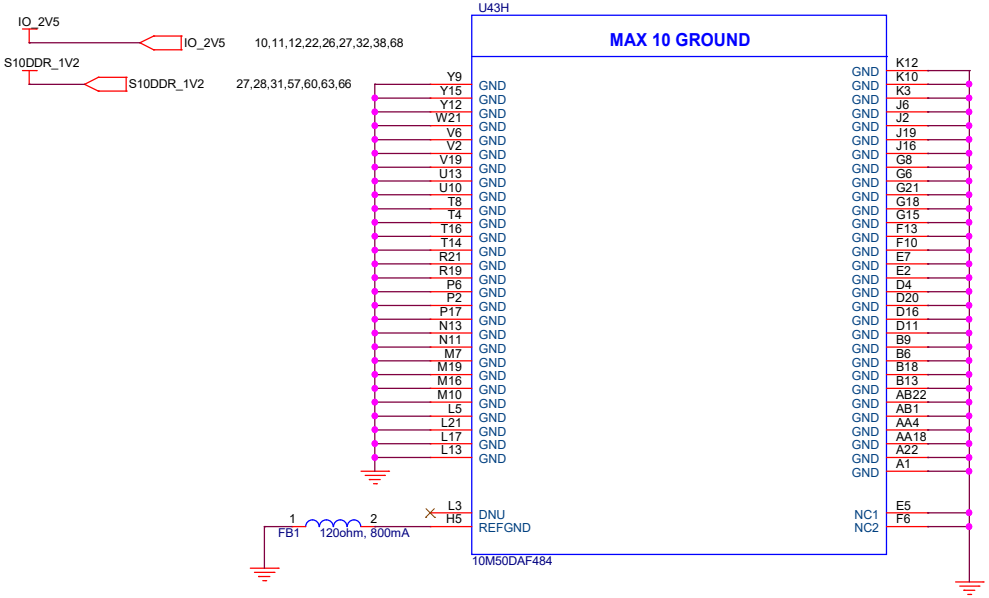
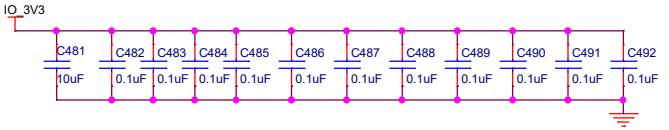
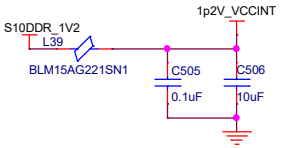
System MAX10 Controller 4

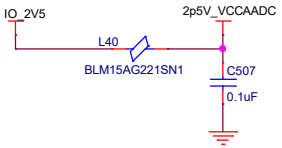


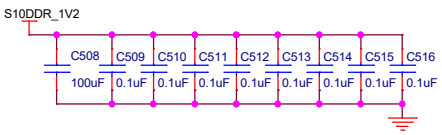


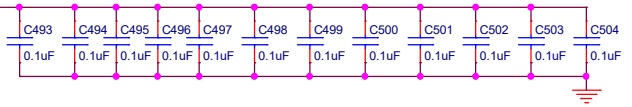


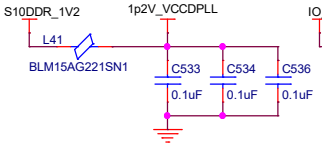


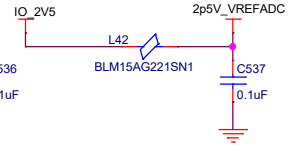


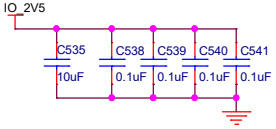


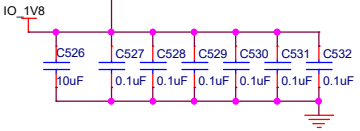


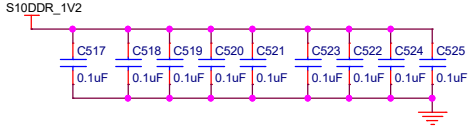


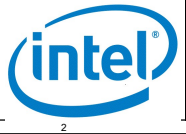












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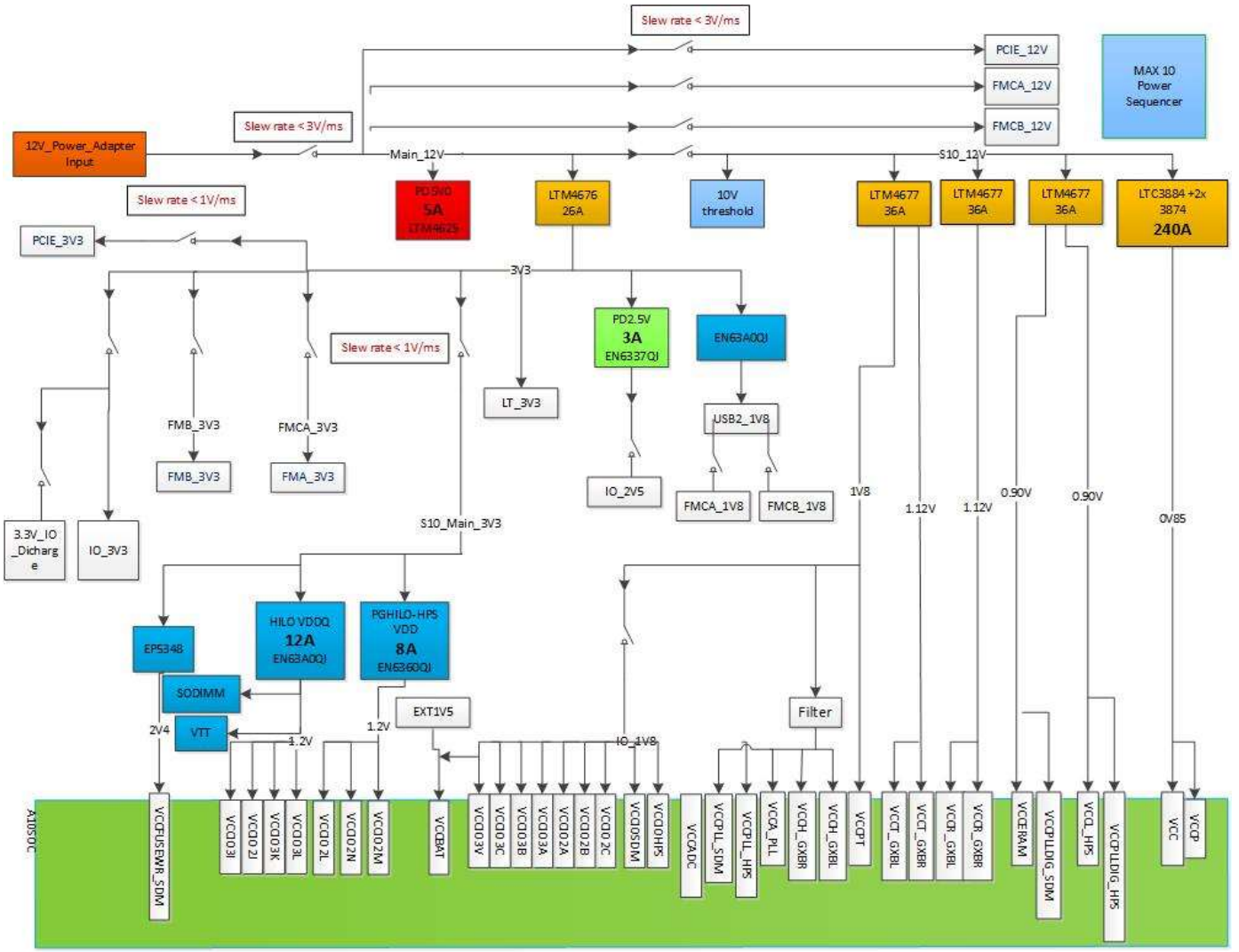
Stratix 10 SOC DEV KIT PDN Diagram



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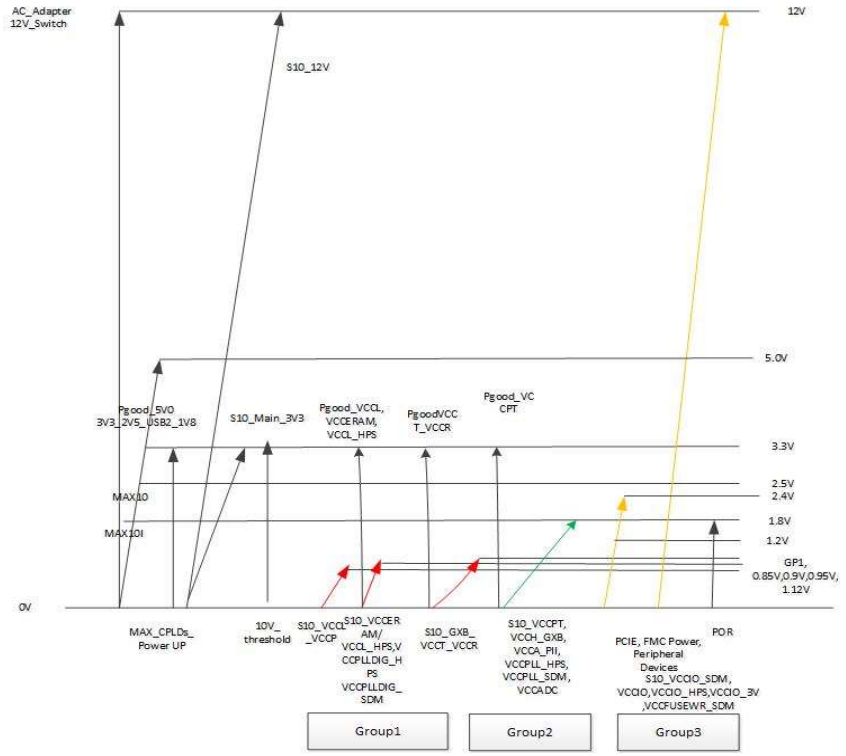
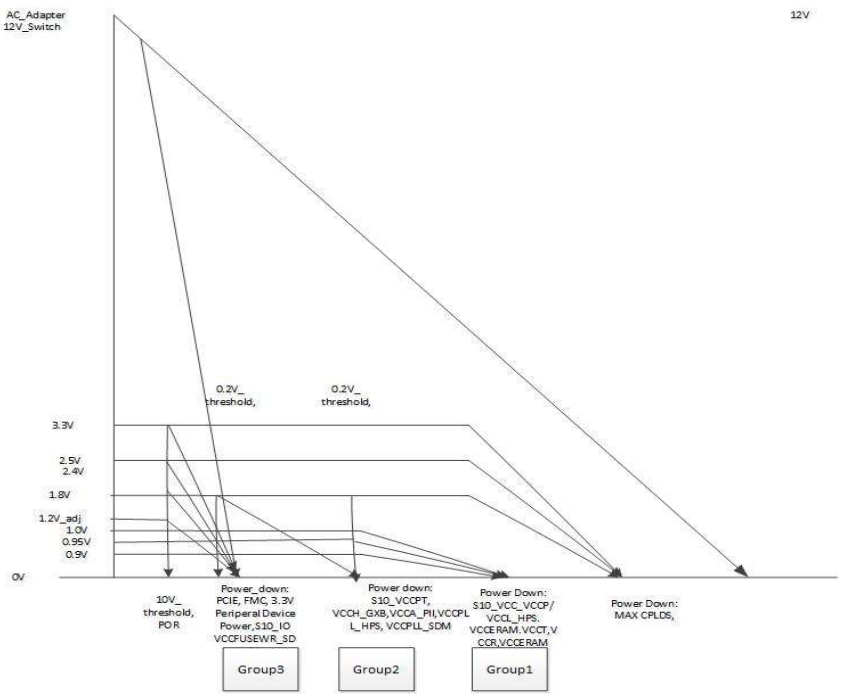
Stratix 10 SOC Power Sequence

S10 Dev KIT Power UP sequence



S10 Dev KIT Power Down sequence



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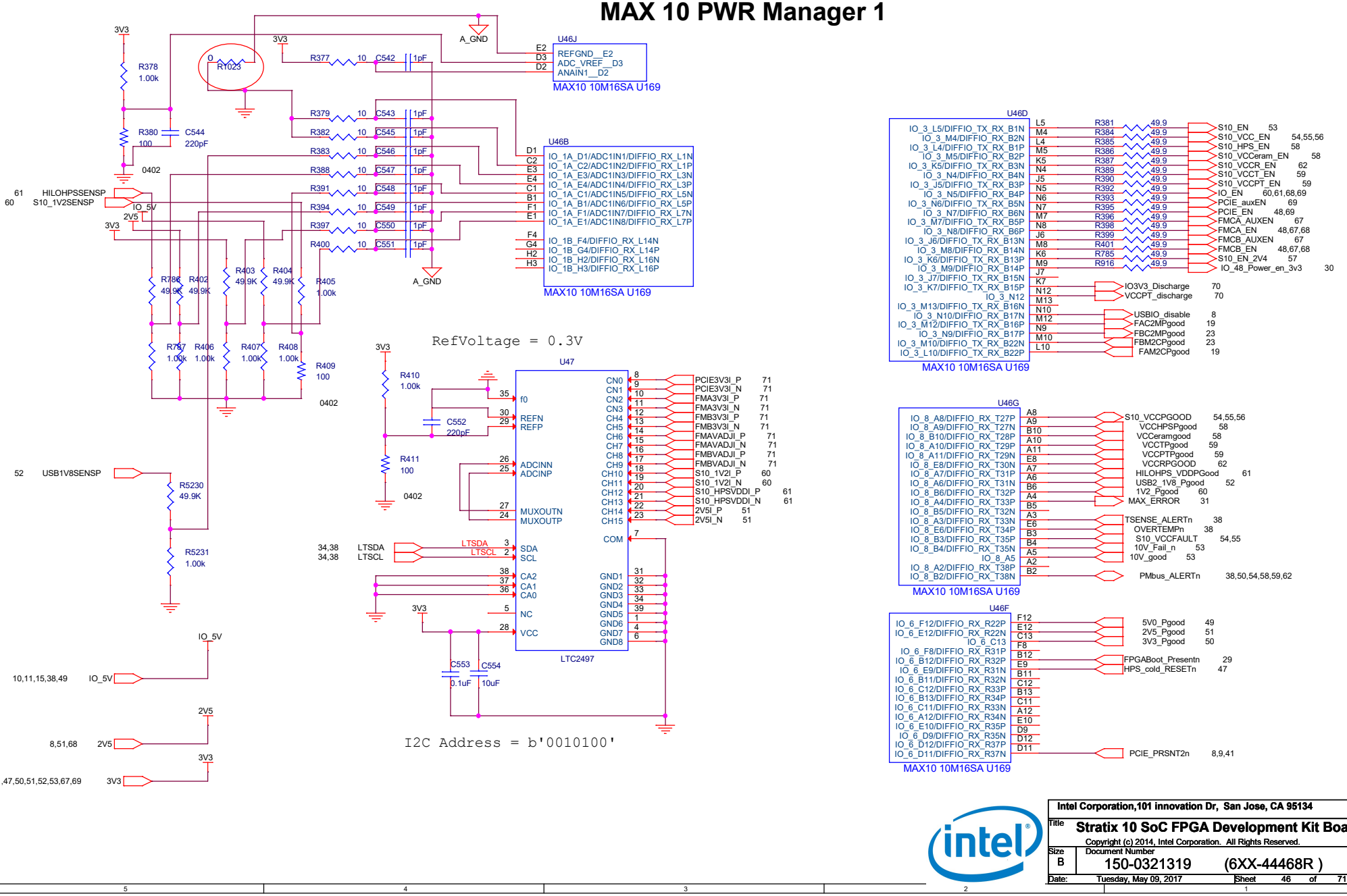
MAX 10 PWR Manager 1



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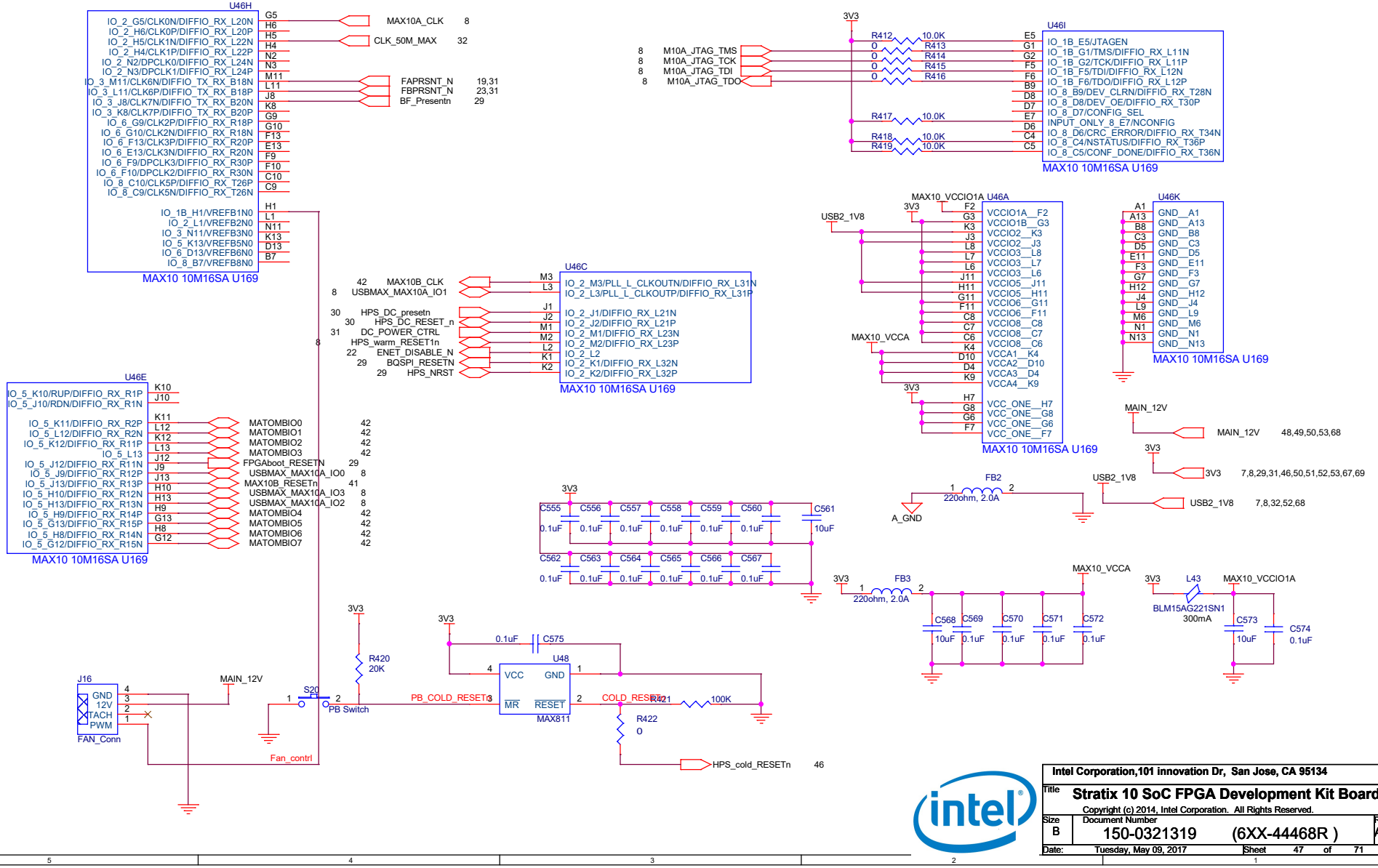
MAX10 PWR Manager 2



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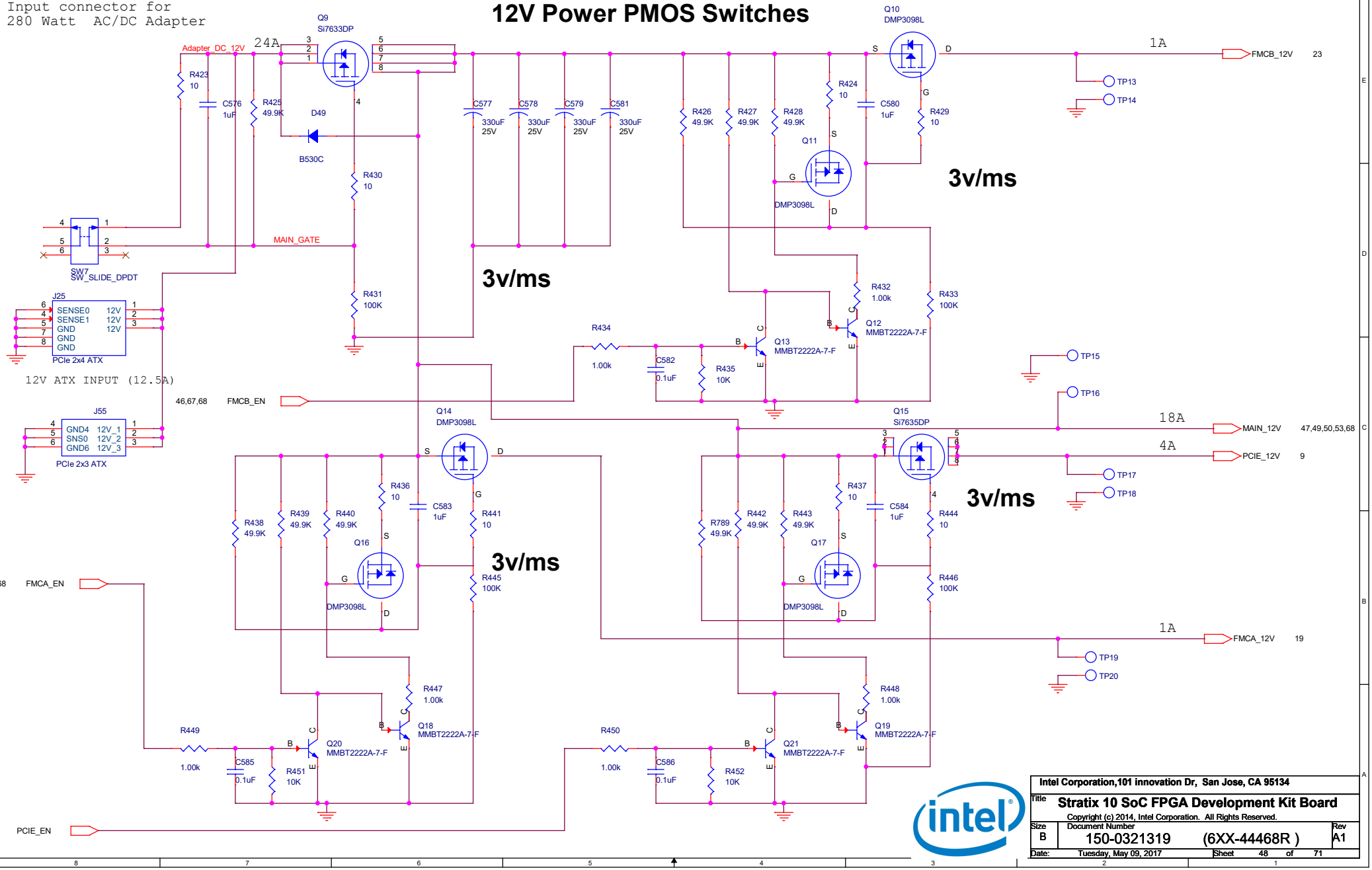
12V Power PMOS Switches

Input connector for
280 Watt AC/DC Adapter



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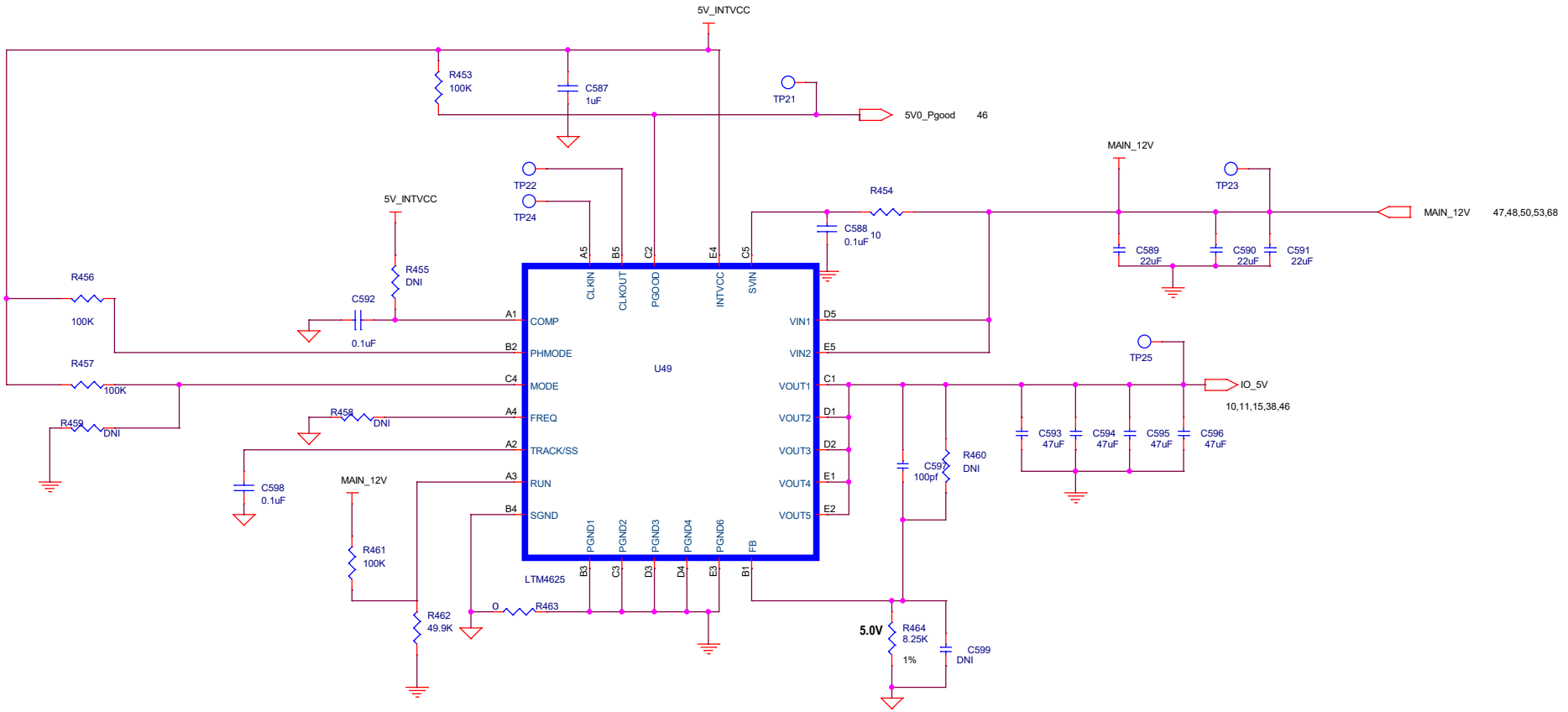
12V to 5V Power Supply



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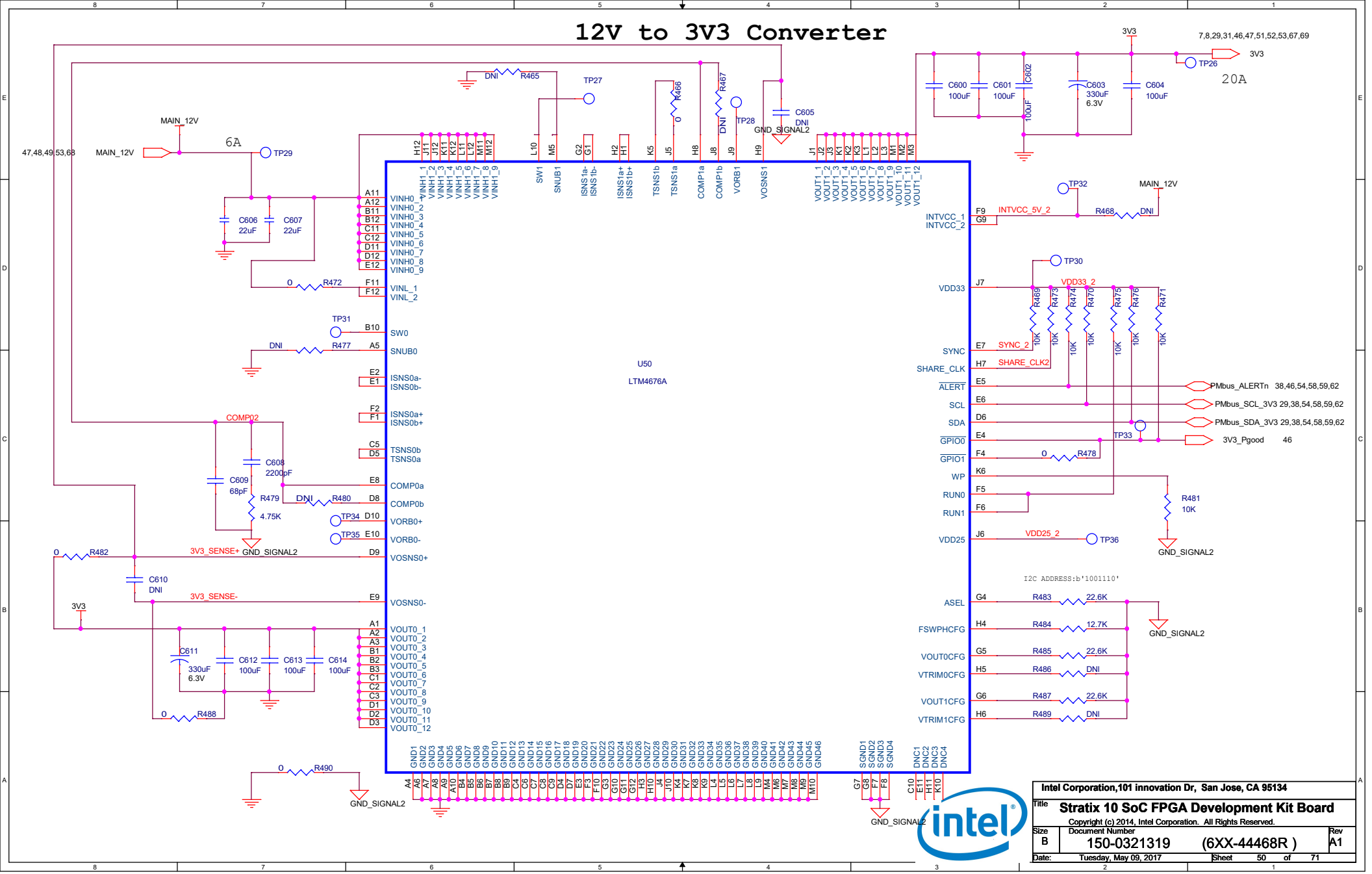
12V to 3V3 Converter



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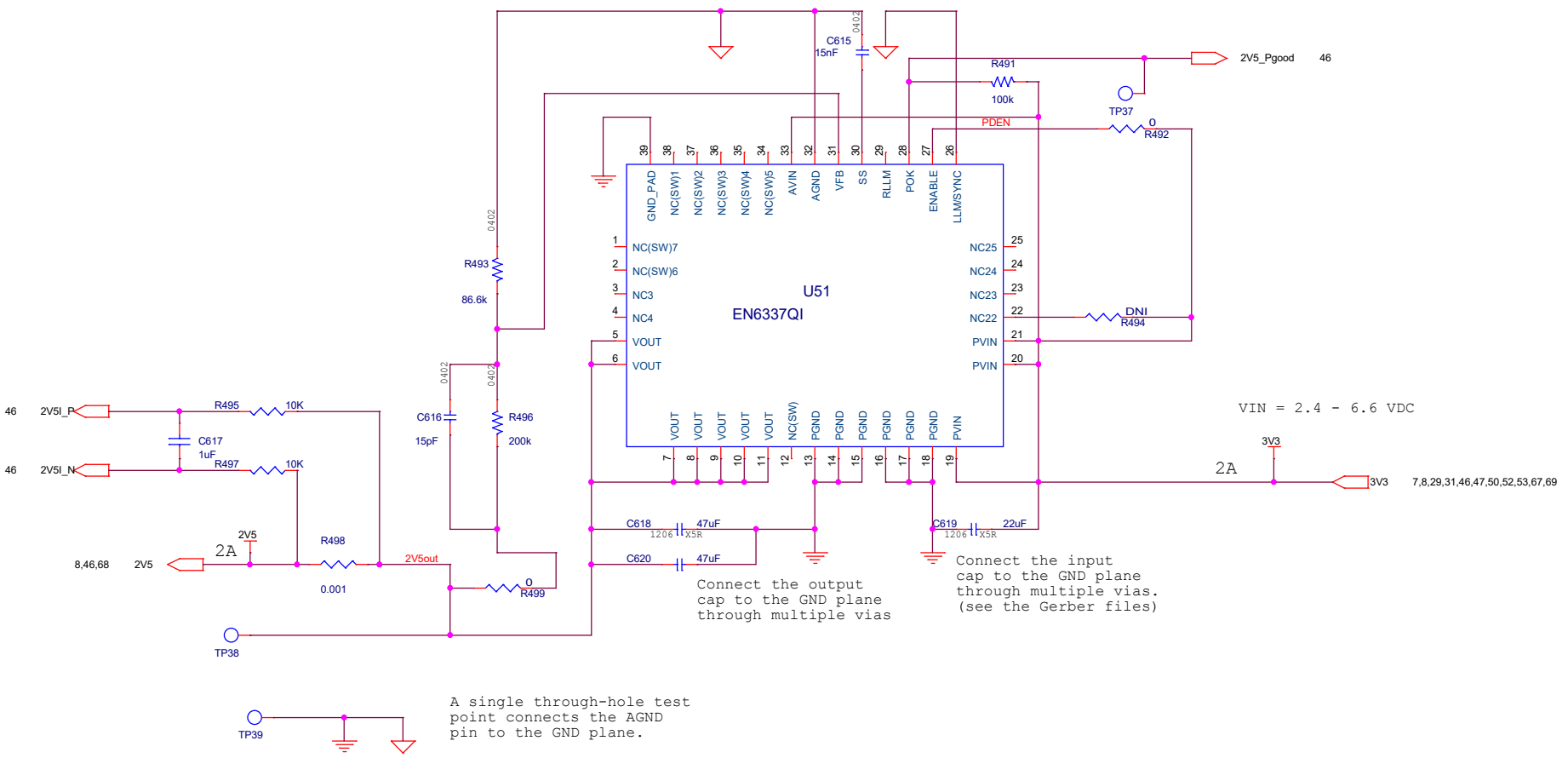
3V3 to 2V5 Converter



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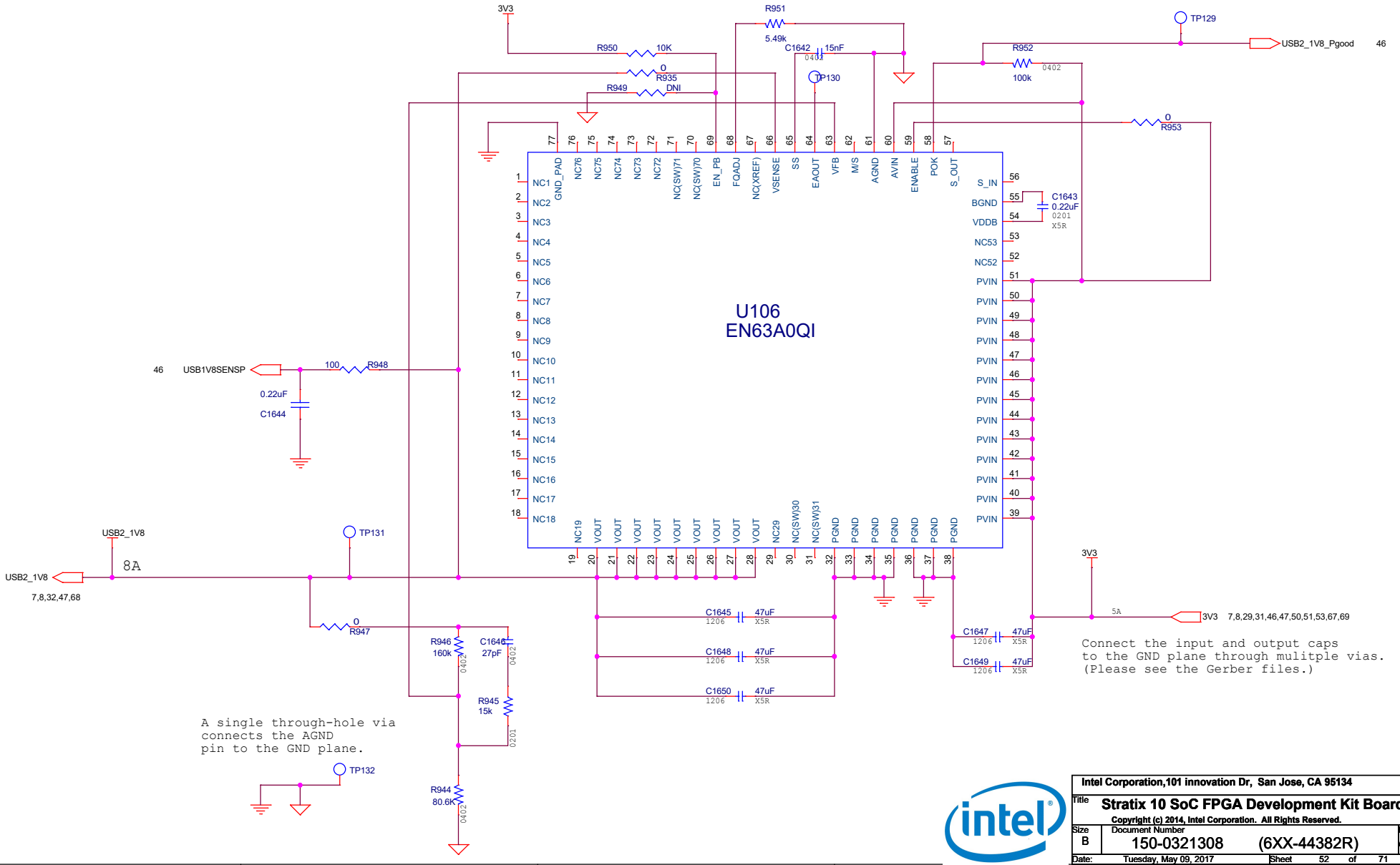
3.3V to 1.8V Converter



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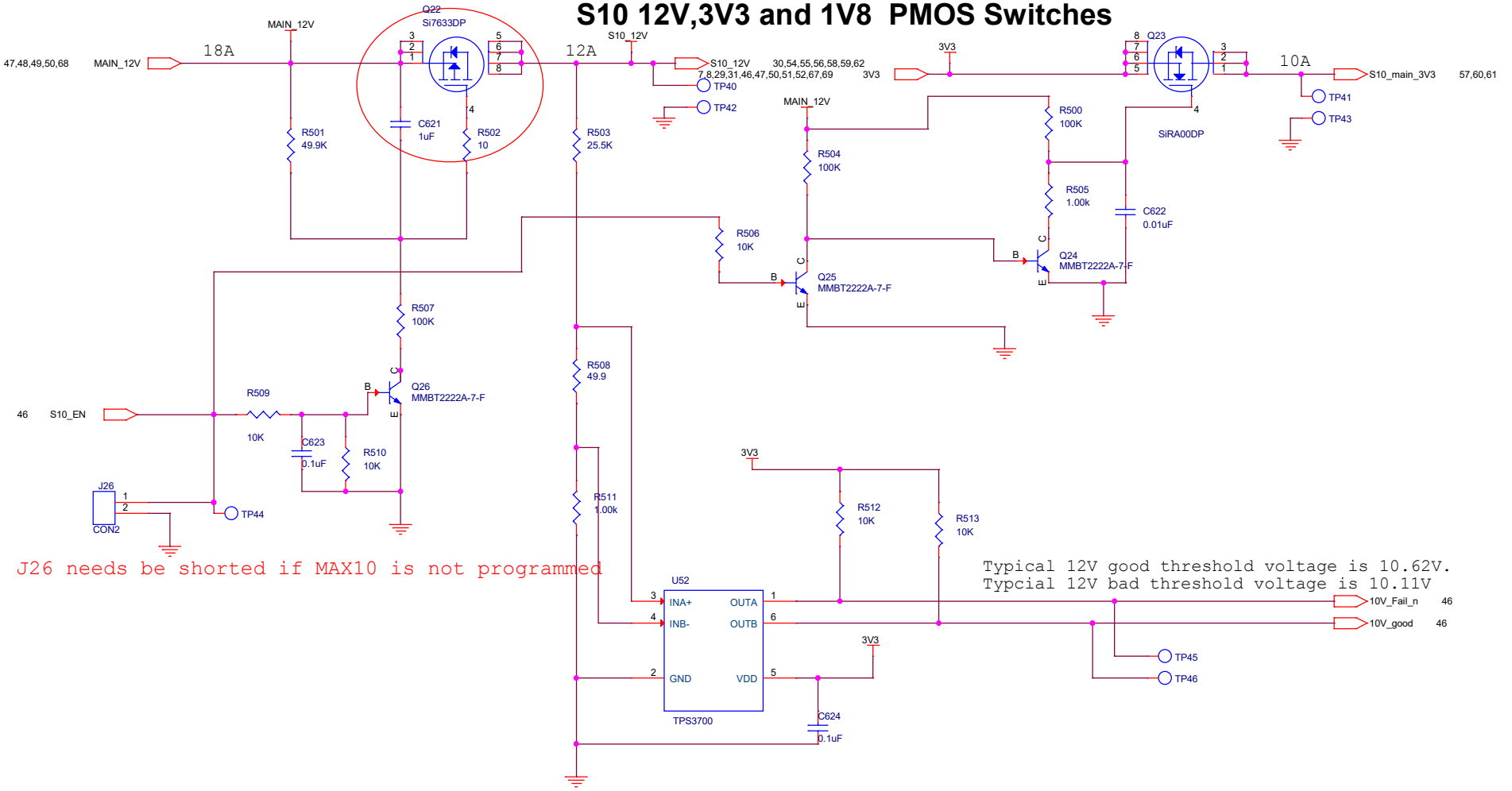
S10 12V,3V3 and 1V8 PMOS Switches



J26 needs be shorted if MAX10 is not programmed

Typical 12V good threshold voltage is 10.62V.
Typcial 12V bad threshold voltage is 10.11V

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12V to Core 1

I2C Address: 0X5A,0X5B and 0X47

Check Phase define

Need 0.85V core voltage

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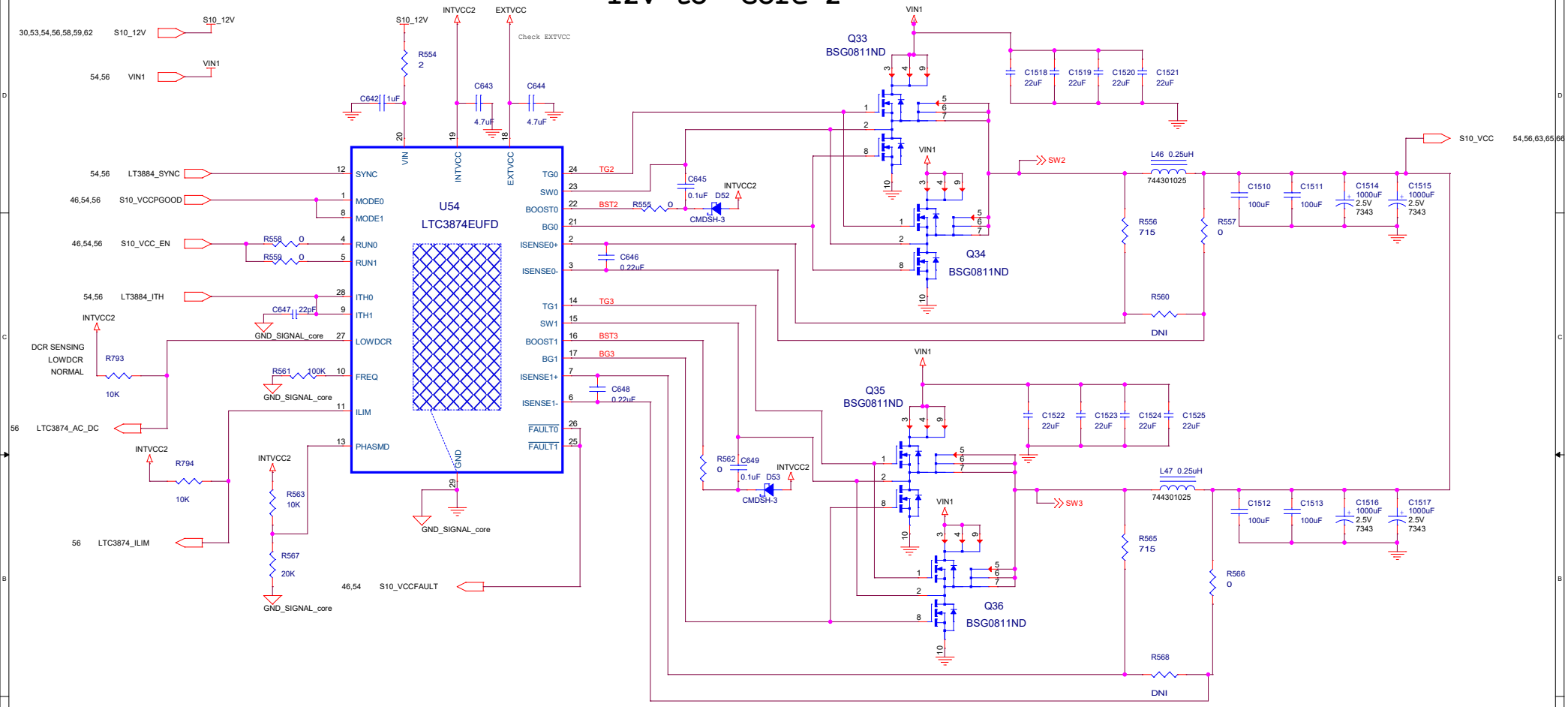
12V to Core 2



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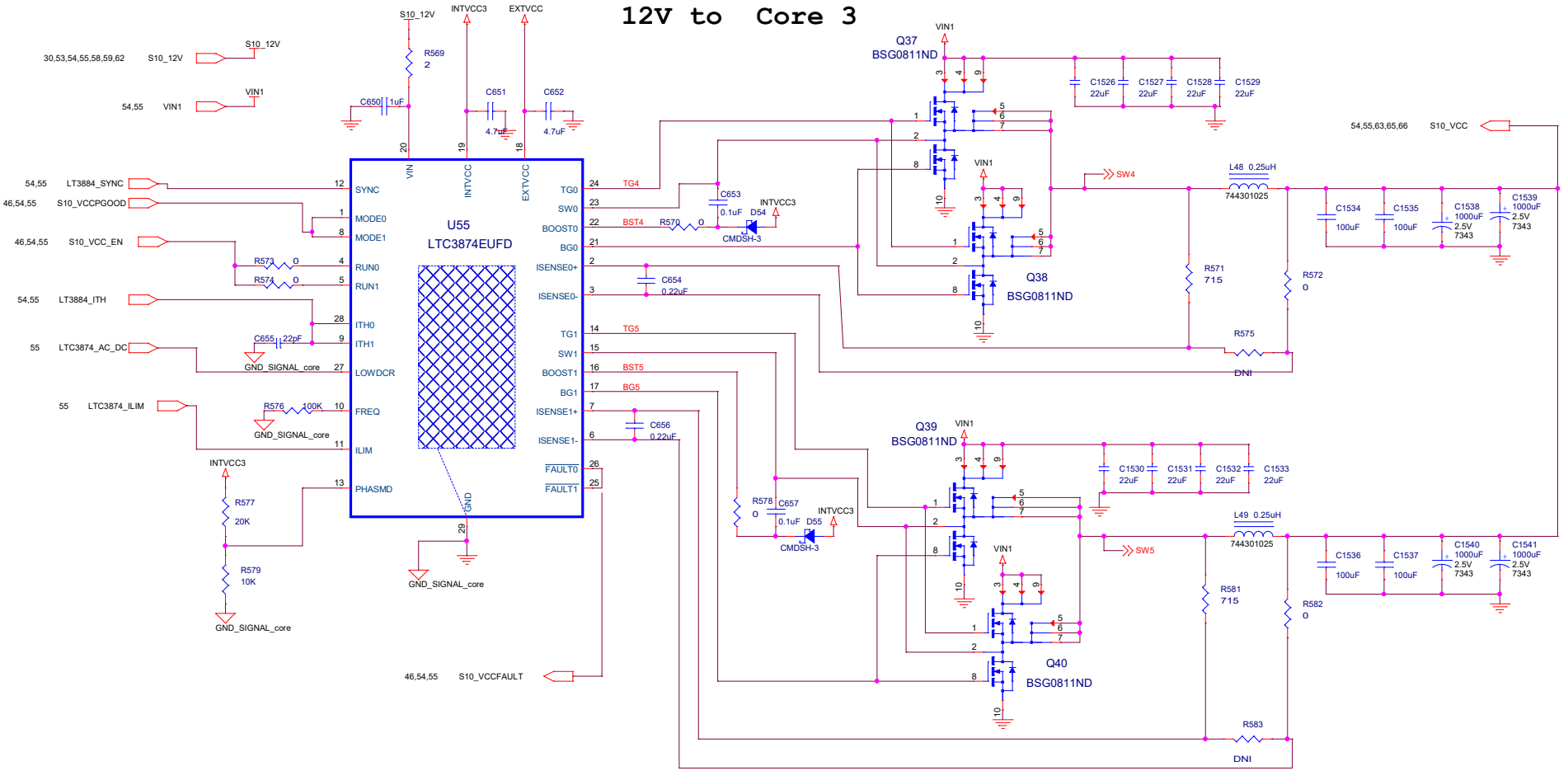
12V to Core 3



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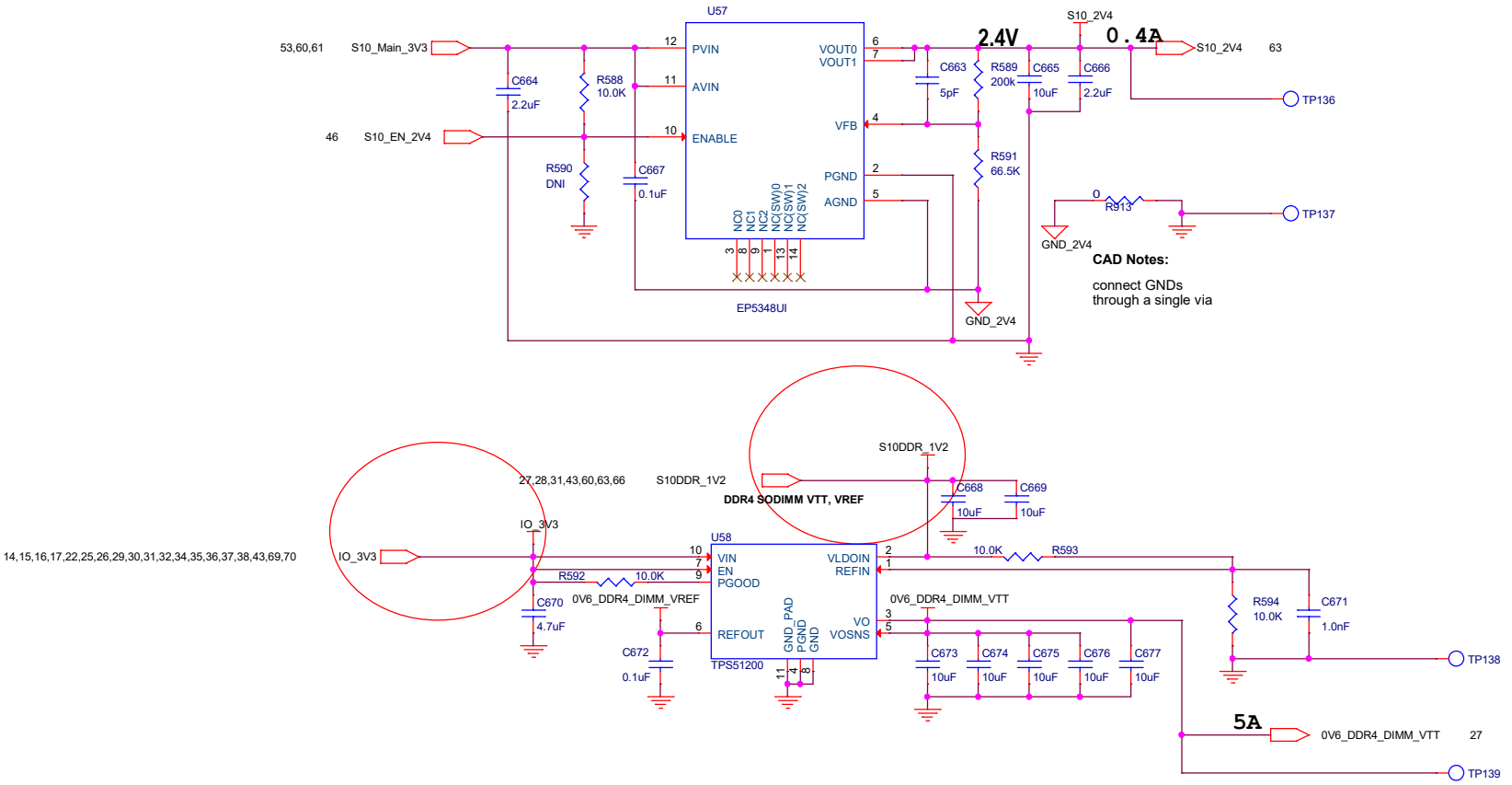
VTT & 2V4 Power



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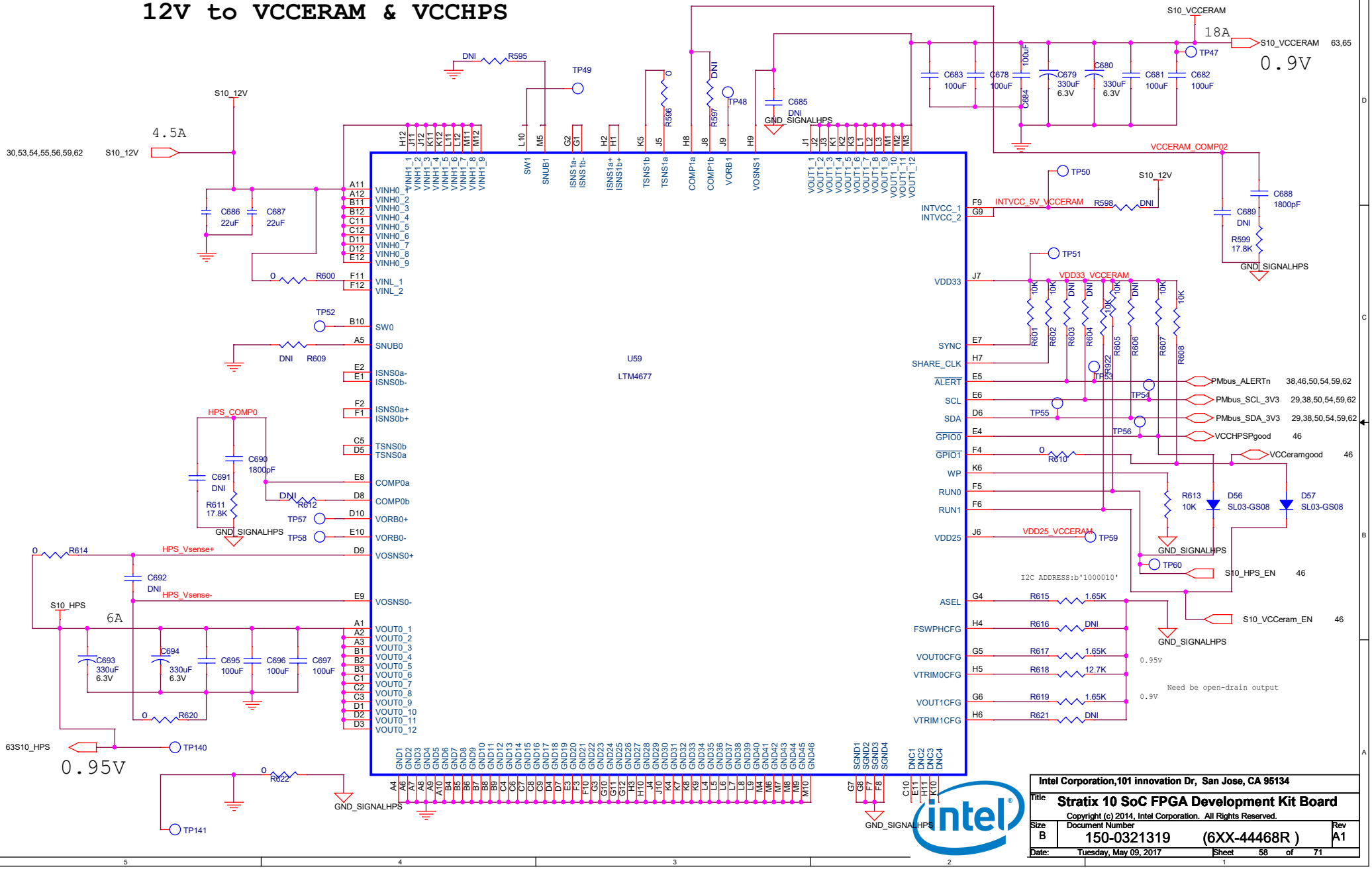
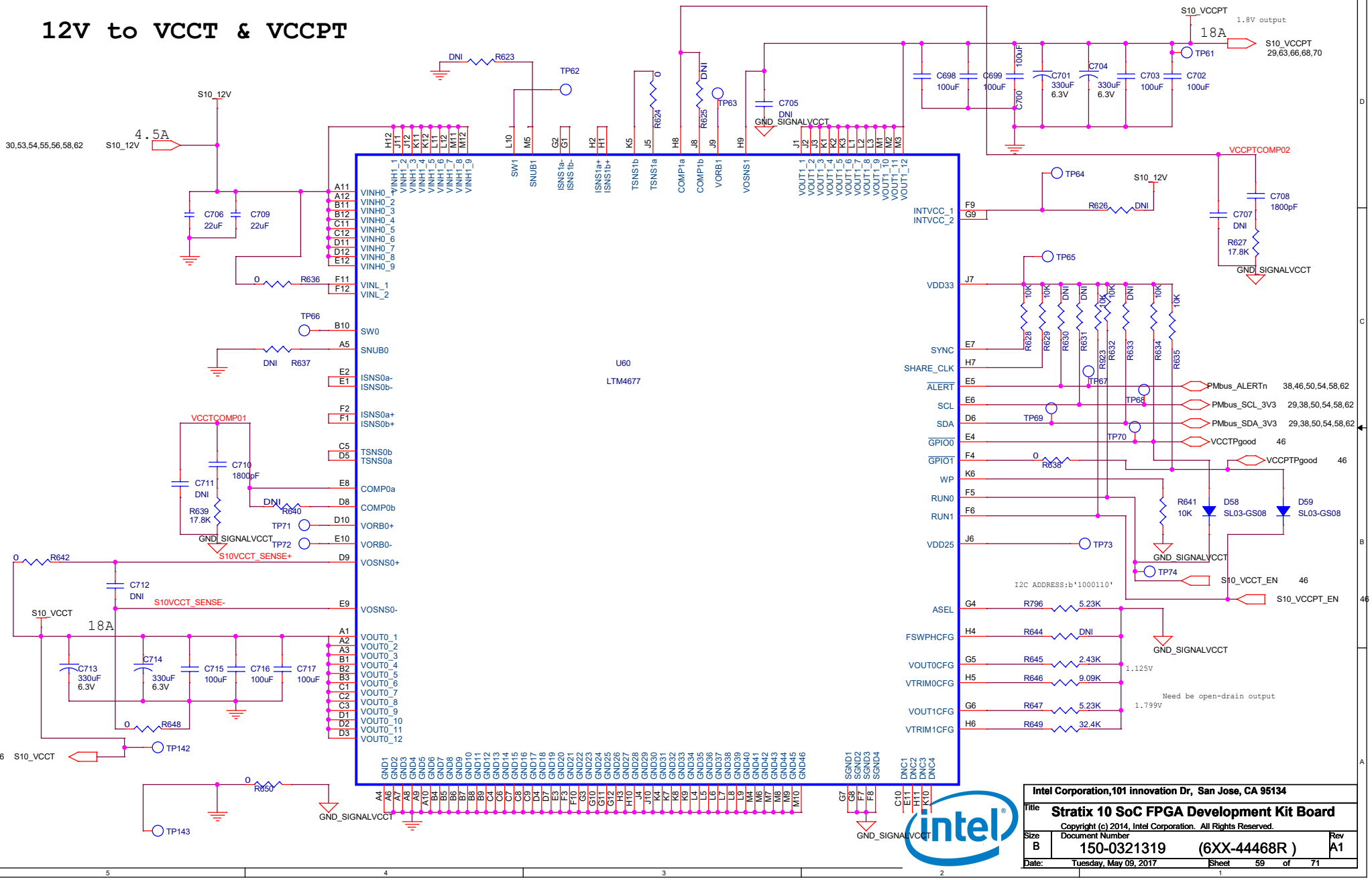
12V to VCCERAM & VCCHPS



12V to VCCT & VCCPT



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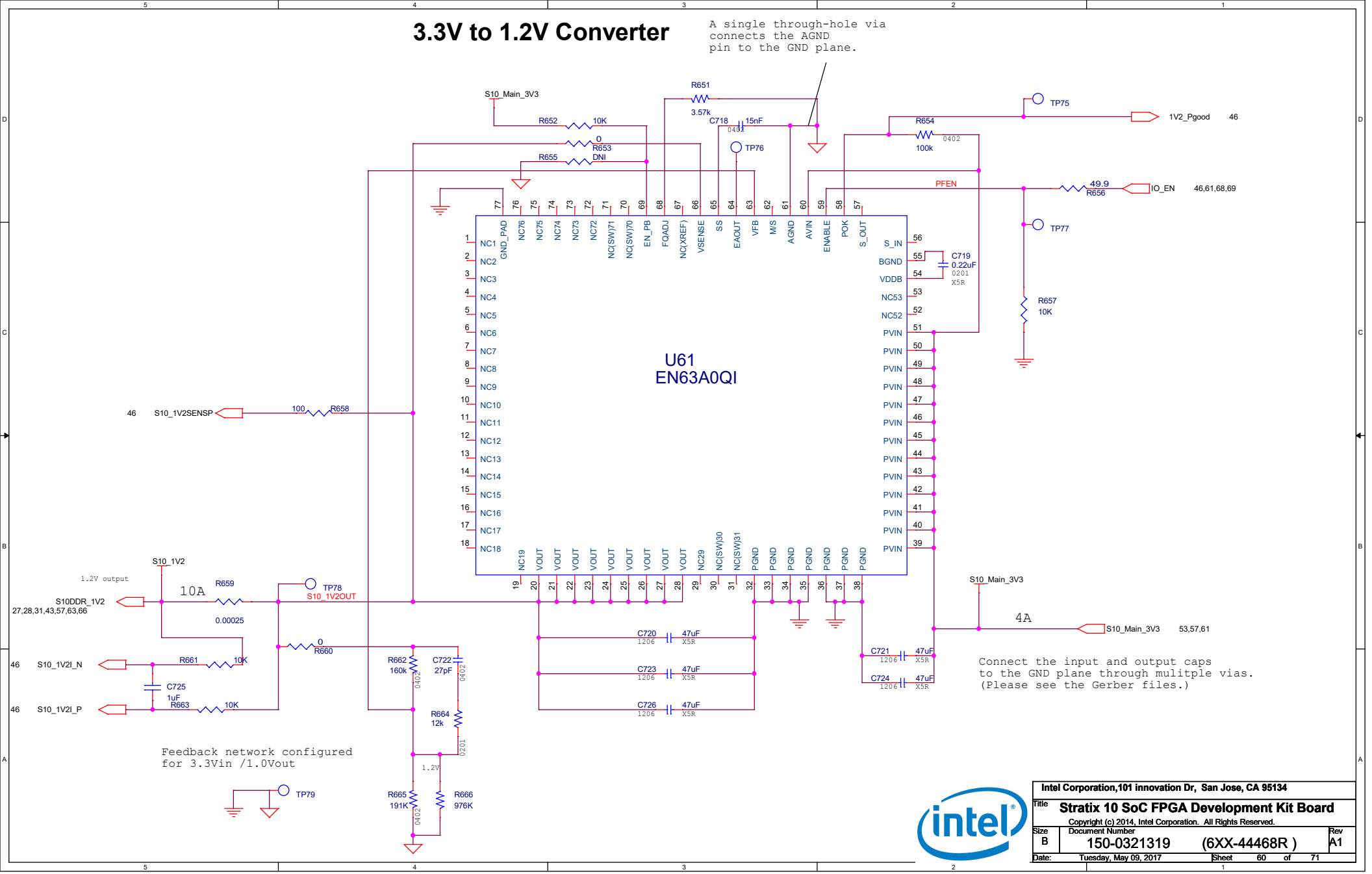
3.3V to 1.2V Converter



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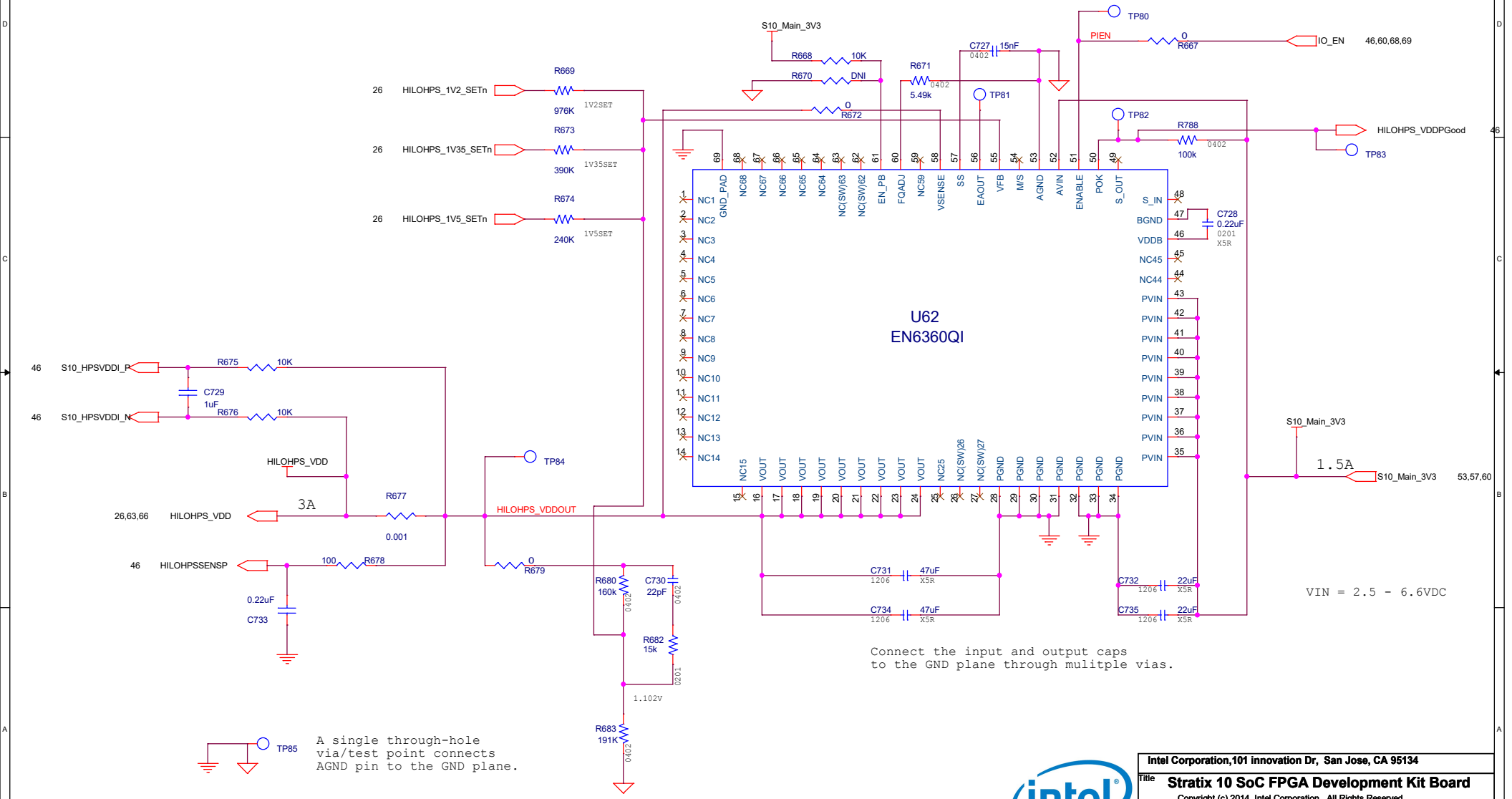
3.3V to HPS HILO VDD converter



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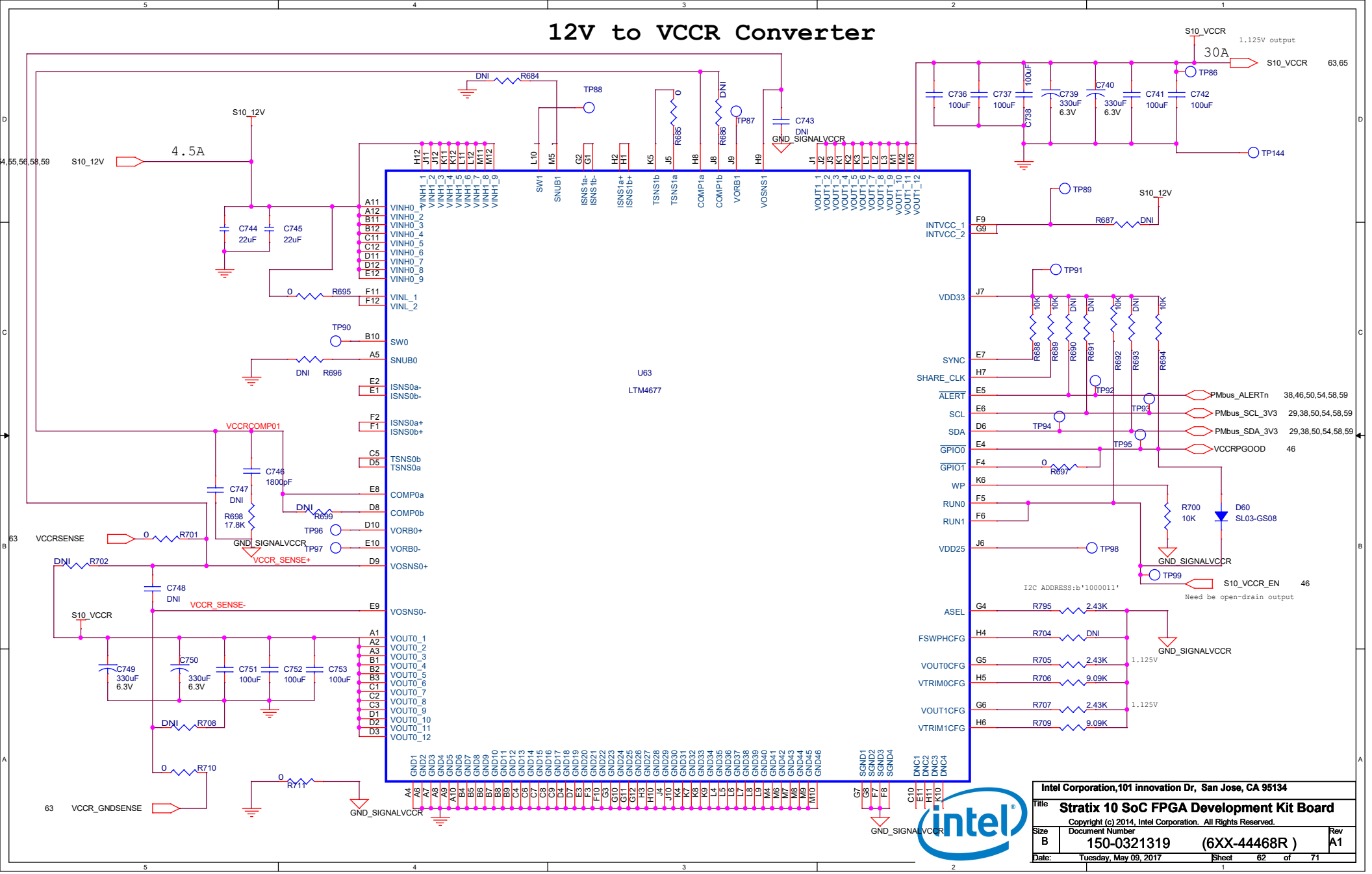
12V to VCCR Converter



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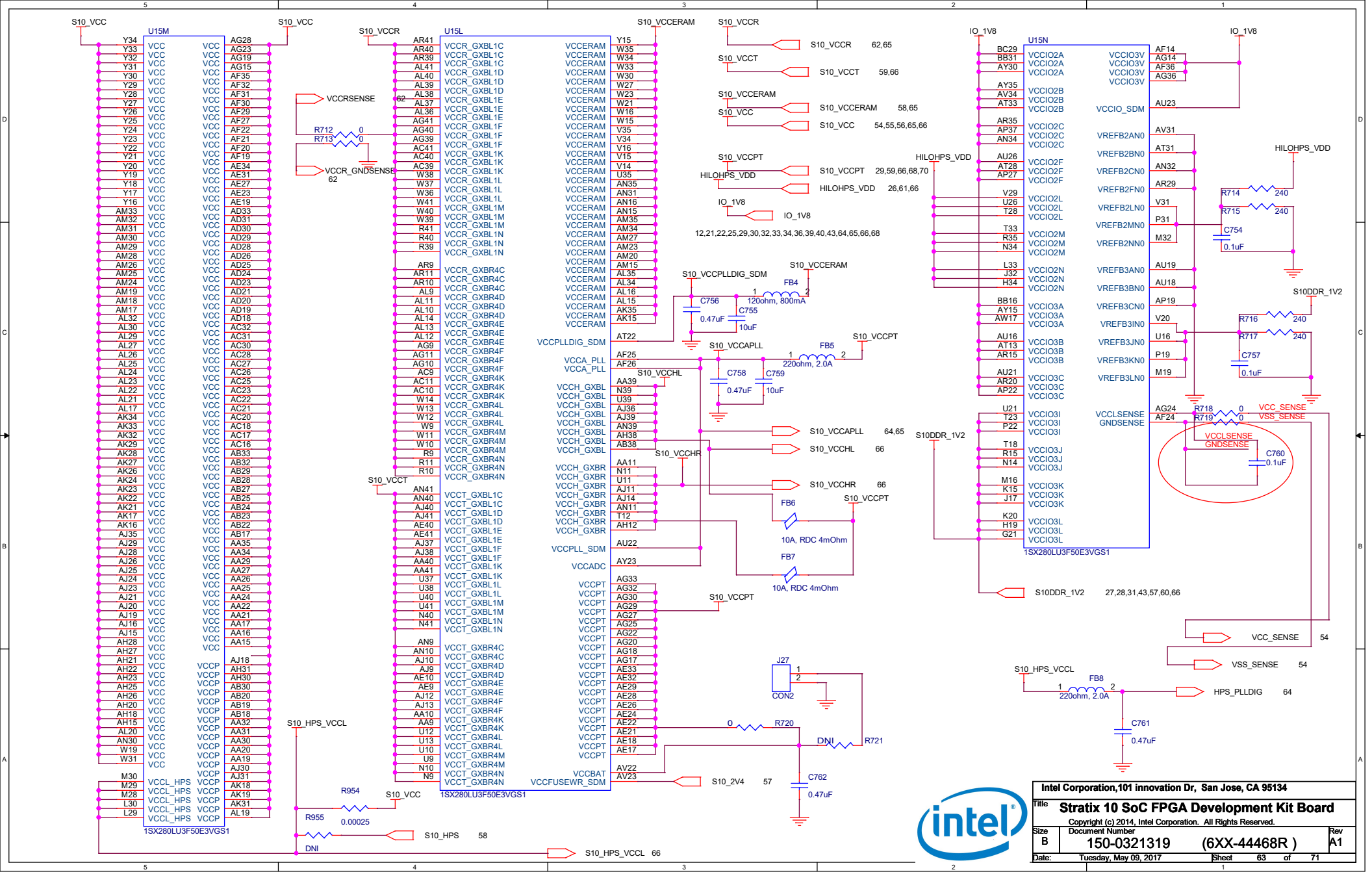

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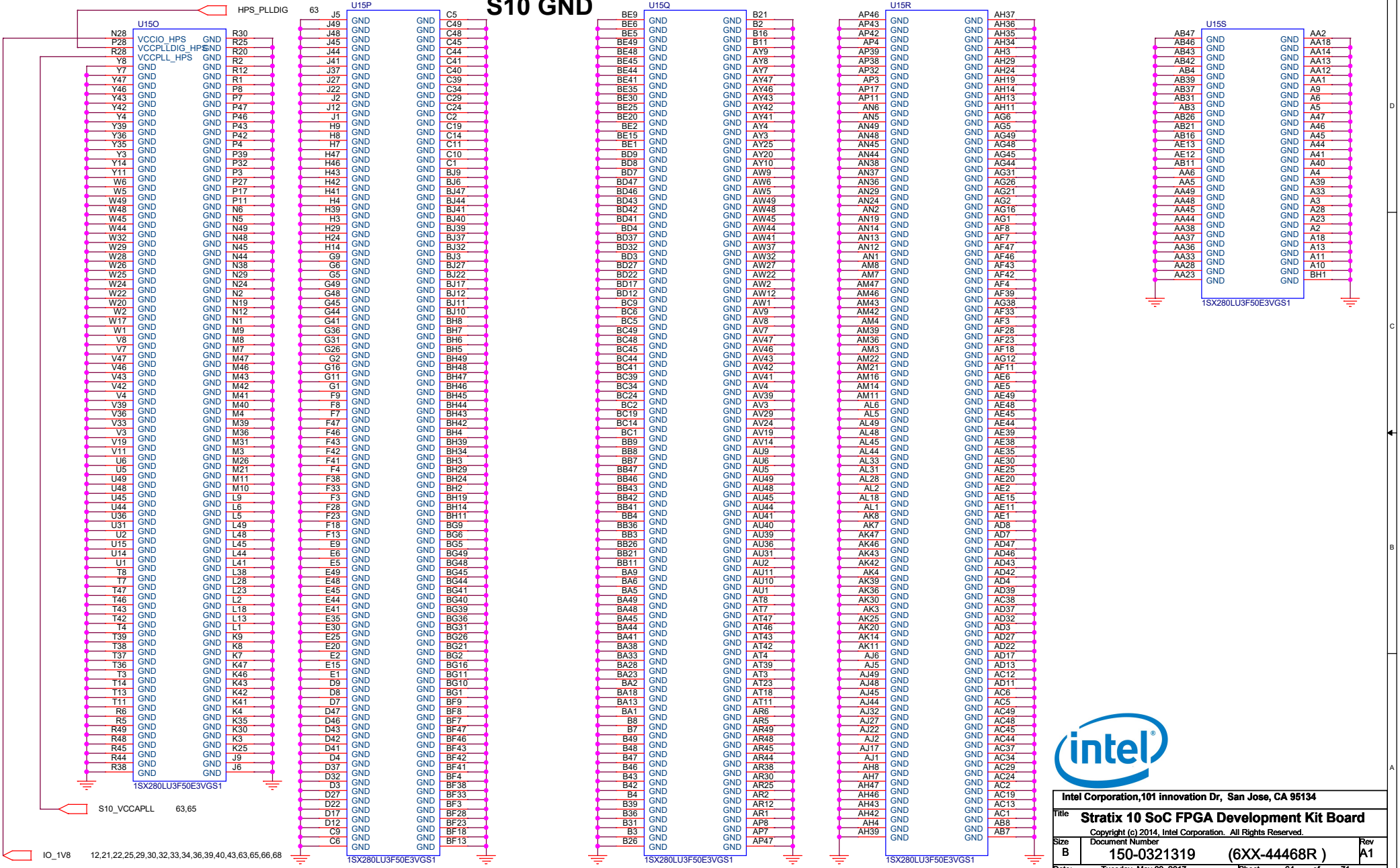
S10 GND



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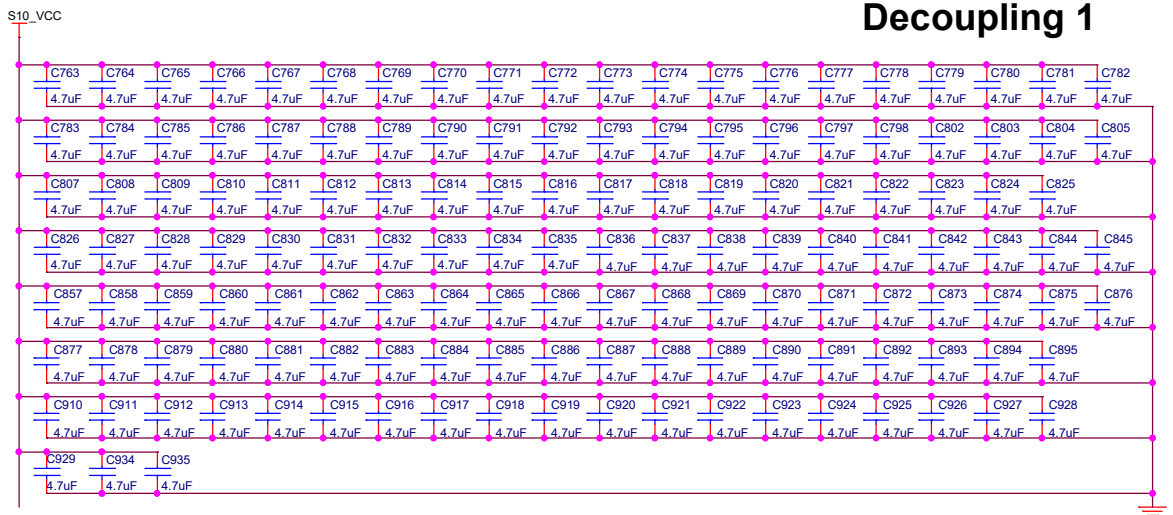
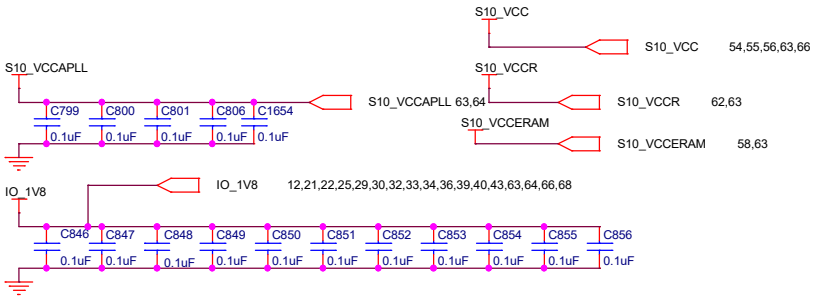
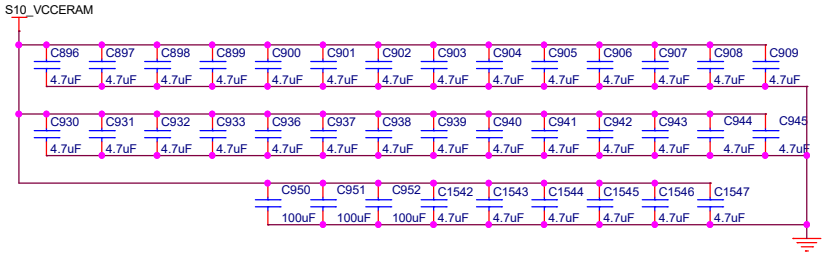
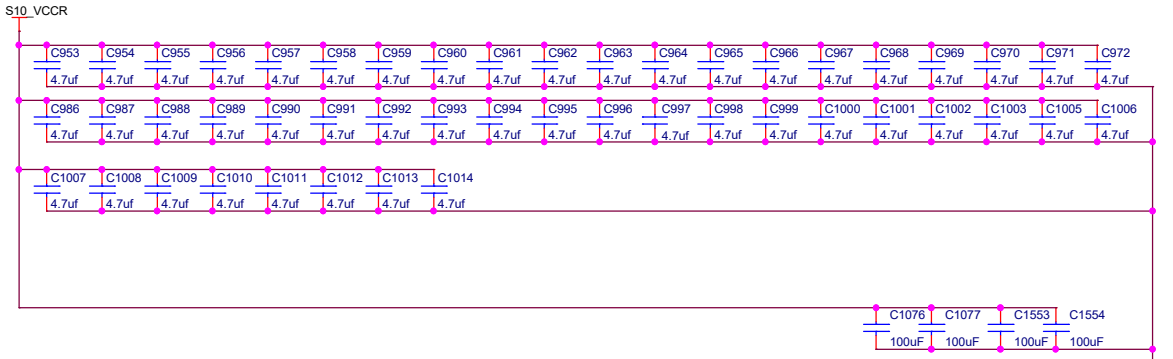
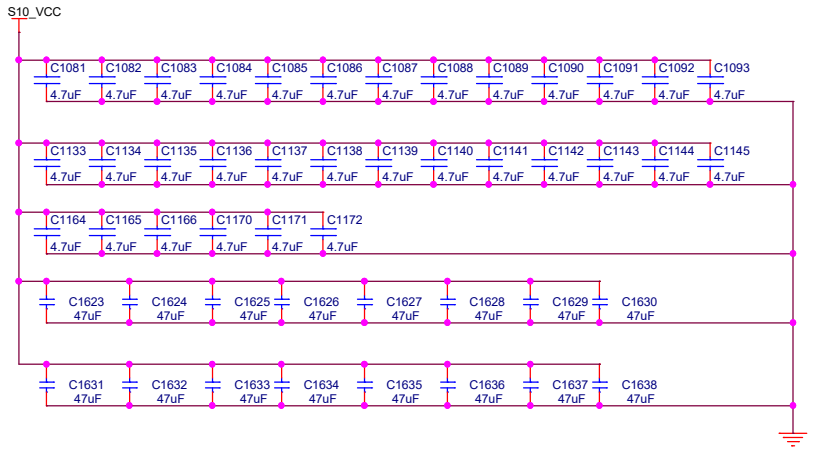
Decoupling 1

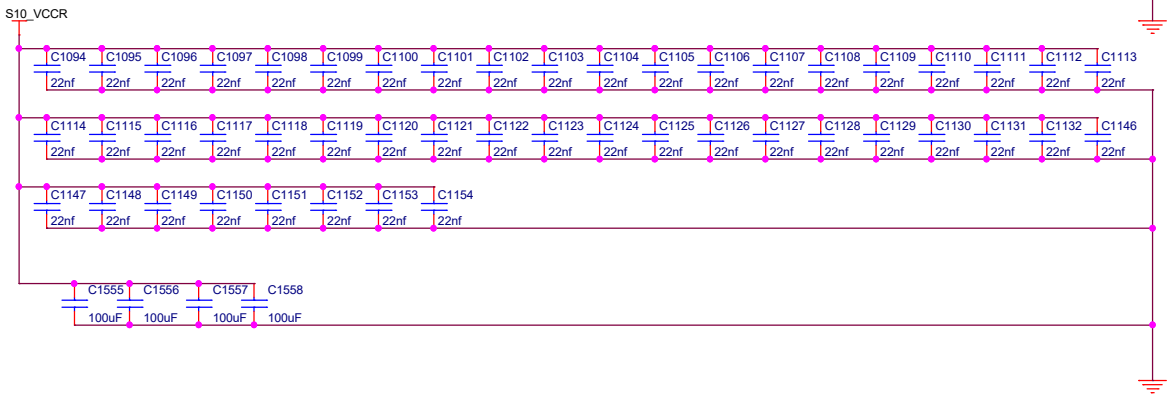












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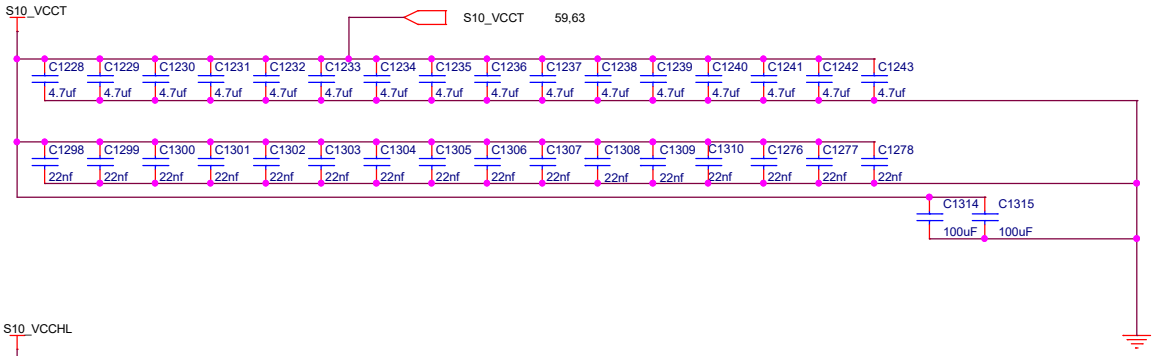
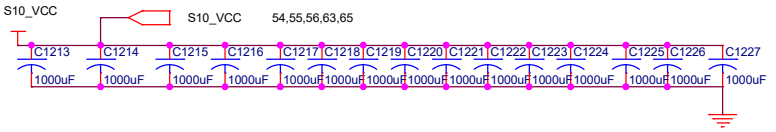
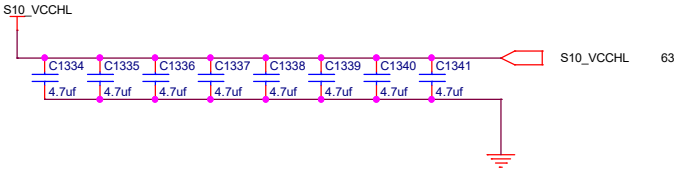
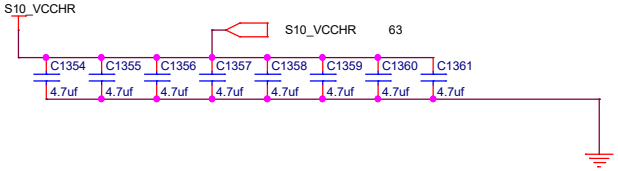
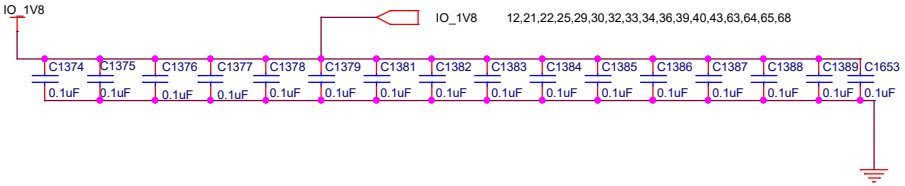
Decoupling 2

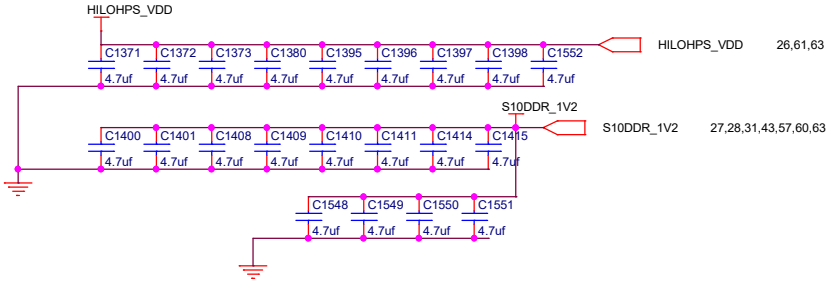


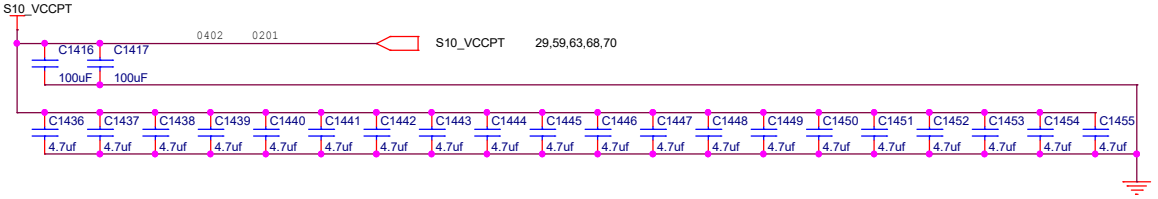


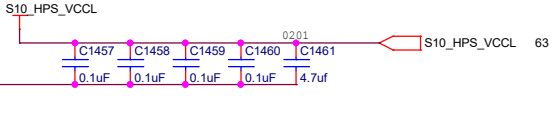












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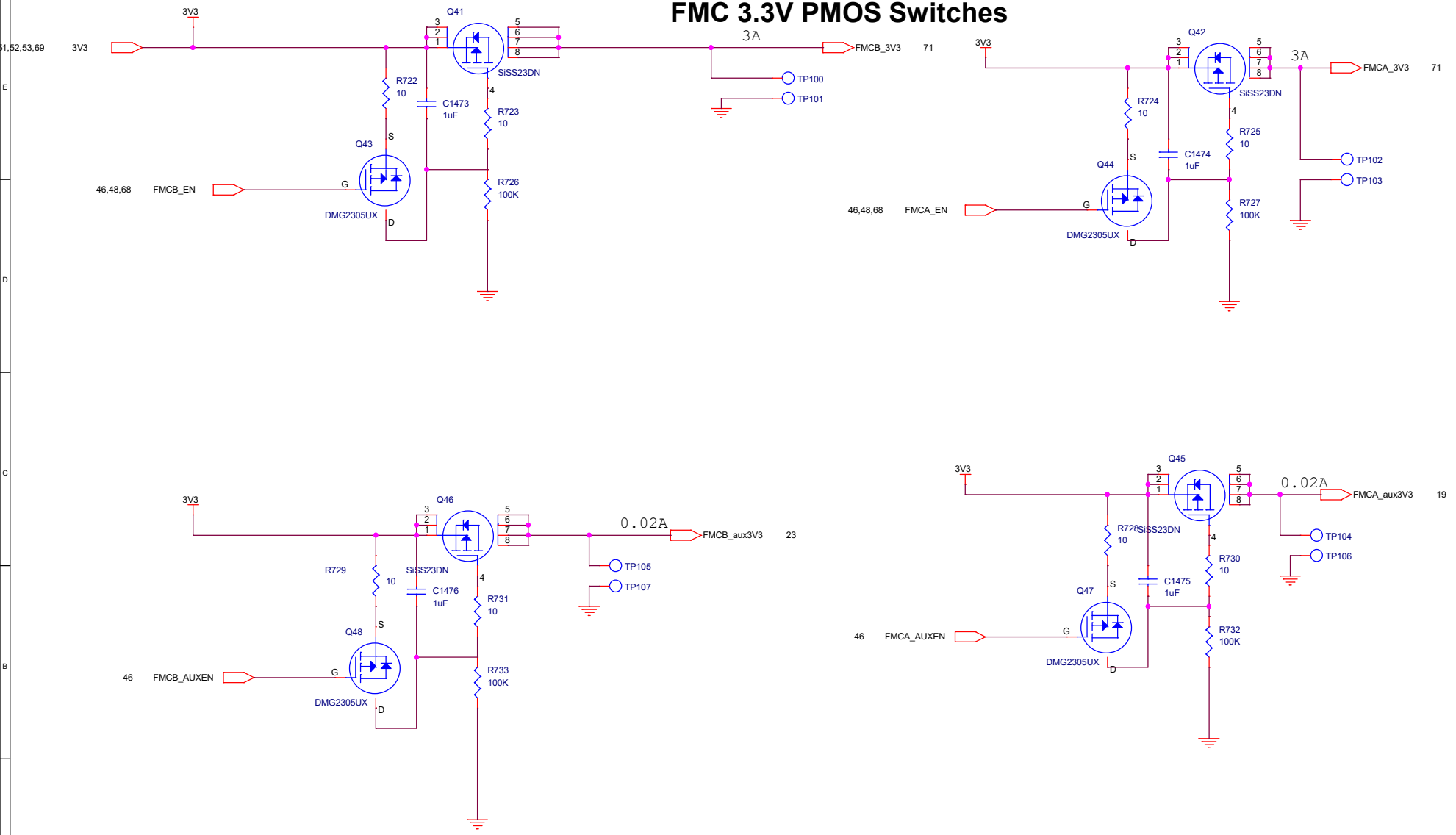
FMC 3.3V PMOS Switches



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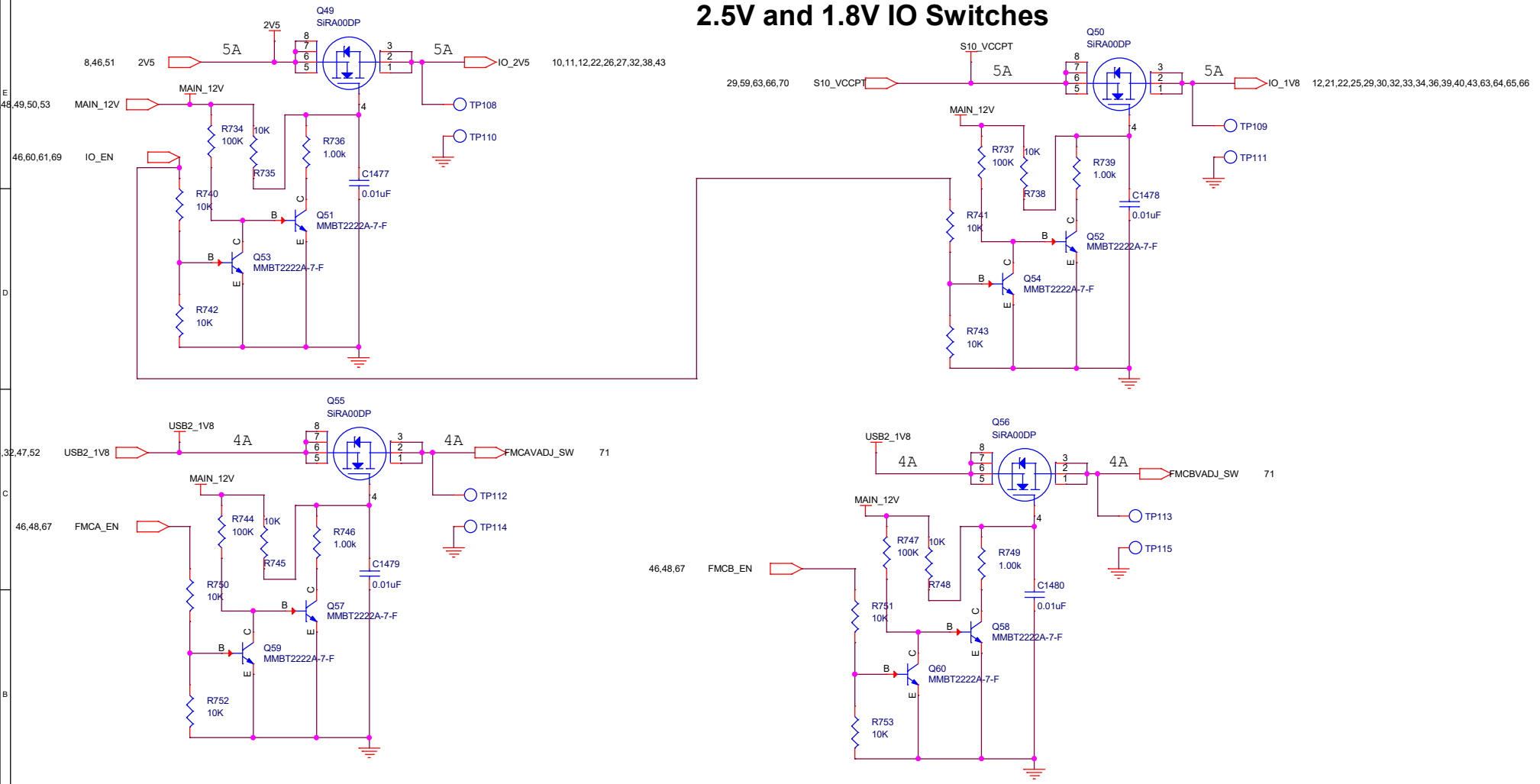
2.5V and 1.8V IO Switches



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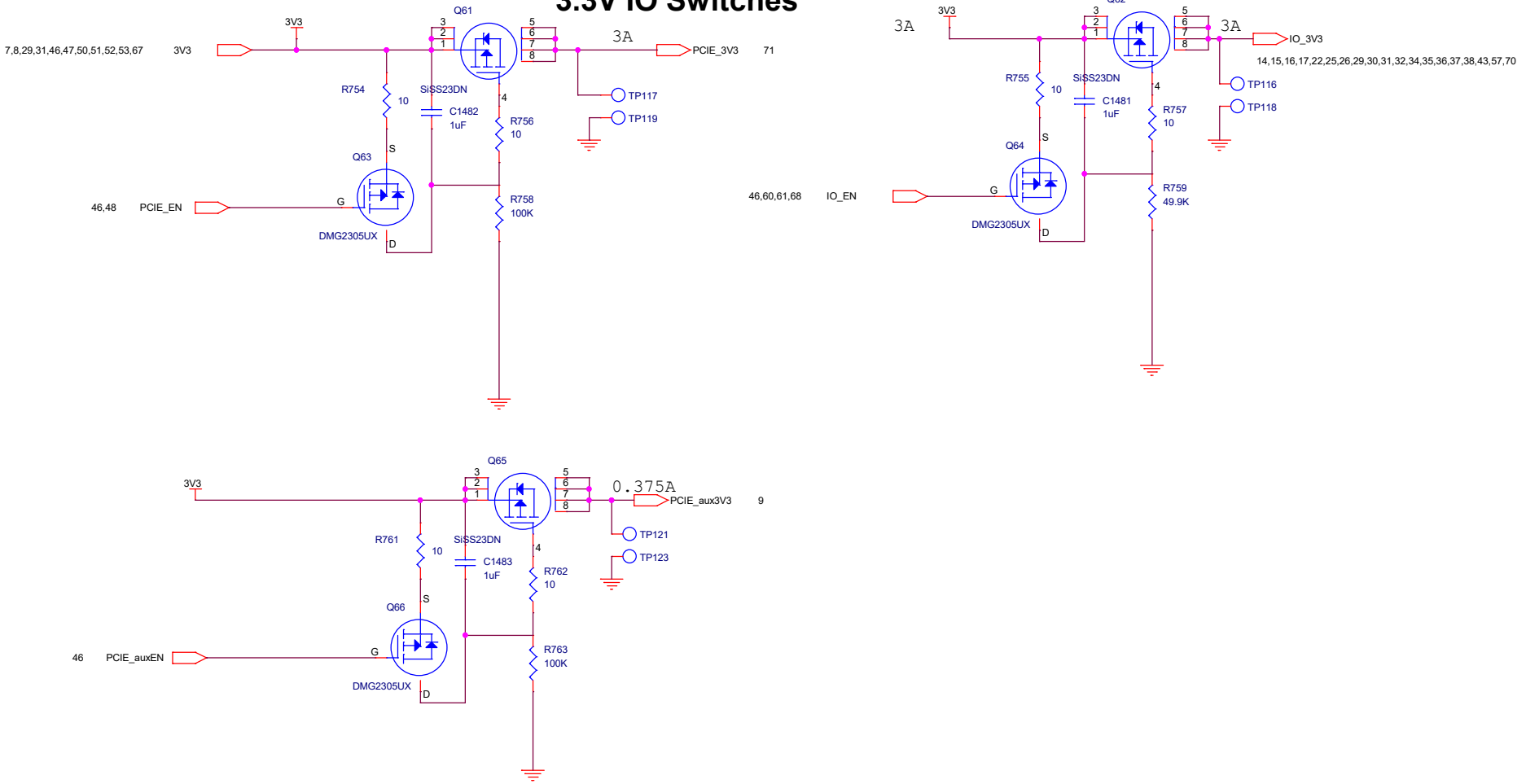
3.3V IO Switches



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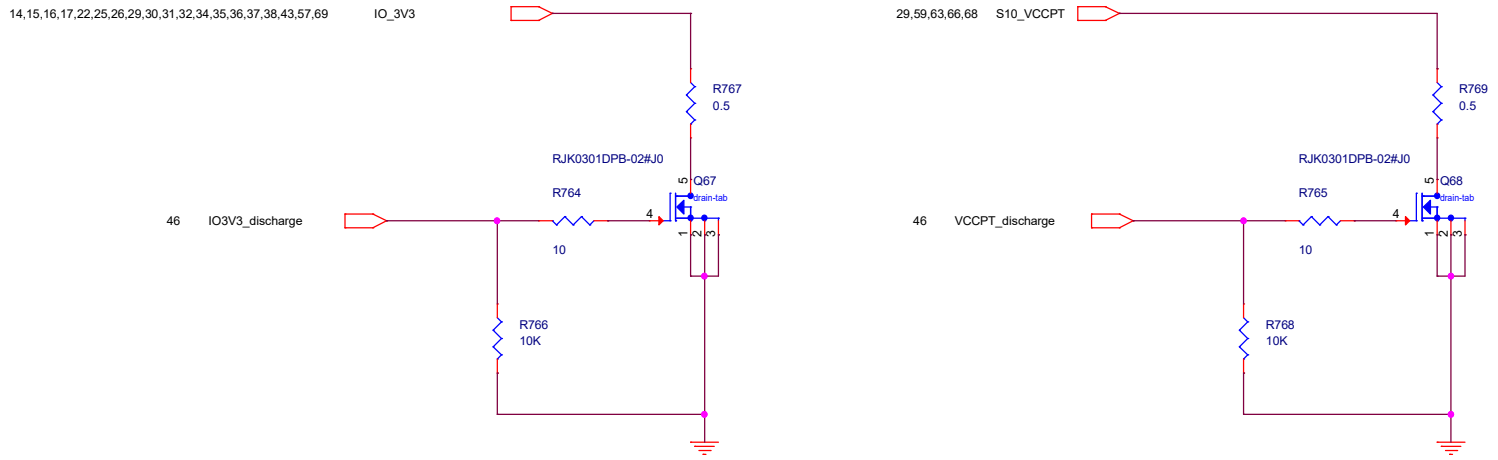
3.3V and 1.8V Discharge Load



50us Discharge time

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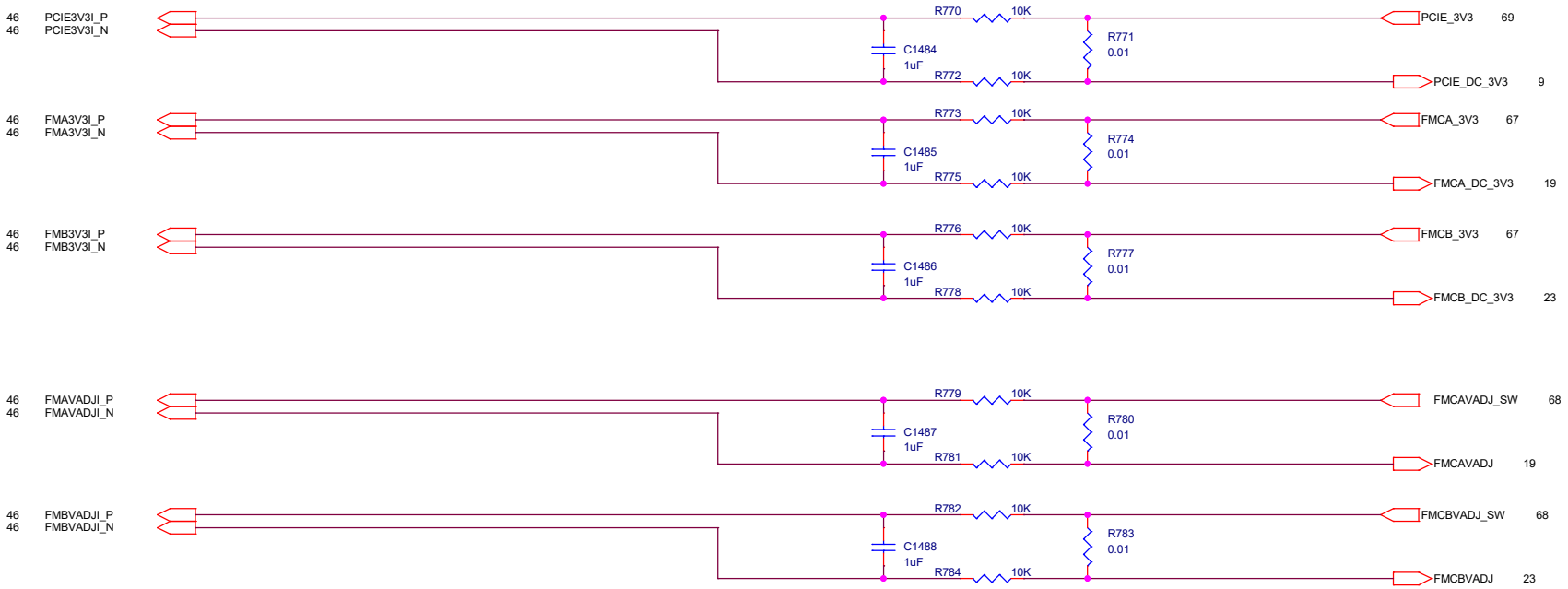
User DC card 3.3V Current Sensors



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